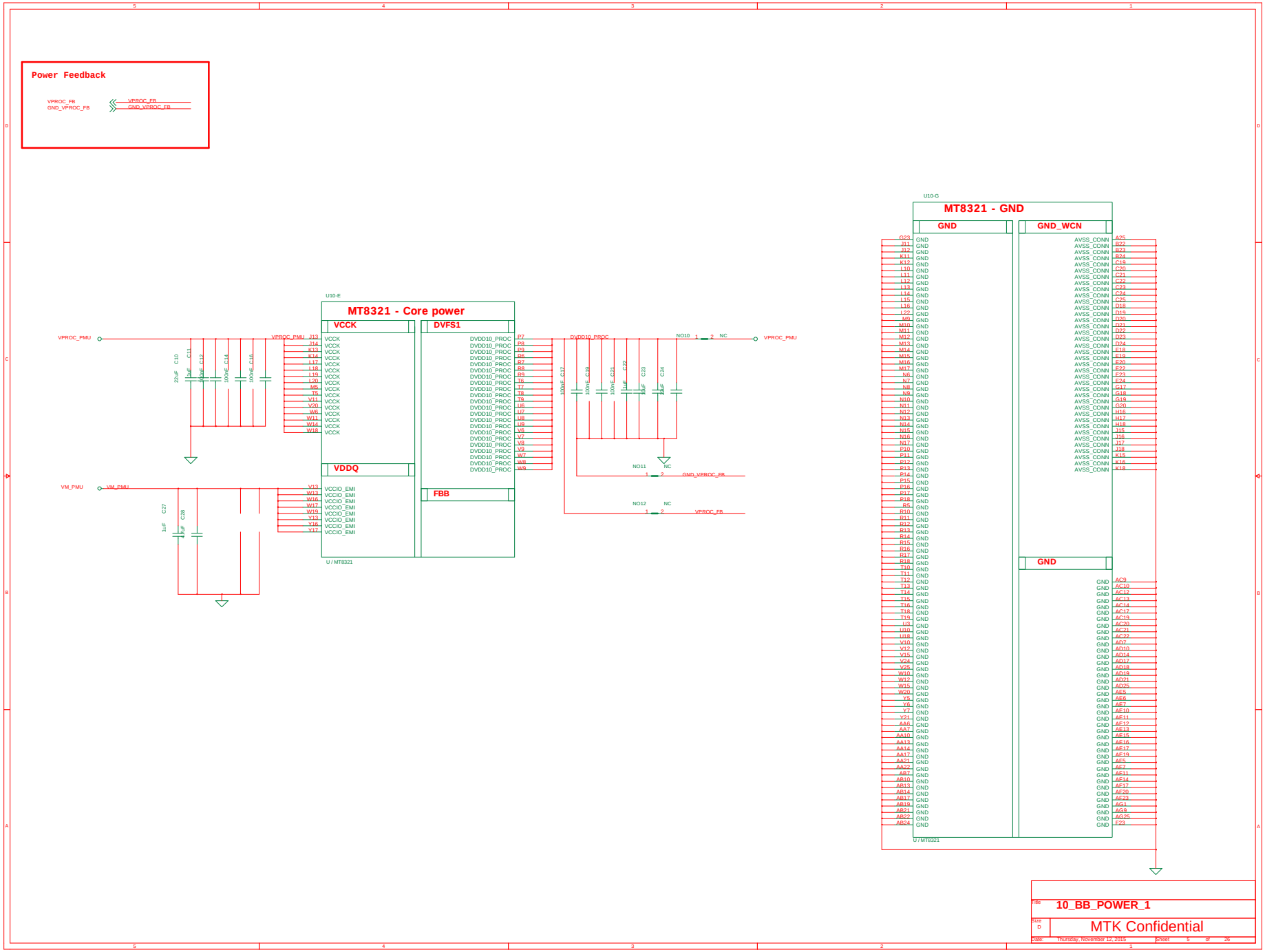
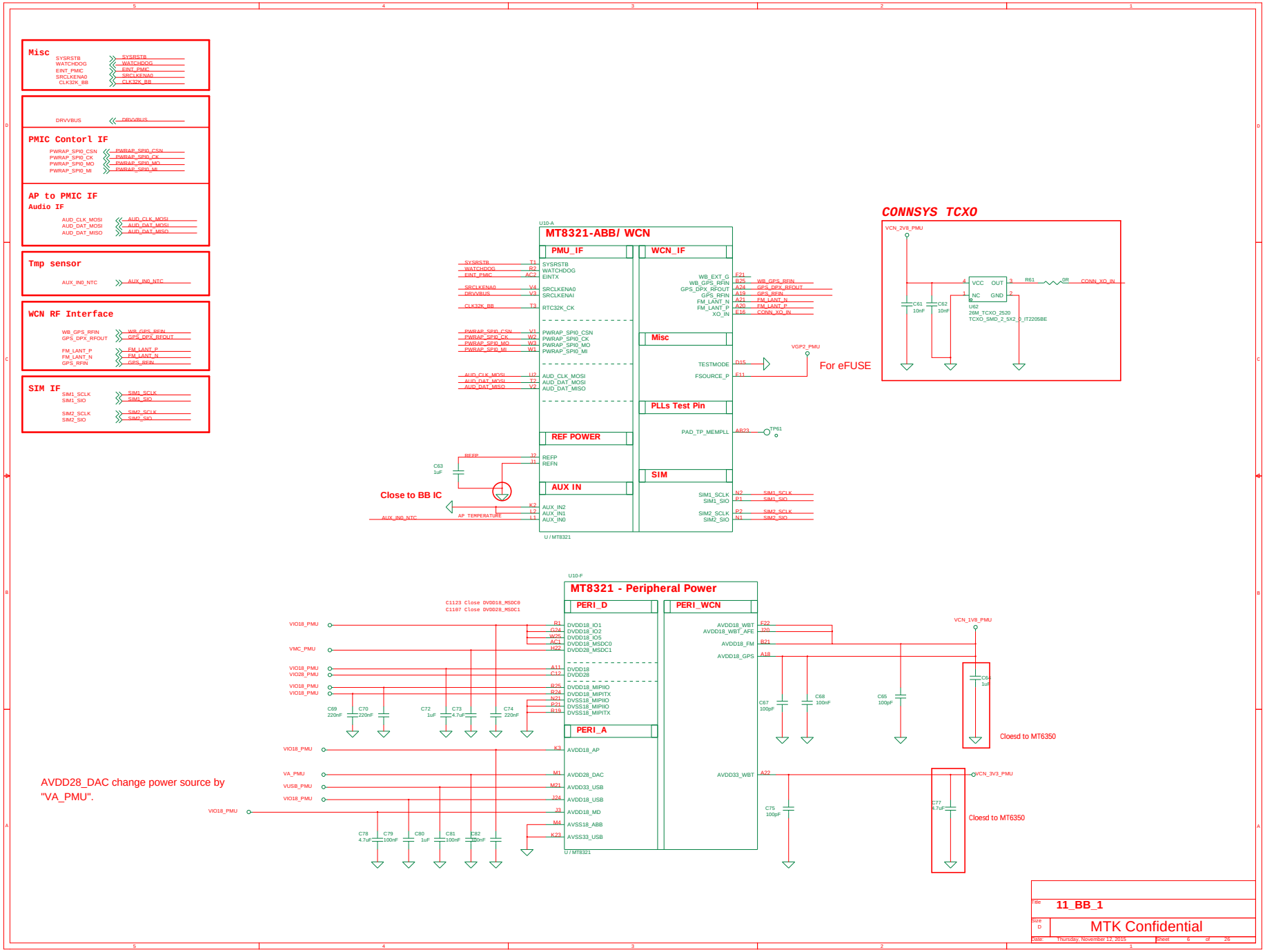
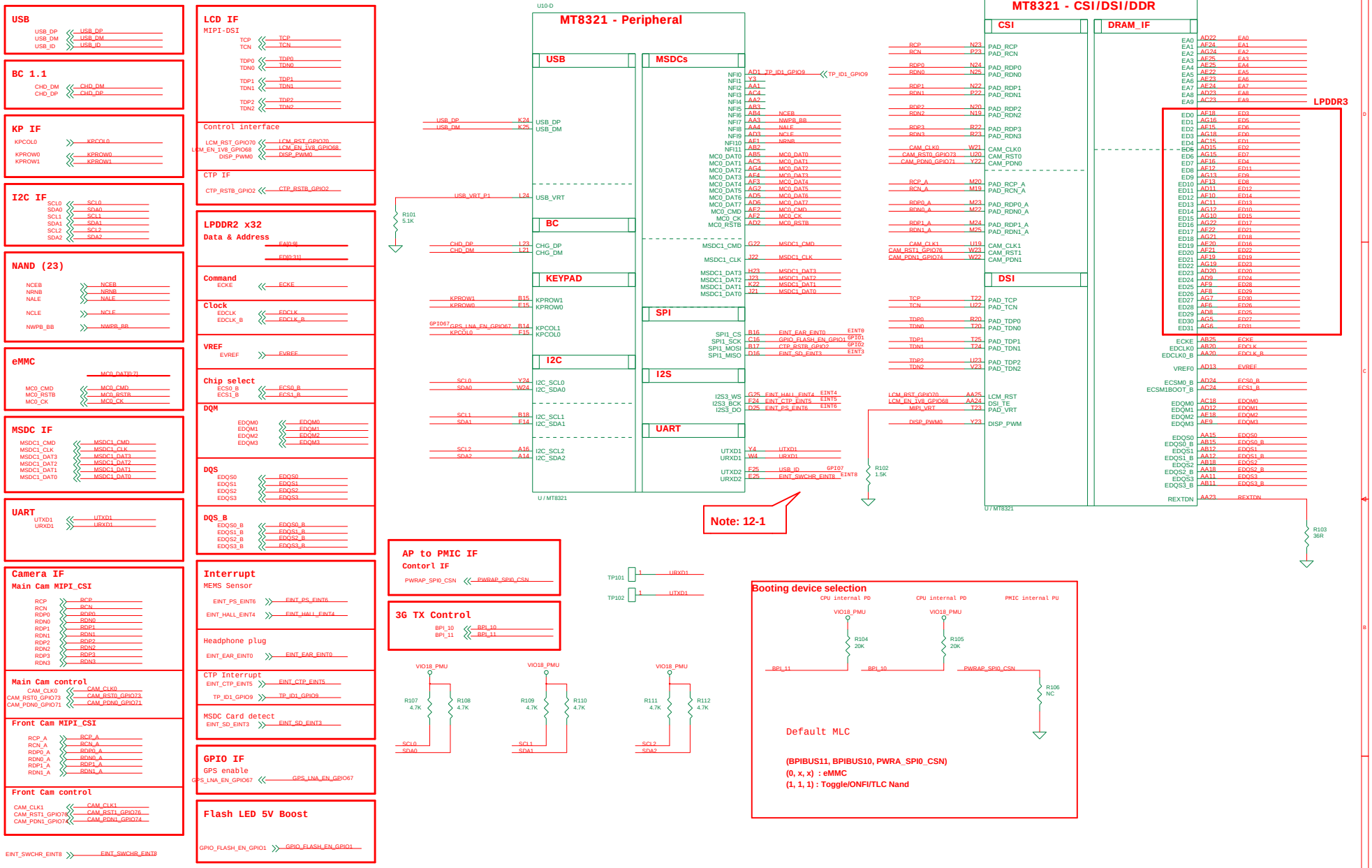


C0402

NC0201_SMD



TCXO_SMD_2_5X2_0_IT2205BE



Schematic design notice of "12_BB_2" page.

Note 12-1:

Do not use UART1 as Power solution enable.

Do not use UART2 as power solution enable, if select UART1 as D/L or calibration path,

Title	12_BB_2
Size D	MTK Confidential
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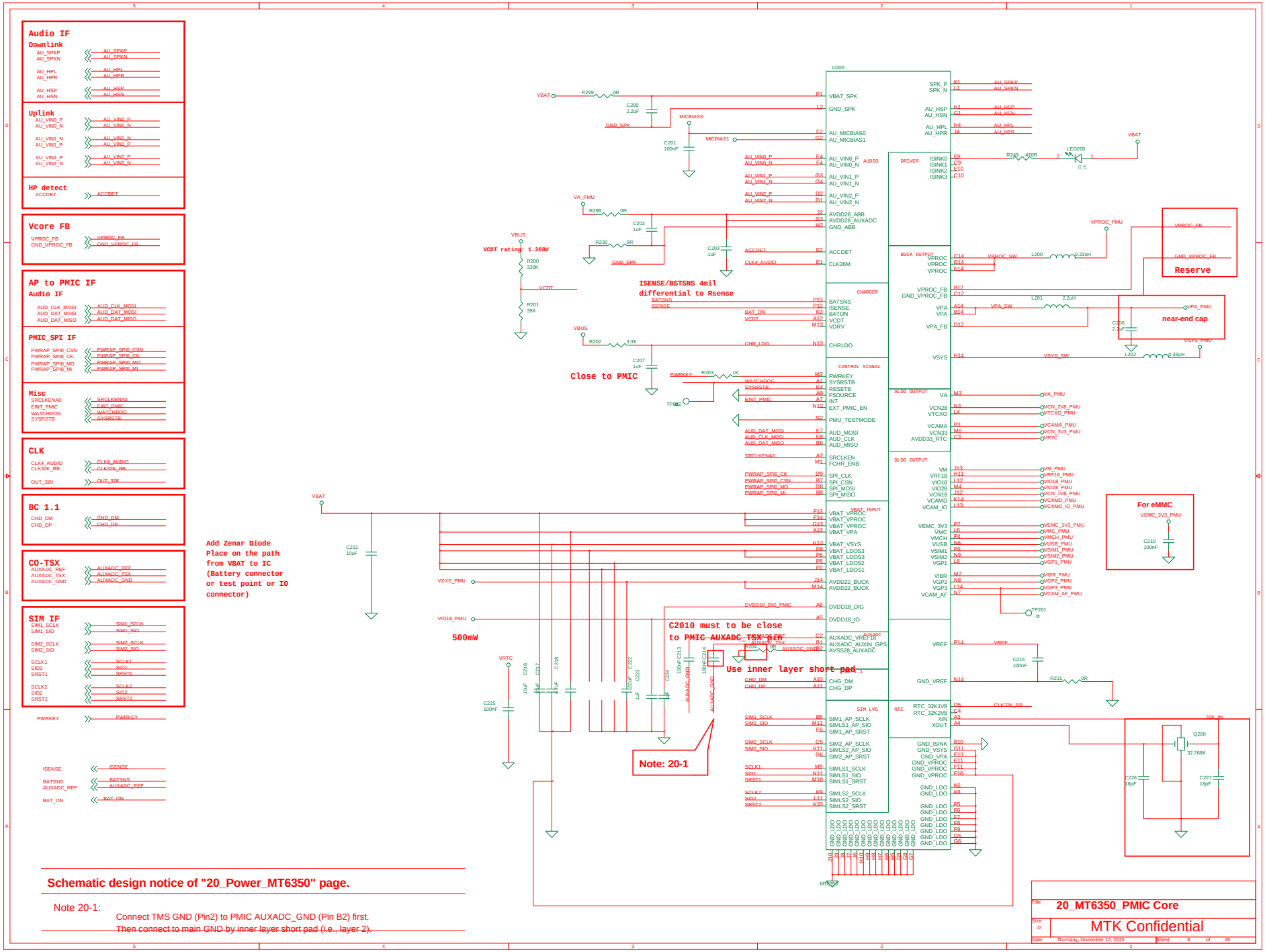
Audio IF
Downlink
Uplink
HP detect
Vcore FB
AP to PMIC IF
Audio IF
PMIC_SPI IF
Misc
CLK
BC 1.1
CO-TSX
SIM IF
U200
VCDT rating: 1.268V
ISENSE/BSTSNS 4mil differential to Rsense
Close to PMIC
Add Zenar Diode Place on the path from VBAT to IC (Battery connector or test point or IO connector)
500mW
C2010 must to be close to PMIC AUXADC_TSX pin
Use inner layer short pad
Note: 20-1
Reserve
near-end cap
For eMMC
Schematic design notice of "20_Power_MT6350" page.
Note 20-1:
Connect TMS GND (Pin2) to PMIC AUXADC_GND (Pin B2) first.
Then connect to main GND by inner layer short pad (i.e., layer 2).
20_MT6350_PMIC Core
MTK Confidential
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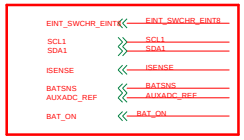
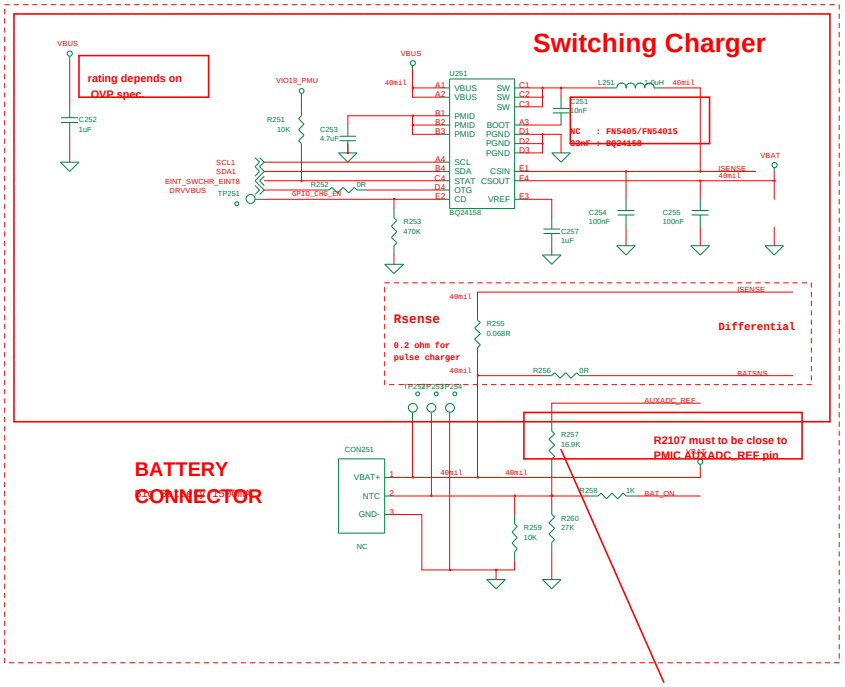
Charger IF





if battery NTC is 10kohm, R310=16.9K, R312=27K
if battery NTC is 47kohm, R310=61.9K, R312=100K
Refer to MT6350 HW design notice

Title	21_Charger
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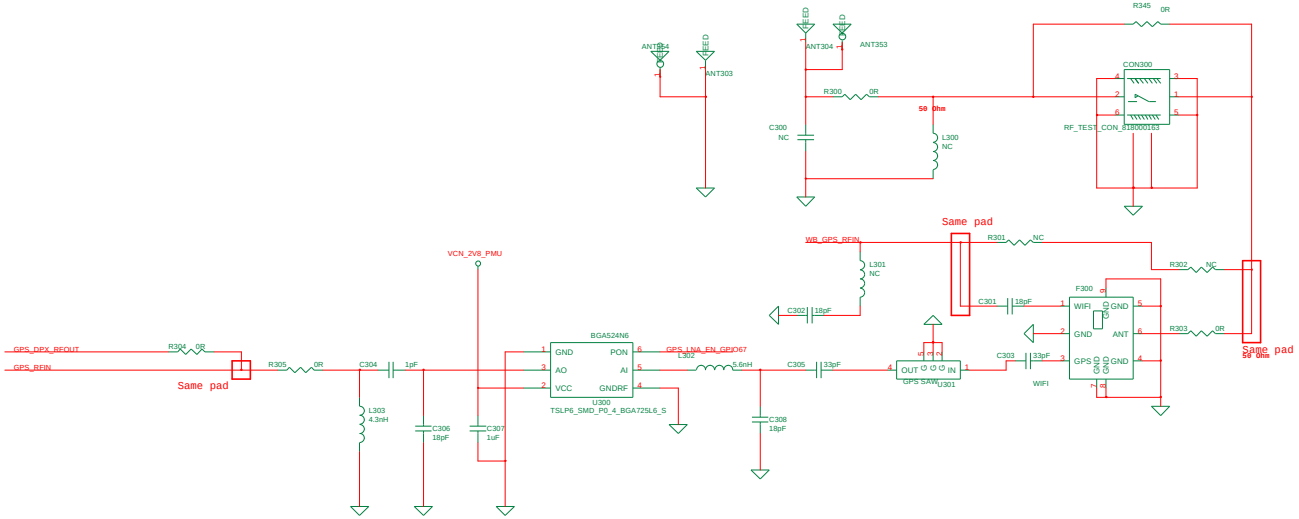
C0402

WCN RF Interface

WB_GPS_RFIN	WB_GPS_RFIN
GPS_DPX_RFOUT	GPS_DPX_RFOUT
GPS_RFIN	GPS_RFIN
GPS_LNA_EN_GPIO67	GPS_LNA_EN_GPIO67



Title	50_BT_FM_GPS_WiFi
Size D	MTK Confidential
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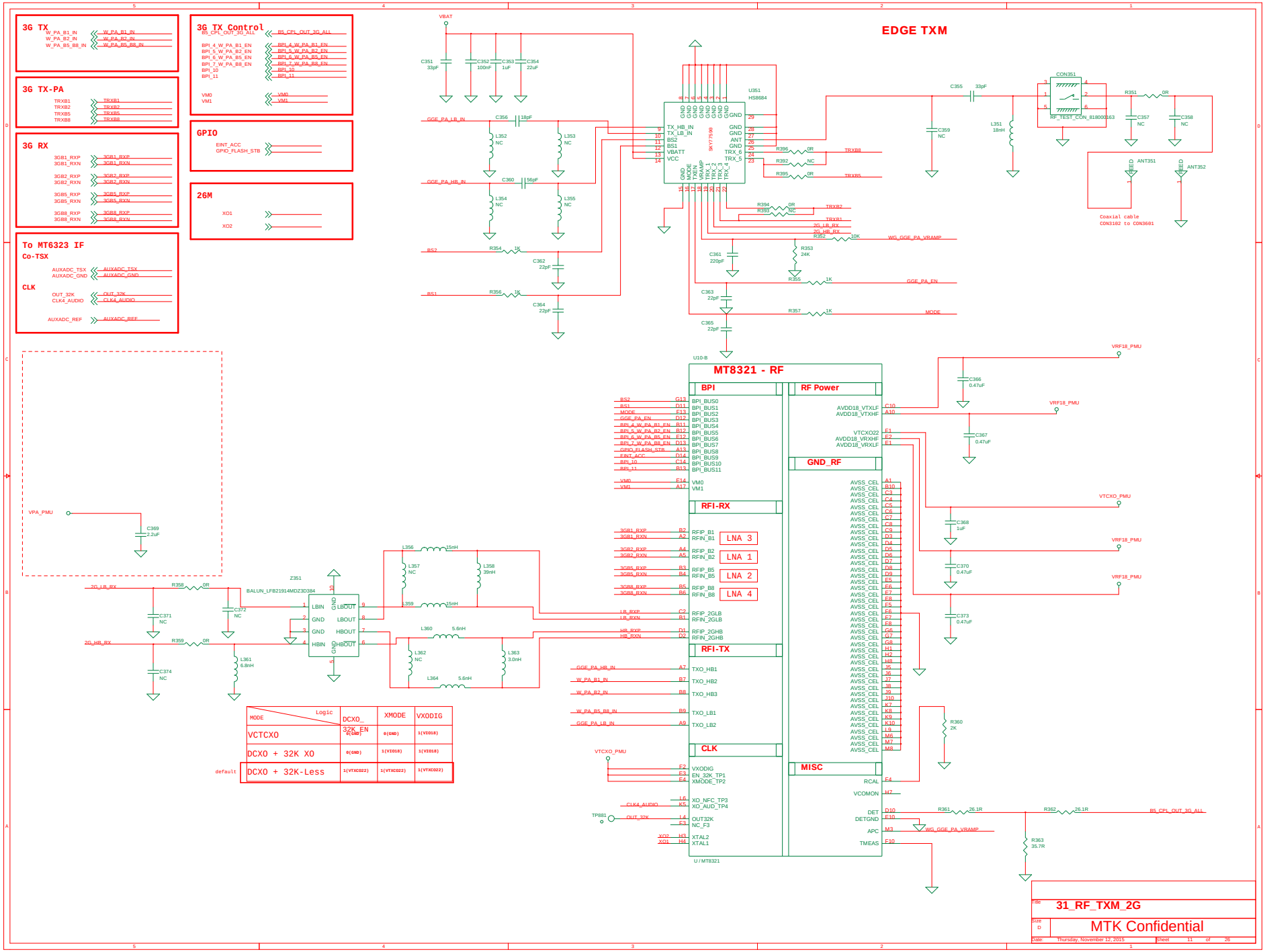
CD402

TSLP6_SMD_P0_4_BGA725L6_S


EDGE TXM
3G TX
W_PA_B1_IN
W_PA_B2_IN
W_PA_B5_B8_IN
3G TX-PA
TRXB1
TRXB2
TRXB5
TRXB8
3G RX
3GB1_RXP
3GB1_RXN
3GB2_RXP
3GB2_RXN
3GB5_RXP
3GB5_RXN
3GB8_RXP
3GB8_RXN
To MT6323 IF
Co-TSX
AUXADC_TSX
AUXADC_GND
CLK
OUT_32K
CLK4_AUDIO
AUXADC_REF
3G TX Control
B5_CPL_OUT_3G_ALL
BPI_4_W_PA_B1_EN
BPI_5_W_PA_B2_EN
BPI_6_W_PA_B5_EN
BPI_7_W_PA_B8_EN
BPI_10
BPI_11
VM0
VM1
GPIO
EINT_ACC
GPIO_FLASH_STB
26M
XO1
XO2
VBAT
C351 33pF
C352 100nF
C353 1uF
C354 22uF
GGE_PA_LB_IN
C356 18pF
L352 NC
L353 NC
GGE_PA_HB_IN
C360 56pF
L354 NC
L355 NC
BS2
R354 1K
C362 22pF
BS1
R356 1K
C364 22pF
U351
HS8684
SKY77590
TX_HB_IN
TX_LB_IN
BS2
BS1
VBATT
VCC
GND
MODE
TXEN
VRAMP
TRX_1
TRX_2
TRX_3
TRX_4
TRX_5
TRX_6
ANT
R396 0R
R392 NC
R395 0R
R394 0R
R393 NC
C361 220pF
R353 24K
R355 1K
C363 22pF
R357 1K
C365 22pF
C355 33pF
C359 NC
L351 18nH
CON351
RF_TEST_CON_818000163
R351 0R
C357 NC
C358 NC
ANT351
ANT352
Coaxial cable
CON3102 to CON3601
2G_LB_RX
R352 10K
WG_GGE_PA_VRAMP
GGE_PA_EN
MODE
VPA_PMU
C369 2.2uF
U10-B
MT8321 - RF
BPI
RF Power
GND_RF
RFI-RX
RFI-TX
CLK
MISC
LNA 3
LNA 1
LNA 2
LNA 4
VRF18_PMU
C366 0.47uF
C367 0.47uF
VTCXO_PMU
C368 1uF
C370 0.47uF
C373 0.47uF
R360 2K
R361 26.1R
R362 26.1R
R363 35.7R
B5_CPL_OUT_3G_ALL
U / MT8321
Z351
BALUN_LFB21914MDZ3D384
R358 0R
R359 0R
C371 NC
C372 NC
C374 NC
L361 6.8nH
L356 15nH
L357 NC
L358 39nH
L359 15nH
L360 5.6nH
L362 NC
L363 3.0nH
L364 5.6nH
LBIN
LBOUT
HBIN
HBOUT
GND
VD
CTL
VTCXO_PMU
TP881
OUT_32K
CLK4_AUDIO
XO2
XO1
VXODIG
EN_32K_TP1
XMODE_TP2
XO_NFC_TP3
XO_AUD_TP4
OUT32K
NC_F3
XTAL2
XTAL1
RCAL
VCOMON
DET
DETGND
APC
TMEAS
MODE
Logic
DCXO_32K_EN
XMODE
VXODIG
VCTCXO
DCXO + 32K XO
DCXO + 32K-Less
default
0(GND)
1(VIO18)
1(VTXCO22)
Title
31_RF_TXM_2G
Size
D
MTK Confidential
Date: Thursday, November 12, 2015
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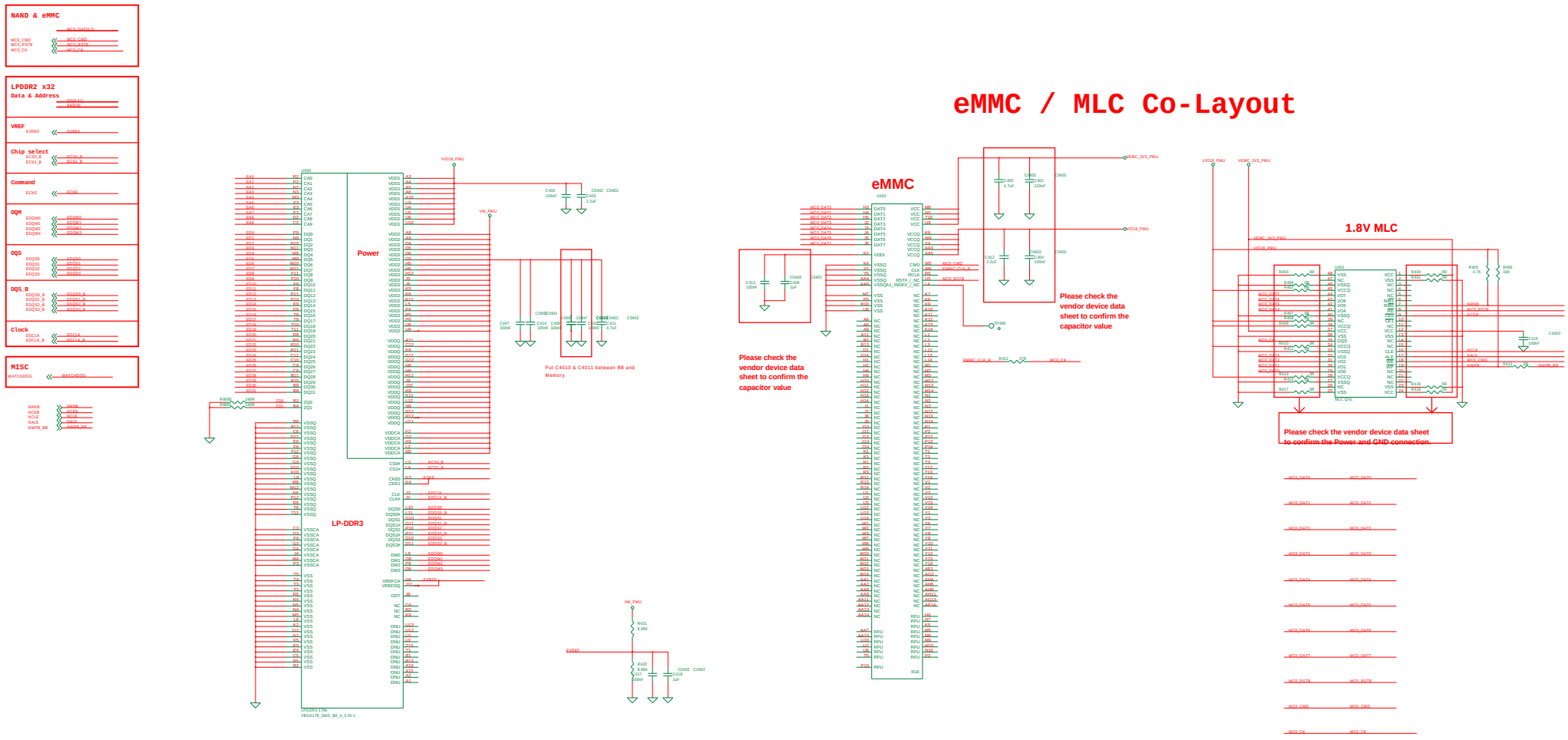
eMMC / MLC Co-Layout



File	40_Memory_eMMC_NAND_LPDDR2
Size	A3
	MTK Confidential
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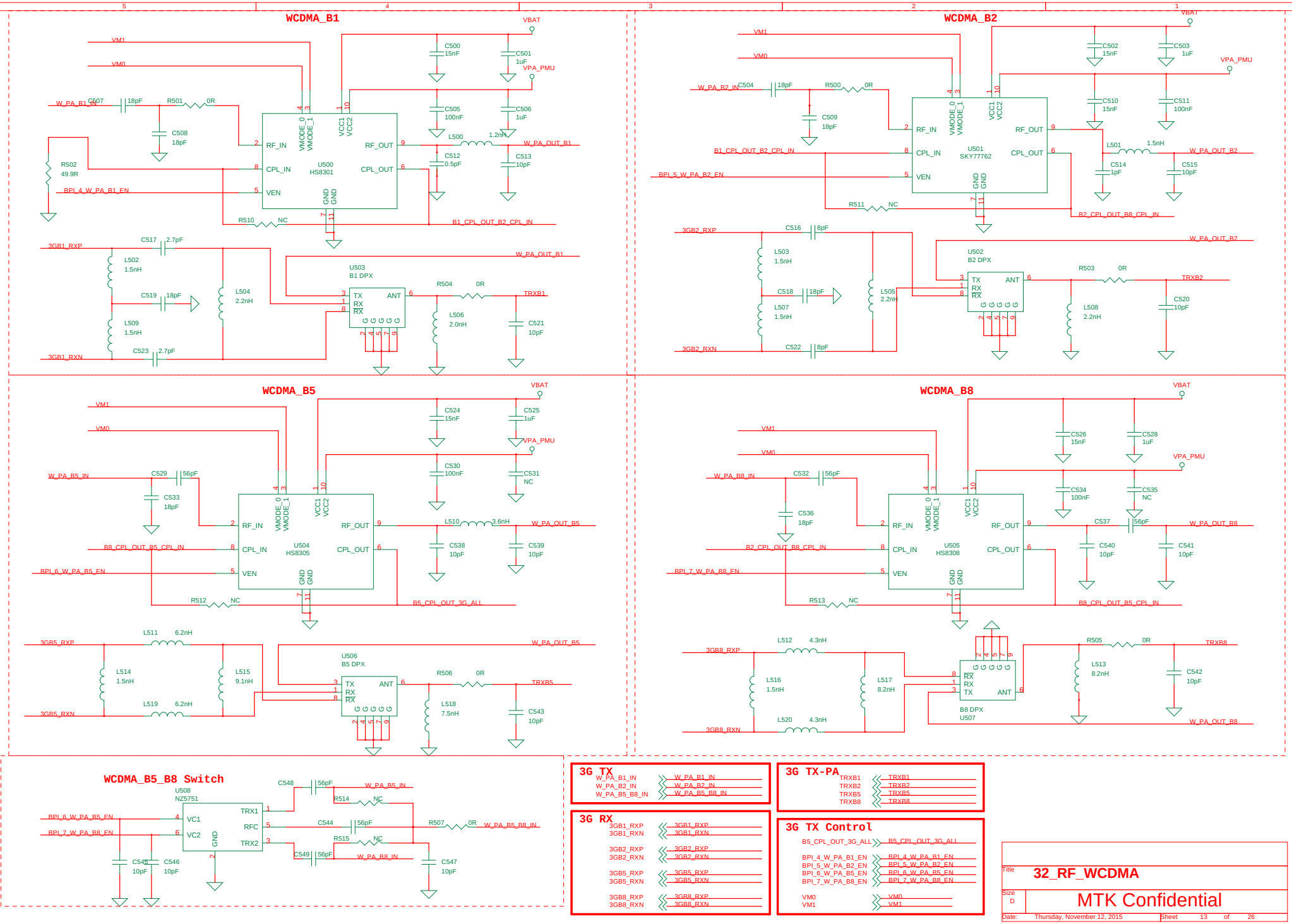

Title	32_RF_WCDMA
Size D	MTK Confidential
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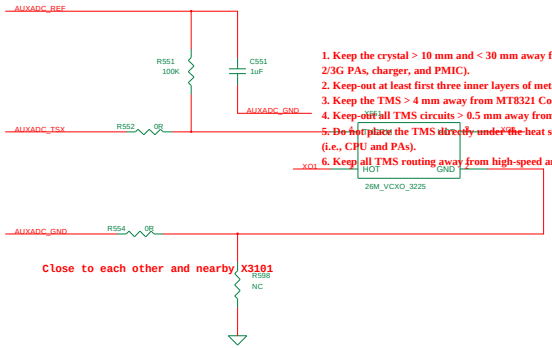
26M

XO1
XO2
AUXADC_REF
AUXADC_TSX
AUXADC_GND

1.Route AUXADC_REF/AUXADC_TSX with 3mil trace width
2.Route AUXADC_REF/AUXADC_TSX as differential trace with well GND shielding
3.Route AUXADC_GND with 15mil trace width under AUXADC_REF/AUXADC_TSX trace to provide return current path



1. Keep the crystal > 10 mm and < 30 mm away from the heat sources (Priority: 2/3G PAs, charger, and PMIC).
2. Keep-out at least first three inner layers of metal for all TMS circuits.
3. Keep the TMS > 4 mm away from MT8321 Co-TMS.
4. Keep-out all TMS circuits > 0.5 mm away from the surrounding metal.
5. Do not place the TMS directly under the heat sources that on the opposite side (i.e., CPU and PAs).
6. Keep all TMS routing away from high-speed and power traces.

Title	33_RF_Clock
Size D	MTK Confidential
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C0402

Flash LED 5V Boost

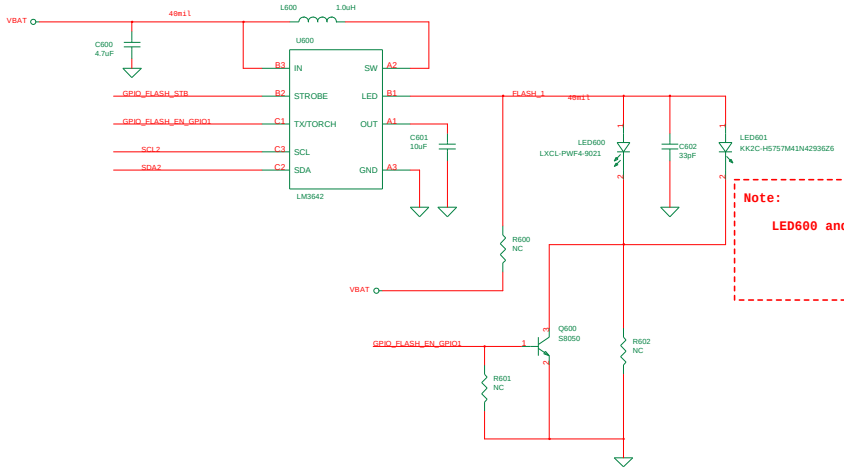
GPIO_FLASH_STB — GPIO_FLASH_STB
GPIO_FLASH_EN_GPIO1 — GPIO_FLASH_EN_GPIO1
SCL2 — SCL2
SDA2 — SDA2

LCM Backlight Driver

LCM_LEDA — LCM_LEDA
LCM_LEDK — LCM_LEDK
DISP_PWM0 — DISP_PWM0

Flash LED 5V Boost

Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)



Note:

LED600 and LED601 dual layout!!

File	23_POWER_THIRD PARTY
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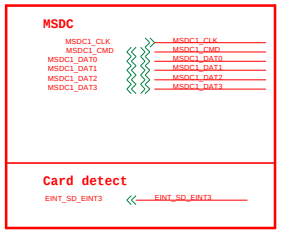
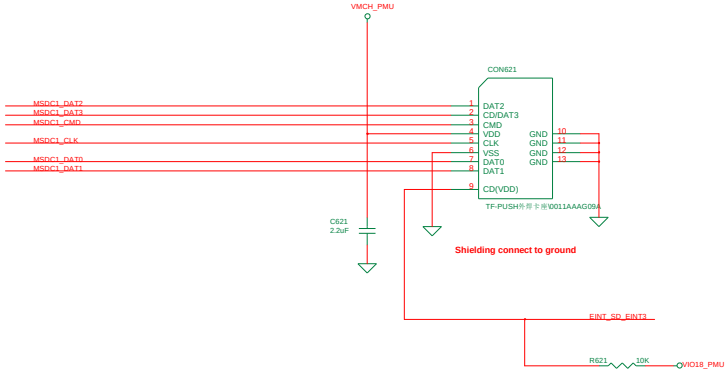


SD CARD



Based on your system level design , if better ESD/desense performance is needed on your system.

Schematic design notice of "41_MEMORY_SD Card" page.

Note 41-1:
The equivalent capacitance of ESD protection device must be <=1pF
-- otherwise it will result in NFC card mode function fail.

Note 41-2: Depends on system design to add ESD protection componemt or not.

Title	41_MEMORY_SD Card
Size D	MTK Confidential
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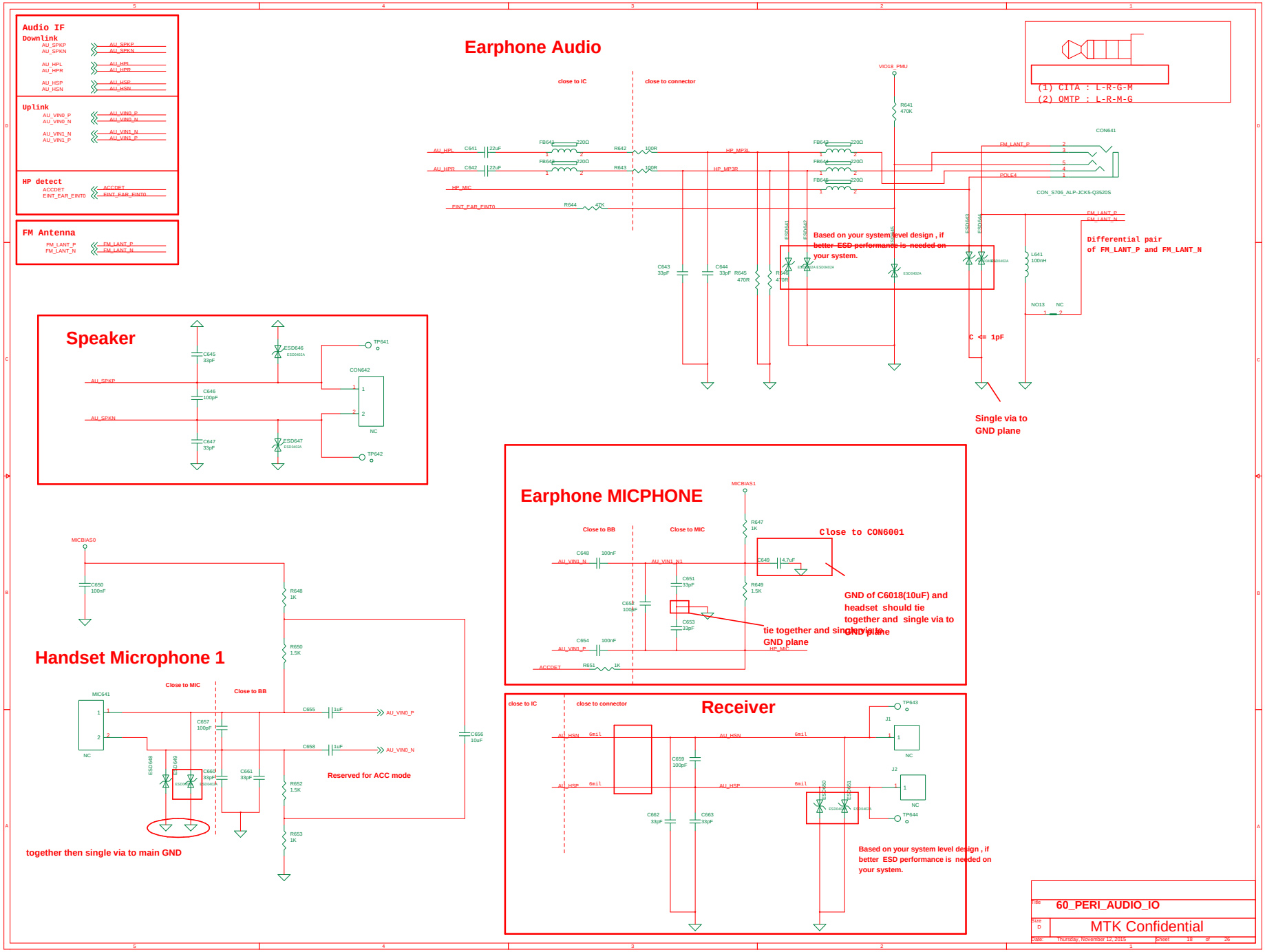
C0402



File	60_PERI_AUDIO_IO
Size D	MTK Confidential
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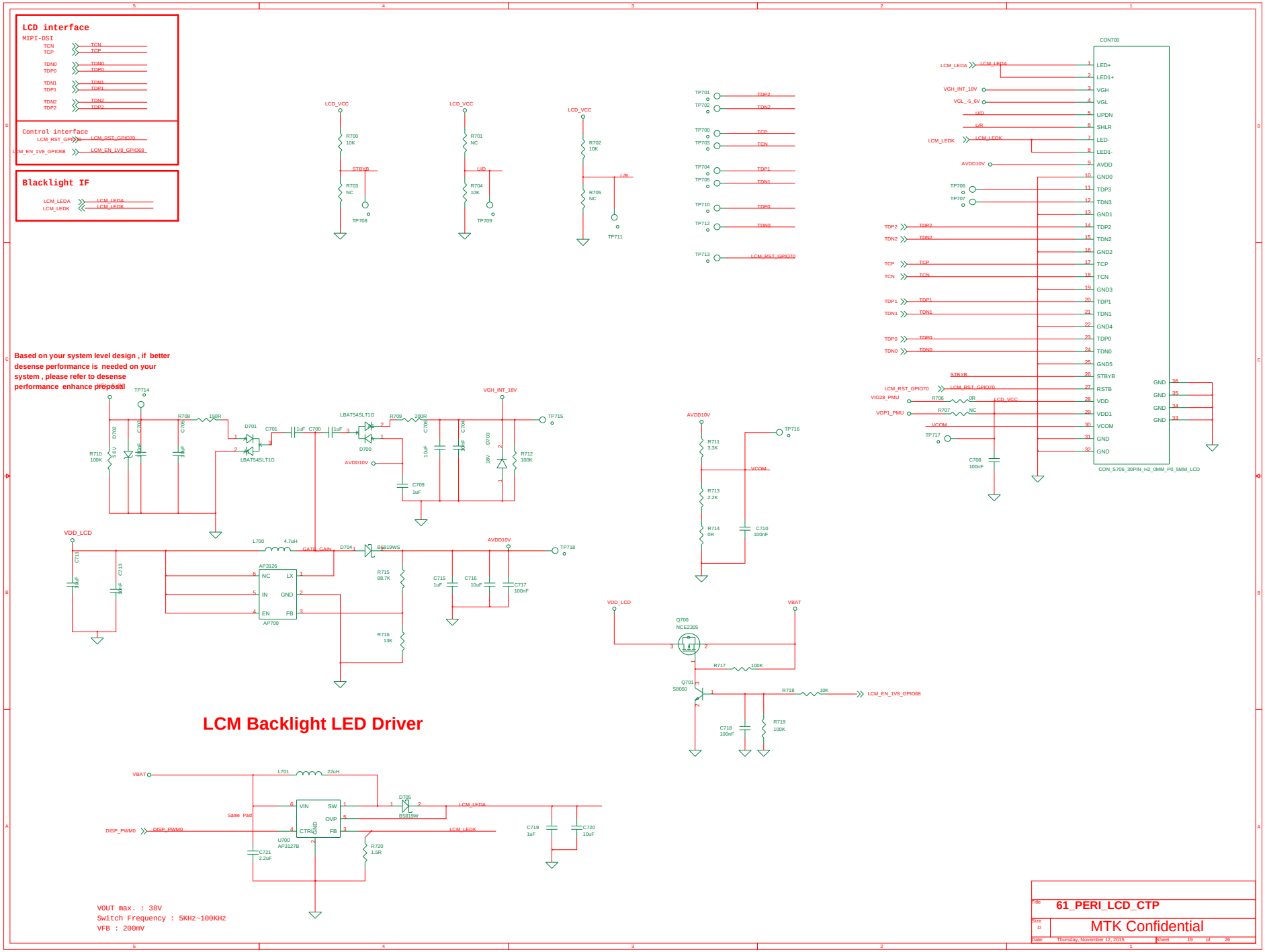
LCD interface
MIPI-DSI
TCN
TCP
TDN0
TDP0
TDN1
TDP1
TDN2
TDP2
Control interface
LCM_RST_GPIO70
LCM_EN_1V8_GPIO68
Blacklight IF
LCM_LEDA
LCM_LEDK
Based on your system level design , if better desense performance is needed on your system , please refer to desense performance enhance proposal
LCM Backlight LED Driver
VOUT max. : 38V
Switch Frequency : 5KHz~100KHz
VFB : 200mV
CON700
CON_S706_30PIN_H2_0MM_P0_5MM_LCD
AP3126
AP700
U700
AP3127B
Q700
NCE2305
Q701
S8050
VDD_LCD
VBAT
VGH_INT_18V
AVDD10V
LCD_VCC
STBYB
UID
L/R
Title
61_PERI_LCD_CTP
Size
D
MTK Confidential
Date:
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of
26

Camera IF

Main Cam MIPI_CSI

RCN	RCN
RCP	RCP
RDN0	RDN0
RDP0	RDP0
RDN1	RDN1
RDP1	RDP1

Main Cam control

CAM_PDN0_GPIO71	CAM_PDN0_GPIO71
CAM_RST0_GPIO73	CAM_RST0_GPIO73
CAM_CLK0	CAM_CLK0

Front Cam MIPI_CSI

RCP_A	RCP_A
RCN_A	RCN_A
RDP0_A	RDP0_A
RDN0_A	RDN0_A

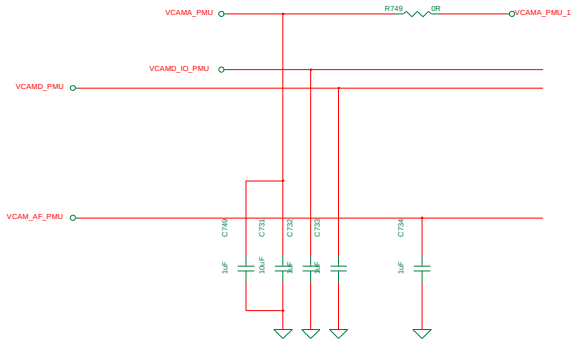
Front Cam control

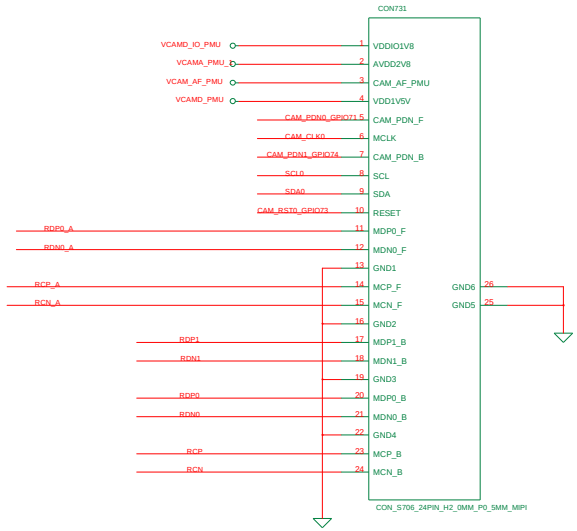
CAM_CLK1	CAM_CLK1
CAM_PDN1_GPIO74	CAM_PDN1_GPIO74

CAM I2C

SCL0	SCL0
SDA0	SDA0

Rear camera (IMX179) I2C address: 0X10 (Write:0x20, Read:0x21)
AF driver (F8N03C) I2C address: 0x0C (Write:0x18 , Read:0x19)





Title	62_PERI_CAMERA
Size D	MTK Confidential
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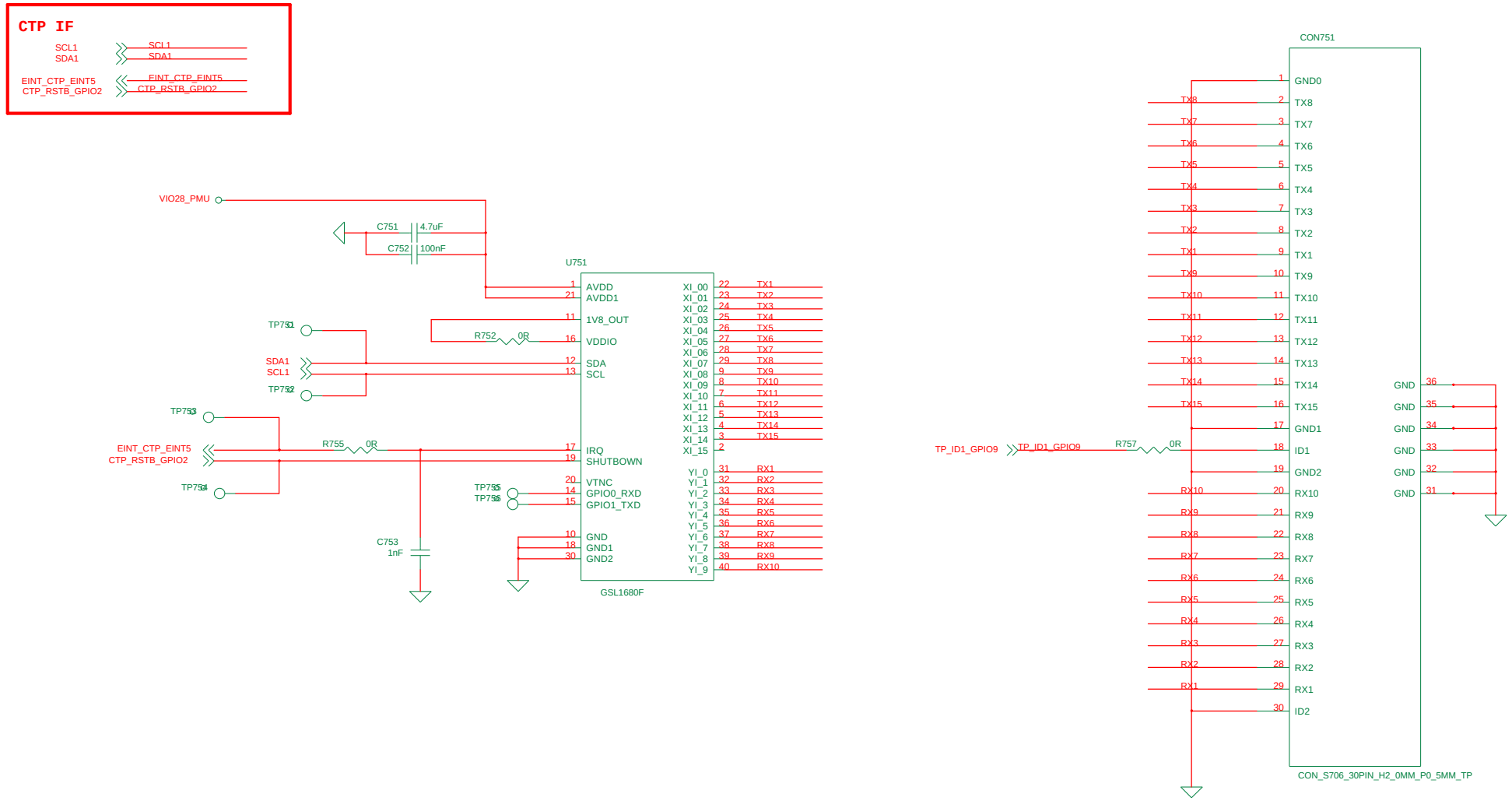
C0402



Title **62_PERI_CAMERA**

Size D

MTK Confidential

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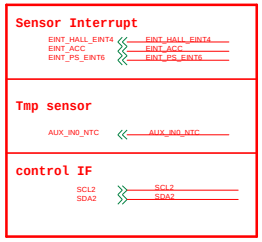
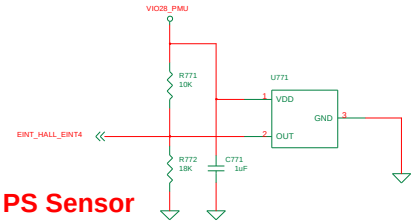
C0402



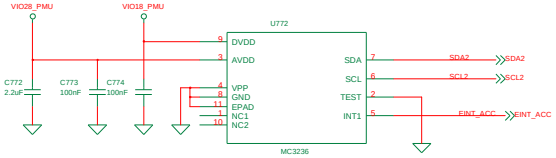


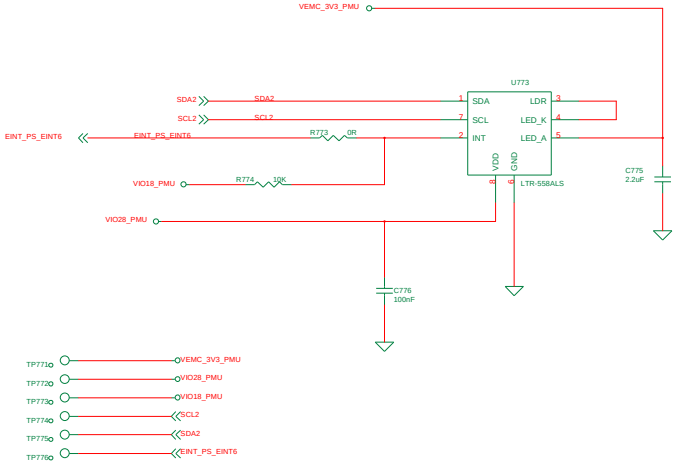
PS Sensor

CM36652 / RGB + PS I2C address: 0X60 (Write:0xC0, Read:0xC1)

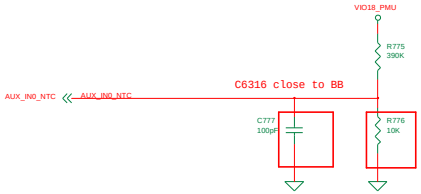
Accelerometer

MC3233 / Accelerometer I2C address: 0x4C (Write:0x98, Read:0x99)





Thermistor / To sense board level temperature



NTC6301 close to BB ,and located in the same layer
(can refer to thermal design notice)

Title	63_PERI_SENSORS
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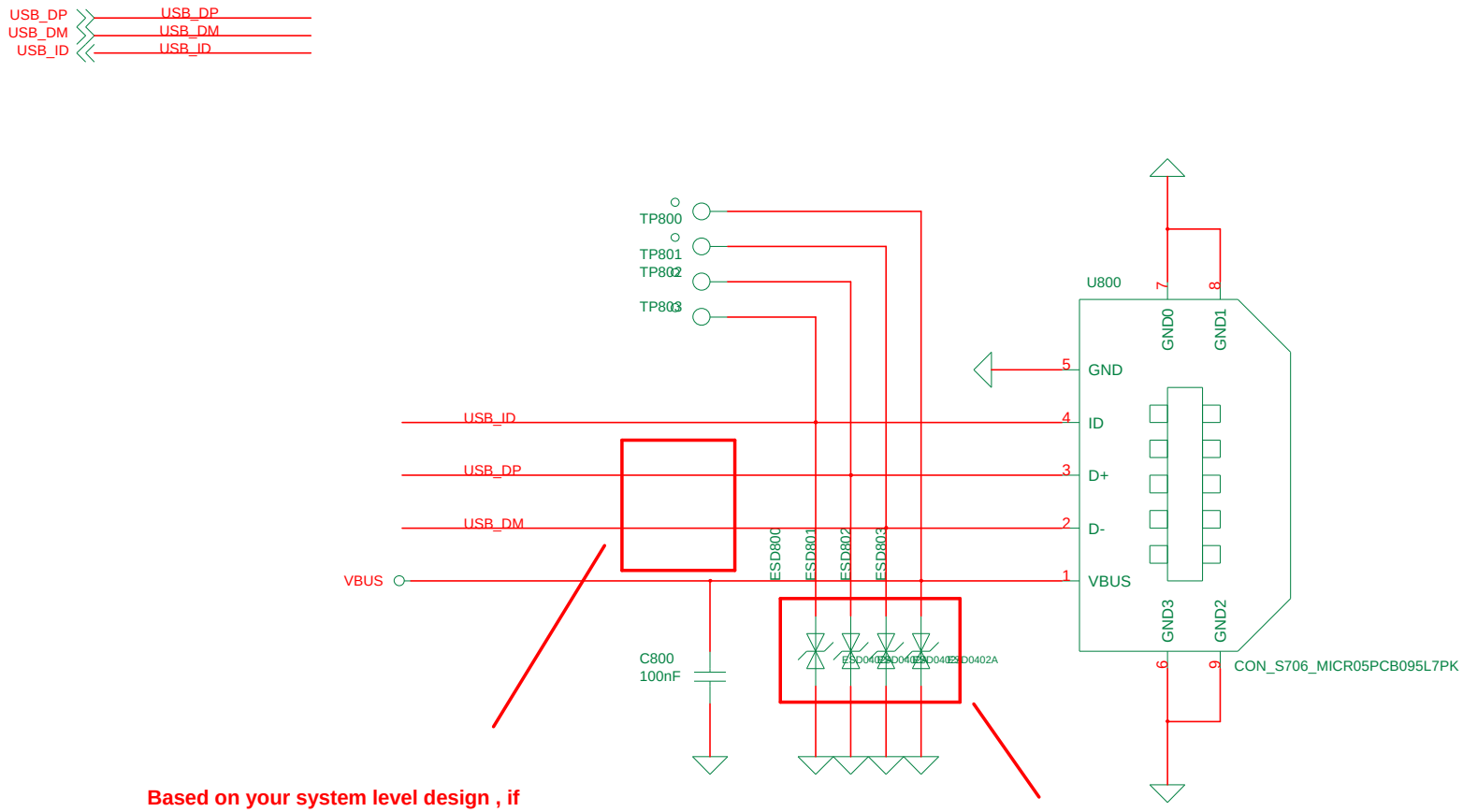
C0602



Based on your system level design , if better desense performance is needed on your system.

Based on your system level design , if better ESD performance is needed on your system.

Title	**64_PERI_USB_MHL**
Size D	MTK Confidential
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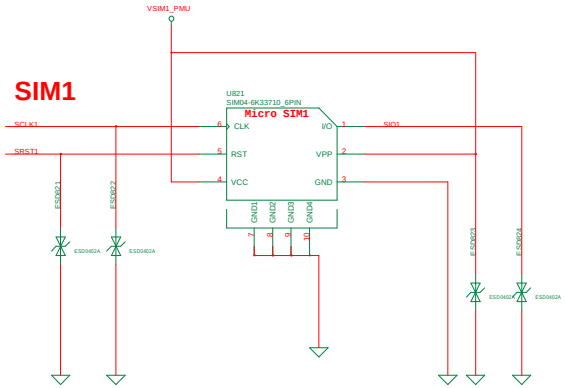
C0402

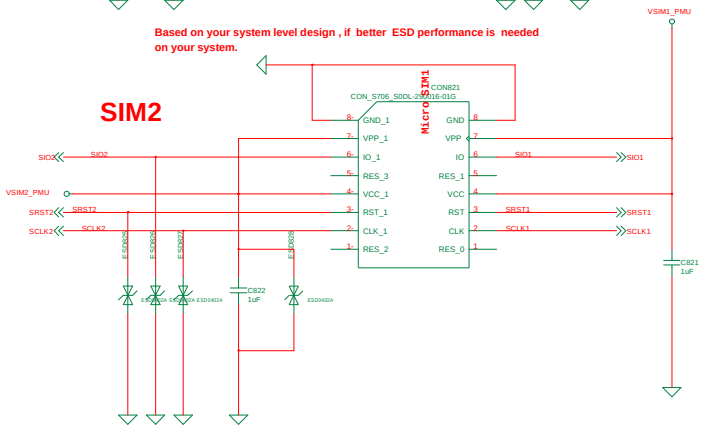
ESD0402A

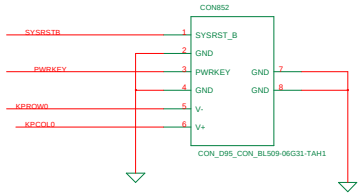
SIM1



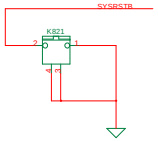
Based on your system level design , if better ESD performance is needed on your system.

SIM2



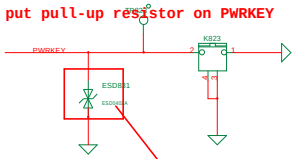


RESET KEY

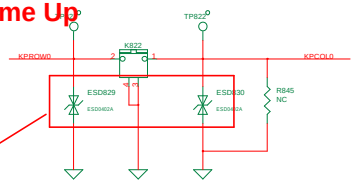


Power Key

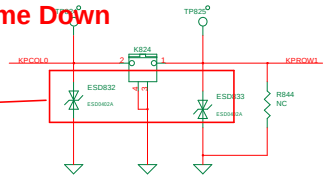
DO NOT put pull-up resistor on PWRKEY



Volume Up



Volume Down



	KCOL0	KCOL1
KROW0	Up	
KROW1	Down	

Based on your system level design , if better ESD performance is needed on your system , please refer to ESD performance enhance proposal

Title	65_PERI_Dual_SIM_ICUSB_KEYPAD
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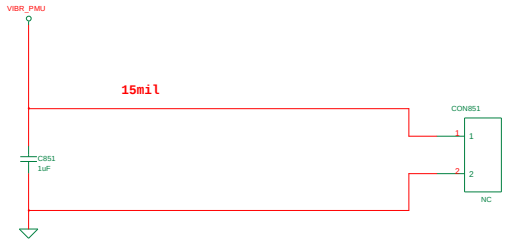
C0603

VIBRATOR



File	66_PERI_VIBRATOR
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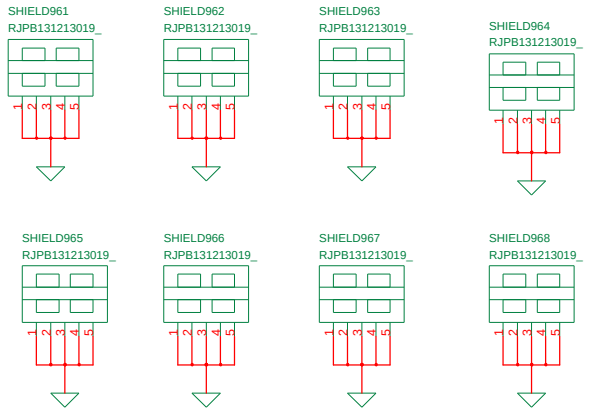
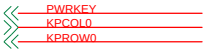
C0402



JTAG

KP IF

PWRKEY
KPCOL0
KPROW0

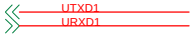


SIM1

SIM1_SCLK

UART

UTXD1
URXD1



for debug ONLY

(SIM1_SCLK , AUD_CLK_MOSI)
(0, 0) : Normal function
(0, 1) : SPI1
(1, 0) : MSDC1
(1, 1) : CAM

FD961 NC
FD962 NC
FD963 NC
FD964 NC

Title	90_DEBUG_IO
Size D	MTK Confidential
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