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SRM955

Hardware Design Manual

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SRM955 Hardware Design Mannual
V1.00

Foreword

Thanks for using the SRM955 module provided by Meige Smart. This product can provide data communication services. Please read the design manual carefully before use, it will help you fully understand the function of the module.

The company is not responsible for property damage or personal injury caused by the user's abnormal operation. Users are requested to develop corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety precautions you should be aware of when using mobile products.

Before making a statement, the company has the right to modify the contents of this manual according to the needs of technological development.

Content

Revision History

Time	Version	Revision Rreason	Author
2022-04	1.00	Initial establishment	Hardware Department

1. Introduction

This document describes the hardware application interface of the module, including circuit connections and radio frequency interfaces in related applications. It can help users to quickly understand the detailed information of the module's interface definition, electrical performance and structural dimensions. Combined with this document and other application documents, users can quickly use modules to design mobile communication applications.

2. Module Overview

The main chip used in the SRM955 series core board is Qualcomm Snapdragon 5G SoC QCM6490, which adopts 6nm process technology and has a built-in 8-core Kryo CPU 6xx (Kryo Gold plus: 1 high-performance core at 2.7GHz, Kryo Gold: 3 high-performance cores at 2.4GHz Performance cores, Kryo Silver: 4 1.9GHz low-power cores).

SRM955 is equipped with UFS3.1+LPDDR5 UMCP by default, and the capacity is 128GB+8GB. SRM955 is a broadband intelligent wireless communication module suitable for 5GNR/TD-LTE/FDD-LTE multiple network standards.

The working frequency bands supported by the SRM955 module are:

5GNR: N2/N5/N12/N25/N30/N38/N41/N48/N66/N71/N77/N78

Among them, N41/N77/78 do 2T4R and support HPUE

- TDD-LTE: B38/B41/B42/B43/B48
- FDD-LTE: B2/B4/B5/B12/B13/B14/B17/B25/B29/B30/B46/B66/B71

SRM955 integrates rich functional interfaces. It can be widely used in video recorders, smart cockpits, smart POS cash registers, logistics terminals, VR Cameras, smart robots, video surveillance, security surveillance, smart information collection equipment, smart handheld terminals, drones and other products under 5G networks.

The physical interface of the module is the 536 PIN LGA pad, which provides the following hardware interfaces:

- One-way LCD interface（MIPI-DSI）
- Five-way Camera interface（MIPI-CSI）
- Four-way flash interface
- Three-way indicator interface
- Two-way USB2.0 interface
- One-way USB3.1 interface
- Four-way analog MIC input interfaces
- Three-way digital MIC interface
- Two sets of I2S interfaces (multiplexing physical interface with digital MIC)
- Three-way analog audio output interface (headphone, earpiece, AUX)
- Two-way UIM card interface
- GPIO interface
- Three-way 1.8V UART interface, support four-wire or two-wire
- Ten-way groups of I2C interfaces
- One set of I3C interface
- Two sets of SPI interfaces
- One set of PCIe interface (2-lane Gen3)
- One SD card interface
- Support GNSS, WiFi, Bluetooth 5.1 function

2.1. Main Features Of The Module

Table 2.1：Main features of the module

Product features		Describe
Platform		Qualcomm QCM6490
CPU		8 nuclear Kryo CPU 6xx
GPU		Adreno GPU 6XX@812MHz
System Memory		UMCP，128GB UFS3.1+8GB LPDDR5
Operating System		Android 11.0
Size		55*45*3.95mm，536pin of LGA package
America Edition		5GNR: N2/N5/N12/N25/N30/N38/N41/N48/N66/N71/N77/N78 Among them, N41/N77/78 do 2T4R and support HPUE TDD-LTE: B38/B41/B42/B43/B48 FDD-LTE: B2/B4/B5/B12/B13/B14/B17/B25/B29/B30/B46/B66/B71
Wi-Fi		WCN6856: 2x2 IEEE 802.11a/b/g/n/ac/ax 2.4G&5G
Bluetooth		BT 5.2
FM		Not support
GNSS		GPS L1&L5/Beidou/Glonass/Galileo/NavIC/IRNSS
Data Access	5G NR	2.12GMbps/450Mbps
	LTE	Cat 12 FDD-LTE 1200/210Mbps

SIM		DSDS Dual SIM Dual Standby 3.0/1.8V Support SIM card hot swap NR Sub-6 SA+/L Sub-6 NSA(NR+LTE)+L
Display		FHD+ 144Hz QCLTM, HDR10+,WCG
		LCD Size: User defined
		Interface: LCM：MIPI DSI 4-lane;
Camera		Interface: Can support five groups of CSI, each group is 4-Lane, supports D-PHY 1.2 (2.5Gbps/lane) or C-PHY 1.2 (10.26Gbps/T)
		Triple 14-bit image signal processing (ISP) + two lite ISP 22 + 22 + 22MP, 64 MP/30 fps
	Video decode	4K60 for H.264/H.265/P9
	Video encode	Up to 4K30 for H.264/H.265
Input Device		Keys (PWR key, Home, RESET, VOL+, VOL-)
		Capacitive TP
Reset		Support hardware reset
Application	The name of	Description of main functions

Interface	the interface	
	VBAT	4pin, module power input, 3.5V ~ 4.35V, nominal value 3.8V
	SDIO	TF Card, up to 128GB
	USB2.0(3.0)	Support OTG USB_BOOT（Force USB boot for emergency download）
	BLSP ports	QUP(SE0~SE7)、QUP1(SE1~SE6), 4-bits each, multiplexed serial interface functions
	UART	Support 3-way UART by default（Expandable via QUP interface）
	I2C	By default, 10 channels of I2C are supported, of which 6 channels are dedicated I2C（Expandable via QUP interface）
	SPI(master only)	Two sets of SPI are supported by default (expandable through the QUP interface）
	ADC	Support 8-channel ADC
	Charging function	Support QC4.0+USB PD
	Motor	Support ERM
	GPIO	103个GPIO
	VCOIN	Battery backup for real time clock
	RF interface	ANT0:（5G:N2/N5/N12/N25/N30/N38/N41/N66/N71 4G:B2/B4/B5/B12/B13/B14/B17/B25/B29/B30/B66/B71 / B38/B41） ANT1:（LTE DRX: B2/B4/B25/B30/B66/B5/B12/B13/B14/B17/B29/B71/B46,N77/N78) ANT2: (N41/N77/N78) ANT3: (N41/N77/N78) ANT4: (LTE TRX: B2/B4/B25/B30/B66,N77/N78) ANT5: GNSS ANT6:WiFi/BT ANT0 ANT7:Wifi ANT1
	Audio	4-way analog MIC interface 3-way digital MIC interface 2 groups of I2S interface (multiplexing physical interface with digital MIC) 1 channel AUX signal (requires external audio PA) 1 way handset 1 channel stereo headphone (including headphone MIC)

2.2. Functional Block Diagram Of The Module

The following figure lists the main functional parts of the module:

QCM6490 baseband chip

- PM7325, PM7350C, PM7250B, PMK7325 power management chip
- WCN6856-WIFI/BT combo chip
- Antenna interface
- LCD/CAM-MIPI interface
- UMCP memory chip
- AUDIO interface
- USB, SD card, SIM card interface, etc.

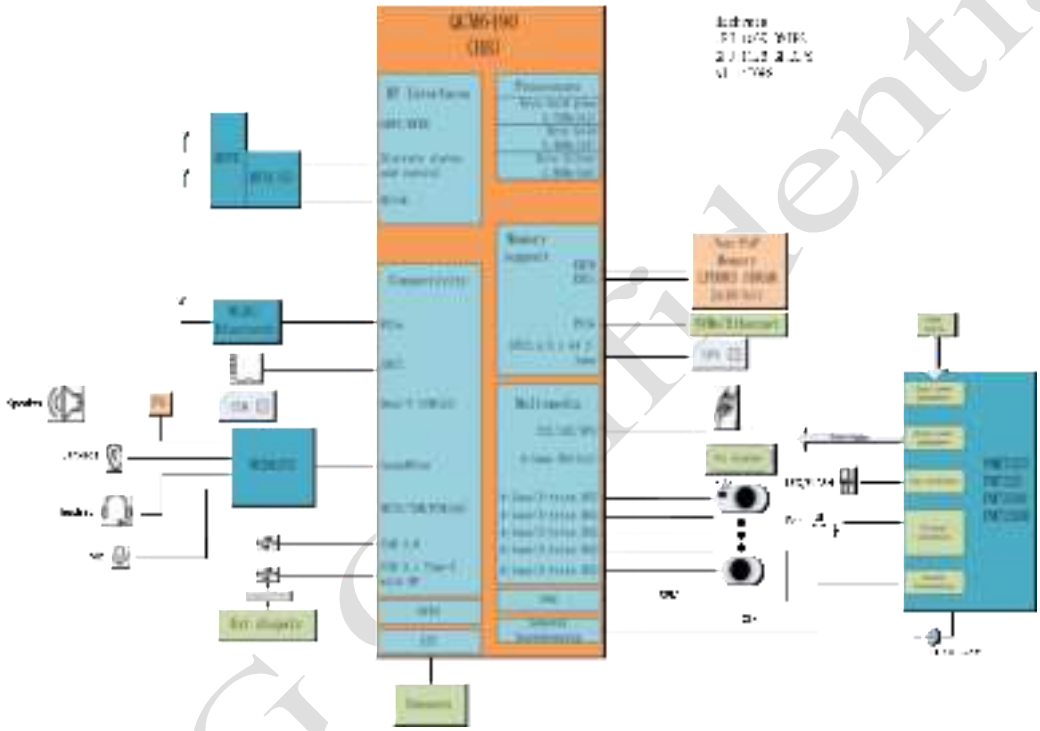


Figure 2.1: Module function box

3. Module Packaging

3.1. Pinout Diagram

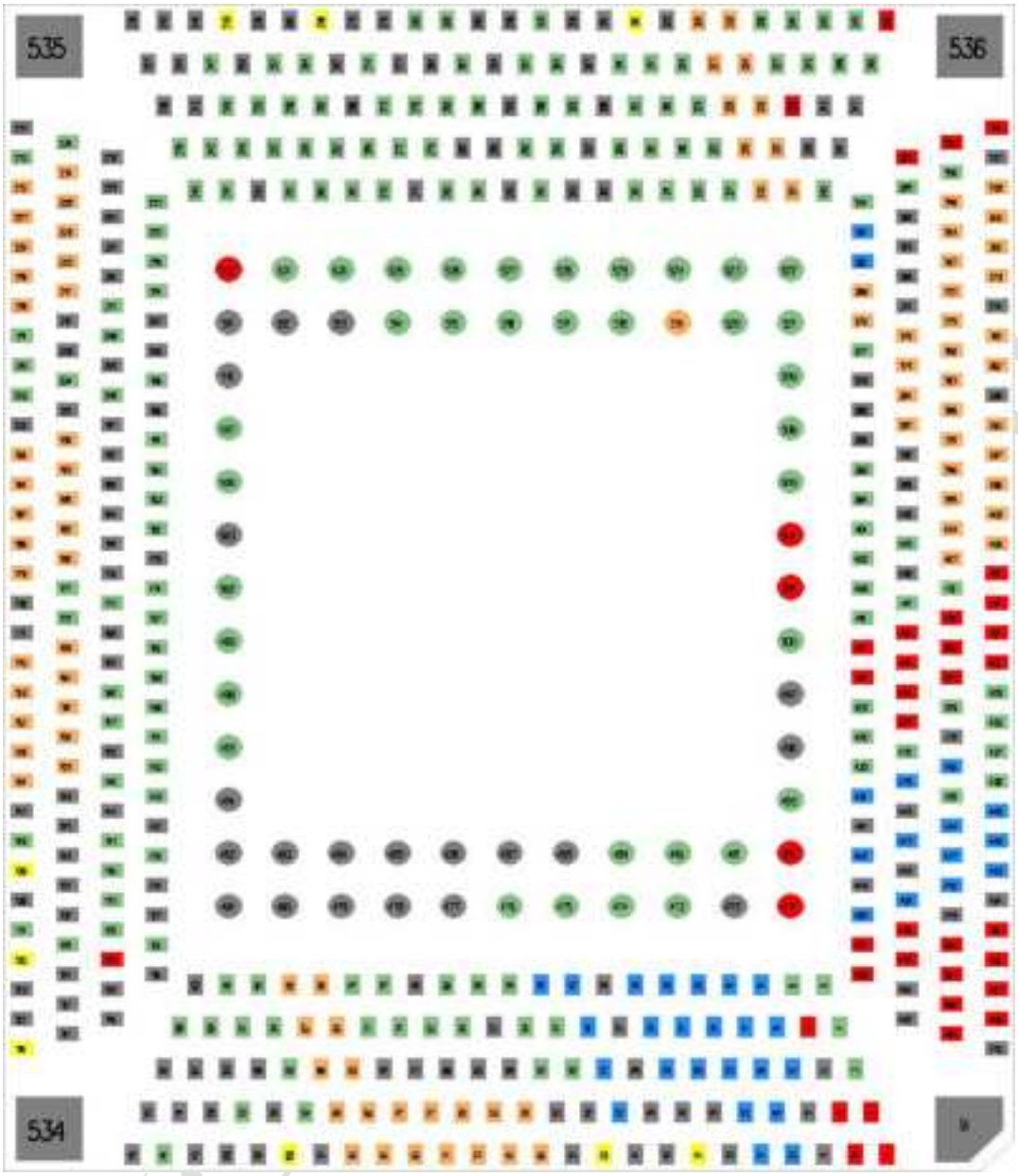


Figure 3.1: Module Pin Diagram

Note: The yellow PIN represents the antenna interface, the orange PIN represents the high-speed signal interface, the blue PIN represents the audio, ADC and other analog signal interfaces, the red PIN represents the power supply interface, and the green PIN represents the general signal interface.

3.2. Description Of Module Pins

Table 3.1: Pin Descriptions

The name of the pin	Pin number	I/O	Describe	Remark
Power				
VBAT	460、461、462、463	I/O	The module provides 4 VBAT power pins. Voltage range 3.5V to 4.35V.	External need to increase capacitance
VPH_PWR	456、457、458、	O	System power output, typical	

	458		value is 3.8V. Can supply power to peripherals.	and surge tube protection
USB_VBUS	466、467、468、469	I/O	Charging input interface and OTG power output interface. Support USB plug-in detection, maximum support 12V charging.	
VCOIN	471	I/O	When the system power VBAT is not in place, the external backup battery provides power to the system real-time clock. The backup battery is charged while VBAT is in place.	Connect a 3V button battery or a large capacitor to the VCOIN pin.
VREG_L2C_1P8(RESERVED)	416	O	1.8V power output, DMIC reserved power, default NC	150mA
VREG_L3C_3P0(TPVDD)	501	O	3.0V power output, can be used for TP VDD power supply	150mA
VREG_L4C_1P8_3P0(VSIM1)	338	O	1.8/3.0V power output, UIM1 power supply pin	150mA
VREG_L5C_1P8_3P0(VSIM2)	350	O	1.8/3.0V power output, UIM2 power supply pin	150mA
VREG_L6C_2P96(SDVIO)	413	O	3V power output for SD card signal pull-up	150mA
VREG_L7C_3P0(SENSOR_VDD)	417	O	3V power output, it will be turned off during standby, and can be used to power the Sensor.	300mA
VREG_L8C_1P8(SENSOR_VDDIO)	504	O	1.8V power output, it will be turned off during standby, used as IO power supply for Sensor, CAM, TP	300mA
VREG_L9C_2P96(SD_VDD)	414	O	3V power output for SD card VCC power supply	600mA
VREG_L11C_2P8(WCN_VDD)	415	O	2.8V power output for WCN_VDD power supply	300mA
VREG_L12C_1P8(OLED VDDIO)	418	O	1.8V power output, it will be turned off during standby, and can be used for OLED IO power supply.	150mA
VREG_L13C_3P0(OLED VCI)	427	O	3V power output, it will be turned off during standby, and can be used for OLED VCI power supply.	150mA
VREG_L2B_3P072(USBHS_VIO)	492	O	3.1V power output for USB_HS, PDPHY, etc.	150mA
VREG_L11B_1P776(SDR_VDD)	125	O	1.776V power output, can be used for RF SDR, QPM and	300mA

			other related power supply	
VREG_L18B_1P8	419	O	1.8V power output, always supply when power on, used for power supply of CPU, Memory, IO pull-up, etc.	300mA
VREG_L19B_1P8(RF_VDDIO)	532	O	1.8V power output, can be used for RFFE loads power supply。	300mA
VREG_SYS_1P8	424	O	1.8V power output, only used for SMB parallel charging chip.	50mA
GND	8、11、12、29、30、32、29、30、32、36、37、38、39、40、41、49、51、52、57、58、63、66、68、73、78、91、98、99、101、103、105、107、108、109、110、111、112、113、115、117、118、119、120、121、122、123、124、125、127、132、134、137、138、140、142、144、145、147、148、152、165、168、171、175、176、178、181、184、189、192、197、198、201、202、205、206、207、209、212、216、221、224、229、230、235、236、237、238、243、244、245、246、250、254、256、265、267、268、271、275、276、277、282、284、289、290、293、294、295、296、300、301、302、306、307、308、315、325、339、341、342、347、357、360、363、368、371、374、378、385、386、389、392、395、400、408、431、440、441、448、449、454、455、464、465、470、472、477、478、479、480、481、482、483、484、485、486、487、488、494、496、497、503、510、511、512、513、533、534、535、536		Ground	
Main Display Interface (MIPI)				
MIPI_DSI0_CLK_N	406	O	MIPI_DSI clock line	
MIPI_DSI0_CLK_P	407	O		
MIPI_DSI0_LANE0_N	390	O	MIPI_DSI data line	
MIPI_DSI0_LANE0_P	391	O		
MIPI_DSI0_LANE1_N	396	O		
MIPI_DSI0_LANE1_P	397	O		
MIPI_DSI0_LANE2_N	398	O		
MIPI_DSI0_LANE2_P	399	O		
MIPI_DSI0_LANE3_N	404	O		
MIPI_DSI0_LANE3_P	405	O		
LCD_RST_N/GPIO44*	393	I/O	LCD reset pin	
LCD_TE/GPIO80*	401	I/O	LCD frame sync signal	
LCD_ID/GPIO46	394	I/O	LCD_ID signal	
BL_PWM/PM7350C_GPIO9	412	I/O	Backlight chip PWM control	

			signal	
UART(1.8V)				
DBG_UART_TX/GPIO22	528	O	UART data transmission	System Debug UART
DBG_UART_RX/GPIO23*	529	I	UART data reception	
UART2_TX/GPIO26	507	O	UART data transmission	
UART2_RX/GPIO27*	506	I	UART data reception	
UART1_TX/GPIO18*	157	O	UART data transmission	
UART1_RX/GPIO19*	158	I	UART data reception	
UIM interface				
UIM1_DATA	344	I	UIM1 data signal	
UIM1_CLK	343	O	UIM1 clock signal	
UIM1_RESET_N	337	O	UIM1 reset signal	
UIM1_PRESENT/GPIO116*	336	I/O	UIM1 insertion monitoring	
UIM2_DATA	349	I	UIM2 data signal	
UIM2_CLK	348	O	UIM2 clock signal	
UIM2_RESET_N	346	O	UIM2 reset signal	
UIM2_PRESENT/GPIO112*	345	I/O	UIM2 insertion monitoring	
REAR CAM				
MIPI_CSI0_CLK_P	232	O	REAR CAM MIPI clock	
MIPI_CSI0_CLK_N	231	O		
MIPI_CSI0_LANE0_P	228	I	REAR CAM MIPI data	
MIPI_CSI0_LANE0_N	227	I		
MIPI_CSI0_LANE1_P	226	I		
MIPI_CSI0_LANE1_N	225	I		
MIPI_CSI0_LANE2_P	220	I		
MIPI_CSI0_LANE2_N	219	I		
MIPI_CSI0_LANE3_P	218	I		
MIPI_CSI0_LANE3_N	217	I		
CCI_I2C0_SCL/GPIO70	223	I/O	REAR CAM I2C_SCL	
CCI_I2C0_SDA/GPIO69	222	I/O	REAR CAM I2C_SDA	
MCAM_PWD_N/GPIO107	215	I/O	REAR CAM sleep signal	
CAM_MCLK0/GPIO64	214	I/O	REAR CAM master clock	
CAM0_RST_N/GPIO20*	213	I/O	REAR CAM reset signal	
FRONT CAM				
MIPI_CSI3_CLK_P	86	O	FRONT CAM MIPI clock	
MIPI_CSI3_CLK_N	85	O		
MIPI_CSI3_LANE0_P	87	I	FRONT CAM MIPI data	

MIPI_CSI3_LANE0_N	84	I		
MIPI_CSI3_LANE1_P	88	I		
MIPI_CSI3_LANE1_N	83	I		
MIPI_CSI3_LANE2_P	89	I		
MIPI_CSI3_LANE2_N	82	I		
MIPI_CSI3_LANE3_P	90	I		
MIPI_CSI3_LANE3_N	81	I		
CCI_I2C3_SCL/GPIO76	94	I/O	FRONT CAM/RESERVED CAM I2C_SCL	
CCI_I2C3_SDA/GPIO75*	93	I/O	FRONT CAM/RESERVED CAM I2C_SDA	
SCAM_PWD_N/GPIO43*	96	I/O	FRONT CAM sleep signal	
CAM_MCLK3/GPIO67	97	I/O	FRONT CAM master clock	
CAM3_RST_N/GPIO78*	95	I/O	FRONT CAM reset signal	
DEPTH CAM				
MIPI_CSI1_CLK_P	80	O	DEPTH CAM MIPI clock	
MIPI_CSI1_CLK_N	79	O		
MIPI_CSI1_LANE0_P	72	I	DEPTH CAM MIPI data	
MIPI_CSI1_LANE0_N	71	I		
MIPI_CSI1_LANE1_P	70	I		
MIPI_CSI1_LANE1_N	69	I		
MIPI_CSI1_LANE2_P	62	I		
MIPI_CSI1_LANE2_N	61	I		
MIPI_CSI1_LANE3_P	60	I		
MIPI_CSI1_LANE3_N	59	I		
CCI_I2C1_SCL/GPIO72*	77	I/O	DEPTH CAM I2C_SCL	
CCI_I2C1_SDA/GPIO71	76	I/O	DEPTH CAM I2C_SDA	
DCAM_PWD_N/GPIO42	75	I/O	DEPTH CAM sleep signal	
CAM_MCLK1/GPIO65	74	I/O	DEPTH CAM master clock	
CAM1_RST_N/GPIO21*	67	I/O	DEPTH CAM reset signal	
RESERVED CAM1				
MIPI_CSI2_CLK_P	180	O	RESERVED CAM1 MIPI clock	
MIPI_CSI2_CLK_N	179	O		
MIPI_CSI2_LANE0_P	186	I	RESERVED CAM1 MIPI data	
MIPI_CSI2_LANE0_N	185	I		
MIPI_CSI2_LANE1_P	188	I		
MIPI_CSI2_LANE1_N	187	I		
MIPI_CSI2_LANE2_P	194	I		
MIPI_CSI2_LANE2_N	193	I		

MIPI_CSI2_LANE3_P	196	I		
MIPI_CSI2_LANE3_N	195	I		
CCI_I2C2_SCL/GPIO74	183	I/O	RESERVED CAM1 I2C_SCL	
CCI_I2C2_SDA/GPIO73	182	I/O	RESERVED CAM1 I2C_SDA	
FP_RST/GPIO35*	313	I/O	RESERVED CAM1 sleep signal	
CAM_MCLK2/GPIO66	190	I/O	RESERVED CAM1 master clock signal	
CAM2_RST_N/GPIO77*	191	I/O	RESERVED CAM1 reset signal	
RESERVED CAM2				
MIPI_CSI4_CLK_P	169	O	RESERVED CAM2 MIPI CLOCK	
MIPI_CSI4_CLK_N	170	O		
MIPI_CSI4_LANE0_P	163	I	RESERVED CAM2 MIPI DATA	
MIPI_CSI4_LANE0_N	164	I		
MIPI_CSI4_LANE1_P	161	I		
MIPI_CSI4_LANE1_N	162	I		
MIPI_CSI4_LANE2_P	155	I		
MIPI_CSI4_LANE2_N	156	I		
MIPI_CSI4_LANE3_P	153	I		
MIPI_CSI4_LANE3_N	154	I		
CAM_MCLK4/GPIO68*	151	I/O	RESERVED CAM2 master clock signal	
GPIO1	172	I/O	RESERVED CAM2 sleep signal	
MI2S_MCLK/GPIO96	283	I/O	RESERVED CAM2 reset signal	
CCI_I2C2_SCL/GPIO74	183	I/O	RESERVED CAM1 I2C_SCL	
CCI_I2C2_SDA/GPIO73	182	I/O	RESERVED CAM1 I2C_SDA	
Audio Port				
MIC1_IN_M	26	I	Main MIC negative	
MIC1_IN_P	25	I	Main MIC positive	
HPHMIC_IN2_P	21	I	Headphone MIC positive	
HPHMIC_IN2_M	22	I	Headphone MIC negative	
MIC3_IN_M	23	I	Noise reduction MIC negative	
MIC3_IN_P	24	I	Noise reduction MIC positive	
MIC_BIAS1	33	O	The BIAS voltage of the main mic and the auxiliary mic, used for silicon microphone design	
MIC_BIAS2	34	O	BIAS voltage of headphone MIC	
MIC_BIAS3	35	O	BIAS voltage of mic4 for silicon wheat design	
MIC4_IN_P	28	I	MIC4 positive	
MIC4_IN_M	27	I	MIC4 negative	

HSJ_HPH_R	16	O	Headphone right channel	
HSJ_HPH_L	15	O	Headphone left channel	
HSJ_HS_DET	13	I	Headphone plug-in detection	
HSJ_HPH_REF	14	I	Headphone reference ground	
WCD_EAR_OUT_P	17	O	earpiece output positive	
WCD_EAR_OUT_M	18	O	Headphone output negative	
WCD_AUX_P	19	O	External amplifier input positive	External amplifier input
WCD_AUX_M	20	O	External power amplifier input negative	
I2S1_DATA1/DMIC2_DATA/GPIO153*	56	I	Digital MIC2 data signal	
I2S1_DATA0/DMIC2_CLK/GPIO152	55	O	Digital MIC2 clock signal	
I2S1_CLK/DMIC1_CLK/GPIO150*	53	O	Digital MIC1 clock signal	
I2S1_WS/DMIC1_DATA/GPIO151*	54	I	Digital MIC1 data signal	
I2S2_DATA0/DMIC3_CLK/GPIO156*	287	O	Digital MIC3 clock signal	
I2S2_DATA1/DMIC3_DATA/GPIO157*	288	I	Digital MIC3 data signal	
SD INTERFACE				
SDCARD_DET_N/GPIO91*	498	I/O	SD card insertion and removal detection signal	
SDC2_CLK	379	I/O	SD card clock signal	
SDC2_CMD	380	I/O	SD card CMD signal	
SDC2_DATA_0	381	I/O	SD card data signal	
SDC2_DATA_1	382	I/O		
SDC2_DATA_2	383	I/O		
SDC2_DATA_3	384	I/O		
I2C				
SENSOR_I2C_SDA/GPIO161	47	I/O	SENSOR_I2C signal	Pull high to VREG_L8C_1P8
SENSOR_I2C_SCL/GPIO162	48	I/O		
NFC_I2C_SDA/GPIO36*	524	I/O	General purpose I2C signals	Pull high to VREG_L18B_1P8
NFC_I2C_SCL/GPIO37	525	I/O		
HDMI_I2C_SDA/GPIO8*	515	I/O	General purpose I2C signals	Pull high to VREG_L18B_1P8
HDMI_I2C_SCL/GPIO9	514	I/O		
TS_I2C_SDA/GPIO52*	409	I/O	TP_I2C signal	Pull high to VREG_L12C_1P8
TS_I2C_SCL/GPIO53	410	I/O		
APPS_I2C_SDA/GPIO4*	252	I/O	General purpose I2C signals	Pull high to

APPS_I2C_SCL/GPIO5	251	I/O		VREG_L18B_1P8
CCI_I2C0_SCL/GPIO70	223	I/O	R-CAM I2C signal	Pull high to CAM_IOVDD_1P8 (external LDO)
CCI_I2C0_SDA/GPIO69	222	I/O		
CCI_I2C2_SCL/GPIO74	183	I/O	F-CAM I2C signal	Pull high to CAM_IOVDD_1P8
CCI_I2C2_SDA/GPIO73	182	I/O		
CCI_I2C1_SCL/GPIO72*	77	I/O	D-CAM I2C signal	Pull high to CAM_IOVDD_1P8
CCI_I2C1_SDA/GPIO71	76	I/O		
CCI_I2C3_SCL/GPIO76	94	I/O	RESERVED CAM I2C signal	Pull high to CAM_IOVDD_1P8
CCI_I2C3_SDA/GPIO75*	93	I/O		
MAG_I2C_SDA/GPIO163	476	I/O	MAG sensor I2C signal	Pull high to VREG_L8C_1P8
MAG_I2C_SCL/GPIO164	475	I/O		
TP				
TS_I2C_SDA/GPIO52*	409	I/O	I2C signal	Pull high to VREG_L12C_1P8
TS_I2C_SCL/GPIO53	410	I/O	I2C signal	
TS_INT_N/GPIO81*	402	I/O	TP interrupt signal	
TS_RST_N/GPIO105	403	I/O	TP reset signal	
USB				
USB0_HS_DP	375	I/O	USB 2.0 DP signal	
USB0_HS_DM	376	I/O	USB 2.0 DM signal	
USB1_HS_D_P	369	I/O	USB 2.0 DP signal	Only supports host mode
USB1_HS_D_M	370	I/O	USB 2.0 DM signal	
USB0_SS_TX1_P	366	O	USB super-speed 1 transmit – plus	
USB0_SS_TX1_M	367	O	USB super-speed 1 transmit – minus	
USB0_SS_RX1_P	372	I	USB super-speed 1 receive – plus	
USB0_SS_RX1_M	373	I	USB super-speed 1 receive – minus	
USB0_SS_TX0_P	364	O	USB super-speed 0 transmit – plus	
USB0_SS_TX0_M	365	O	USB super-speed 0 transmit – minus	
USB0_SS_RX0_P	358	I	USB super-speed 0 receive – plus	

USB0_SS_RX0_M	359	I	USB super-speed 0 receive – minus	
USB_CC1	5	I/O	CC1 pin for the Type-C	
USB_CC2	6	I/O	CC2 pin for the Type-C	
PM7250B_USB_SBU1	3	I	Type-C side band signal SBU1; protected to 22 V max	
PM7250B_USB_SBU2	4	O	Type-C side band signal SBU2; protected to 22 V max	
USB_CONN_THERM	442	I	USB Type-C connector temperature sensor.	
USB_ID/GPIO60*	377	I	USB ID signal	
DP_AUX_P	361	I/O	DP_AUX_P signal	
DP_AUX_M	362	I/O	DP_AUX_M signal	
USB_CC_DIR	426	O	1.8V tri-state output indicates CC connection direction	Type-C: This pin is connected to 518pin Micro-USB: The pin NC
USB_OPTION	425	I	Select different PON items according to the pull-down resistor value	Type-C: The pin NC Micro-USB: This pin is grounded
USB_PHY_PS	518	I/O	USB_PHY_PS	Type-C: This pin is connected to 426pin Micro-USB: Connect this pin to the ground with a 1K resistor
Antenna interface				
ANT_0	316	I/O	2/3/4/5G main antenna	
ANT_1	50	I/O	2/3/4/5G diversity antenna, 5G main antenna	
ANT_2	31	I/O	5G SRS Antenna	
ANT_3	266	I/O	5G SRS Antenna	
ANT_4	255	I/O	5G main antenna, ENDC main antenna	
WIFI_CH1	116	I/O	WIFI/BT Antenna	
WIFI_CH0	100	I/O	WIFI/BT Antenna	
GPS_L1_ANT	130	I	GPS Antenna	
GPS_L5_ANT	139	I	GPS Antenna	
GPIO and default function (* to support interrupt wake-up port)				
GPIO0*	173	I/O	General-purpose GPIO, no default function	
GPIO1	172	I/O	General-purpose GPIO, no default function	
PCIE1_RESET_N/GPIO2	204	I/O	General purpose GPIO, default is PCIE1_RESET_N	

PCIE1_WAKE_N/GPIO3*	203	I/O	Generic GPIO, default is PCIE1_WAKE_N	
APPS_I2C_SDA/GPIO4*	252	I/O	General GPIO, default is APPS_I2C_SDA	
APPS_I2C_SCL/GPIO5	251	I/O	Generic GPIO, default is APPS_I2C_SCL	
EDP_CABC_EN/GPIO6	253	I/O	General-purpose GPIO, no default function	
GPIO7*	257	I/O	General-purpose GPIO, no default function	
HDMI_I2C_SDA/GPIO8*	515	I/O	Generic GPIO, default is HDMI_I2C_SDA	
HDMI_I2C_SCL/GPIO9	514	I/O	Generic GPIO, default is HDMI_I2C_SCL	
GPS_L1_ELNA_CTRL/GPIO10	128	I/O	General-purpose GPIO, no default function	
GNSS_L5_ELNA_CTRL/GPIO11*	133	I/O	General-purpose GPIO, no default function	
GPIO12*	499	I/O	General-purpose GPIO, no default function	
GPIO13	261	I/O	General-purpose GPIO, no default function	
GPIO14	262	I/O	General-purpose GPIO, no default function	
GPIO15*	160	I/O	General-purpose GPIO, no default function	
GPIO16*	502	I/O	General-purpose GPIO, no default function	
GPIO17	159	I/O	General-purpose GPIO, no default function	
UART1_TX/GPIO18*	157	I/O	General purpose GPIO, default is UART1_TX	
UART1_RX/GPIO19*	158	I/O	General purpose GPIO, default is UART1_RX	
CAM0_RST_N/GPIO20*	213	I/O	General purpose GPIO, default is CAM0_RST_N	
CAM1_RST_N/GPIO21*	67	I/O	General purpose GPIO, default is CAM1_RST_N	
DBG_UART_TX/GPIO22	528	I/O	Generic GPIO, default is DBG_UART_TX	
DBG_UART_RX/GPIO23*	529	I/O	Generic GPIO, default is DBG_UART_RX	
HOME_KEY/GPIO24*	530	I/O	Generic GPIO, default is HOME_KEY	
VOL_DOWN/GPIO25*	531	I/O	General-purpose GPIO, default is VOL_DOWN	
UART2_TX/GPIO26	507	I/O	General purpose GPIO, default is UART2_TX	
UART2_RX/GPIO27*	506	I/O	General purpose GPIO, default is UART2_RX	
FP_INT/GPIO34*	314	I/O	General-purpose GPIO, no default function	
FP_RST/GPIO35*	313	I/O	General-purpose GPIO, no default function	
NFC_I2C_SDA/GPIO36*	524	I/O	Generic GPIO, default is NFC_I2C_SDA	
NFC_I2C_SCL/GPIO37	525	I/O	Generic GPIO, default is NFC_I2C_SCL	
NFC_EN/GPIO38	474	I/O	General-purpose GPIO, no default function	

NFC_CLK_REQ/GPIO39*	321	I/O	General-purpose GPIO, no default function	
NFC_DWL_REQ/GPIO40*	323	I/O	General-purpose GPIO, no default function	
NFC_INT/GPIO41*	473	I/O	General-purpose GPIO, no default function	
DCAM_PWD_N/GPIO42	75	I/O	General purpose GPIO, default is DCAM_PWD_N	
SCAM_PWD_N/GPIO43*	96	I/O	Generic GPIO, default is SCAM_PWD_N	
LCD_RST_N/GPIO44*	393	I/O	General purpose GPIO, default is LCD_RST_N	
GPIO45*	318	I/O	General-purpose GPIO, no default function	
LCD_ID/GPIO46	394	I/O	General-purpose GPIO, no default function	
GPIO47*	324	I/O	General-purpose GPIO, no default function	
NFC_SPI_MISO/GPIO48*	320	I/O	General-purpose GPIO, no default function	
NFC_SPI_MOSI/GPIO49	319	I/O	General-purpose GPIO, no default function	
NFC_SPI_SCLK/GPIO50	312	I/O	General-purpose GPIO, no default function	
NFC_SPI_CS/GPIO51*	311	I/O	General-purpose GPIO, no default function	
TS_I2C_SDA/GPIO52*	409	I/O	General purpose GPIO, default is TS_I2C_SDA	
TS_I2C_SCL/GPIO53	410	I/O	General purpose GPIO, default is TS_I2C_SCL	
GPIO54*	309	I/O	General-purpose GPIO, no default function	
AUDIO_PA_EN/GPIO55*	310	I/O	General-purpose GPIO, default is external audio PA enable	
SPI1_MISO/GPIO56*	522	I/O	General-purpose GPIO, no default function	
SPI1_MOSI/GPIO57	523	I/O	General-purpose GPIO, no default function	
SPI1_SCK/GPIO58	521	I/O	General-purpose GPIO, no default function	
SPI1_CS/GPIO59*	520	I/O	General-purpose GPIO, no default function	
USB_ID/GPIO60*	377	I/O	Generic GPIO, default is USB_ID	
FP_WAKE/GPIO61*	322	I/O	General-purpose GPIO, no default function	
WSA0_EN/GPIO63*	114	I/O	General-purpose GPIO, no default function	
CAM_MCLK0/GPIO64	214	I/O	General purpose GPIO, default is CAM_MCLK0	
CAM_MCLK1/GPIO65	74	I/O	General purpose GPIO, default is CAM_MCLK1	
CAM_MCLK2/GPIO66	190	I/O	General purpose GPIO, default is CAM_MCLK2	
CAM_MCLK3/GPIO67	97	I/O	Generic GPIO, default is CAM_MCLK3	
CAM_MCLK4/GPIO68*	151	I/O	General purpose GPIO, default is CAM_MCLK4	
CCI_I2C0_SDA/GPIO69	222	I/O	General purpose GPIO, default is CCI_I2C0_SDA	

CCI_I2C0_SCL/GPIO70	223	I/O	General purpose GPIO, default is CCI_I2C0_SCL	
CCI_I2C1_SDA/GPIO71	76	I/O	General purpose GPIO, default is CCI_I2C1_SDA	
CCI_I2C1_SCL/GPIO72*	77	I/O	General purpose GPIO, default is CCI_I2C1_SCL	
CCI_I2C2_SDA/GPIO73	182	I/O	Generic GPIO, default is CCI_I2C2_SDA	
CCI_I2C2_SCL/GPIO74	183	I/O	General purpose GPIO, default is CCI_I2C2_SCL	
CCI_I2C3_SDA/GPIO75*	93	I/O	General purpose GPIO, default is CCI_I2C3_SDA	
CCI_I2C3_SCL/GPIO76	94	I/O	General purpose GPIO, default is CCI_I2C3_SCL	
CAM2_RST/GPIO77*	191	I/O	General purpose GPIO, default is CAM2_RST	
CAM3_RST/GPIO78*	95	I/O	General purpose GPIO, default is CAM3_RST	
PCIE1_CLK_REQ_N/GPIO79*	527	I/O	General purpose GPIO, default is PCIE1_CLK_REQ_N	
LCD_TE/GPIO80*	401	I/O	General purpose GPIO, default is LCD_TE	
TS_INT_N/GPIO81*	402	I/O	General purpose GPIO, default is TS_INT_N	
SDCARD_DET_N/GPIO91*	498	I/O	Generic GPIO, default is SDCARD_DET_N	
CAM_MCLK5/GPIO93*	174	I/O	General-purpose GPIO, no default function	
MI2S_MCLK/GPIO96	283	I/O	General-purpose GPIO, no default function	
GYRO_INT/GPIO102*	508	I/O	General purpose GPIO, default is GYRO_INT	
ACCL_INT/GPIO103*	516	I/O	General purpose GPIO, default is ACCL_INT	
PRESSURE_INT/GPIO104*	526	I/O	Generic GPIO, default is PRESSURE_INT	
TS_RST_N/GPIO105	403	I/O	General purpose GPIO, default is TS_RST_N	
MCAM_PWD_N/GPIO107	215	I/O	Generic GPIO, default is MCAM_PWD_N	
UIM2_PRESENT/GPIO112*	345	I/O	Dedicated GPIO, can only be used as UIM2_PRESENT	
UIM1_PRESENT/GPIO116*	336	I/O	Dedicated GPIO, can only be used as UIM1_PRESENT	
QCM_RFFE1_CLK_GRFC_2/GPIO119*	269	I/O	Dedicated GPIO, reserved for radio frequency	
QCM_RFFE1_DATA_GRFC_3/GPIO120	270	I/O	Dedicated GPIO, reserved for radio frequency	
SAR_INT_N/GPIO141*	146	I/O	General-purpose GPIO, no default function	
ALSP_INT_N/GPIO142*	317	I/O	General purpose GPIO, default is ALSP_INT_N	
I2S1_CLK/DMIC1_CLK/GPIO150*	53	I/O	General-purpose GPIO, no default function	
I2S1_WS/DMIC1_DATA/GPIO151*	54	I/O	General-purpose GPIO, no default function	
I2S1_DATA0/DMIC2_CLK/GPIO152	55	I/O	General-purpose GPIO, no default function	
I2S1_DATA1/DMIC2_DATA/GPIO153*	56	I/O	General-purpose GPIO, no default function	

I2S2_CLK/SWR_CLK/GPIO154	285	I/O	General-purpose GPIO, no default function	
I2S2_WS/SWR_DATA/GPIO155*	286	I/O	General-purpose GPIO, no default function	
I2S2_DATA0/DMIC3_CLK/GPIO156*	287	I/O	General-purpose GPIO, no default function	
I2S2_DATA1/DMIC3_DATA/GPIO157*	288	I/O	General-purpose GPIO, no default function	
SNS_I3C0_SDA/GPIO159	490	I/O	General-purpose GPIO, no default function	
SNS_I3C0_SCL/GPIO160	489	I/O	General-purpose GPIO, no default function	
SENSOR_I2C_SDA/GPIO161	47	I/O	General purpose GPIO, default is SENSOR_I2C_SDA	
SENSOR_I2C_SCL/GPIO162	48	I/O	General purpose GPIO, default is SENSOR_I2C_SCL	
MAG_I2C_SDA/GPIO163	476	I/O	General-purpose GPIO, no default function	
MAG_I2C_SCL/GPIO164	475	I/O	General-purpose GPIO, no default function	
Other Functional Feet				
FORCED_USB_BOOT	517	I	Boot up to 1.8V (VREG_L18B_1P8) to enter emergency download mode	
PM_MID_CHG	1、2、9、10	I	Mid point of the charger. Charger buck input. Joint point for DC/charging.	
VIB_DRV_P	7	O	Motor output positive, support ERM	
PM7250B_GPIO1/ADC1	42	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO5/ADC2	43	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO8/ADC3	44	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO11/ADC4	45	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO12/ADC5	46	I/O	PM7250B_GPIO, used as ADC by default	
PM7325_GPIO2/ADC6	434	I/O	PM7325_GPIO, used as ADC by default	
PM7325_AMUX4	435	I	Analog multiplexer (AMUX) input	
PM7325_AMUX2	436	I	Analog multiplexer (AMUX) input	
SMB1355_INT/PM7250B_GPIO6	432	I/O	PM7250B_GPIO, used as SMB1355_INT by default	
DISPLAY_BIAS_DRIVER_EN/PM7250B_GPIO2	437	I/O	PM7250B_GPIO, used as DISPLAY_BIAS_DRIVER_EN by default	
EDP_PWM/PM7350C_GPIO8	411	I/O	PM7350C_GPIO, can be used as PWM output	
FLASH_LED1	421	O	Flash positive, 1.5A output	
FLASH_LED2	422	O	Flash positive, 1.5A output	
FLASH_LED3	423	O	Flash positive, 0.8A output	
FLASH_LED4	420	O	Flash positive, 0.8A output	
IRIS_RED	351	O	RED_LED indicator positive	

IRIS_GREEN	352	O	GREEN _LED indicator positive	
IRIS_BLUE	353	O	BLUE_LED indicator positive	
SMB_SPMI_CLK	387	O	SMB_SPMI_CLK	Inter-chip communicati on for parallel charging
SMB_SPMI_DATA	388	I/O	SMB_SPMI_CLK	
SMB_ICHG_FB	438	I	Current sense plus from the external parallel charger.	
SMB_EN_CHG	439	O	Enable/disable control pin for parallel SMB (slave) charger.	
SMB_THERM	444	I	Inductor temperature sensor.	When using SMB1393, pull down the 40.2K resistor
IUSB_OUT	433	O	Buffered voltage signal proportional to USB input current. Output to the charge pump. Needed for regulating the input current limit with the charge pump	reserved port
DC_IN_PSNS	428	I	DC charging power sense input	
DC_IN_PON	429	I	DC charging power-on trigger	
DC_IN_EN	430	O	DC barrel jack charging power source enable/disable pin. KeepsDC charger input disabled during USB charging.	
LN_BB_CLK2	519	O	LN_BB_CLK2（19.2MHz clock , for NFC）；	
KPD_PWR_N	509	I	Power Key	
PM_RESIN_N	505	I	Hardware reset key	
KYPD_VOLP_N	493	I	Control volume+	
CBL_PWR_N	491	I	Power-on automatic power-on control pin	
WCD_RESET_N	494	I/O	Internal audio chip reset signal	NC processing
AOSS_SLEEP_INDICATOR	500	I/O	AOSS_SLEEP_INDICATOR	
CHARGER_SKIN_THERM	443	I	Analog multiplexer (AMUX) input, used for charging related temperature detection by default	
BATT_ID	445	I	Battery ID detection input	To fake presence of battery and have charging enabled, use a 100 kΩ pull-down to GND on BATT_ID. To fake presence of battery and have charging

				disabled, use 2 kΩ to 14 kΩ pull-down to GND on BATT_ID.
BATT_THERM	446	I	Battery temperature detection input	To fake a good battery temperature, connect a 100 kΩ pull-down to GND on BATT_THERM.
VBATT_PACK_SNS_M	447	I	Battery voltage detection input negative pole	Connect to battery negative ground
VBATT_CONN_VSENSE_M	450	I	Battery voltage detection input negative pole	Connect to battery negative
VBATT_CONN_VSENSE_P	451	I	Battery voltage detection input positive	Connect to battery positive
VBATT_CONN_ISNS_M	452	I	Reserved	Connect to battery positive
VBATT_CONN_ISNS_P	453	I	Reserved	Connect to battery positive
PCIE1_TX0_P	334	O	PCIe TX0	
PCIE1_TX0_M	327	O		
PCIE1_TX1_P	332	O	PCIe TX1	
PCIE1_TX1_M	329	O		
PCIE1_RX0_P	333	I	PCIe RX0	
PCIE1_RX0_M	328	I		
PCIE1_RX1_P	331	I	PCIe RX1	
PCIE1_RX1_M	330	I		
PCIE1_REFCLK_P	335	O	PCIe REFCLK	
PCIE1_REFCLK_M	326	O		
RESERVED	64、65、92、102、104、106、126、129、131、135、136、141、143、149、150、166、167、177、199、200、208、210、211、233、234、239、240、241、242、247、248、249、258、259、260、263、264、272、273、		RESERVED pin	

	274、278、279、280、281、291、292、297、298、299、303、304、305、340、354、355、356			

GPIO*：Indicates an interrupt pin that can wake up the system

3.3. Mechanical Dimensions

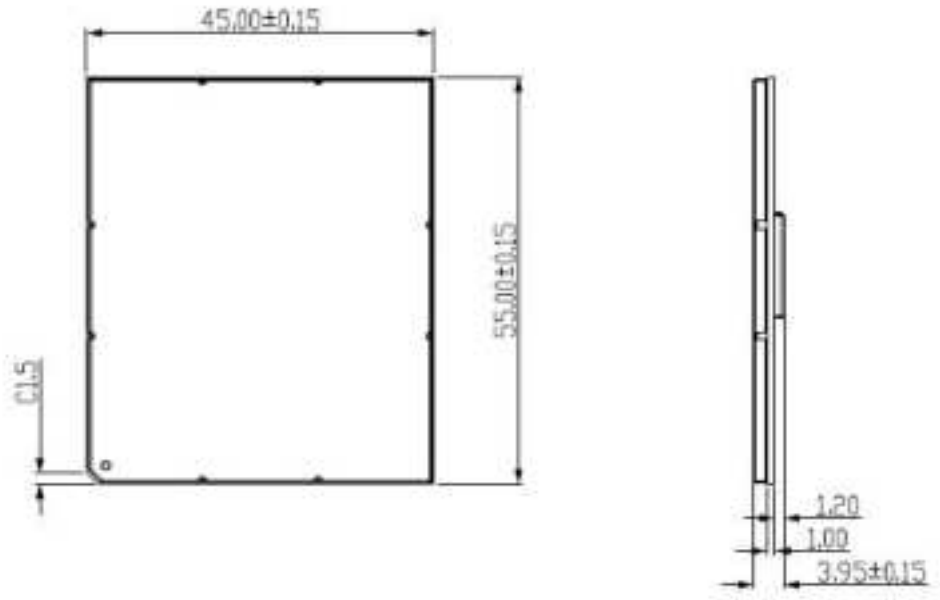


Figure 3.1: TOP View & Side View

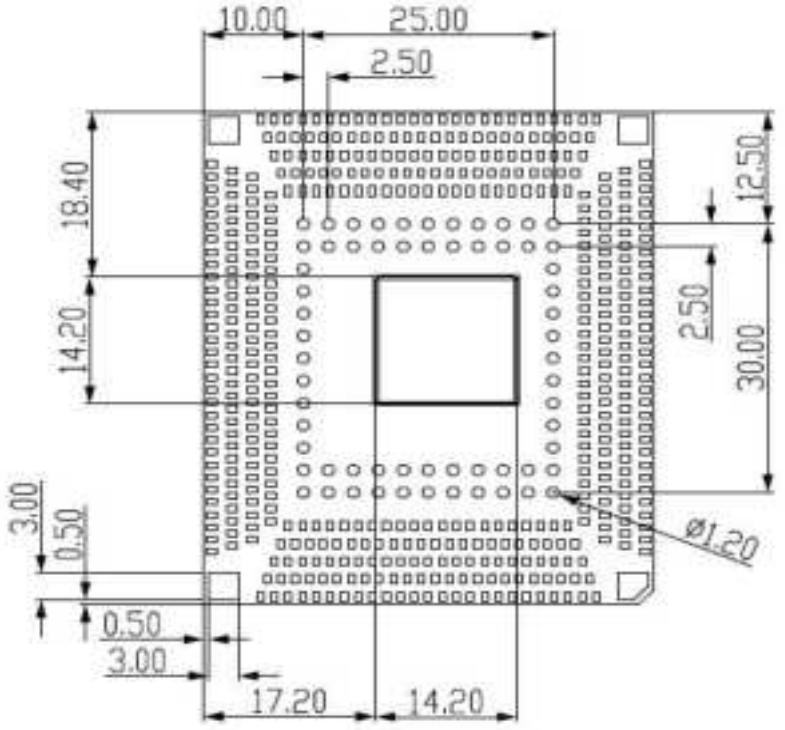


Figure 3.2: BOTTOM View

3.4. Recommended Package

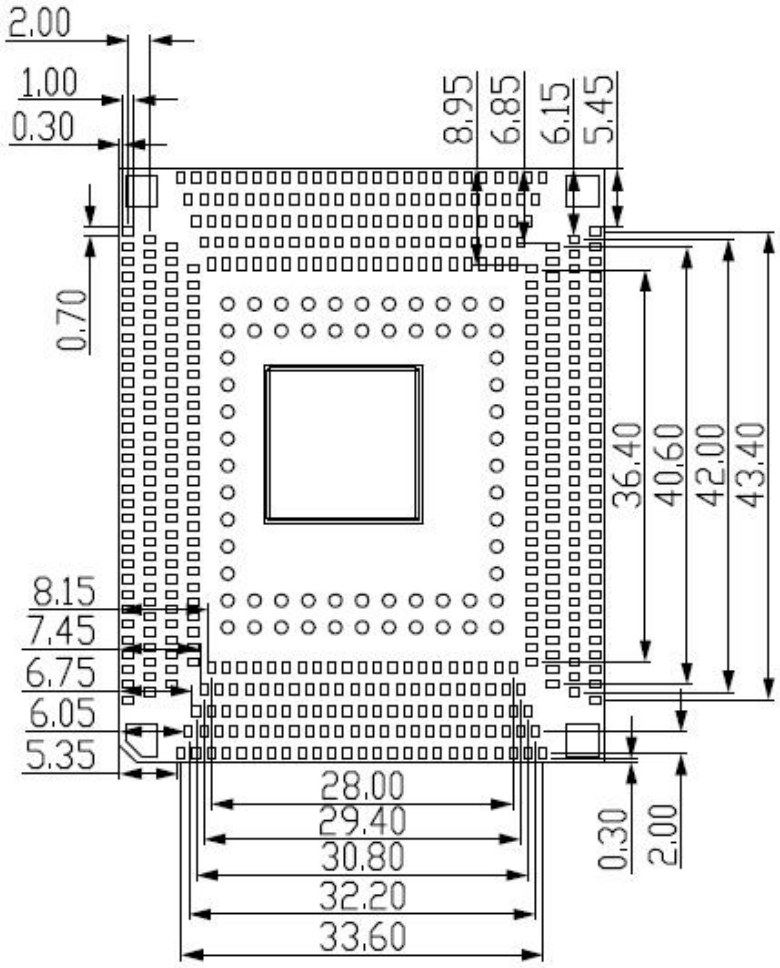


Figure 3.3: Recommended Package

4. Interface Application

4.1. Power

If it is a battery device, the voltage input range of the module VBAT is 3.5V to 4.35V. In the 5G frequency band, when the module transmits at the maximum power, the peak current can reach up to 4A instantaneously, resulting in a large voltage drop on VBAT. It is recommended to use a large capacitor for voltage regulation close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. At the same time, in order to prevent ESD and surge damage to the chip, it is recommended to use a suitable TVS tube and a 5.1V/500mW Zener diode on the VBAT pin of the module. During PCB layout, capacitors and diodes should be placed as close as possible to the VBAT pin of the module. Users can directly power the module with a 3.8V lithium-ion battery. When using a battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

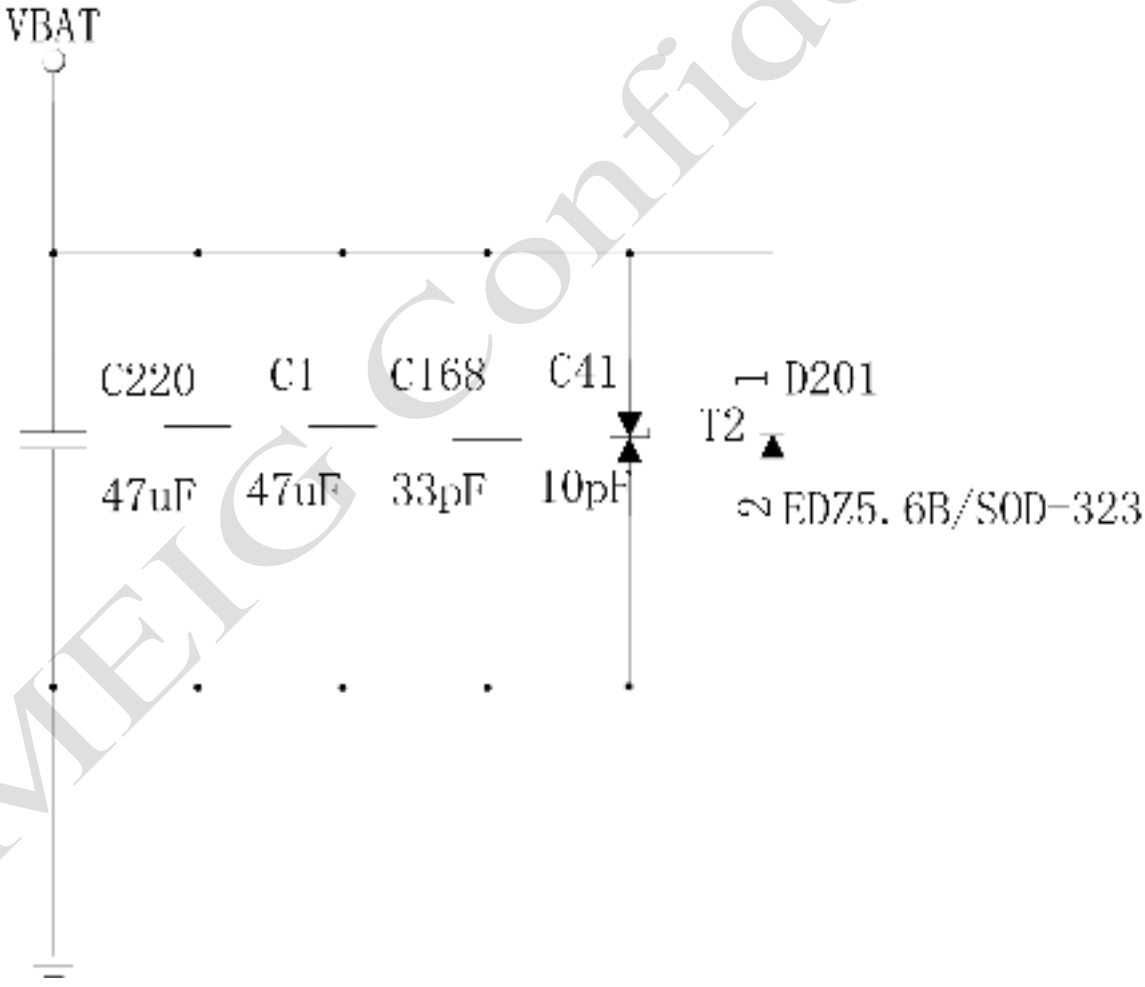


Figure 4.1: VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 5V-12V, and the recommended circuit that can use DC-DC power supply is shown in the figure below:

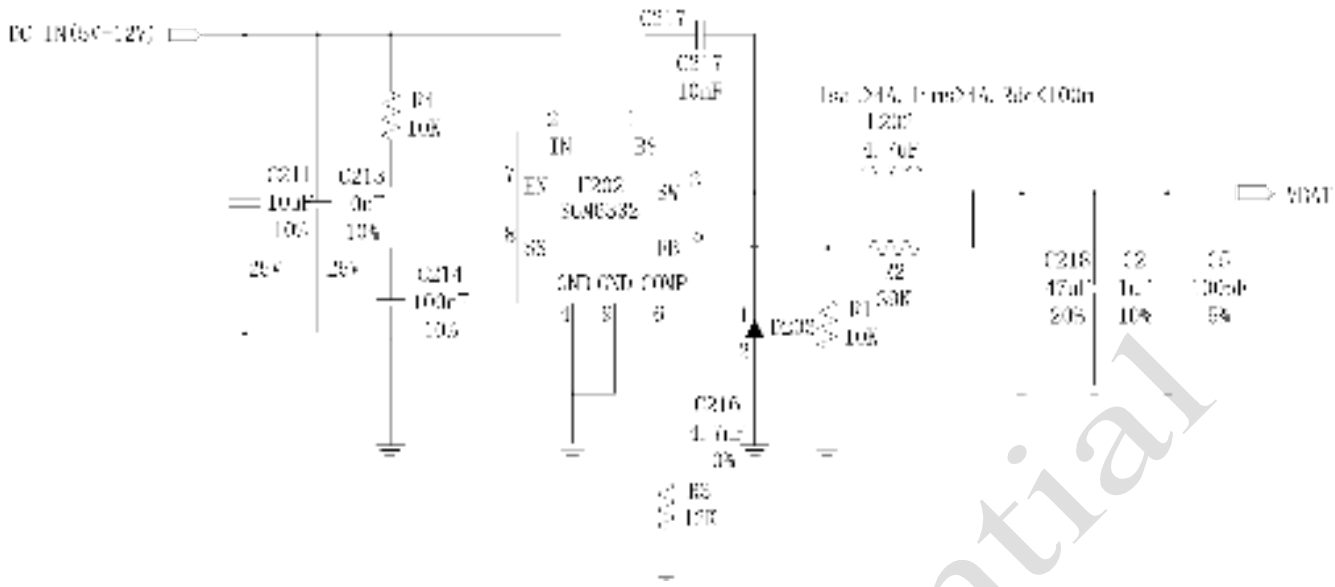


Figure 4.2: DC-DC power supply circuit

4.1.1. Power Pin

VBAT pins (460, 461, 462, 463) are used for power input. In the user's design, please pay special attention to the design of the power supply part to ensure that even when the module current consumption reaches 4A, the drop of VBAT should not be lower than 3.5 V. If the voltage drops below 3.5V, the module may shut down. The PCB trace from the VBAT pin to the power supply should be wide enough to reduce voltage droop during transmission burst mode.

Figure 4.3: Minimum voltage at which VBAT drops

4.2. Power On And Off

Do not turn on the module when the temperature and voltage limits of the module are exceeded. In extreme cases such operations can lead to permanent damage to the module.

4.2.1. Power-on Of The Module

The user can turn on the module by pulling down the KPD_PWR_N pin (509) for at least 5 seconds. This pin has been pulled up to 1.8V inside the module. The recommended circuit is as follows; or pull down the CBL_PWR_N pin (491), CBL_PWR_N can realize the function of automatic power-on after power-on by means of a 1K pull-down resistor to ground, and it is not necessary to release this signal after power-on.

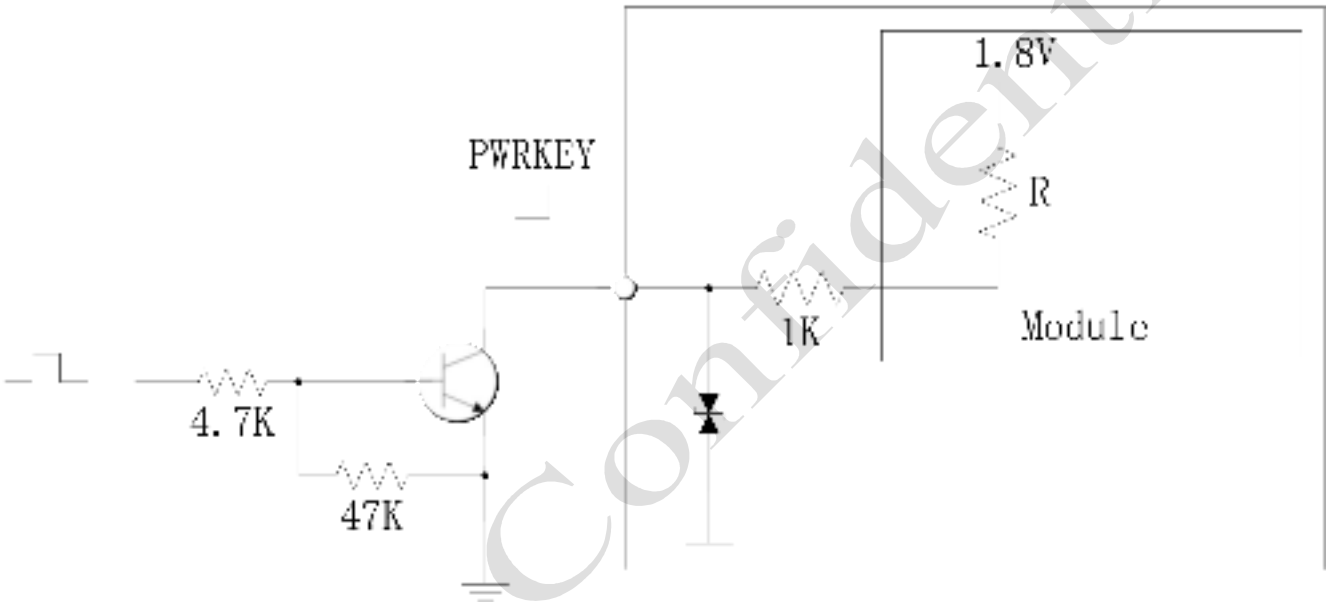


Figure 4.4: Using an external signal to drive the module to boot

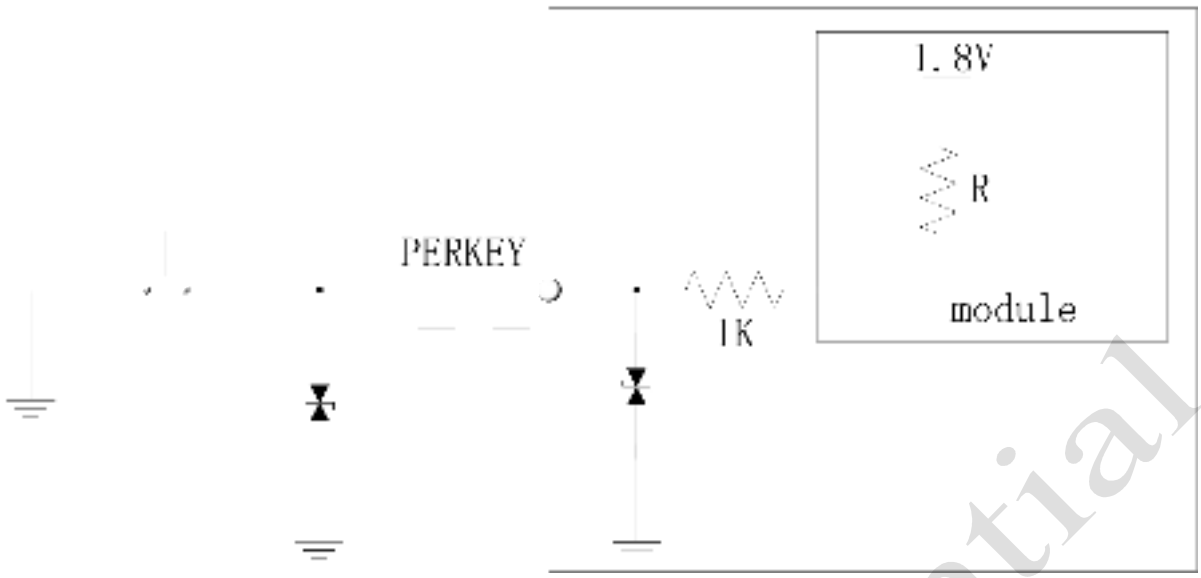


Figure 4.5: Power on using the button circuit

4.2.2. Module Shutdown

User can shutdown using KPD_PWR_N pin

4.2.2.1. PWRKEY Shutdown

User can shut down by pulling the KPD_PWR_N signal low for at least 3 seconds. The shutdown circuit can refer to the design of the startup circuit. After the module detects the shutdown action, a prompt window will pop up on the screen to confirm whether to perform the shutdown action.

Users can implement forced shutdown by pulling KPD_PWR_N low for at least 15 seconds.

4.2.3. Module Reset

The SRM955 module supports the hardware reset function, and the user can quickly restart the module by pulling down the PM_RESIN_N pin (505) of the module. The recommended circuit is as follows:

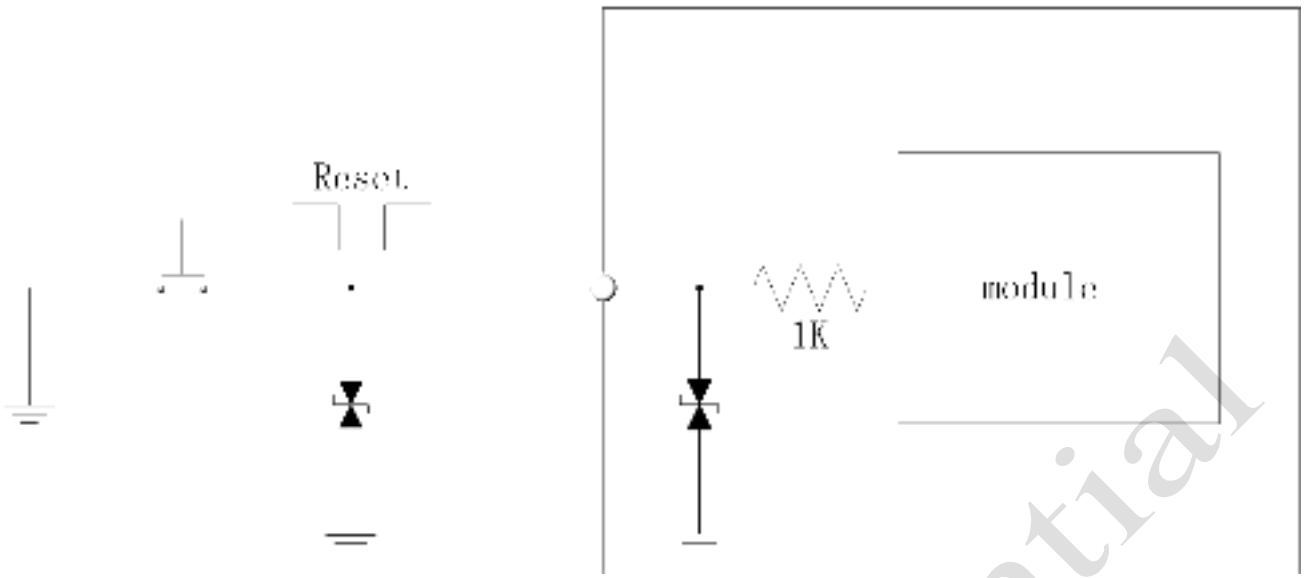


Figure 4.6: Reset using key circuit

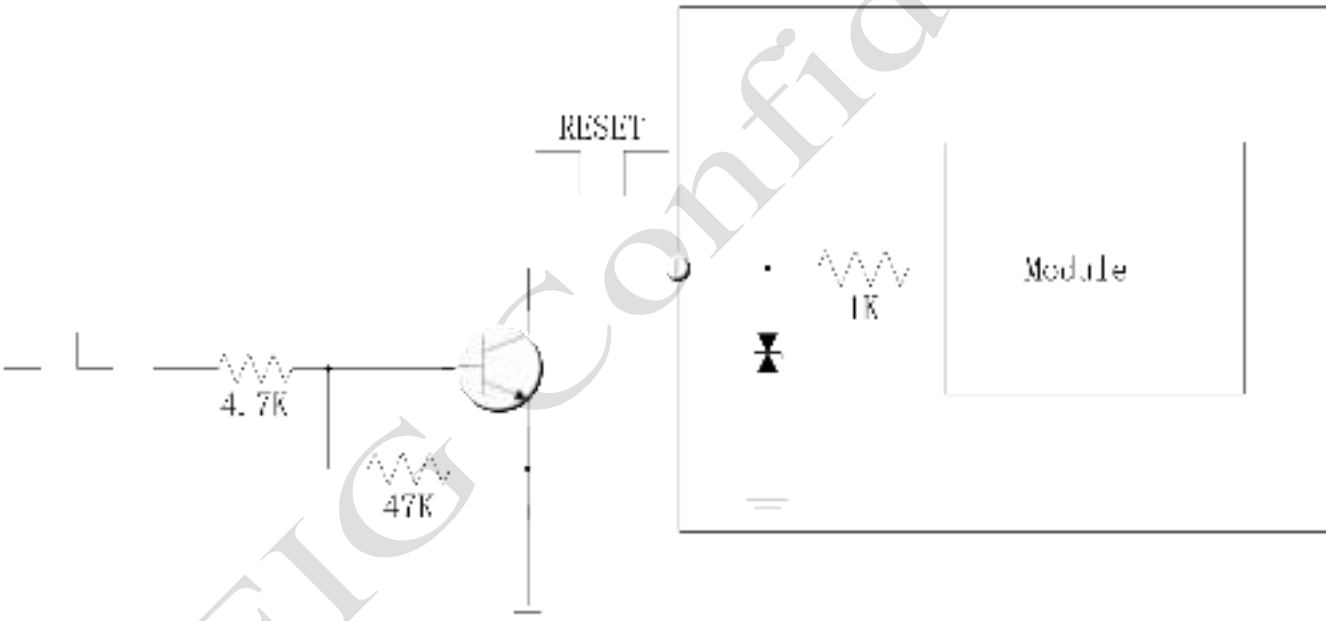


Figure 4.7: Resetting the module using an external signal

When the pin is at a high level, the typical voltage is 1.8V, so users with a level of 3V or 3.3V cannot directly use the GPIO of the MCU to drive this pin, and an isolation circuit needs to be added. The hardware parameters of PM_RESIN_N can refer to the following table:

Table 4.1: PM_RESIN_N hardware parameters

Pin	Describe	Minimum	Typical value	Maximum	Unit
PM_RESIN_N	Input high level	1.17	-	-	V
	Input low level	-	-	0.63	V
	Valid time of pull low	500		-	ms

4.3. VCOIN Power

When VBAT is disconnected, the user needs to save the real-time clock, so the VCOIN pin (471) cannot be left floating, and should be connected to a large capacitor or battery. When a large capacitor is connected, the recommended value is 100uF, which can keep the real-time clock for 20 seconds. When the RTC power supply uses an external large capacitor or battery to supply power to the RTC inside the module, the reference design circuit is as follows:

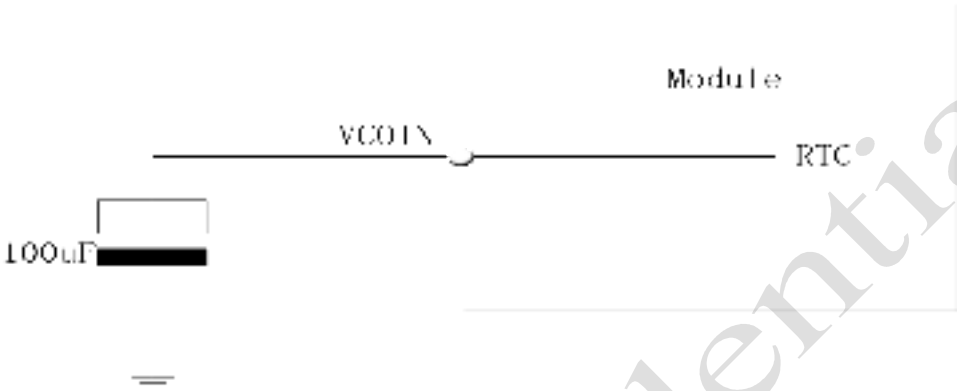


Figure 4.8: External Capacitor Powering the RTC

Non-rechargeable battery powered:

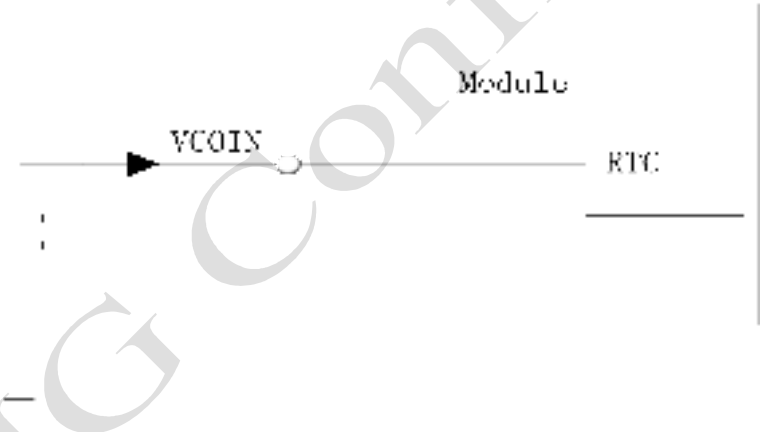


Figure 4.9: Non-rechargeable battery powering the RTC

Rechargeable battery powered:

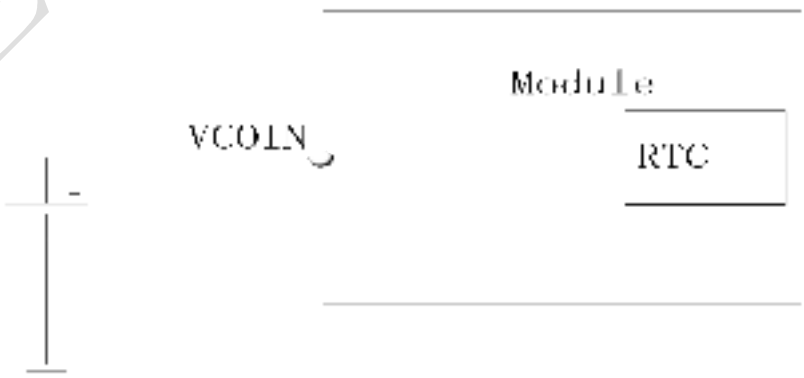


Figure 4.10: Rechargeable battery powers RTC

The VCOIN power supply is typically 3.0V.

4.4. Power Output

The SRM955 has multiple power outputs. For SD card, SIM card, sensor, touch panel, external LDO, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high-frequency interference.

Table 4.2: Power supply description

Power	Default voltage (V)	Drive current (mA)
VREG_L2C_1P8(RESERVED)	1.8	150mA
VREG_L3C_3P0(TPVDD)	3.0	150mA
VREG_L4C_1P8_3P0(VSIM1)	1.8/3.0	150mA
VREG_L5C_1P8_3P0(VSIM2)	1.8/3.0	150mA
VREG_L6C_2P96(SDVIO)	2.96	150mA
VREG_L7C_3P0(SENSOR_VDD)	3.0	300mA
VREG_L8C_1P8(SENSOR_VDDIO)	1.8	300mA
VREG_L9C_2P96(SD_VDD)	2.96	600mA
VREG_L11C_2P8(WCN_VDD)	2.8	300mA
VREG_L12C_1P8(OLED VDDIO)	1.8	150mA
VREG_L13C_3P0(OLED VCI)	3.0	150mA
VREG_L2B_3P072(USBHS_VIO)	3.072	150mA
VREG_L11B_1P776(SDR_VDD)	1.776	300mA
VREG_L18B_1P8	1.8	300mA
VREG_L19B_1P8(RF_VDDIO)	1.8	300mA
VREG_SYS_1P8	1.8	50mA
VPH_PWR	3.8	>1A

4.5. Serial Port

SRM955 provides 3 serial ports for communication, of which 2 groups of interfaces support four-wire serial ports. The number of serial ports can also be expanded through the QUP interface.

Table 4.3: UART pin descriptions

Name	Pin	Direction	Features
GPIO16*	502	I	UART1_CTS
GPIO17	159	O	UART1_RTS
UART1_TX/GPIO18*	157	O	UART1_TX
UART1_RX/GPIO19*	158	I	UART1_RX
DBG_UART_TX/GPIO22	528	O	Debug UART data transmission
DBG_UART_RX/GPIO23*	529	I	Debug UART data reception
HOME_KEY/GPIO24*	530	I	UART2_CTS
VOL_DOWN/GPIO25*	531	O	UART2_RTS
UART2_TX/GPIO26	507	O	UART2_TX
UART2_RX/GPIO27*	506	I	UART2_RX

You can refer to the connection method below:

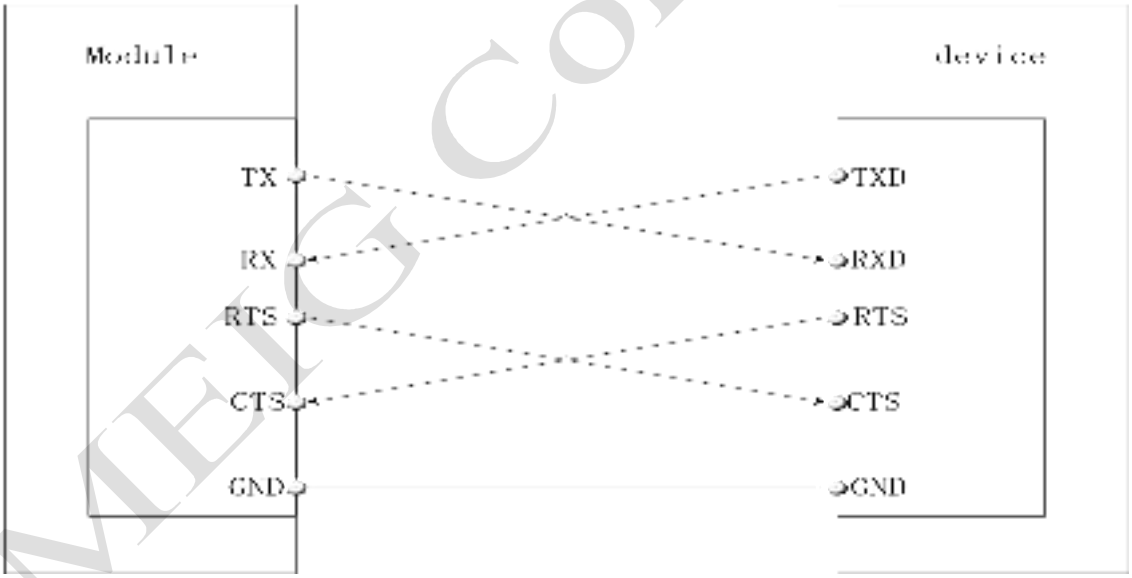


Figure 4.11: Serial connection diagram

When the level of the serial port used by the user does not match the module, in addition to adding a level conversion IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low-speed signals can refer to this two circuits.

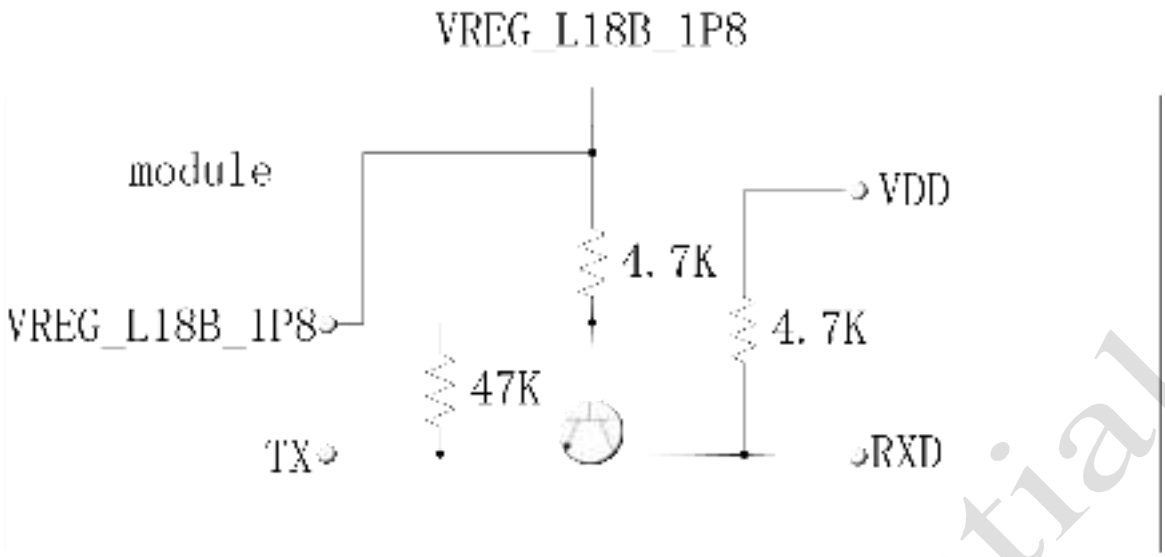


Figure 4.12: TX Connection Diagram

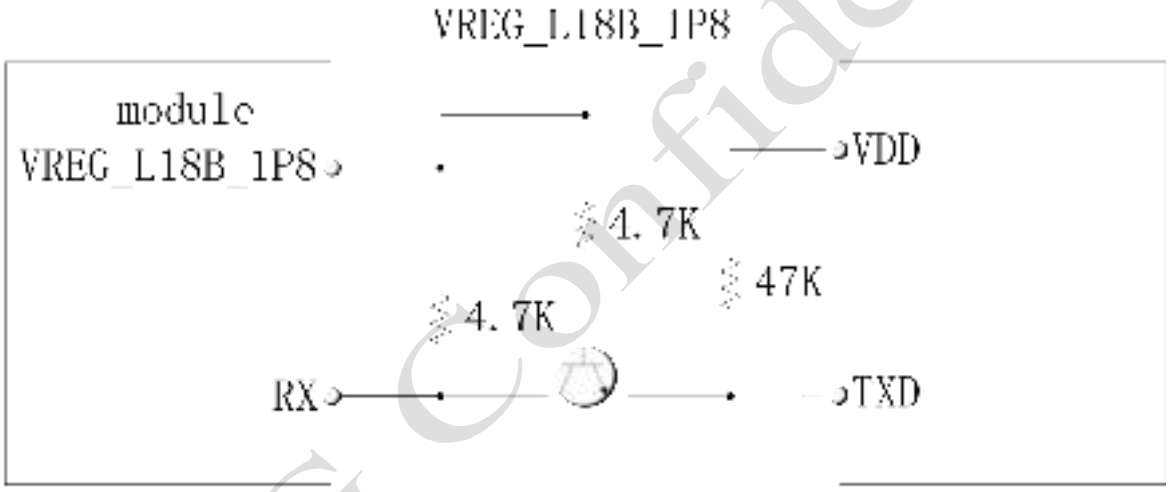


Figure 4.13: RX connection diagram

Note: When using Figure 4.12 and 4.13 for level isolation, it is necessary to pay attention to using VREG_L18B_1P8 as the pull-up power supply. VREG_L12C_1P8 or VREG_L8C_1P8 will enter low power consumption mode during sleep, so it is not recommended to use it.

Table 4.4: Serial hardware parameters

Describe	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Output low level	-	0.45	V
Output high level	1.35	-	V

Note: 1. The serial port of the module is a CMOS interface and cannot be directly connected to RS232 signals. If needed, please use RS232 conversion chip.

2. If the 1.8V output of the module cannot meet the high level range of the user, please add a level conversion circuit.

4.6. MIPI Interface

SRM955 supports MIPI interface for Camera and LCD. MIPI is a high-speed signal line. In the layout stage, please strictly follow the impedance and length requirements, control the equal length of the differential pair within the group and between the groups, and keep the total length as short as possible.

4.6.1. LCD Interface

SRM955 module supports MIPI interface of 1 group of LCD display screen, and has the identification signal of compatible screen. The screen resolution can support up to FHD+. The signal interface is shown in the table below. When Layout, please strictly control the differential 85 ohm impedance and the equal length of the signal line within and between groups.

The MIPI interface of the module is in the 1.2V power domain. When the user needs to be compatible with the screen design, the LCD_ID pin of the module can be used. The LCD_VCC power supply can use VREG_L13C_3P0 or an external LDO power supply. The specific solution can be selected according to the current consumption

Table 4.5: Screen Interface Definition

Screen Interface			
MIPI_DSI0_CLK_N	406	O	MIPI_LCD clock line
MIPI_DSI0_CLK_P	407	O	
MIPI_DSI0_LANE0_N	390	O	MIPI_LCD data line
MIPI_DSI0_LANE0_P	391	O	
MIPI_DSI0_LANE1_N	396	O	
MIPI_DSI0_LANE1_P	397	O	
MIPI_DSI0_LANE2_N	398	O	
MIPI_DSI0_LANE2_P	399	O	
MIPI_DSI0_LANE3_N	404	O	
MIPI_DSI0_LANE3_P	405	O	
LCD_RST_N/GPIO44*	393	I/O	LCD reset pin
LCD_TE/GPIO80*	401	I/O	LCD frame sync signal
LCD_ID/GPIO46	394	I/O	LCD_ID signal

LCD_ID of the module, this pin is GPIO inside. When used as LCD_ID, please confirm the internal circuit of the LCD. If the resistor divider method is used inside the LCD, please pay attention to the voltage to meet the high level or low level range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common mode inductor on the side close to the LCD.

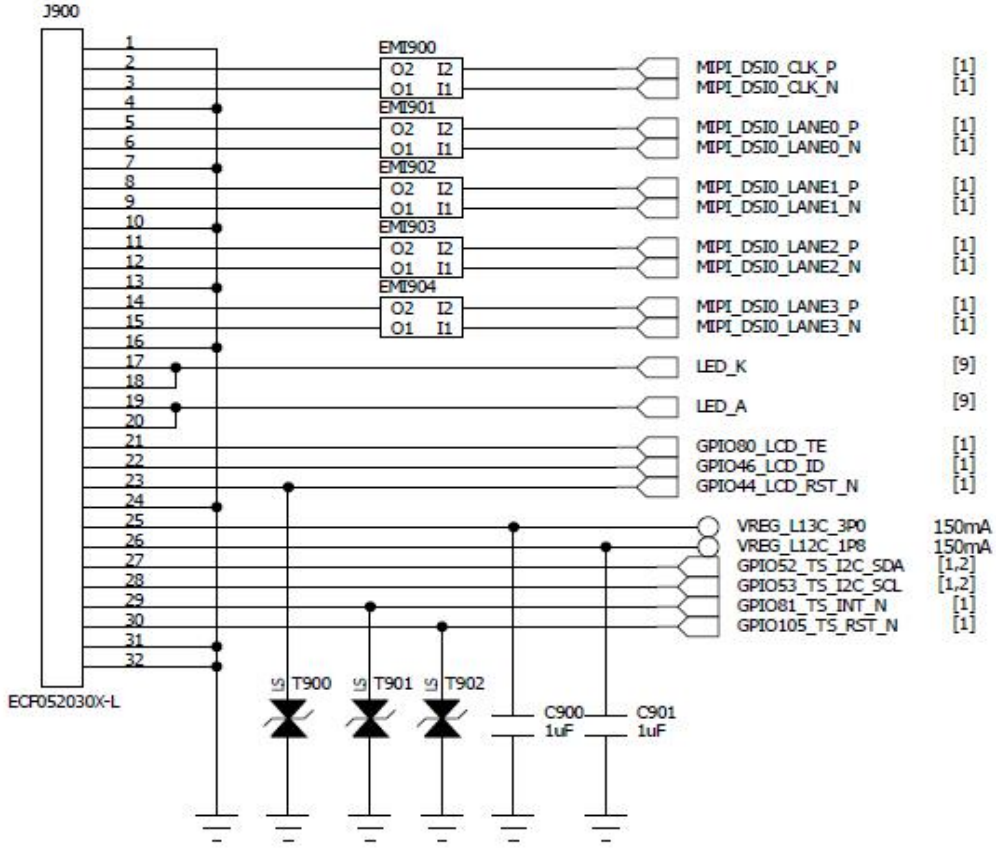


Figure 4.14: Schematic diagram of LCD interface circuit

SRM955 can control the external backlight chip to adjust the backlight brightness through the BL_PWM/PM7350C_GPIO9 signal of the module, and the modulation method is PWM mode.

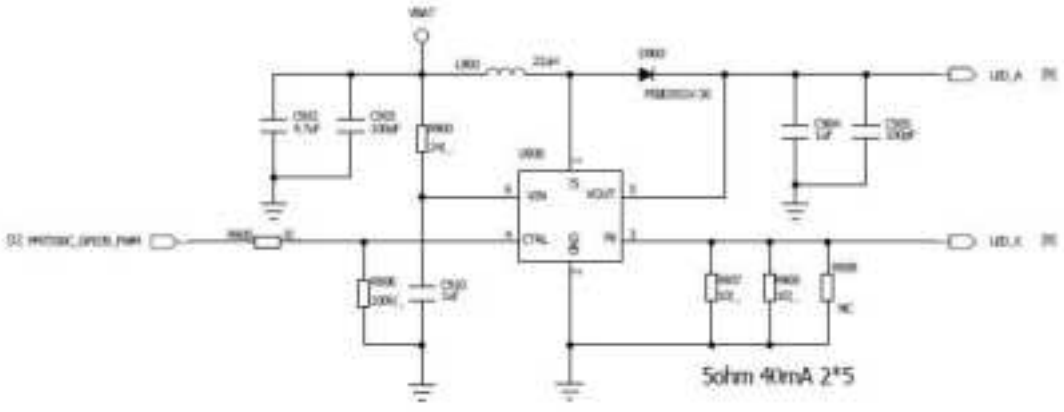


Figure 4.15: Schematic diagram of backlight driving

Note: 1. The backlight circuit should choose the chip according to the backlight circuit of the LCD. The user should read the LCD documentation carefully and choose the correct driver chip. The reference circuit provided in this document is a series-type PWM dimming backlight drive circuit; if it is a series-type one-line dimming backlight drive circuit, it needs to be controlled by GPIO.

4.6.2. MIPI Camera Interface

The SRM955 module supports 5 groups of MIPI interface Camera, each group supports 4 lane data lines, and each lane supports a maximum rate of 2.5Gbps. It can be used for the design of main camera, secondary camera, depth of field camera, etc.; it can also be used for the design of MIPI interface scanning head. The module does not provide the power required by the Camera, including AVDD-2.8V, AFVDD-2.8V (focus motor power supply) and DVDD-1.2V (CAM core voltage), all of which require external LDO generation.

Table 4.6: MIPI Camera Interface Definition

REAR CAM				
MIPI_CSI0_CLK_P	232	O	REAR CAM MIPI clock	
MIPI_CSI0_CLK_N	231	O		
MIPI_CSI0_LANE0_P	228	I	REAR CAM MIPI data	
MIPI_CSI0_LANE0_N	227	I		
MIPI_CSI0_LANE1_P	226	I		
MIPI_CSI0_LANE1_N	225	I		
MIPI_CSI0_LANE2_P	220	I		
MIPI_CSI0_LANE2_N	219	I		
MIPI_CSI0_LANE3_P	218	I		
MIPI_CSI0_LANE3_N	217	I		
CCI_I2C0_SCL/GPIO70	223	I/O	REAR CAM I2C_SCL	
CCI_I2C0_SDA/GPIO69	222	I/O	REAR CAM I2C_SDA	
MCAM_PWD_N/GPIO107	215	I/O	REAR CAM sleep signal	
CAM_MCLK0/GPIO64	214	I/O	REAR CAM master clock	
CAM0_RST_N/GPIO20*	213	I/O	REAR CAM reset signal	
FRONT CAM				
MIPI_CSI3_CLK_P	86	O	FRONT CAM MIPI CLOCK	
MIPI_CSI3_CLK_N	85	O		
MIPI_CSI3_LANE0_P	87	I	FRONT CAM MIPI data	
MIPI_CSI3_LANE0_N	84	I		
MIPI_CSI3_LANE1_P	88	I		
MIPI_CSI3_LANE1_N	83	I		
MIPI_CSI3_LANE2_P	89	I		
MIPI_CSI3_LANE2_N	82	I		
MIPI_CSI3_LANE3_P	90	I		
MIPI_CSI3_LANE3_N	81	I		
CCI_I2C3_SCL/GPIO76	94	I/O	FRONT CAM/RESERVED CAM I2C_SCL	
CCI_I2C3_SDA/GPIO75*	93	I/O	FRONT CAM/RESERVED CAM I2C_SDA	
SCAM_PWD_N/GPIO43*	96	I/O	FRONT CAM sleep signal	

CAM_MCLK3/GPIO67	97	I/O	FRONT CAM master clock	
CAM3_RST_N/GPIO78*	95	I/O	FRONT CAM reset signal	
DEPTH CAM				
MIPI_CSI1_CLK_P	80	O	DEPTH CAM MIPI clock	
MIPI_CSI1_CLK_N	79	O		
MIPI_CSI1_LANE0_P	72	I	DEPTH CAM MIPI data	
MIPI_CSI1_LANE0_N	71	I		
MIPI_CSI1_LANE1_P	70	I		
MIPI_CSI1_LANE1_N	69	I		
MIPI_CSI1_LANE2_P	62	I		
MIPI_CSI1_LANE2_N	61	I		
MIPI_CSI1_LANE3_P	60	I		
MIPI_CSI1_LANE3_N	59	I		
CCI_I2C1_SCL/GPIO72*	77	I/O	DEPTH CAM I2C_SCL	
CCI_I2C1_SDA/GPIO71	76	I/O	DEPTH CAM I2C_SDA	
DCAM_PWD_N/GPIO42	75	I/O	DEPTH CAM sleep signal	
CAM_MCLK1/GPIO65	74	I/O	DEPTH CAM master clock	
CAM1_RST_N/GPIO21*	67	I/O	DEPTH CAM reset signal	
RESERVED CAM1				
MIPI_CSI2_CLK_P	180	O	RESERVED CAM1 MIPI clock	
MIPI_CSI2_CLK_N	179	O		
MIPI_CSI2_LANE0_P	186	I	RESERVED CAM1 MIPI data	
MIPI_CSI2_LANE0_N	185	I		
MIPI_CSI2_LANE1_P	188	I		
MIPI_CSI2_LANE1_N	187	I		
MIPI_CSI2_LANE2_P	194	I		
MIPI_CSI2_LANE2_N	193	I		
MIPI_CSI2_LANE3_P	196	I		
MIPI_CSI2_LANE3_N	195	I		
CCI_I2C2_SCL/GPIO74	183	I/O	RESERVED CAM1 I2C_SCL	
CCI_I2C2_SDA/GPIO73	182	I/O	RESERVED CAM1 I2C_SDA	
FP_RST/GPIO35*	313	I/O	RESERVED CAM1 sleep signal	
CAM_MCLK2/GPIO66	190	I/O	RESERVED CAM1 master clock signal	
CAM2_RST_N/GPIO77*	191	I/O	RESERVED CAM1 reset signal	
RESERVED CAM2				
MIPI_CSI4_CLK_P	169	O	RESERVED CAM2 MIPI Clock	
MIPI_CSI4_CLK_N	170	O		

MIPI_CSI4_LANE0_P	163	I	RESERVED CAM2 MIPI data	
MIPI_CSI4_LANE0_N	164	I		
MIPI_CSI4_LANE1_P	161	I		
MIPI_CSI4_LANE1_N	162	I		
MIPI_CSI4_LANE2_P	155	I		
MIPI_CSI4_LANE2_N	156	I		
MIPI_CSI4_LANE3_P	153	I		
MIPI_CSI4_LANE3_N	154	I		
CAM_MCLK4/GPIO68*	151	I/O	RESERVED CAM2 master clock signal	
GPIO1	172	I/O	RESERVED CAM2 sleep signal	
MI2S_MCLK/GPIO96	283	I/O	RESERVED CAM2 reset signal	
CCI_I2C2_SCL/GPIO74	183	I/O	RESERVED CAM1 I2C_SCL	
CCI_I2C2_SDA/GPIO73	182	I/O	RESERVED CAM1 I2C_SDA	

If the user designs to use the CAMERA module with auto focus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the CAMERA driver chip. The correct connection is as shown below:

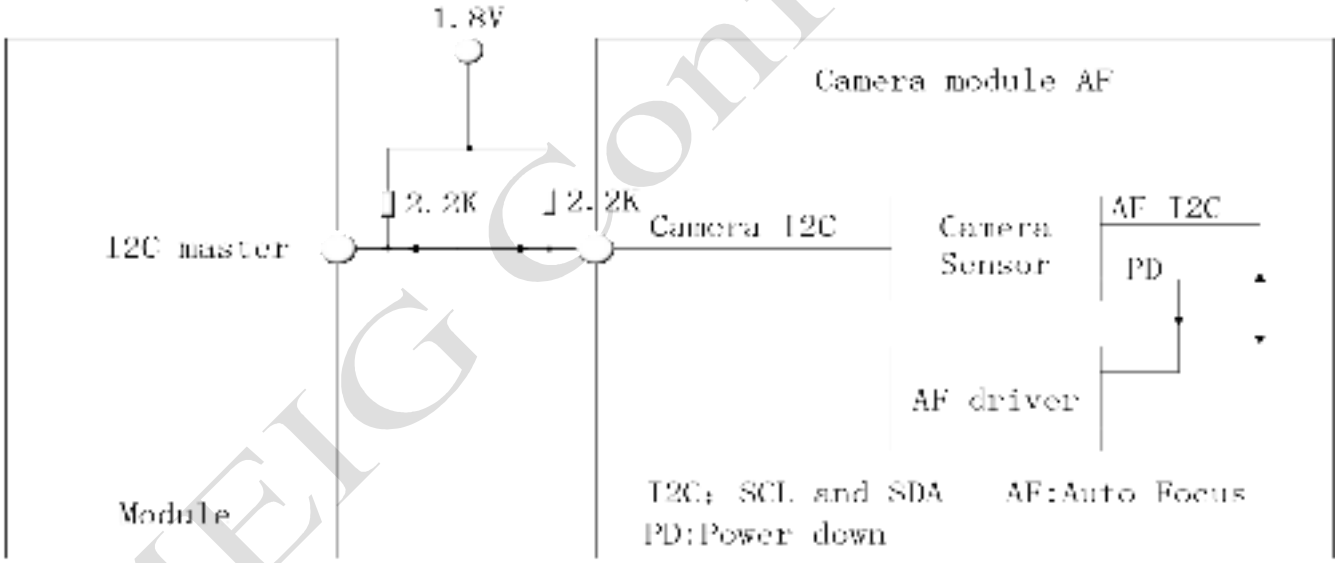


Figure 4.16: Schematic diagram of correct CAMERA connection

The MIPI interface rate is relatively high. Users should control the 85 ohm differential impedance during the routing stage. At the same time, please pay attention to the requirements of the routing length. It is not recommended to add small capacitors on the MIPI signal line, which may affect the rising edge time of MIPI data. , resulting in invalid MIPI data.

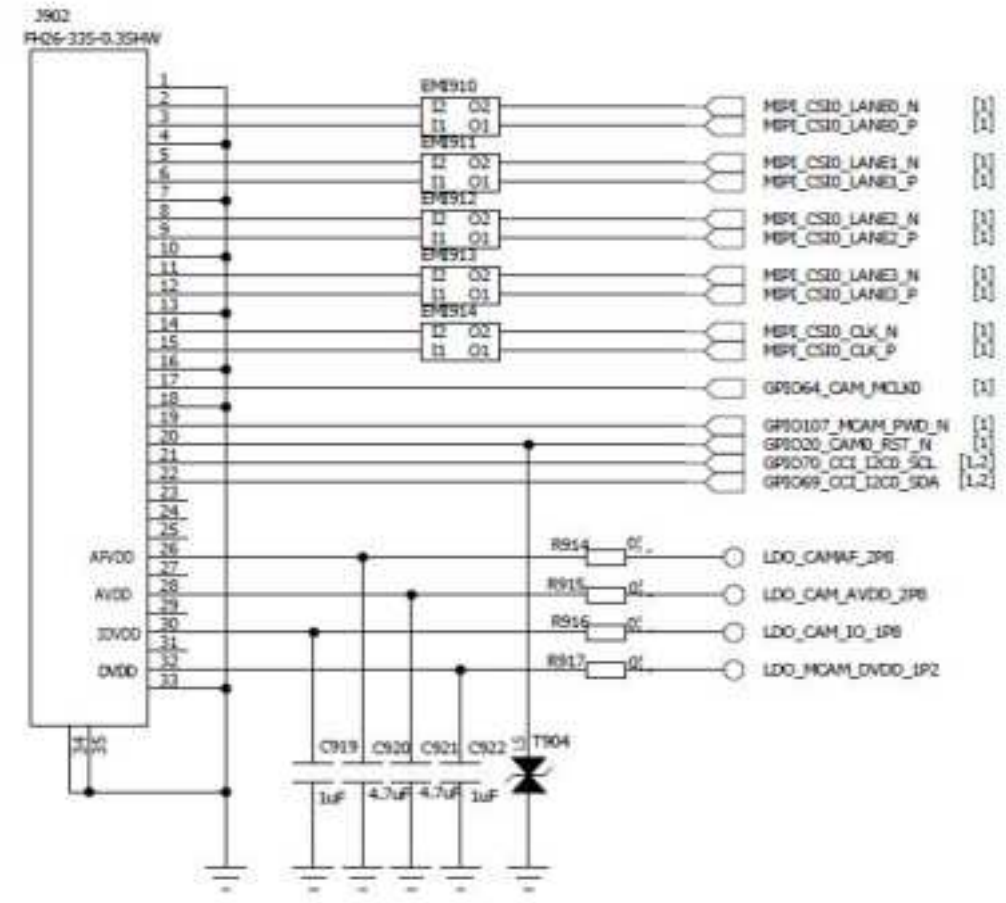


Figure 4.17: MIPI Camera reference circuit

Important note: When designing the camera function, you need to pay attention to the placement of the connector. There will be a little man indicating the imaging direction in the camera specification. Make sure that the little man is standing on the long side of the LCD, otherwise the camera image will be flipped At 90°, the software cannot adjust. As shown in the two figures below.

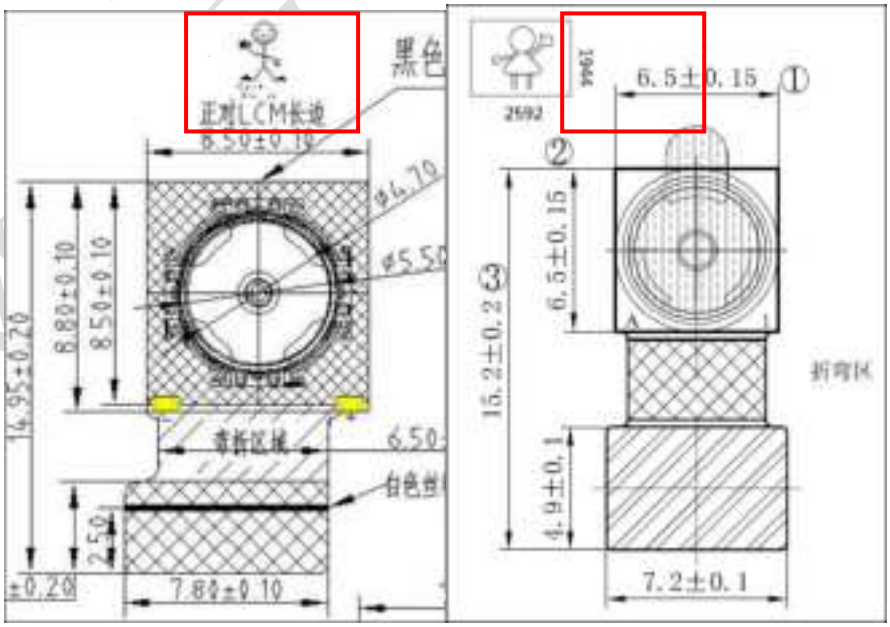


Figure 4.18: Schematic diagram of camera imaging

4.7. Resistive Touch Interface

The module does not provide a resistive touch screen interface. If the user needs to use resistive touch, a dedicated chip needs to be added externally. The module can provide an I2C interface.

4.8. Capacitive Touch Interface

The module provides a set of I2C interfaces that can be used to connect the capacitive touch screen. The default interface pins of the capacitive touch screen are defined in the following table.

Table 4.7: Capacitive Touch Interface Definition

Name	Pin	Input/Output	Description
TS_I2C_SDA/GPIO52*	409	I/O	I2C signal
TS_I2C_SCL/GPIO53	410	I/O	I2C signal
TS_INT_N/GPIO81*	402	I/O	TP interrupt signal
TS_RST_N/GPIO105	403	I/O	TP reset signal
VREG_L12C_1P8(OLED VDDIO)	418	PO	VDDIO_1.8V power supply
VREG_L3C_3P0(TPVDD)	501	PO	VDD_3.0V power supply

Note: The interface definition of capacitive touch can be adjusted by software, and users can change GPIO and I2C according to design needs.

4.9. Audio Interface

The module provides 4 channels of analog audio input, MIC1_IN_P/M is used to connect the main microphone; HPHMIC_IN2_P/M can be used to connect the headphone microphone, MIC3_IN_P/M is used to connect the noise reduction microphone, and MIC4_IN_P/M is reserved. The module also provides three analog audio outputs (HSJ_HPH_L/R, WCD_EAR_OUT_P/M, WCD_AUX_P/M). The audio pins are defined in the following table:

Table 4.8: Audio pin definition

MIC1_IN_M	26	I	Main MIC negative	
MIC1_IN_P	25	I	Main MIC positive	
HPHMIC_IN2_P	21	I	Headphone MIC positive	
HPHMIC_IN2_M	22	I	Headphone MIC negative	
MIC3_IN_M	23	I	Noise reduction MIC negative	
MIC3_IN_P	24	I	Noise reduction MIC positive	
MIC_BIAS1	33	O	The BIAS voltage of the main mic and the auxiliary mic, used for silicon microphone design	
MIC_BIAS2	34	O	BIAS voltage of headphone MIC	
MIC_BIAS3	35	O	BIAS voltage of mic4 for silicon wheat design	
MIC4_IN_P	28	I	MIC4 positive	
MIC4_IN_M	27	I	MIC4 negative	
HSJ_HPH_R	16	O	Headphone right channel	
HSJ_HPH_L	15	O	Headphone left channel	
HSJ_HS_DET	13	I	Headphone plug-in detection	
HSJ_HPH_REF	14	I	Headphone Audio Reference Ground	
WCD_EAR_OUT_P	17	O	earpiece output positive	
WCD_EAR_OUT_M	18	O	Headphone output negative	
WCD_AUX_P	19	O	External amplifier input positive	External amplifier input
WCD_AUX_M	20	O	External power amplifier input negative	
I2S1_DATA1/DMIC2_DATA/GPIO153*	56	I	Digital MIC2 data signal	
I2S1_DATA0/DMIC2_CLK/GPIO152	55	O	Digital MIC2 clock signal	
I2S1_CLK/DMIC1_CLK/GPIO150*	53	O	Digital MIC1 clock signal	
I2S1_WS/DMIC1_DATA/GPIO151*	54	I	Digital MIC1 data signal	
I2S2_DATA0/DMIC3_CLK/GPIO156*	287	O	Digital MIC3 clock signal	
I2S2_DATA1/DMIC3_DATA/GPIO157*	288	I	Digital MIC3 data signal	

It is recommended that the user choose the following circuit according to the actual application to get better sound

effect.

4.9.1. Receiver Interface Circuit

The receiver interface circuit places the following devices near the REC end, B302 and B303 can be changed to magnetic beads according to the actual effect.

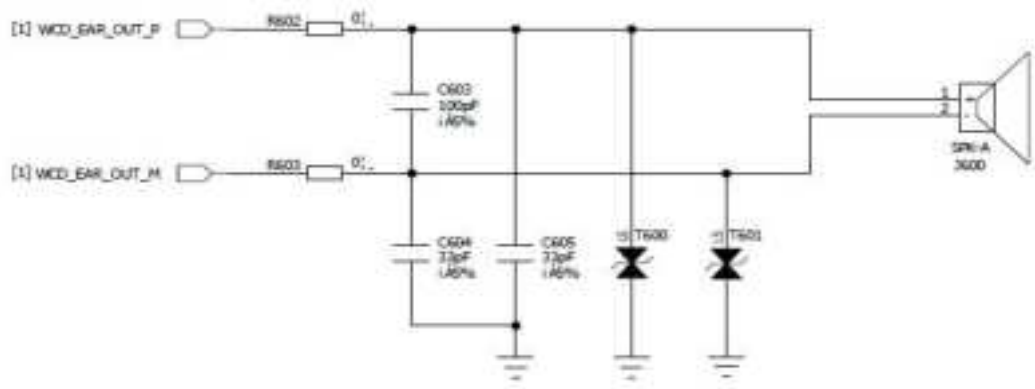
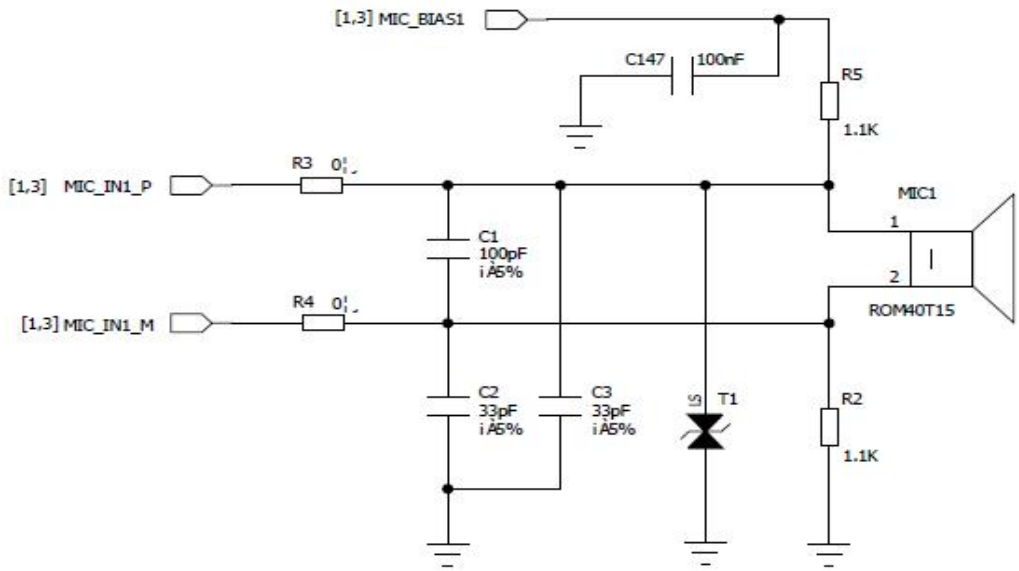


Figure 4.19: Receiver Interface Circuit

4.9.2. Microphone Receiver Circuit

The figure below shows the interface circuit of electret microphone and MEMS microphone

Please refer to the circuit design in strict accordance with the following figure according to the different selection of the user's microphone.



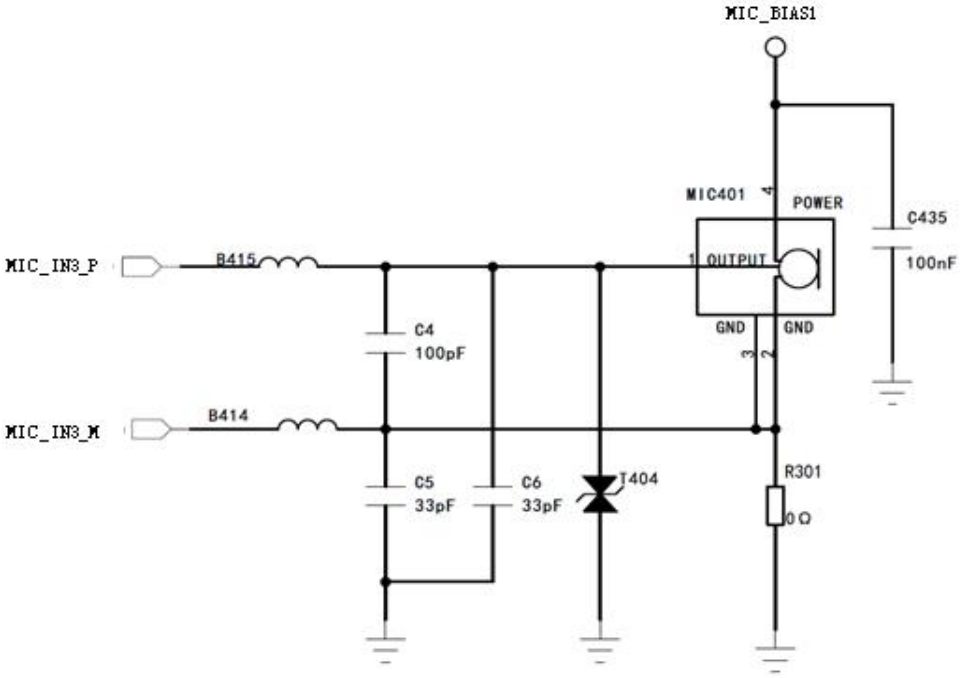


Figure 4.20: Electret microphone, analog silicon microphone interface circuit

4.9.3. Headphone Interface Circuit

The module integrates a stereo headphone jack. It is recommended that users reserve ESD devices in the design stage to prevent ESD damage. The HSJ_HS_DET pin of the module can be set as an interrupt. The software defaults to this pin as an earphone interrupt. Users can use this pin to detect the plugging and unplugging of the earphone.

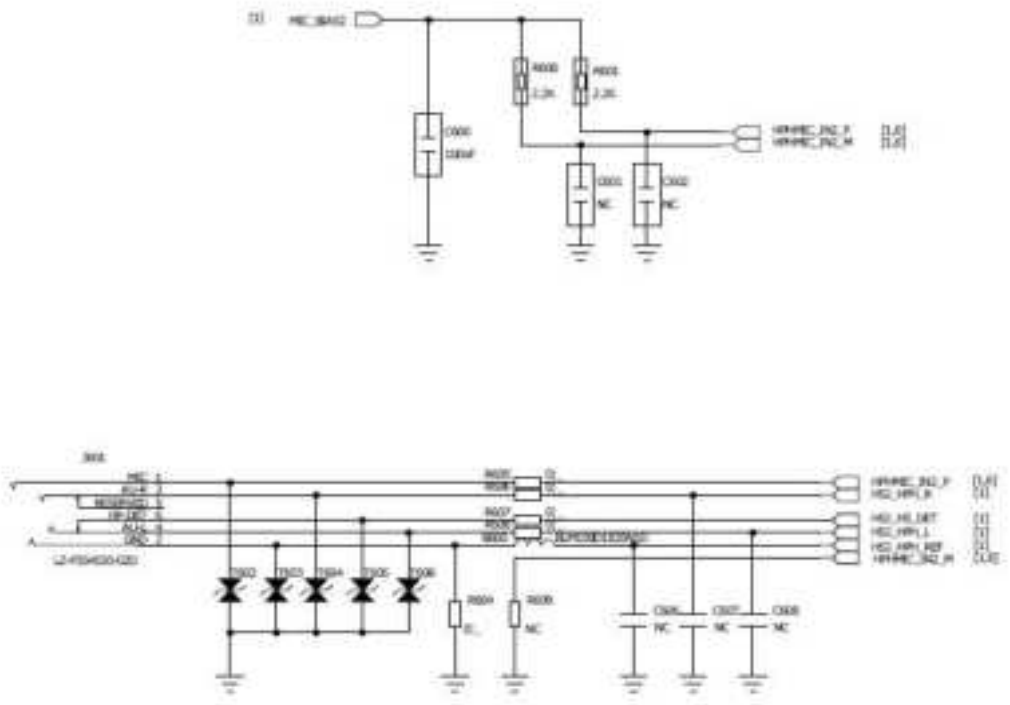


Figure 4.21: Headphone Interface Circuit

Notice:
1. The headset seat in Figure 4.24 is a normal -closed method. If the user uses a commonly opened method, please modify the detection circuit according to the actual pin and modify the software accordingly.
2. We recommend the headset detection foot HSJ_HS_DET and HSJ_HPH_L to form a detection circuit (the connection method in the figure above), because the HSJ_HPH_L inside the chip has a drop -down resistance, which can ensure that the HSJ_HS_DETT and HSJ_HPH_L are low. Connect, please reserve the position of a 1K drop -down resistance on the HSJ_HPH_R.

3 The standard of the headset interface is the European standard OMPT. If you need to design the US -standard CTIA interface, you need to change the GND and MIC signals on the network. If you want to be compatible with two headphones, you need to connect special chips, such as Ti-TS3A226AE.

4.9.4. Circuit Of The Speaker Interface

There is no internal audio amplifier inside the module. The audio amplifier needs to be added to the outside. WCD_AUX_P, WCD_AUX_M is used as a differential input signal. The reference circuit is shown in the figure below.

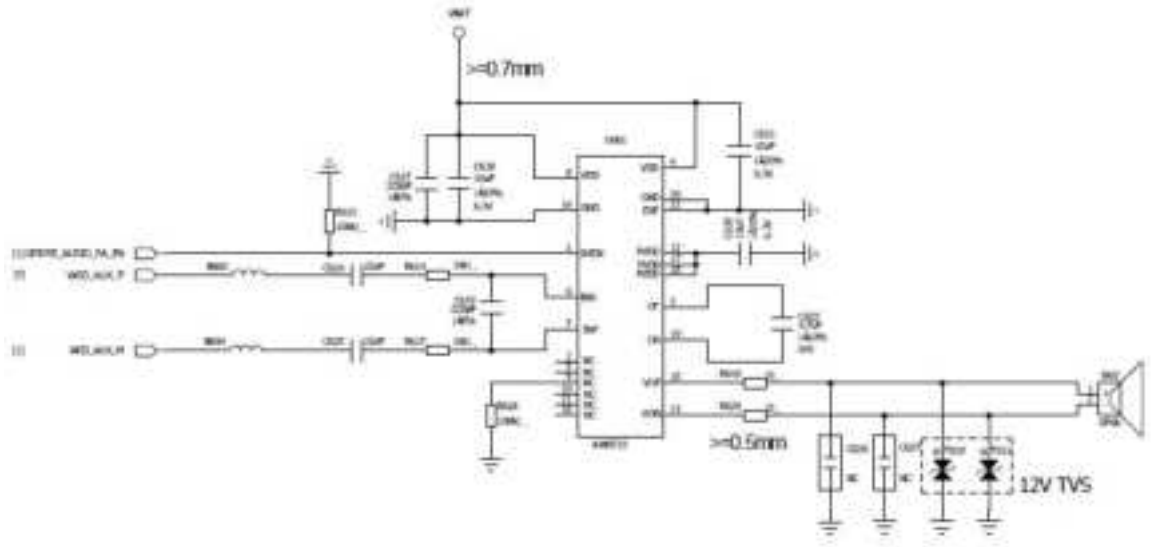


Figure 4.22: Recommended circuit with external audio amplifiers

4.9.5. I2S Interface

There are two groups of I2S interfaces compatible with GPIO in the module. The pins used for this function are as follows:

Table 4.9: I2S interface PIN foot definition

Name	Pin	Input/Output	Description
I2S1_CLK/DMIC1_CLK/GPIO150*	53	O	I2S1_ SLK
I2S1_WS/DMIC1_DATA/GPIO151*	54	O	I2S1_ WS
I2S1_DATA0/DMIC2_CLK/GPIO152	55	I/O	I2S1 DATA0
I2S1_DATA1/DMIC2_DATA/GPIO153*	56	I/O	I2S1_ DATA1
I2S2_CLK/SWR_CLK/GPIO154	285	O	I2S2_ SLK
I2S2_WS/SWR_DATA/GPIO155*	286	O	I2S2_WS
I2S2_DATA0/DMIC3_CLK/GPIO156*	287	I/O	I2S2_ DATA0

I2S2_DATA1/DMIC3_DATA/GPIO15 7*	288	I/O	I2S2_ DATA1

4.10. USB Interface

SRM955 supports 2 USB 2.0 interface, 1 USB 3.1 interface. When layout, you must control the 90 ohm differential impedance, follow the differential long line according to the differential pair, and control the length of the external wiring.

Table 4.10: definition of USB interface switching pin

USB0_HS_DP	375	I/O	USB 2.0 DP signal	
USB0_HS_DM	376	I/O	USB 2.0 DM signal	
USB1_HS_D_P	369	I/O	USB 2.0 DP signal	Only support Host mode
USB1_HS_D_M	370	I/O	USB 2.0 DM signal	
USB0_SS_TX1_P	366	O	USB super-speed 1 transmit – plus	
USB0_SS_TX1_M	367	O	USB super-speed 1 transmit – minus	
USB0_SS_RX1_P	372	I	USB super-speed 1 receive – plus	
USB0_SS_RX1_M	373	I	USB super-speed 1 receive – minus	
USB0_SS_TX0_P	364	O	USB super-speed 0 transmit – plus	
USB0_SS_TX0_M	365	O	USB super-speed 0 transmit – minus	
USB0_SS_RX0_P	358	I	USB super-speed 0 receive – plus	
USB0_SS_RX0_M	359	I	USB super-speed 0 receive – minus	
USB_CC1	5	I/O	CC1 pin for the Type-C	
USB_CC2	6	I/O	CC2 pin for the Type-C	
PM7250B_USB_SBU1	3	I	Type-C side band signal SBU1; protected to 22 V max	
PM7250B_USB_SBU2	4	O	Type-C side band signal SBU2; protected to 22 V max	
USB_CONN_THERM	442	I	USB Type-C connector temperature sensor.	
USB_ID/GPIO60*	377	I	USB ID signal	
DP_AUX_P	361	I/O	DP_AUX_P signal	
DP_AUX_M	362	I/O	DP_AUX_M signal	
USB_CC_DIR	426	O	1.8V tri-state output indicates CC connection direction	Type-C: This pin is connected to 518pin Micro-USB: The pin NC
USB_OPTION	425	I	Select different PON items according to the pull-down resistor value	Type-C: The pin NC Micro-USB: This pin is grounded
USB_PHY_PS	518	I/O	USB_PHY_PS	Type-C: This pin is connected to 426pin Micro-USB:

				Connect this pin to the ground with a 1K resistor

The module also supports OTG function.

The USB insertion detection of the module is realized by VBUS and DP/DM data line. When the USB line is inserted, the VBUS voltage is detected first, and then the up-down state of the DM/DP is detected to determine whether the USB data line or the charger is inserted. Therefore, if the user needs to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is in high-speed mode. It is recommended to connect a common mode inductor in series near the USB connector, which can effectively suppress EMI interference. At the same time, the USB interface is an external interface, and the DM/DP must add a TVS tube to prevent electrostatic damage caused by plugging and unplugging the data cable. When selecting TVS, users should pay attention to the load capacitance should be less than 1pf. VBUS also needs to increase the TVS tube, if there is a need for anti-surge, but also add a surge-proof tube. The connection diagram is as follows:

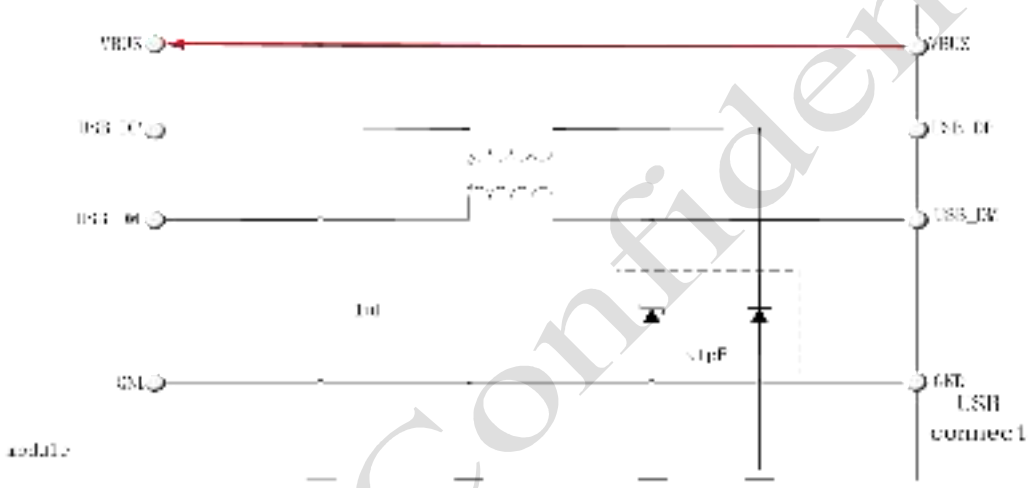


Figure 4.23: USB Connection Diagram

4.10.2. DP Screen Interface

The USB3.0 interface and the DP screen interface share the relevant PIN pins, and the multiplexing combination relationship is as follows:

Phy_mode	Port select		QMP lane	Type-C receptable pins	Connector pin label
	0	1			
USB3 Only the two Tx/Rx pairs are assigned, but only one is in use	Tx	–	lane_0_0	Tx1±	A2, A3
	Rx	–	lane_0_1	Rx1±	B11, B10
	–	Tx	lane_1_0	Tx2±	B2, B3
	–	Rx	lane_1_1	Rx2±	A11, A10
DP Only. All four lanes as Tx are assigned to DP	DP ML2	DP ML1	lane_0_0	Tx1±	A2, A3
	DP ML3	DP ML0	lane_0_1	Rx1±	B11, B10
	DP ML1	DP ML2	lane_1_0	Tx2±	B2, B3
	DP ML0	DP ML3	lane_1_1	Rx2±	A11, A10
Concurrent DP/USB. Two lanes assigned to USB and two to DP	Tx	DP ML1	lane_0_0	Tx1±	A2, A3
	Rx	DP ML0	lane_0_1	Rx1±	B11, B10
	DP ML1	Tx	lane_1_0	Tx2±	B2, B3
	DP ML0	Rx	lane_1_1	Rx2±	A11, A10

Figure 4.24: The multiplexing relationship between the USB3.1 interface and the DP screen interface

4.11. UIM Card Interface

SRM955 can support two SIM card interfaces at the same time to realize dual card dual standby. Support SIM card hot swap, can automatically identify 1.8V and 3.0V cards. The following figure is the SIM recommended interface circuit. In order to protect the SIM card, it is recommended to use a TVS device for electrostatic protection. Devices of the peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

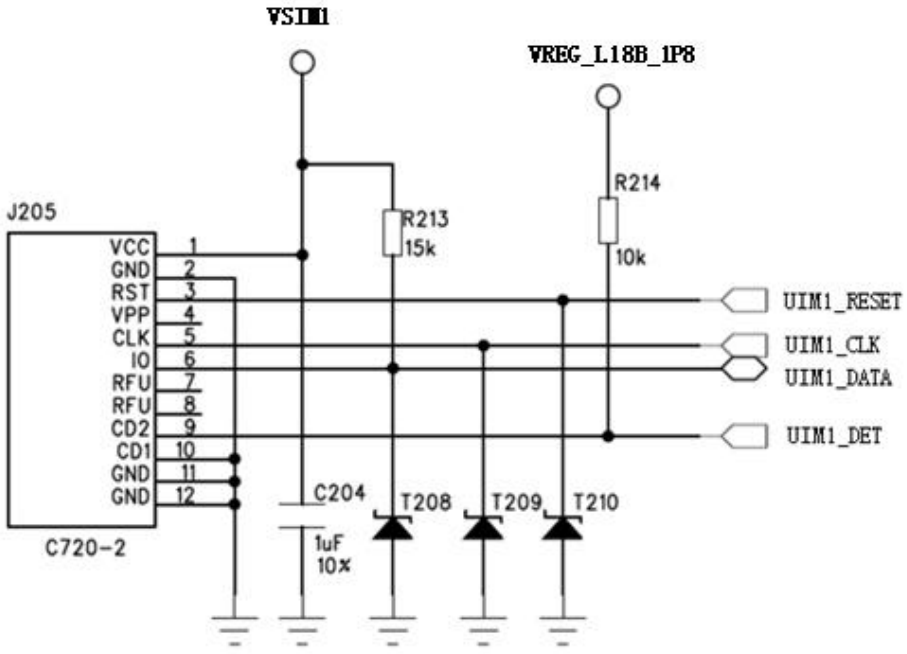


Figure 4.25: UIM card interface circuit

4.12. SD Card Interface

SRM955 supports SD card interface, up to 128GB

The reference circuit is as follows:

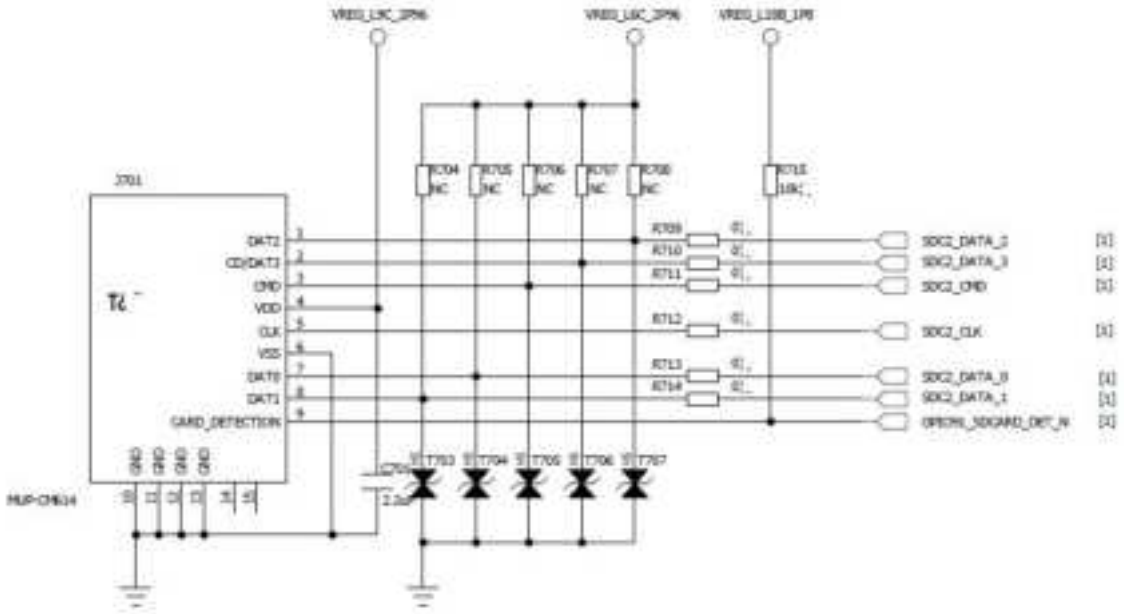


Figure 4.26: SD Card Interface Circuit

4.13. I2C Bus Interface

The SRM955 module supports 10-channel hardware I2C bus interface and 5-channel camera dedicated CCI interface. The pin definitions and default functions are as follows:

Table 4.11: I2C interface pin description

SENSOR_I2C_SDA/GPIO161	47	I/O	SENSOR_I2C signal	Pull high to VREG_L8C_1P8
SENSOR_I2C_SCL/GPIO162	48	I/O		
NFC_I2C_SDA/GPIO36*	524	I/O	General purpose I2C signals	Pull high to VREG_L18B_1P8
NFC_I2C_SCL/GPIO37	525	I/O		
HDMI_I2C_SDA/GPIO8*	515	I/O	General purpose I2C signals	Pull high to VREG_L18B_1P8
HDMI_I2C_SCL/GPIO9	514	I/O		
TS_I2C_SDA/GPIO52*	409	I/O	TP_I2C signal	Pull high to VREG_L12C_1P8
TS_I2C_SCL/GPIO53	410	I/O		
APPS_I2C_SDA/GPIO4*	252	I/O	General purpose I2C signals	Pull high to VREG_L18B_1P8
APPS_I2C_SCL/GPIO5	251	I/O		
CCI_I2C0_SCL/GPIO70	223	I/O	R-CAM I2C signal	Pull high to CAM_IOVDD_1P8 (external LDO)
CCI_I2C0_SDA/GPIO69	222	I/O		
CCI_I2C2_SCL/GPIO74	183	I/O	F-CAM I2C signal	Pull high to CAM_IOVDD_1P8
CCI_I2C2_SDA/GPIO73	182	I/O		
CCI_I2C1_SCL/GPIO72*	77	I/O	D-CAM I2C signal	Pull high to CAM_IOVDD_1P8
CCI_I2C1_SDA/GPIO71	76	I/O		
CCI_I2C3_SCL/GPIO76	94	I/O	RESERVED CAM I2C signal	Pull high to CAM_IOVDD_1P8
CCI_I2C3_SDA/GPIO75*	93	I/O		
MAG_I2C_SDA/GPIO163	476	I/O	MAG sensor I2C signal	Pull high to VREG_L8C_1P8
MAG_I2C_SCL/GPIO164	475	I/O		

Note: When using as an I2C bus interface, connect a 2.2KΩ pull-up resistor to 1.8V.

4.14. Analog To Digital Converter（ADC）

The SRM955 module provides multiple ADCs by the internal power management chip, supports 1.8V input, and has an accuracy of 15bit. See table below.

Table 4.12: The pin description of ADC interface

Pin Name	PIN number	I/O	Description	Remark
PM7250B_GPIO1/ADC1	42	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO5/ADC2	43	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO8/ADC3	44	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO11/ADC4	45	I/O	PM7250B_GPIO, used as ADC by default	
PM7250B_GPIO12/ADC5	46	I/O	PM7250B_GPIO, used as ADC by default	
PM7325_GPIO2/ADC6	434	I/O	PM7325_GPIO, used as ADC by default	
PM7325_AMUX4	435	I	Analog multiplexer (AMUX) input	
PM7325_AMUX2	436	I	Analog multiplexer (AMUX) input	

4.15. PWM

BL_PWM/PM7350C_GPIO9 (412PIN), EDP_PWM/PM7350C_GPIO8 (411PIN) can be used for LCD backlight adjustment, and the backlight brightness can be adjusted by adjusting the duty cycle.

4.16. Antenna Interface

The module provides 8 antenna interfaces such as ANT_0, ANT_1, ANT_2, ANT_3, ANT_4, WIFI_ANT0, WIFI_ANT1, GNSS_ANT, etc. In order to ensure that the user's product has good wireless performance, the antenna selected by the user should meet the requirements of an input impedance of 50 ohms and a standing wave coefficient of less than 2 in the working frequency band.

4.16.1 WAN ANT(ANT_0/1)

The module provides ANT_0/1 antenna interface, the antenna on the user's motherboard should be connected to the antenna pin of the module using a microstrip line or stripline with a characteristic impedance of 50 ohms.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

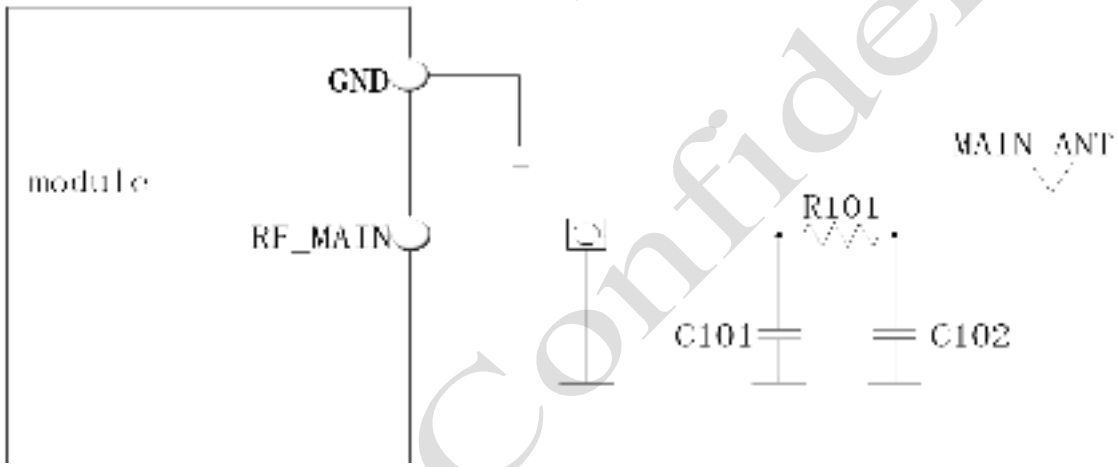


Figure 4.27: ANT_0/1/2/3 antenna interface connection circuit

In the figure, R101, C101, and C102 are antenna matching devices, and the specific component values can be determined after the antenna factory has debugged the antenna. Among them, R101 defaults to 0R, and C101 and C102 default to not.

If there are fewer components that can be placed between the antenna and the module output, or when the RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the following figure:

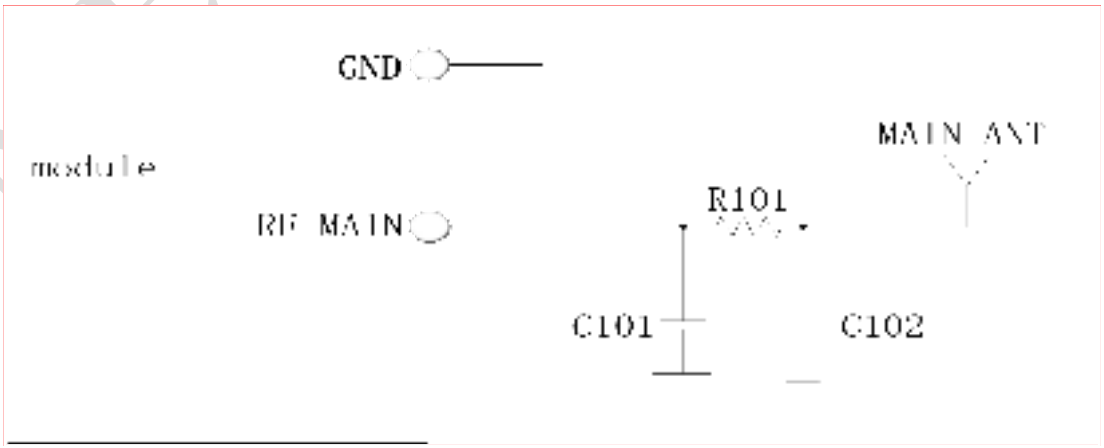


Figure 4.28: ANT_0/1/2/3 antenna interface simplified connection circuit

In the above picture, R101 is pasted 0R by default, and C101 and C102 are not pasted by default.

4.16.2 GPS Antenna

The module provides the GNSS antenna pin RF_GPS, the antenna on the user's motherboard should use a microstrip line or stripline with a characteristic impedance of 50 ohms to connect to the antenna pin of the module. There is no LNA integrated inside the module.

To improve GNSS reception performance, customers can use an external active antenna. The recommended circuit connection is shown in the following figure:

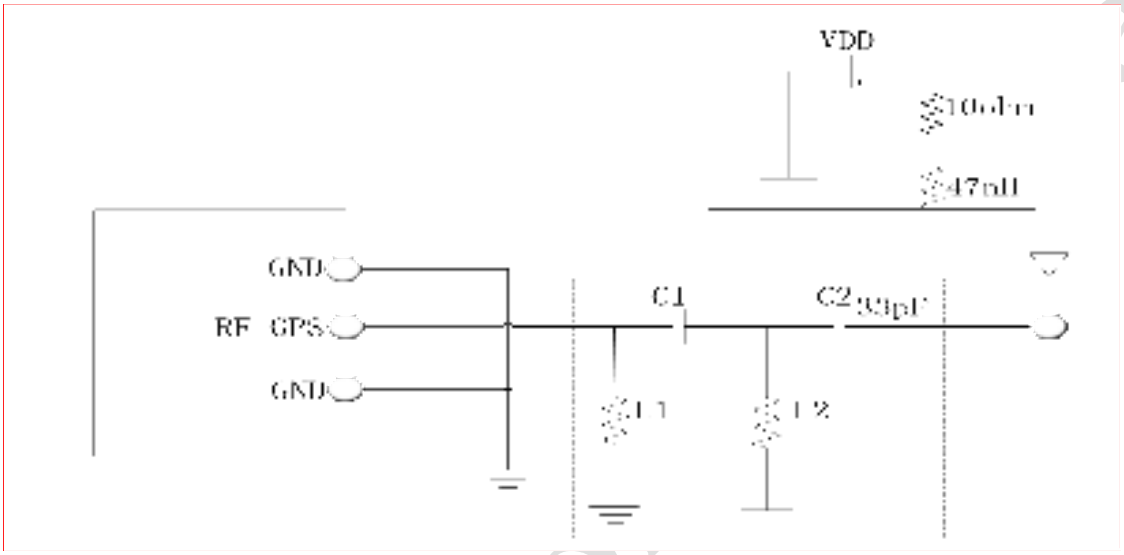


Figure 4.29: Connecting Active Antennas

4.16.3 WiFi/BT Antenna

The module provides Wifi ANT_0/1 antenna pins, and the antenna on the user's motherboard should be connected to the module's antenna pins using a microstrip line or stripline with a characteristic impedance of 50 ohms.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

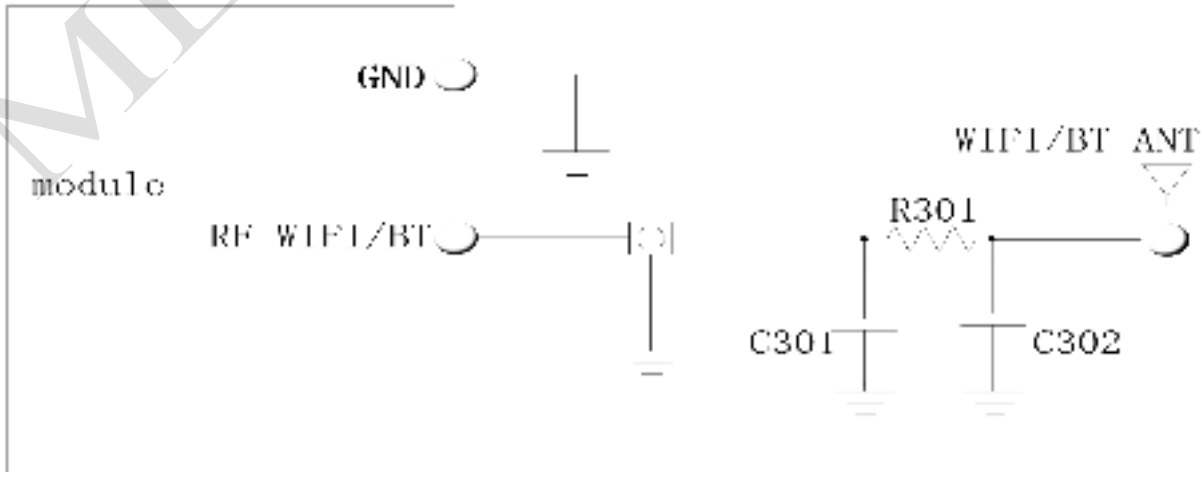


Figure 4.30: WiFI_BT antenna interface connection circuit

In the figure, R301, C301, and C302 are antenna matching devices, and the specific component values can be determined after the antenna factory has debugged the antenna. Among them, R301 defaults to 0R, C301 and C302 do not default.

If there are fewer components that can be placed between the antenna and the module output, or when the RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the following figure:

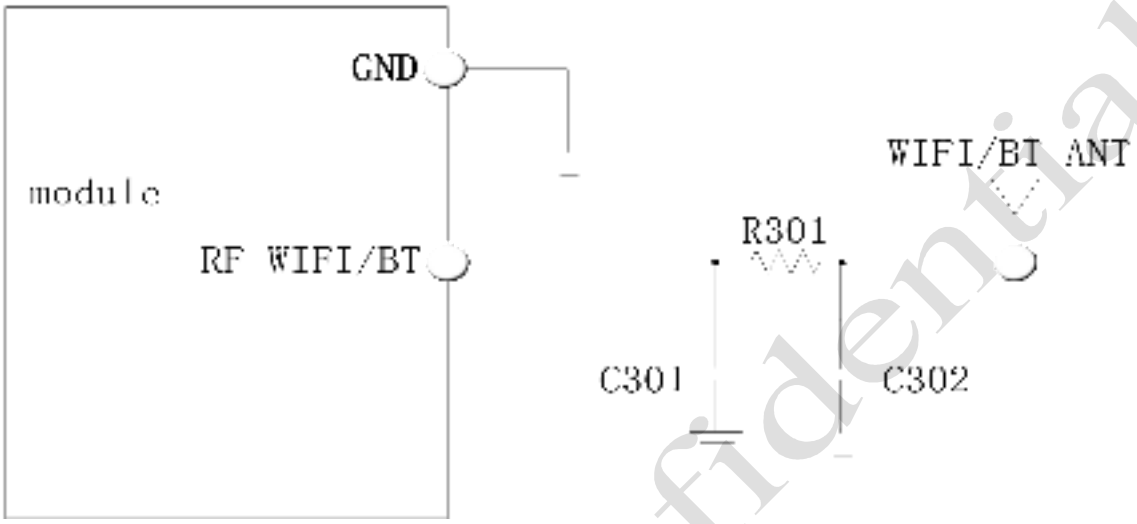


Figure 4.31: WIFI_BT antenna interface simplified connection circuit

In the above picture, R301 is pasted 0R by default, and C301 and C302 are not pasted by default.

5. PCB Layout

The quality of a product's performance largely depends on the PCB traces. As mentioned earlier, if the PCB layout is unreasonable, it may cause interference problems such as card dropping. The way to solve these interferences is often to redesign the PCB. If a good PCB layout can be planned in the early stage, so that the PCB routing is smooth, it can save a lot of time. , Of course, it can also save a lot of costs. This chapter mainly introduces some matters that users should pay attention to in the PCB layout stage to minimize interference problems and shorten the user's research and development cycle.

The SRM955 module is an intelligent module with its own Android operating system. It includes sensitive data lines such as high-speed USB and MIPI. It also has strict requirements on the length and impedance of the signal lines. If the high-speed signal processing is not good, it will cause serious EMI. If the problem is more serious, it will also affect the identification of USB and the display of LCD. Therefore, when using the SRM955 module, the PCB design requirements are much higher than that of the previous 4G module. Please read this chapter carefully to reduce the subsequent hardware debugging cycle.

When using the SRM955 module, users are required to use at least a 6-layer first-order design on the PCB, which is convenient for impedance control and signal line shielding.

5.1. Module PIN Distribution

Before PCB layout, you must first understand the pin distribution of the module, and rationally arrange the related devices and interfaces according to the distribution defined by the pins. Please refer to Figure 3.1 to determine the distribution of the module's functional pins.

5.2. PCB Layout Guidelines

There are several aspects to pay attention to in the PCB layout stage:

5.2.1. Antenna

Antenna part design, SRM955 module has a total of 8 antenna interfaces, they are: ANT_0, ANT_1, ANT_2, ANT_3, ANT_4, WIFI_ANT0, WIFI_ANT1, GNSS_ANT. Attention should be paid to the placement of components and RF wiring:

- The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pins of the module;
- The antenna matching circuit needs to be placed close to the antenna end;
- The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;
- The components and connections between the antenna pins of the module and the antenna connector must be kept away from high-speed signal lines and strong interference sources, and avoid crossing or parallel with any signal lines on adjacent layers.
- The length of the RF line between the antenna pin of the module and the antenna connector should be as short as possible, and it should absolutely avoid the situation of crossing the entire PCB board.
- If the antenna is connected by a coaxial radio frequency line, care should be taken to avoid making the coaxial radio frequency line straddle the SIM card, power supply circuit, and high-speed digital circuit to minimize mutual influence.

5.2.2. Power

The power trace should not only consider VBAT, but also the return GND of the power supply. The trace of the positive pole of VBAT must be short and thick, and the trace must first pass through a large capacitor, a Zener diode, and then to the power PIN of the module. There are multiple PAD exposed coppers at the bottom of the module. It is necessary to ensure that the GND path from these exposed copper areas to the power supply is the shortest and most unobstructed. In this way, the current path of the entire power supply can be guaranteed to be the shortest and the interference can be minimized.

5.2.3. SIM Card

The SIM card has a large area and has no anti-EMI interference devices, so it is more susceptible to interference. Therefore, when laying out, first ensure that the SIM card is far away from the antenna and the antenna extension cable inside the product, and is placed as close to the module as possible. When routing the PCB, pay attention to To protect the SIM_CLK signal, the SIM_DATA, SIM_RST and SIM_VDD signals of the SIM card should be kept away from the power supply and high-speed signal lines. If it is not handled properly, it will easily cause the card not to recognize or drop the card, so please follow the following principles when designing:

- During the PCB layout stage, the SIM card holder must be kept away from the GSM antenna;
- The SIM card wiring should be kept as far away as possible from RF lines, VBAT and high-speed signal lines, and the SIM card wiring should not be too long;
- The GND of the SIM card holder should maintain good connectivity with the GND of the module, so that

the two GNDs are equipotential;

- To prevent SIM_CLK from interfering with other signals, it is recommended to protect SIM_CLK;
- It is recommended to place a 100nF capacitor on the SIM_VDD signal line close to the SIM card holder;
- Place a TVS near the SIM card holder, the parasitic capacitance of the TVS should not be greater than 50pF, and a 51Ω resistor in series with the module can enhance ESD protection;
- The SIM card signal line can reserve 22pf capacitance to ground to prevent radio frequency interference.
- The return path of VBAT has a large current passing through, so the SIM card wiring should avoid the return path of VBAT as much as possible.

5.2.4. T Card

The CLK signal (SDC2_CLK) of the T card should be grounded separately, and the ground wire of the grounding path should be appropriately increased with ground holes; the rest of the data lines should be combined to three-dimensionally cover the ground; the total load capacitance of each signal line is less than 5pF (including the TVS capacitance value and filter capacitor).

5.2.5. MIPI

MIPI is a high-speed signal line. The user must pay attention to protection during the layout stage to keep it away from the signal line that is easily disturbed. It must be processed with GND on the top, bottom, left, and right. To ensure the consistency of impedance, try not to bridge different GND planes.

When choosing an ESD device for the MIPI interface, please choose a TVS with a small capacitance value. It is recommended that the parasitic capacitance be less than 1pF.

MIPI routing requirements are as follows:

The total length of the wiring should not exceed 130mm

- It is required to control 85 ohm differential impedance with an error of ±10%.
- The length error of the differential line within the group is controlled within 0.7mm.
- The length error between groups is controlled within 1.4mm.

5.2.6. USB

The module supports high-speed USB interface with a rate of 480Mbps. Users are recommended to add a common mode inductor in the schematic design stage, which can effectively suppress EMI interference. If users need to increase electrostatic protection, please choose a TVS tube with parasitic capacitance less than 1pF. Please refer to the following precautions when Layout:

- The common mode inductor should be close to the side of the USB connector.
- It is required to control 90 ohm differential impedance with an error of ±10%.
- The length error of USB2.0 differential line is controlled within 2mm, and the length error of USB3.1 differential line is controlled within 0.7mm.
- If the Type-C over DP function is available, the length error between different differential line pairs of USB3.1 is required to be controlled within 10mm, and the length error of the DP_AUX differential line is controlled within 7mm.
- If the USB has a charging function, please pay attention to the VBUS trace as wide as possible.
- If there are test points, try to avoid bifurcation of the traces, and place the test points on the path of the

traces.

Table 5.1: Length of USB traces inside the module

Signal	Length(mm)	Length Error (P-N)
USB0_HS_DP	26.49155	-0.02mm
USB0_HS_DM	26.51779	
USB1_HS_D_P	20.69148	0.04mm
USB1_HS_D_M	20.65643	
USB0_SS_TX1_P	26.99998	0.008mm
USB0_SS_TX1_M	26.99197	
USB0_SS_RX1_P	25.79985	0.008mm
USB0_SS_RX1_M	25.79123	
USB0_SS_TX0_P	26.2734	-0.12mm
USB0_SS_TX0_M	26.39373	
USB0_SS_RX0_P	28.19452	-0.37mm
USB0_SS_RX0_M	28.42193	

5.2.7. Audio

The module supports 3 channels of analog audio signals. Analog signals are susceptible to interference from high-speed digital signals. So please stay away from high-speed digital signal lines. The module supports the GSM standard, and the GSM signal can interfere with the audio through coupling and conduction. Users can add 33pF and 10pF capacitors to the audio path to filter out coupling interference. The 33pF capacitor mainly filters out the interference in the GSM850/EGSM900 frequency band, and the 10pF capacitor mainly filters out the interference in the DCS1800 frequency band. The coupling interference of TDD has a lot to do with the user's PCB design. In some cases, the TDD in the GSM850/EGSM900 frequency band is more serious, and in some cases the TDD interference in the DCS1800 frequency band is serious. Therefore, users can select the required filter capacitors according to the actual test results, and sometimes even do not need to paste filter capacitors.

The GSM antenna is the main source of coupling interference for TDD, so users should pay attention to keeping the audio traces away from the GSM antenna and VBAT during PCB layout and routing. It is best to place a set of audio filter capacitors close to the module end, and another set close to the interface end. The audio output should be routed according to the differential signal rules.

The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the "squeak" sound at the output end of the SPK,.Therefore, when designing the schematic diagram, it is best to connect some large-capacity capacitors and series magnetic beads in parallel at the input end of the Audio PA.

TDD and GND are also closely related. If the GND is not handled properly, many high-frequency interference signals will interfere with the MIC and Speaker through bypass capacitors and other devices. Therefore, the user should ensure the good performance of the GND during the PCB design stage.

5.2.8. Other

The serial port interface of the module should also keep the distance as short as possible.

6. Electrical, Reliability

6.1. Absolute Maximum

The table below shows the absolute maximum values that the module can withstand, exceeding these limits may result in permanent damage to the module.

Table 6.1: Absolute Maximum Values

Parameter	Minimum	Typical Value	Maximum	Unit
VBAT	--0.3	-	6	V
VBUS	--0.3	-	28	V
Peak Current	-	-	4	A

6.2. Operating Temperature

The following table shows the operating temperature range of the module:

Table 6.2: Module operating temperature

Parameter	Minimum	Typical Value	Maximum	Unit
Operating Temperature	-25	-	75	℃
Storage Temperature	-40	-	90	℃

6.3. Operating Voltage

Table 6.3: Module operating voltage

Parameter	Minimum	Typical Value	Maximum	Unit
VBAT	3.5	3.8	4.35	V
VBUS	3.7	5	12.6	V

6.4. Digital Interface Features

Table 6.4: Digital Interface Characteristics (1.8V)

Parameter	Description	Minimum	Typical Value	Maximum	Unit
V_{IH}	Input high level voltage	1.17	1.8	2.1	V
V_{IL}	Input low level voltage	-0.3	0	0.63	V
V_{OH}	Output high level voltage	1.35	-	1.8	V
V_{OL}	Output low level voltage	0	-	0.45	V

6.5. Characteristics Of SIM_VDD

Table 6.5: SIM_VDD characteristics

Parameter	Description	Minimum	Typical Value	Maximum	Unit
Vo	The output voltage	1.65	1.8	1.95	V
		-	2.95	-	
Io	The output current	-	-	150	mA

6.6. Features Of PWRKEY

Table 6.6: Features of PWRKEY

Parameter	Description	Minimum	Typical Value	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	2000			ms

6.7. Features Of VCOIN

Table 6.7: VCOIN Characteristics

Parameter	Description	Minimum	Typical Value	Maximum	Unit
$VCOIN_{-IN}$	VCOIN input voltage	2.1	3.0	3.25	V
$VCOIN_{-OUT}$	VCOIN output voltage	-	3.0	-	V

6.8. Current Consumption (VBAT=3.8V)

Table 6.8: Current consumption

Parameter	Description	Condition	Minimum	Typical Value	Maximum	Unit
VBAT	Voltage	Voltage must be between maximum and minimum	3.5	3.8	4.35	V
Ivbat	Average current	Shutdown mode	-	-	200	uA
		GSM standby power consumption	-	-	TBD	mA
		WCDMA standby power consumption	-	-	TBD	mA
		TD-S standby power consumption	-	-	TBD	mA
		CDMA standby power consumption	-	-	TBD	mA
		FDD standby power consumption			TBD	mA
		TDD standby power consumption			TBD	mA
	Call consumption	GSM900 CH62 32dBm	-	-	TBD	mA
		WCDMA2100 CH10700 22.5 dBm	-	-	TBD	mA
	Digital transmission	GPRS GSM900 CH62 PCL5 1DL 4UL	-	-	TBD	mA
		EGPRS GSM900 CH62 PCL8 1DL 4UL	-	-	TBD	mA
Imax	Peak current	Power control at maximum output power	-	-	4	A

6.9. Static Protection

The modules are not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling and operating the module.

6.10. Module Working Frequency

The following table lists the operating frequency band of the module, which conforms to the 3GPP TS 05.05 technical specification.

Table 6.9: Module operating frequency band

Frequency band	Reception	Emission	Physical channel
LTE B2	1930 ~ 1990 MHz	1850 ~ 1910 MHz	TX: 18600 ~ 19199
			RX: 600~1199
LTE B4	2110 ~ 2155 MHz	1710 ~ 1755 MHz	TX: 19950~20399
			RX: 1950~2399
LTE B5	869 ~ 894MHz	824 ~ 849MHz	TX: 20400~20649
			RX: 2400~2649
LTE B12	729 ~ 746MHZ	699 ~ 716MHZ	TX: 23010~23179
			RX: 5010~5179
LTE B13	746 ~ 756MHz	777 ~ 787MHz	TX: 23180~23279
			RX: 5180~5279
LTE B14	758 ~ 768MHZ	788 ~ 798MHz	TX: 23280~23379
			RX: 5280~5379
LTE B17	734 ~ 746MHZ	704 ~ 716MHz	TX: 23730~23849
			RX: 5730~5849
LTE B25	1930 ~ 1995 MHz	1850 ~ 1915 MHz	TX: 26040~26689
			RX: 8040~8689
LTE B29	717 ~ 728 MHz		RX: 9660 ~ 9769
LTE B30	1880 ~ 1920 MHz	1880 ~ 1920 MHz	TX: 27660~27759
			RX: 9770~9869
LTE B46	5150 ~ 5925 MHz		RX: 46790~54539
LTE B71	663 ~ 698 MHz	617 ~ 652 MHz	TX: 133122~133471
			RX: 68586~68935
LTE B66	2110 ~ 2200 MHz	1710 ~ 1780 MHz	TX: 131972~132671
			RX: 66436~67335
LTE B38	2570 ~ 2620 MHz	2570 ~ 2620 MHz	37750 ~ 38249
LTE B41	2496 ~ 2690 MHz	2496 ~ 2690 MHz	39650 ~ 41589
LTE B42	3400 ~ 3600 MHz	3400 ~ 3600 MHz	41590 ~ 43589
LTE B43	3600 ~ 3800 MHz	3600 ~ 3800 MHz	43590 ~ 45589
LTE B48	3550 ~ 3700 MHz	3550 ~ 3700 MHz	55240 ~ 56739
N2	1930 ~ 1990 MHz	1850 ~ 1910 MHz	TX: 370000 ~ 382000
			RX: 386000~398000
N5	869 ~ 894MHz	824 ~ 849MHz	TX: 164800~169800
			RX: 173800~178800
N12	729 ~ 746MHZ	699 ~ 716MHZ	TX: 139800~143200

			RX: 145800~149200
N25	1930 ~ 1995 MHz	1850 ~ 1915 MHz	TX: 370000~383000
			RX: 386000~399000
N30	1880 ~ 1920 MHz	1880 ~ 1920 MHz	TX: 461000~463000
			RX: 470000~472000
N38	2570 ~ 2620 MHz	2570 ~ 2620 MHz	514000~524000
N41	2496 ~ 2690 MHz	2496 ~ 2690 MHz	500202 ~ 537000
N48	3550 ~ 3700 MHz	3550 ~ 3700 MHz	636667 ~ 646666
N66	2110 ~ 2200 MHz	1710 ~ 1780 MHz	TX: 342000~356000
			RX: 422000~440000
N71	663 ~ 698 MHz	617 ~ 652 MHz	TX: 132600~139600
			RX: 123400~130400
N78	3300 ~ 3800 MHz	3300 ~ 3800MHz	620334 ~ 653000
N77	3300 ~ 4200MHz	3300 ~ 4200MHz	620000 ~ 680000

6.11. RF Characteristics

The table below lists the conducted RF output power of the module in accordance with 3GPP TS 05.05 technical specification, 3GPP TS 134121-1 standard.

Table 6.10: Conducted output power

Frequency band	Standard output power (dBm)	Output Power Tolerance (dBm)
LTE	23 dBm	±2.7
NA-FDD	23 dBm	(+2/-2.5)
NA-TDD	26 dBm	(+2/-3)

6.12. Module Conducted Receive Sensitivity

The following table lists the conducted reception sensitivity of the module, which is tested under static conditions.

Table 6.11: Conducted Receive Sensitivity

Frequency band	Receive Sensitivity (Typical)	Receive Sensitivity (Maximum)
N1	TBD(10M)	3GPP requirements
	TBD (50M)	3GPP requirements
N3	TBD (10M)	3GPP requirements
	TBD (30M)	3GPP requirements
N28	TBD (10M)	3GPP requirements
	TBD (30M)	3GPP requirements
N41	TBD (10M)	3GPP requirements
	TBD (100M)	3GPP requirements
N78	TBD (10M)	3GPP requirements
	TBD (100M)	3GPP requirements
N79	TBD (10M)	3GPP requirements
	TBD (100M)	3GPP requirements
LTE FDD/TDD	TBD (100M)	3GPP requirements
	See Table 6.12	3GPP requirements

Table 6.12: LTE Reference Sensitivity 3GPP Dual Antenna Requirements (QPSK)

E-UTRA band number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex Mode
1							FDD
2							FDD
3							FDD
4							FDD
5							FDD
6							FDD
7							FDD
8							FDD

9							FDD
10							FDD
11							FDD
12							FDD
13							FDD
14							FDD
...							
17							FDD
18							FDD
19							FDD
20							FDD
21							FDD
22							FDD
23							FDD
24							FDD
25							FDD
26							FDD
27							FDD
28							FDD
31							FDD
...							
33							TDD
34							TDD
35							TDD
36							TDD
37							TDD
38							TDD
39							TDD
40							TDD
41							TDD

6.13. The Main RF Performance Of WIFI

The following table lists the main RF performance under WIFI conduction.

Table 6.13: Main RF performance parameters under WIFI conduction

2.4G transmission performance					
	802.11B	802.11G	802.11N	802.11AX	
Transmit power (minimum rate)					dBm
Transmit Power (Max Rate)					dBm
EVM (maximum rate)					dB
2.4G reception performance					
Receive sensitivity	802.11B	802.11G	802.11N	802.11AX	
Minimum speed					dBm
Maximum speed					dBm
5G launch performance					
	802.11A	802.11N	802.11AC	802.11AX	
Transmit power (minimum rate)					dBm
Transmit Power (Max Rate)	15	14	12	11	dBm
EVM (Maximum rate)					dB
5G reception performance					
Receive sensitivity	802.11A	802.11N	802.11AC	802.11AX	
Minimum speed					dBm
Maximum speed					dBm
6G launch performance					
	802.11A	802.11AX			
Transmit power (minimum rate)					
Transmit Power (Max Rate)					
EVM (Maximum rate)					
6G reception performance					
Receive sensitivity	802.11A	802.11AX			
Minimum speed					dBm
Maximum speed					dBm

6.14. Main RF Performance Of BT

The following table lists the main RF performance under BT conduction.

Table 6.14: Main RF performance parameters under BT conduction

Launch performance				
Transmit power	DH5	2DH5	3DH5	
				dBm
Receiving performance				
Receive sensitivity	DH5	2DH5	3DH5	
				dBm

6.15. Key RF Performance Of GNSS

The following table lists the main RF performance under GNSS conduction.

Table 6.15: Main RF performance parameters under GNSS conduction

GNSS working frequency band: 1575.42MHZ				
GNSS carrier-to-noise ratio CN0: 40dB/Hz				
GNSS Sensitivity:	Capture (cold start)	Capture (warm start)	Track	
				dBm
GNSS start-up time	Hot start	Warm start	Cold start	
				s

7. Production

7.1. Top And Bottom Views Of The Module

Figure 7.1: Module top and bottom views (not yet available)

7.2. Recommended Welding Furnace Temperature Curve

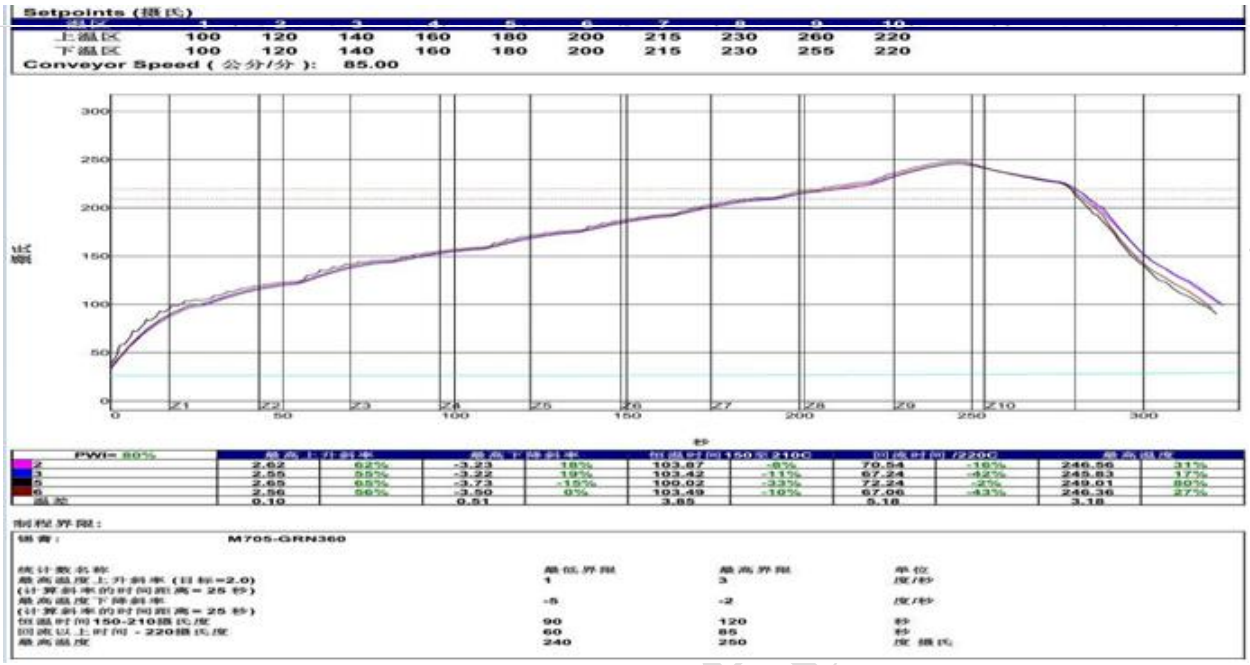


Figure 7.2: Recommended soldering furnace temperature curve for modules

7.3. Moisture Sensitive Characteristics (MSL)

The SRM955 module complies with humidity sensitivity class 3. Under the environmental conditions of temperature <30 degrees and relative humidity <60%, dry packaging executes J-STD-020C specification according to IPC/JEDEC standard. Shelf life is at least 6 months in the unopened condition under ambient conditions of temperature <40 degrees and relative humidity <90%. After unpacking, Table 22 lists the shelf life of the modules corresponding to different moisture sensitivity levels.

Table 7.1: Humidity sensitivity level distinction

Grade	Factory environment++30 ℃/60%RH
1	Under the condition of environmental 3+30 ℃/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Forced baking before use. After baking, the module must be picked within the time limit specified on the label.

After sealing, under the environmental conditions of the temperature <30 degrees and relative humidity <60%, SMT patch is performed within 168 hours. If the above conditions are not met, it is necessary to bake. Note: Oxidation risk: Baking SMD packaging may cause metal oxidation, if excessive causes welding problems during the circuit board assembly process. The temperature and time of baking SMD packaging are limited to weldable considerations. The accumulation of baking time should not exceed 96 hours at the temperature greater than 90 ° C and up to 125 ° C.

7.4. Baking Demand

Due to the wet sensitivity characteristics of the module, the SRM955 should be baked sufficiently before the reflow welding, otherwise the module may cause permanent damage during the return welding process. SRM955 should be baked 192 hours in a low-temperature container with a temperature of 40 ° C +5 ° C /-0 ° C and a relative humidity of less than 5%, or 72 in high temperature containers of the module for 80 ° C ± 5 ° C. Calf -hour baking. The user should notice that the tray is not high to resist, and the user should take the module out of the tray to bake, otherwise the tray may be damaged by high temperature.

Table 7.2: Baking requirements:

Baking temperature	Humidity	Baking time
40°C±5°C	<5%	192 hours
120°C±5°C	<5%	4 hours

8. Support The List Of Peripheral Devices

SRM955 peripheral devices can support devices contained in the platform QVL. The following is a software default adaptering device.

Table 8.1: Support the list of display screen models

Manufacturer	Driver IC	Specification
ZONEWAY/中正威	ILI9881P	1280x720

Table 8.2: List of supporting Camera model

Manufacturer	Driver IC	Specification
YDOPTICS/远大	s5k3m2xx	13M
YDOPTICS/远大	s5k4h7	8M
SUNNYOPTICAL/舜宇	S5K5E8	5M

Table 8.3: Support touch screen model list

Manufacturer	Driver IC	Specification
ZONEWAY/中正威	GT5688	5"

Table 8.4: Support GSENSOR model list

Manufacturer	Driver IC	Specification
Bosch/博世	BMI120	9-Axis,16-bit

Table 8.5: Support the ECOMPASS model list

Manufacturer	Driver IC	Specification
ACEINNA /新纳传感	GM303	3-Axis,14-bit

Table 8.6: Support PS/ALS Sensor model list

Manufacturer	Driver IC	Specification
LITEON/光宝	LTR-553ALS-01	ALS+PS

Table 8.7: Support Gyro Sensor model list

Manufacturer	Driver IC	Specification
Bosch/博世	BMI120	9-axis,16bit/16bit

9. Appendix

9.1. Related Documentation

Table 9.1: Related documents

Serial number	File name	Annotation
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)； Mobile Station (MS) conformance specification； Part 1： Conformance specification
[8]	AN_Serial Port	AN_Serial Port

9.2. Terminology And Explanation

Table 9.2: Terms and explanations

The term	Explanation
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module

SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
TEL	Telephone
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

9.3. Reuse Function

Table 9.3: Reuse function

GPIO QUP configurations

	GPIO number	Serial engine	Multiplexed interfaces		
QUP0	GPIO_0	SE0	UART_CTS	SPI_MISO	I2C_SDA/I3C_SDA
	GPIO_1		UART_RFR	SPI_MOSI	I2C_SCL/I3C_SCL
	GPIO_2		UART_TX	SPI_SCLK	–
	GPIO_3		UART_RX	SPI_CS0	–
	GPIO_4	SE1	UART_CTS	SPI_MISO	I2C_SDA/I3C_SDA
	GPIO_5		UART_RFR	SPI_MOSI	I2C_SCL/I3C_SCL
	GPIO_6		UART_TX	SPI_SCLK	–
	GPIO_7		UART_RX	SPI_CS0	–
	GPIO_8	SE2	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_9		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_10		UART_TX	SPI_SCLK	–
	GPIO_11		UART_RX	SPI_CS0	–
	GPIO_12	SE3	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_13		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_14		UART_TX	SPI_SCLK	–
	GPIO_15		UART_RX	SPI_CS0	–
	GPIO_16	SE4	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_17		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_18		UART_TX	SPI_SCLK	–
	GPIO_19		UART_RX	SPI_CS0	–
	GPIO_20	SE5	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_21		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_22		UART_TX	SPI_SCLK	–
	GPIO_23		UART_RX	SPI_CS0	–
	GPIO_24	SE6	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_25		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_26		UART_TX	SPI_SCLK	–
	GPIO_27		UART_RX	SPI_CS0	–
	GPIO_28	SE7	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_29		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_30		UART_TX	SPI_SCLK	–
	GPIO_31		UART_RX	SPI_CS0	–
	GPIO_2		–	SPI_CS_1	–

	GPIO number	Serial engine	Multiplexed interfaces		
	GPIO_3		–	SPI_CS_2	–
	GPIO_6		–	SPI_CS_3	–
QUP1	GPIO_32	SE0	UART_CTS	SPI_MISO	I2C_SDA/SPMI
	GPIO_33		UART_RFR	SPI_MOSI	I2C_SCL/SPMI
	GPIO_34		UART_TX	SPI_SCLK	–
	GPIO_35		UART_RX	SPI_CS0	–
	GPIO_36	SE1	UART_CTS	SPI_MISO	I2C_SDA/I3C_SDA
	GPIO_37		UART_RFR	SPI_MOSI	I2C_SCL/I3C_SCL
	GPIO_38		UART_TX	SPI_SCLK	–
	GPIO_39		UART_RX	SPI_CS0	–
	GPIO_40	SE2	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_41		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_42		UART_TX	SPI_SCLK	–
	GPIO_43		UART_RX	SPI_CS0	–
	GPIO_44	SE3	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_45		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_46		UART_TX	SPI_SCLK	–
	GPIO_47		UART_RX	SPI_CS0	–
	GPIO_48	SE4	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_49		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_50		UART_TX	SPI_SCLK	–
	GPIO_51		UART_RX	SPI_CS0	–
	GPIO_55		–	SPI_CS1	–
	GPIO_54		–	SPI_CS2	–
	GPIO_38		–	SPI_CS3	–
	GPIO_52	SE5	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_53		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_54		UART_TX	SPI_SCLK	–
	GPIO_55		UART_RX	SPI_CS0	–
	GPIO_56	SE6	UART_CTS	SPI_MISO	I2C_SDA
	GPIO_57		UART_RFR	SPI_MOSI	I2C_SCL
	GPIO_58		UART_TX	SPI_SCLK	–
	GPIO_59		UART_RX	SPI_CS_0	–
	GPIO_62		–	SPI_CS_1	–
	GPIO_63		–	SPI_CS_2	–
	GPIO_50		–	SPI_CS_3	–
	GPIO_60	SE7	UART_CTS	SPI_MISO	I2C_SDA

The GPIO32 and GPIO33 are only used inside the module. The reuse function of the same QUP/SE can only be used at the same time.

9.4. Safety Warning

Pay attention to the following security precautions in the process of using or repairing any terminal or mobile phone. Terminal devices should be informed of the following security information. Otherwise, Meig will not bear any consequences that the user does not follow these warning operations.

Table 9.4: Security warning

Identify	Requirement
	When you are next to hospitals or medical equipment, you can observe the restrictions of your mobile phone. You need to turn off the terminal or mobile phone, otherwise the medical equipment may cause misunderstanding due to radio frequency interference.
	Close the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the plane. Ignoring the above matters will violate local laws and may cause flight accidents.
	Do not use mobile terminals or mobile phones before flammable gas. When close to explosive operations, chemical factories, fuel libraries or gas stations, turn off the mobile terminal. It is very dangerous to operate the mobile terminal next to any potential explosion.
	The mobile terminal will receive or emit radiofrequency energy when booting. It will interfere with the TV, radio, computer or other electrical equipment.
	The road is safety first! Do not hold the terminal or mobile phone when driving the transportation, please use the non -mentioned device. Parking before using handheld terminals or mobile phones.
	The GSM mobile terminal is operated under the radio frequency signal and the honeycomb mesh, but it cannot be connected when used. For example, there is no toll or invalid SIM card. When you are in this situation and you need an emergency service, remember to use an emergency call. In order to be able to call and receive a phone call, the mobile terminal must be turned on and the service area with a strong mobile signal. When some determined network services or telephone functions are not allowed to use emergency calls, such as function locks and keyboard locks. These functions should be lifted before using an emergency call. Some networks require effective SIM card support.

Shenzhen Maggie Smart Technology Co., Ltd. Shanghai Branch
Contact Address: Building 5, Building G, No. 2337, Gu Dai Road, Minhang District, Shanghai
Post Code:200233
Telephone:+862154278676
Fax:+862154278679
URL:www.meigchina.com

15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

15.21 Changes or modification warning.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help

RF warning for Mobile device:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 15 22 24 27 96

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not application

2.5 Trace antenna designs

Not application

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

Antenna Type(Dipole)	BT/2.4Gwifi 3.95 dBi; U-NII-1 1.46dBi; U-NII-2A 1.52dBi; U-NII-2C 1.29dBi; U-NII-3 1.48dBi; U-NII-5 0.96dBi; U-NII-6 0.75dBi; U-NII-7 0.77dBi; U-NII-8 1.56dBi;
Antenna connector	SMA

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: “Contains FCC ID: 2APJ4-SRM955”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

Industry Canada statement

This complies with ISED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

5G WIFI statement

The device is restricted to indoor use when operated in 5150MHz~5350MHz to reduce the potential for interference and 5600-5650 MHz frequency band cannot use in Canada.

Radiation Exposure Statement:

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with greater than 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé à plus de 20 cm entre le radiateur et votre corps.

IC statement

The final end product must be labeled in a visible area with the following "Contains IC: 23860-SRM955"

The Host Marketing Name (HMN) must be indicated at any location on the exterior of the host product or product packaging or product literature, which shall be available with the host product

or online.

This radio transmitter [IC: 23860-SRM955] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Frequency range	Manufacturer	Peak gain	Impedance	Antenna type
2400-2483.5Mhz	TOXU TECHNOLOGY CO., LTD.	3.95 dBi	50ohm	Dipole
U-NII-1	TOXU TECHNOLOGY CO., LTD.	1.46dBi	50ohm	Dipole
U-NII-2A	TOXU TECHNOLOGY CO., LTD.	1.52dBi	50ohm	Dipole
U-NII-2C	TOXU TECHNOLOGY CO., LTD.	1.29dBi	50ohm	Dipole
U-NII-3	TOXU TECHNOLOGY CO., LTD.	1.48dBi	50ohm	Dipole
U-NII-5	TOXU TECHNOLOGY CO., LTD.	0.96dBi	50ohm	Dipole
U-NII-6	TOXU TECHNOLOGY CO., LTD.	0.75dBi	50ohm	Dipole
U-NII-7	TOXU TECHNOLOGY CO., LTD.	0.77dBi	50ohm	Dipole
U-NII-8	TOXU TECHNOLOGY CO., LTD.	1.56dBi	50ohm	Dipole

1.The OEM integrator must be aware not to provide information to the end user regarding how to install or remove this RF module in the user manual of the end product. The user manual which is provided by OEM integrators for end users must include the following information in a prominent location.

L'intégrateur OEM doit être conscient de ne pas fournir d'informations à l'utilisateur final sur la manière d'installer ou de retirer ce module RF dans le manuel d'utilisation du produit final. Le manuel d'utilisation fourni par les intégrateurs OEM pour les utilisateurs finaux doit inclure les informations suivantes dans un emplacement visible.

2.To comply with IC RF exposure compliance requirements, the antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter, except in accordance with IC multi-transmitter product procedures. Pour se conformer aux exigences de conformité de l'exposition RF IC, l'antenne utilisée pour cet émetteur ne doit pas être co-localisée ou fonctionner en conjonction avec une autre antenne ou un autre émetteur, sauf conformément aux procédures du produit multi-émetteur IC.

3.The final system integrator must ensure there is no instruction provided in the user manual or customer documentation indicating how to install or remove the transmitter module except such device has implemented two-ways authentication between module and the host system. L'intégrateur système final doit s'assurer qu'aucune instruction n'est fournie dans le manuel de l'utilisateur ou dans la documentation du client indiquant comment installer ou retirer le module

transmetteur, sauf qu'un tel dispositif a mis en place une authentification bidirectionnelle entre le module et le système hôte.

4. The host device shall be properly labelled to identify the module within the host device. The end product must be labeled in a visible area with the following: "Contains IC:23860-SRM955 " Any similar wording that expresses the same meaning may be used.

Le périphérique hôte doit être correctement étiqueté pour identifier le module dans le périphérique hôte. Le produit final doit être étiqueté dans une zone visible avec: "Contains IC: 23860-SRM955 " Toute formulation similaire exprimant la même signification peut être utilisée.

The IC Statement below should also be included on the label. When not possible, the IC Statement should be included in the User Manual of the host device. "This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le onctionnement."

Comply with RSS-247 and Serves as the general condition,are instruction to OEM if integrator install the module, and use the external antenna that are able to be detached. the following notice .

1） the device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

2）for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;

3）for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits as appropriate

4） where applicable, antenna type(s), antenna models(s), and worst-case tilt angle(s) necessary to remain compliant with the e.i.r.p. elevation mask requirement set forth in section 6.2.2.3 shall be clearly indicated.

5）les dispositifs fonctionnant dans la bande de 5 150 à 5 250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;

6） pour les dispositifs munis d'antennes amovibles, le gain maximal d'antenne permis pour les dispositifs utilisant les bandes de 5 250 à 5 350 MHz et de 5 470 à 5 725 MHz doit être conforme à la limite de la p.i.r.e;

7） pour les dispositifs munis d’antennes amovibles, le gain maximal d’antenne permis (pour les dispositifs utilisant la bande de 5 725 à 5 850 MHz) doit être conforme à la limite de la p.i.r.e. spécifiée, selon le cas;

8） lorsqu’il y a lieu, les types d’antennes (s’il y en a plusieurs), les numéros de modèle de l’antenne et les pires angles d’inclinaison nécessaires pour rester conforme à l’exigence de la p.i.r.e. applicable au masque d’élévation, énoncée à la section 6.2.2.3, doivent être clairement indiqués.

Indoor Client 6XD

a. Contention-Based Protocol, as demonstrated in the test report, is permanently embedded in the module and is not host-dependent.

b. The device will only associate and connect with a low-power indoor access point or subordinate device and never directly connect to other client devices.

c. This device will always initiate transmission under the control of a low-power indoor AP or subordinate except for brief transmissions before joining a network. These short messages will only occur if the client has detected an indoor AP or subordinate operating on a channel. These brief messages will have a time-out mechanism such that if it does not receive a response from an AP it will not continually repeat the request.

d. Transmissions will be lower or equal to the power advertised by the indoor low-power access point or subordinate and never above the maximum output power allowed by the FCC grant for equipment class 6XD.

Devices shall not be used for control of or communications with unmanned aircraft systems