

## Delta Description LISA-U

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## 1 Document Mission/Scope

### 1.1 Mission

Aim of this document is to describe the differences between system configurations in terms of HW and/or FW and provide analysis of their impact on the system behavior.

### 1.2 Scope

The document is addressed to the project team and the people involved in the testing and certification of LISA-U family wireless modules.

## 2 List of Acronyms

| Abbreviation / Term | Explanation / Definition                   |
|---------------------|--------------------------------------------|
| FCC                 | Federal Communications Commission          |
| FW                  | Firmware                                   |
| GCF                 | Global Certification Forum                 |
| HW                  | Hardware                                   |
| IC                  | Industry Canada                            |
| IMEI                | International Mobile Equipment Identity    |
| PTCRB               | PCS Type Certification Review Board        |
| SVN                 | Software Version Number                    |
| UMTS                | Universal Mobile Telecommunications System |
| TCB                 | Telecommunication Certification Body       |

### 3 Affected Products

| Product:     | 2G Bands [MHz]    | 3G Bands [MHz]             | Voice / Data |
|--------------|-------------------|----------------------------|--------------|
| LISA-U200-04 | 850/900/1800/1900 | 800/850/900/1700/1900/2100 | • / •        |
| LISA-U201-04 | 850/900/1800/1900 | 800/850/900/1900/2100      | • / •        |

### 4 System Configuration

Current configuration:

| Product:     | Baseline FW: | Baseline HW | SVN |
|--------------|--------------|-------------|-----|
| LISA-U200-03 | 23.41        | 146AB2      | 07  |
| LISA-U201    | 23.41        | 214001      | 07  |

New configuration:

| Product:     | Baseline FW: | Baseline HW | SVN |
|--------------|--------------|-------------|-----|
| LISA-U200-04 | 23.41        | 146DB0      | 07  |
| LISA-U201-04 | 23.41        | 214C00      | 07  |

### 5 Cross reference table: Product vs FCC and IC code

| Product      | FCC ID      | IC code         | HVIN         |
|--------------|-------------|-----------------|--------------|
| LISA-U200-04 | XPYLISAU200 | 8595A-LISAU200N | LISA-U200-01 |
| LISA-U200-03 | XPYLISAU200 | 8595A-LISAU200N | LISA-U200-01 |
| LISA-U201    | XPYLISAU201 | 8595A-LISAU201  | LISA-U201    |
| LISA-U201-04 | XPYLISAU201 | 8595A-LISAU201  | LISA-U201    |

## 6 Delta System Description

### 6.1 SW Modem changes

No

Same baseline SW

### 6.2 Hardware Modem change

#### 6.2.1 LISA-U200-04 compare to LISA-U200-03

- Same Form Factor
  - Schematics and PCB layout - changes
    - o PA new version of the same component, pin to pin compatible and electrically equivalent component and there is no change to the radio parameters
    - o BB RTC 32 KHz Crystal replaced with a pin to pin equivalent from a different manufacturer (for economy of scale)
    - o Change of the PCB layout and some passives replaced with equivalent one of different size in order to fit the new Winbond NAND memory combo
      - New System memory Vs old System memory
        - It is an electrically compatible, external dimension differs by 1mm
        - Pin to Pin compatible: No
        - RAM Specification are still by JEDEC
        - Memory speed
          - o RAM: As per the relative datasheets, the new memory part (Winbond) allows a maximum clock frequency of 200MHz while the Cypress part is specified for a maximum clock frequency of 166MHz.
          - o Flash: Different technologies between new part (Winbond) and old part (Cypress). The new memory part (Winbond) has a NAND flash while Cypress is based on a NOR flash. The NAND minimum write cycle time (tWC) and read cycle time (tRC) are both specified at 35ns. The NOR based flash (Cypress) specifies a minimum clock period of 9.26ns while the minimum write cycle time (tWC) is 60ns.
  - o Max clock
    - o RAM: The maximum LPDDR1 clock frequency in use is 172MHz. On the previous memory (Cypress), the DDR part in use had the same technology, LPDDR1. In this latter case, the maximum clock frequency used was 160MHz
    - o Flash: The measured write and read cycle time for Winbond (NAND) are: tRC = 52ns; tWC=41ns
    - o The measured clock period and tWC for Cypress (NOR) are: tclk = 12.5ns; tWC = 330ns
- Power draw:

|               |                                                           |             |      |              |     |
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- o The power consumption of the module is expected to be the same as before the memory change, seeing that the memory impact on the overall current consumption is negligible at module level
  - o Same antenna switch
  - o Same RF filters
  - o Same reference frequency
  - o Same processor (BB)
- Same RF chip
- Modification of the housing:NA
- BOM:
  - o Yes except for the componets replaced

### 6.2.2 LISA-U201-04 compare to LISA-U200

- Same Form Factor
- Schematics and PCB layout - changes
  - o Change of the PCB layout and some passives replaced with equivalent one of different size in order to fit the new Winbond NAND memory combo
    - New System memory Vs old System memory
      - It is an electrically compatible, external dimension differs by 1mm
      - Pin to Pin compatible:No
      - RAM Specification are still by JEDEC
      - Memory speed
        - o RAM: As per the relative datasheets, the new memory part (Winbond) allows a maximum clock frequency of 200MHz while the Cypress part is specified for a maximum clock frequency of 166MHz.
        - o Flash: Different technologies between new part (Winbond) and old part (Cypress). The new memory part (Winbond) has a NAND flash while Cypress is based on a NOR flash. The NAND minimum write cycle time (tWC) and read cycle time (tRC) are both specified at 35ns. The NOR based flash (Cypress) specifies a minimum clock period of 9.26ns while the minimum write cycle time (tWC) is 60ns.
  - o
    - Max clock
      - o RAM: The maximum LPDDR1 clock frequency in use is 172MHz. On the previous memory (Cypress), the DDR part in use had the same technology, LPDDR1. In this latter case, the maximum clock frequency used was 160MHz
      - o Flash: The measured write and read cycle time for Winbond (NAND) are: tRC = 52ns; tWC=41ns
      - o The measured clock period and tWC for Cypress (NOR) are: tclk = 12.5ns; tWC = 330ns
- Power draw:

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- o The power consumption of the module is expected to be the same as before the memory change, seeing that the memory impact on the overall current consumption is negligible at module level
- Same antenna switch
- Same RF filters
- Same reference frequency
- Same processor (BB)
- Same RF chip
- Modification of the housing:NA
- BOM:
  - o Yes except for the componets replaced

### 6.2.3 SARA-

## 7 Impact

The following certification schemes will apply

| Scope    | Impact |
|----------|--------|
| FCC / IC | C2PC.  |
| PTCRB    | ECO    |

## 8 References

### 8.1 External

None

### 8.2 Internal

None

## 9 Document change report

| Revision | Change Reference |    | Record of changes made to previous released version |                  |
|----------|------------------|----|-----------------------------------------------------|------------------|
|          | Date             | CR | Section                                             | Comment          |
| 1.0      | 30/05/2019       | NA | ALL                                                 | Document Created |
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| 3.0      | 05/09/2019       | NA | ALL                                                 | Document Created |

## 10 Approval

| Revision | Approver(s)  | Date       | Source/signature          |
|----------|--------------|------------|---------------------------|
| 1.0      | Giulio Comar | 30/05/2019 | Document stored on server |

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