AG525R-GL QuecOpen Hardware Design

Automotive Module Series

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About the Document

Revision History

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-	2020-04-04	Leon HUANG/ Alex ZHANG/ Evan SHEN/	Creation of the document
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1 Introduction

QuecOpen® is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of QuecOpen® solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With QuecOpen® solution, development flow for wireless application and hardware design will be simplified. Main features of QuecOpen® solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports remote upgrade of firmware over the air
- Improves products' cost-performance ratio, and enhances products' competitiveness

This document, describing AG525R-GL QuecOpen® module and its air interface and hardware interfaces connected to your applications, informs you of the interface specifications, electrical and mechanical details, as well as other related information of the module.

With the application notes and user guides provided separately, you can easily use the module to design and set up mobile applications.

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2020AG525RGL.
4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:
❒GSM850:≤8.446dBi
❒GSM1900:≤10.030dBi
❒WCDMA II/ LTE Band 2/7/25/38/41:≤8.000dBi

❒WCDMA IV/ LTE Band 4/66:≤5.000dBi
❒WCDMA V/ LTE Band 5:≤9.416dBi
❒LTE Band 12:≤8.734dBi
❒LTE Band 13:≤9.173dBi
❒LTE Band 26:≤9.337dBi
❒LTE Band 71:≤8.447dBi
5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XMR2020AG525RGL" or "Contains FCC ID: XMR2020AG525RGL" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

1.1. IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

To comply with IC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

❒GSM850:≤5.16dBi
❒GSM1900:≤10.030dBi
❒WCDMA II/ LTE Band 2/7/25/38/41:≤8.000dBi
❒WCDMA IV/ LTE Band 4/66:≤5.000dBi
❒WCDMA V/ LTE Band 5:≤6.13dBi
❒LTE Band 12:≤5.63dBi
❒LTE Band 13:≤5.94dBi
❒LTE Band 26:≤6.08dBi
❒LTE Band 71:≤5.48dBi

The host product shall be properly labelled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

"Contains IC: 10224A-2020AG525R" or "where: 10224A-2020AG525R is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:"Contient IC: 10224A-2020AG525R " ou "où: 10224A-2020AG525R est le numéro de certification du module.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

AG525R-GL QuecOpen module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.497 GHz.

AG525R-GL QuecOpen module is a series of automotive-grade LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication modules with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides GNSS function (optional) and audio function to meet specific application demands.

AG525R-GL QuecOpen contains global main bands to meet varied market demands.

Engineered to meet the demanding requirements in automotive applications and other harsh operating conditions, the module offers a premium solution for high performance automotive and intelligent transportation system (ITS) applications, such as fleet management, onboard vehicle telematics, in-car entertainment systems, emergency calling, and roadside assistance.

With a compact profile of 38.0 mm × 42.0 mm × 2.65 mm, the module can meet almost all requirements for automobile applications. It is an SMD type module which can be embedded into applications through its 400 LGA pins.

Table 1: Frequency Bands of AG525R-GL QuecOpen® Module

Network Type	AG525R-GL QuecOpen Module
LTE-FDD (with Rx-diversity)	B1/B2/B3/B4/B5/B7/B8/B9/B11/B12/B13/B18/B19/B20/B21/B25/B26/ B28/B29 [1]/B30 [1]/B32 [1]/B66/B71
LTE-TDD (with Rx-diversity)	B34/B38/B39/B40/B41
2CA (DL)	B12+B12/B25/B30/B66 B13+B66 B19+B21 B1+B18/B19/B1/B20/B28/B38/B3/B40/B41/B5/B7/B8 B20+B32/B38/B40

	B21+B28 B25+B25/B26 B28+B38/B40/B41/B28 B29+B30/B66 B2+B12/B13/B29/B2/B30/B4/B5/B66/B71/B7 B30+B66 B34+B41 B38+B38 B39+B41/B39 B3+B18/B19/B20/B28/B38/B3/B40/B41/B5/B7/B8 B40+B40 B41+B41 B4+B12/B13/B29/B30/B4/B5/B71/B7 B5+B25/B30/B38/B40/B41/B5/B66/B7 B66+B66/B71 B7+B12/B20/B28/B32/B66/B7/B8 B8+B11/B32/B38/B39/B40/B41/B8
3CA (DL)	B12+B66+B66 B12+B12+B66 B13+B66+B66 B1+B1+B28/B3/B5/B7/B41/B8 B1+B3+B18/B19/B20/B28/B38/B3/B40/B41/B5/B7/B8 B1+B40+B40 B1+B41+B41 B1+B5+B40/B7 B1+B7+B20/B28/B7/B8 B1+B8+B38/B40 B20+B38+B38 B20+B40+B40 B25+B25+B25/B2 B28+B40+B40 B28+B41+B41 B29+B30+B66 B29+B66+B66 B2+B12+B12/B30/B66 B2+B13+B66 B2+B29+B30/B66 B2+B2+B12/B13/B29/B30/B4/B5/B66/B71/B7 B2+B30+B66 B2+B4+B12/B13/B29/B30/B4/B5/B71/B7 B2+B5+B30/B66/B7/B5 B2+B66+B66/B71 B2+B7+B12/B66/B7 B30+B66+B66

	B39+B41+B4 B39+B39+B41 B3+B28+B40/B41 B3+B3+B20/B28/B41/B7/B8/B38/B40/B5 B3+B40+B40 B3+B41+B41 B3+B5+B40/B7 B3+B7+B20/B28/B7/B8 B3+B8+B38/B40 B40+B40+B40 B41+B41+B41 B4+B12+B12/B30 B4+B29+B30 B4+B4+B12/B13/B29/B30/B5/B71/B7 B4+B5+B30/B5 B4+B7+B12/B7 B5+B30+B66 B5+B40+B40 B5+B5+B66/B30 B5+B66+B66 B5+B7+B7 B66+B66+B66/B71 B7+B12+B66/B12 B7+B20+B32 B7+B66+B66 B7+B7+B8/B28/B20/B66 B8+B39+B39 B8+B40+B40 B8+B41+B41 B8+B8+B39/B41
WCDMA (with Rx-diversity)	B1/B2/B3/B4/B5/B8/B19
GSM	850/900/1800/1900 MHz
GNSS	Optional

NOTE

[1)] LTE-FDD B29, B30 and B32 support Rx only.

2.2. Key Features

The following table describes detailed features of the module.

Table 2: Key Features

Feature	Details
Power Supply	**VBAT_BB/VBAT_RF:** ● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850/EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800/PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850/EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800/PCS1900 8-PSK ● Class 3 (24dBm +1/-3 dB) for WCDMA bands ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands ● Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	● Support up to 3 × CA Cat 12 LTE FDD and TDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Support 2 × 2 MIMO in DL direction ● LTE-FDD: Max. 600 Mbps (DL)/75 Mbps (UL) ● LTE-TDD: Max. 467 Mbps (DL)/45 Mbps (UL)
UMTS Features	● Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA ● Support QPSK, 16-QAM and 64-QAM modulation ● DC-HSDPA: Max 42 Mbps (DL) ● HSUPA: Max 5.76 Mbps (UL) ● WCDMA: Max 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** ● Support GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Max 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Support EDGE multi-slot class 33 (33 by default) ● Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: CS 1-4 and MCS 1-9 ● Uplink coding schemes: CS 1-4 and MCS 1-9 ● Max 296 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	● Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/HTTPS/ MMS/FTPS/SSL protocols ● Support PAP and CHAP used for PPP connections

SMS	● Text and PDU modes ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	Support USIM/SIM card: 1.8/3.0 V
Audio Features	● Provide one digital audio interface: I2S interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
I2S Interface	Used for external codec function
PCM Interface	● Used for external BT function ● Support 16-bit linear data format ● Support long frame sync and short frame sync ● Support master and slave modes, but must be the master in long frame sync
USB Interfaces	● USB 3.0 and 2.0 interfaces (slave mode by default; support USB master mode), with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, firmware upgrade, software debugging, and voice over USB* ● Support USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6~5.4, and Android 4.x/5.x/6.x/7.x/8.x/9.x
UART Interfaces	**UART1:** ● Baud rate reach up to 921600 bps, 115200 bps by default ● Support RTS and CTS hardware flow control **BT UART:** ● Baud rate reach up to 921600 bps, 115200 bps by default ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output, 115200 bps baud rate
SDIO Interface	Support eMMC 4.5.1
SPI Interfaces	● Support master mode only ● Maximum clock frequency rate: 50 MHz
I2C Interface	● Compliant with I2C specification version 3.0 ● Multi-master is not supported ● Used for codec configuration by default
RGMII Interface	Support 10/100/1000 Mbps
Wireless Connectivity Interface*	● PCIe (Gen2) interface for WLAN ● UART & PCM interfaces for Bluetooth*

Rx-diversity	Support LTE/WCDMA Rx-diversity
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV)
Physical Characteristics	● Dimensions: (38.0 ±0.2) mm × (42.0 ±0.2) mm × (2.65 ±0.2) mm ● Weight: approx. 9.23 g
Temperature Range	● Operation temperature range: -35 °C to +75 °C [1)] • Extended temperature range: -40 °C to +85 °C [2)] ● eCall temperature range: -40 °C to +90 °C [3)] ● Storage temperature range: -40 °C to +95 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant, and emergency call can be dialed out with a maximum power and data rate.
2. [2)] Within extended temperature range, the module remains fully functional and retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.
3. [3)] Within eCall temperature range, the emergency call function must be functional until the module is broken. When the ambient temperature is between 75 °C and 90 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of emergency call.
4. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR4X + NAND flash
- Radio frequency
- Peripheral interfaces

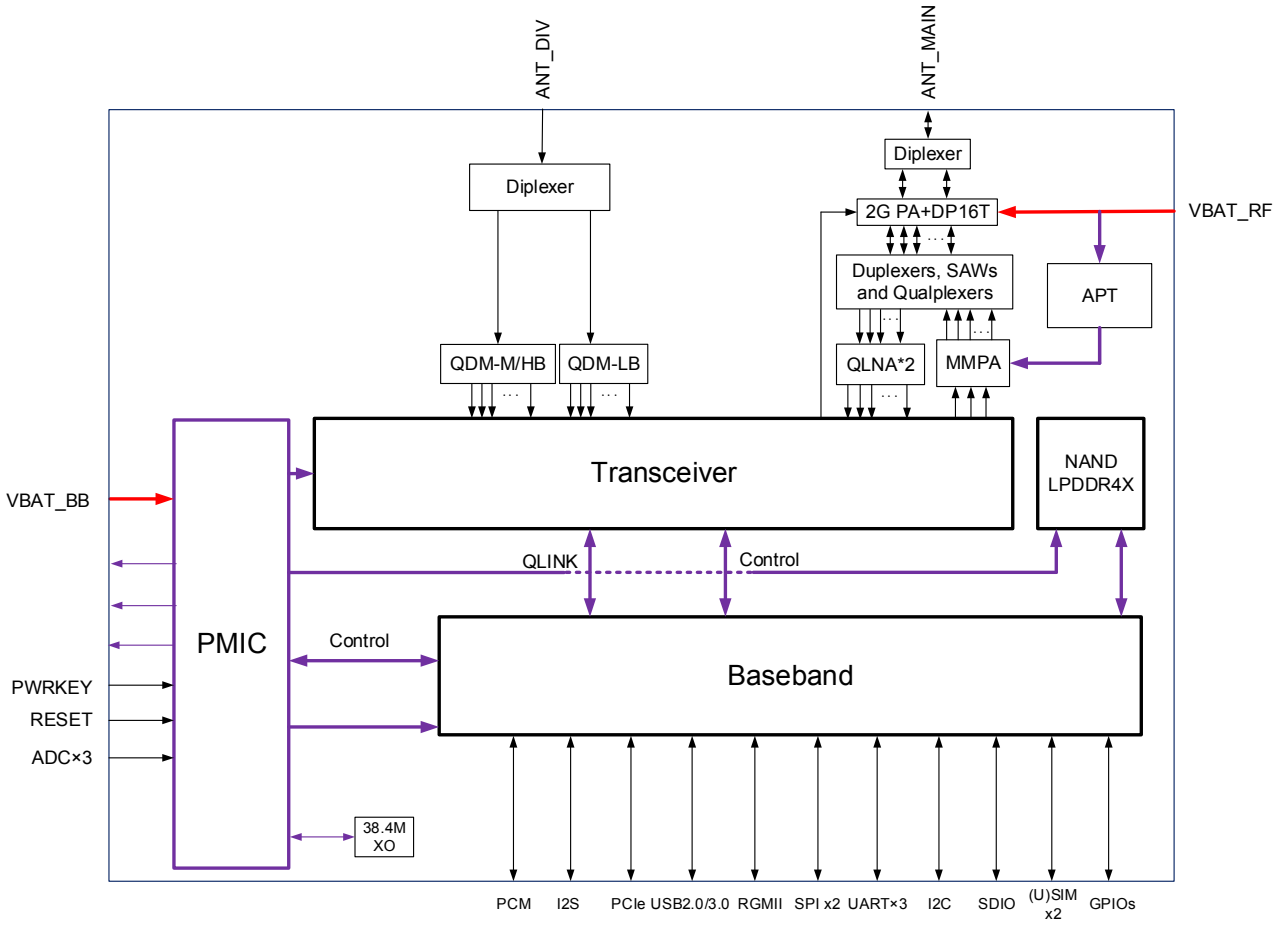

Figure 1: Functional Diagram for AG525R-GL QuecOpen®

2.4. Evaluation Board

To help you develop applications conveniently with the module, Quectel supplies the evaluation board (EVB), USB data cables, a pair of earphones, antennas and other peripherals to control or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The module is designed with 400 LGA pins that can be connected to cellular application platforms. Module interfaces are described in detail in the following sub-chapters:

- Power supply
- (U)SIM interfaces
- USB 2.0/3.0 interface
- UART interfaces
- I2S and I2C interfaces
- SDIO interface
- SPI interfaces
- RGMII interface
- WLAN and BT interfaces*
- ADC interfaces
- USB_BOOT interface
- GPIO interfaces

NOTE

"*" means under development.

3.2. Pin Assignment

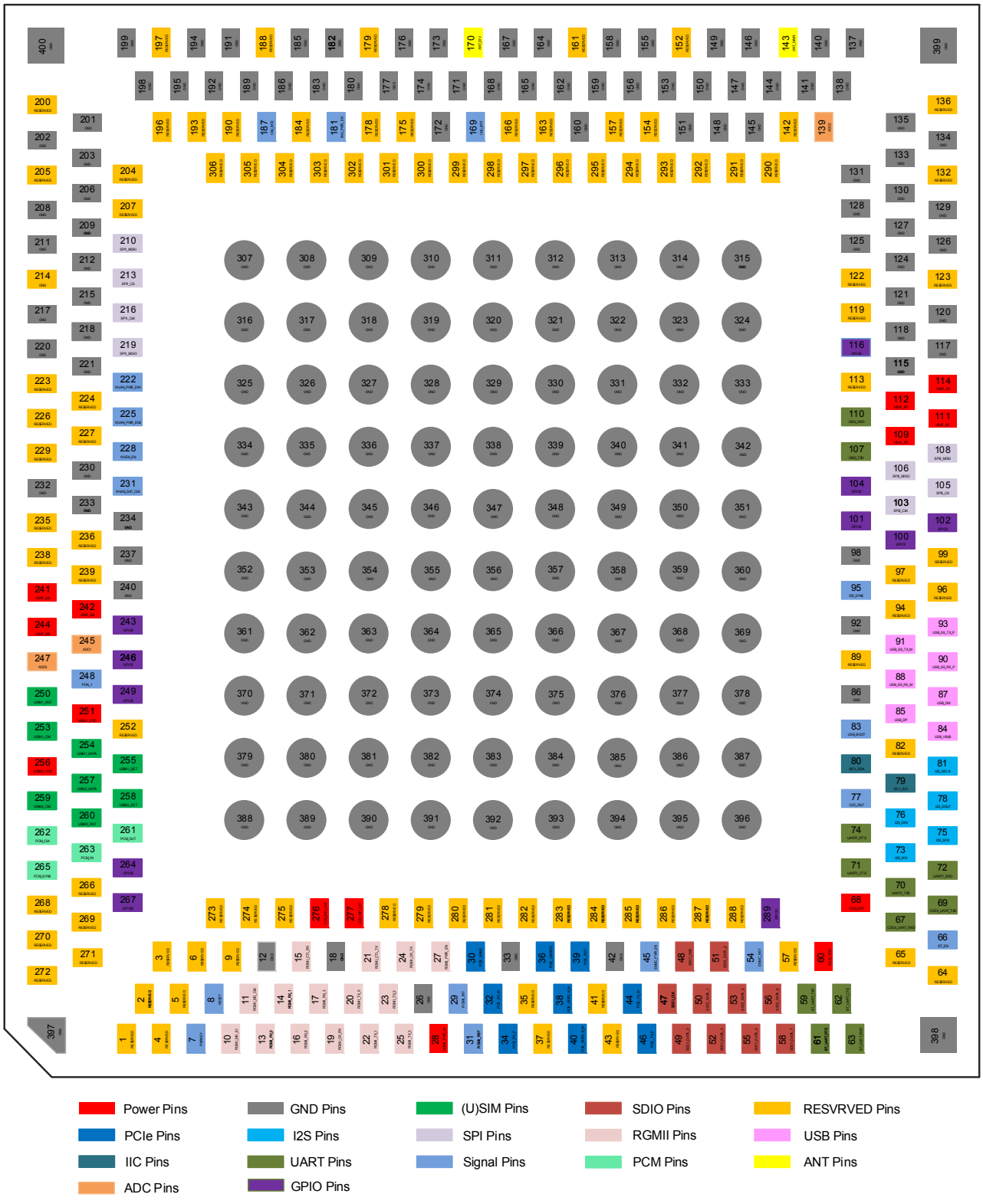

Figure 2: Pin Assignment (Top View)

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground in the design.

3.3. Pin Description

The following tables show the pin definition of the module and the alternate functions of multiplexing pins.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
DI	Digital input
DO	Digital output
H	High level
IO	Bidirectional
L	Low level
OD	Open drain
PD	Pull down
PI	Power input
PO	Power output
PU	Pull up
R	Slew-rate limited
S	Schmitt trigger input

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	241, 242, 244	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	109, 111, 112, 114	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 2 A.
VDD_EXT	68	PO	1.8 V output power supply for external circuits	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits.
VDD_WIFI_VM	276	PO	Power supply for Wi-Fi	Vnorm = 1.35 V	If unused, keep it open.
VDD_WIFI_VH	277	PO	Power supply for Wi-Fi	Vnorm = 1.95 V	If unused, keep it open.
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124–131, 133–135, 137, 138, 140, 141, 144–151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171–174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201–203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307–400				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	Internally pulled up to 1.8 V. Active low.
PON_1	248	DI	Pulling it high will turn on the module automatically		Valid trigger range: 0.78–1.89 V. Active high
RESET	8	DI	Reset the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	Internally pulled up to 1.8 V. Active low.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	251	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.

				For 3.0 V (U)SIM: Vmax = 3.05 V Vmin = 2.7 V	If unused, keep it open.
USIM1_DATA	254	IO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.36 V V_{IH}min = 1.26 V V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{IL}max = 0.57 V V_{IH}min = 2.0 V V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM1_CLK	253	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM1_RST	250	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	256	PO	(U)SIM2 card power supply	**For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
USIM2_DATA	257	IO	(U)SIM2 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.36 V	If unused, keep it open.

				V_{IH}min = 1.26 V V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{IL}max = 0.57 V V_{IH}min = 2.0 V V_{OL}max = 0.4 V V_{OH}min = 2.28 V	
USIM2_CLK	259	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM2_RST	260	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep it open.
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	84	DI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnorm = 5.0 V	
USB_DP	85	AI/ AO	USB differential data bus (+)		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	87	AI/ AO	USB differential data bus (-)		
USB_SS_TX_P	93	AO	USB 3.0 super-speed transmit (+)		Compliant with USB 3.0 standard specification. Require differential impedance of 90 Ω.
USB_SS_TX_M	91	AO	USB 3.0 super-speed		

			transmit (-)		
USB_SS_RX_P	90	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	88	AI	USB 3.0 super-speed receive (-)		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	100	IO	General-purpose input/output	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
GPIO2	101	IO	General-purpose input/output		
GPIO3	102	IO	General-purpose input/output		
GPIO4	104	IO	General-purpose input/output		
GPIO5	116	IO	General-purpose input/output		
GPIO6	243	IO	General-purpose input/output		
GPIO7	246	IO	General-purpose input/output		
GPIO8	249	DO	General-purpose output	V_{IL}min = TBD V_{IL}max = 0.63 V V_{IH}min = 0.9 V V_{IH}max = TBD V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
GPIO9	264	IO	General-purpose input/output	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
GPIO10	267	IO	General-purpose input/output		
GPIO11	289	IO	General-purpose input/output		
UART1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_CTS	71	DO	UART1 clear to	V_{OL}max = 0.45 V	1.8 V power domain.

			send	V_{OH}min = 1.35 V	Can be configured to GPIOs. If unused, keep them open.
UART1_RTS	74	DI	UART1 request to send	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
UART1_TXD	70	DO	UART1 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART1_RXD	72	DI	UART1 receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
BT UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_UART_TXD	59	DO	BT UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIO. If unused, keep them open.
BT_UART_RXD	63	DI	BT UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
BT_UART_RTS	61	DI	BT UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
BT_UART_CTS	62	DO	BT UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	110	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.
DBG_TXD	107	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2C1 Interface (for Codec Configuration by Default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	79	OD	I2C1 serial clock		External pull-up

I2C1_SDA	80	OD	I2C1 serial data		resistor is required. 1.8 V only. Can be configured to GPIO. If unused, keep them open.
I2S Interface (for Codec Configuration by Default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CDC_RST	77	DO	Codec reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIO. If unused, keep them open.
I2S_MCLK	81	DO	Clock output for codec	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S_WS	73	IO	I2S word select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
I2S_SCK	75	DO	I2S clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S_DIN	76	DI	I2S data in	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
I2S_DOUT	78	DO	I2S data out	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	265	IO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Can be configured to GPIO. If unused, keep them open.
PCM_CLK	262	IO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	

PCM_IN	263	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
PCM_OUT	261	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	40	AO	PCIe reference clock (+)		Require differential impedance of 95 Ω. If unused, keep them open.
PCIE_REFCLK_M	38	AO	PCIe reference clock (-)		
PCIE_TX_M	44	AO	PCIe transmit (-)		
PCIE_TX_P	46	AO	PCIe transmit (+)		
PCIE_RX_M	32	AI	PCIe receive (-)		
PCIE_RX_P	34	AI	PCIe receive (+)		
PCIE_CLKREQ	36	IO	PCIe clock request	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain If unused, keep them open.
PCIE_RST	39	DO	PCIe reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCIE_WAKE	30	DI	PCIe wakeup	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_MD_IO	10	IO	RGMII MDIO management data	Power domain determined by RGMII_PWR_IN	If unused, keep them open.
RGMII_MD_CLK	11	DO	RGMII MDC management clock		
RGMII_RX_0	13	DI	RGMII receive data bit 0		

RGMII_RX_1	14	DI	RGMII receive data bit 1		
RGMII_CTL_RX	15	DI	RGMII receive control		
RGMII_RX_2	16	DI	RGMII receive data bit 2		
RGMII_RX_3	17	DI	RGMII receive data bit 3		
RGMII_CK_RX	19	DI	RGMII receive clock		
RGMII_TX_0	20	DO	RGMII transmit data bit 0		
RGMII_CTL_TX	21	DO	RGMII transmit control		
RGMII_TX_1	22	DO	RGMII transmit data bit 1		
RGMII_TX_2	23	DO	RGMII transmit data bit 2		
RGMII_CK_TX	24	DO	RGMII transmit clock		
RGMII_TX_3	25	DO	RGMII transmit data bit 3		
RGMII_PWR_EN	27	DO	Enable external LDO to supply power to RGMII_PWR_IN	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RGMII_PWR_IN	28	PI	Power input for internal RGMII circuit		1.8/2.5 V power supply input. If RGMII is not be used, connect it to VDD_EXT.
RGMII_INT	29	DI	RGMII PHY interrupt output	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.
RGMII_RST	31	DO	Reset output for RGMII PHY	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO Interface (for eMMC by default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_VDD	60	PI	SDIO power supply		connect it to VDD_EXT.

SDC1_DATA_0	49	IO	SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V	1.8 V power domain for eMMC applications. If unused, keep it open.
SDC1_DATA_1	50	IO	SDIO data bit 1		
SDC1_DATA_2	51	IO	SDIO data bit 2		
SDC1_DATA_3	52	IO	SDIO data bit 3		
SDC1_CMD	48	IO	SDIO command		
SDC1_DATA_4	53	IO	SDIO data bit 4	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain Can be configured to GPIOs. If unused, keep them open.
SDC1_DATA_5	55	IO	SDIO data bit 5		
SDC1_DATA_6	56	IO	SDIO data bit 6		
SDC1_DATA_7	58	IO	SDIO data bit 7		
SDC1_CLK	47	DO	SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.4 V	1.8 V power domain for eMMC applications. If unused, keep it open.
EMMC_RST	54	DO	eMMC reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
EMMC_PWR_EN	45	DO	eMMC power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CLK	216	DO	SPI1 clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open. Can be configured into GPIOs.
SPI1_CS	213	DO	SPI1 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI1_MISO	219	DI	SPI1 master-in salve-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI2_CLK	103	DO	SPI2 clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

SPI2_CS	105	DO	SPI2 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI2_MISO	106	DI	SPI2 master-in salve-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SPI2_MOSI	108	DO	SPI2 master-out slave-in	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	247	AI	General-purpose ADC interface	Voltage Range: 0–1.875 V	If unused, keep it open.
ADC1	245	AI	General-purpose ADC interface	Voltage Range: 0–1.875 V	If unused, keep it open.
ADC2	139	AI	General-purpose ADC interface	Voltage Range: 0–1.875 V	If unused, keep it open.
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	83	DI	Force the module into emergency download mode		1.8 V power domain. If unused, keep it open.
BT_EN	66	DO	BT function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
DR_SYNC	95	DO	Navigation 1PPS time sync output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
IMU_INT1	169	DI	IMU interrupt 1	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep them open.
IMU_INT2	187	DI	IMU interrupt 2	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
IMU_PWR_EN	181	DO	IMU power enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

WLAN_PWR_EN2	225	DO	WLAN power supply enable control 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_EN	228	DO	WLAN enable	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
COEX_UART_RXD	67	DI	LTE&WLAN/BT coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.
COEX_UART_TXD	69	DO	LTE&WLAN/BT coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_SLP_CLK	231	DO	WLAN sleep clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_MAIN	143	AI/AO	Main antenna interface		50 Ω impedance.
ANT_DIV	170	AI	Diversity antenna interface		

RESERVED Pins

Pin Name	Pin No.	Comment
RESERVED	1-6, 9, 35, 37, 41, 43, 57, 64, 65, 82, 89, 94, 96, 97, 99, 113, 119, 122, 123, 132, 136, 142, 152, 154, 157, 161, 163, 166, 175, 178, 179, 184, 188, 190, 193, 196, 197, 200, 204, 205, 207, 214, 223, 224, 226, 227, 229, 235, 236, 238, 239, 252, 266, 268–275, 278–288, 290–306	Keep these pins open.

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground in the design.

Table 5: Alternate Functions of Multiplexing Pins

Pin No.	Pin Name	Default Function	Alternate Function 1	Alternate Function 2	Reset [1]	Wake up Interrupt [2]	Power Domain	Remark
27	RGMII_PWR_EN	RGMII			BS-PD, L	Y	1.8 V	
29	RGMII_INT				BS-PD, L	Y	1.8 V	
31	RGMII_RST				BS-PD, L	Y	1.8 V	
30	PCIE_WAKE	PCIe			BS-PD, L	Y	1.8 V	
36	PCIE_CLKREQ				BS-PD, L	Y	1.8 V	
39	PCIE_RST				BS-PD, L	Y	1.8 V	
45	EMMC_PWR_EN	SDIO			BS-PD, L	Y	1.8 V	
53	SDC1_DATA_4		GPIO_92		BSH-PD, L	N	1.8 V	
54	EMMC_RST				BS-PD, L	Y	1.8 V	
55	SDC1_DATA_5		GPIO_93		BSH-PD, L	Y	1.8 V	
56	SDC1_DATA_6		GPIO_94		BSH-PD, L	Y	1.8 V	
58	SDC1_DATA_7		GPIO_95		BSH-PD, L	Y	1.8 V	
59	BT_UART_TXD	UART	GPIO_63		BS-PD, L	N	1.8 V	
61	BT_UART_RTS		GPIO_65		BS-PD, L	Y	1.8 V	
62	BT_UART_CTS		GPIO_66		BS-PD, L	N	1.8 V	
63	BT_UART_RXD		GPIO_64		BS-PD, L	Y	1.8 V	
67	COEX_UART_RXD				BS-PD, L	Y	1.8 V	
69	COEX_UART_TXD				BS-PD, L	N	1.8 V	BOOT_CONFIG_0
70	UART1_TXD		GPIO_20		BS-PD, L	N	1.8 V	

71	UART1_CTS		GPIO_23		BS-PD, L	N	1.8 V
72	UART1_RXD		GPIO_21		BS-PU, L	Y	1.8 V
74	UART1_RTS		GPIO_22		BS-PD, L	Y	1.8 V
107	DBG_TXD				BS-PD, L	N	1.8 V
110	DBG_RXD				BS-PD, L	Y	1.8 V
265	PCM_SYNC	PCM	I2S_WS	GPIO_12	BS-PD, L	Y	1.8 V
262	PCM_CLK		I2S_SCK	GPIO_15	BS-PD, L	Y	1.8 V
263	PCM_IN		I2S_DIN	GPIO_13	BS-PD, L	Y	1.8 V
261	PCM_OUT		I2S_DOUT	GPIO_14	BS-PD, L	Y	1.8 V
77	CDC_RST		GPIO_86		BS-PD, L	Y	1.8 V
81	I2S_MCLK		GPIO_62		BS-PD, L	N	1.8 V
78	I2S_DOUT	I2S	PCM_OUT	GPIO_18	BS-PD, L	Y	1.8 V
75	I2S_SCK		PCM_CLK	GPIO_19	BS-PD, L	Y	1.8 V
76	I2S_DIN		PCM_IN	GPIO_17	BS-PD, L	Y	1.8 V
73	I2S_WS		PCM_SYNC	GPIO_16	BS-PD, L	Y	1.8 V
79	I2C1_SCL	I2C			BSR-PD, L	Y	1.8 V
80	I2C1_SDA				BSR-PD, L	Y	1.8 V
250	USIM1_RST	(U)SIM			BSH-PD, L	N	1.8/2.85 V
253	USIM1_CLK				BSH-PD, L	N	1.8/2.85 V
254	USIM1_DATA				BSH-PD, L	N	1.8/2.85 V
255	USIM1_DET				BS-PD, L	Y	1.8 V
260	USIM2_RST				BSH-PD, L	Y	1.8/2.85 V

259	USIM2_CLK			BSH-PD, L	N	1.8/2.85 V
257	USIM2_DATA			BSH-PD, L	N	1.8/2.85 V
258	USIM2_DET			BS-PD, L	Y	1.8 V
210	SPI1_MOSI	SPI	GPIO_72	BS-PD, L	N	1.8 V
213	SPI1_CS		GPIO_74	BS-PD, L	N	1.8 V
216	SPI1_CLK		GPIO_75	BS-PD, L	Y	1.8 V
219	SPI1_MISO		GPIO_73	BS-PD, L	N	1.8 V
108	SPI2_MOSI		GPIO_4	BS-PD, L	N	1.8 V
105	SPI2_CS		GPIO_6	BS-PD, L	Y	1.8 V
103	SPI2_CLK		GPIO_7	BS-PD, L	N	1.8 V
106	SPI2_MISO		GPIO_5	BS-PD, L	Y	1.8 V
66	BT_EN	Others		BS-PD, L	Y	1.8 V
83	USB_BOOT			BS-PD, L	N	1.8 V
95	DR_SYNC			BS-PD, L	Y	1.8 V
169	IMU_INT1		GPIO_88	BS-PD, L	Y	1.8 V
181	IMU_PWR_EN		GPIO_91	BS-PD, L	N	1.8 V
187	IMU_INT2		GPIO_82	BS-PD, L	Y	1.8 V
222	WLAN_PWR_EN1			BS-PD, L	Y	1.8 V
225	WLAN_PWR_EN2			BS-PD, L	Y	1.8 V
228	WLAN_EN			BS-PD, L	Y	1.8 V
100	GPIO1			BS-PD, L	Y	1.8 V
101	GPIO2			BS-PD, L	Y	1.8 V

102	GPIO3	GPIO		BS-PD, L	N	1.8 V
104	GPIO4			BS-PD, L	N	1.8 V
116	GPIO5			BS-PD, L	N	1.8 V
243	GPIO6			BS-PD, L	N	1.8 V
246	GPIO7			BS-PD, L	Y	1.8 V
249	GPIO8			L	N	1.8 V
264	GPIO9			BS-PD, L	Y	1.8 V
267	GPIO10			BS-PD, L	N	1.8 V
289	GPIO11			BS-PD, L	Y	1.8 V

NOTES

1. "**Alternate Function 1/2**" takes effect only after software configuration.
2. [1)] See ***Table 4*** for more details about the symbol description.
3. [2)] If the GPIOs without interrupt function are configured as interrupt GPIOs, power consumption of the module will be increased. ("Y" means "interrupt function supported". "N" means "interrupt function not supported".)
4. Pins 69 and 83 cannot be pulled up before power-up.

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** can set the module into airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

The module is able to reduce its current consumption to a minimum value during the sleep mode. This chapter mainly introduces some ways to enter or exit from sleep mode. The diagram below illustrates the current consumption of the module during sleep mode.

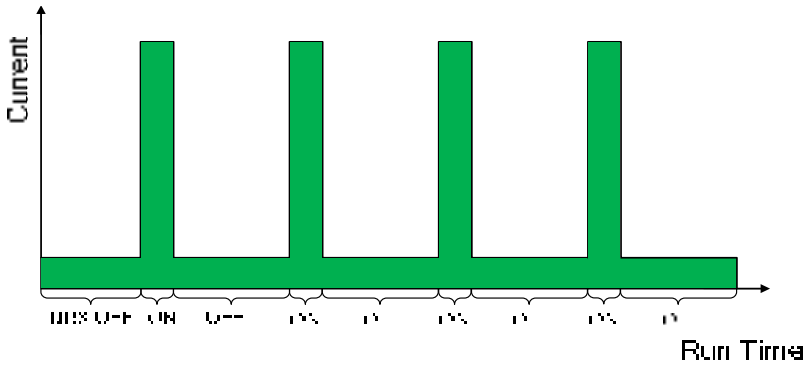

Figure 3: Sleep Mode Current Consumption Diagram

NOTE

DRX cycle index values are broadcasted by the base station through the wireless network.

3.5.1.1. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions must be met to let the module enter sleep mode.

- Use sleep API to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 5*** are under non-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters suspended state.

The following figure shows the connection between the module and the host.

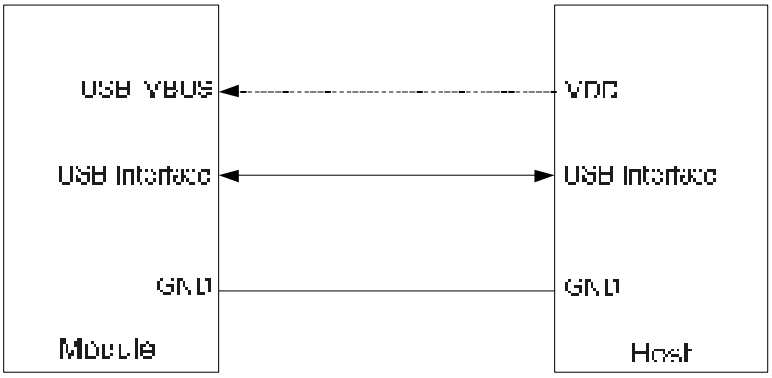

Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has URC to report, it will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.2. USB Application without USB Remote Wakeup Function

If the host supports USB suspend/resume, but does not support remote wake-up function, it needs to be woken up via the module's GPIO.

There are three preconditions to let the module enter sleep mode.

- Use sleep & wakeup API to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 5*** are under non-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters suspended state.

The following figure shows the connection between the module and the host.

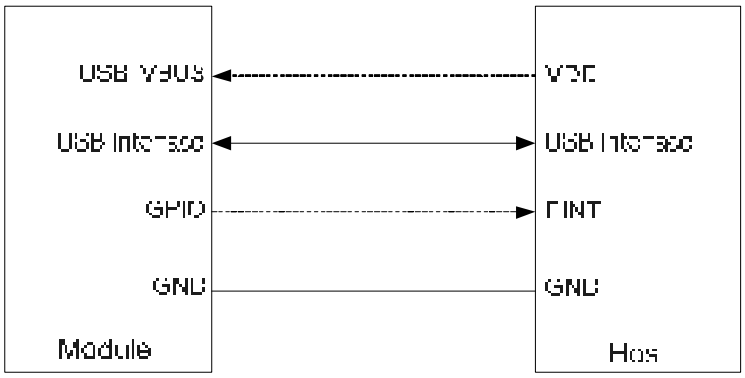

Figure 5: Sleep Mode Application without USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has URC to report, the module's GPIO signal can be used to wake up the host.

3.5.1.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to set the module to sleep mode.

- Use sleep API to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 5*** are under non-wakeup status.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

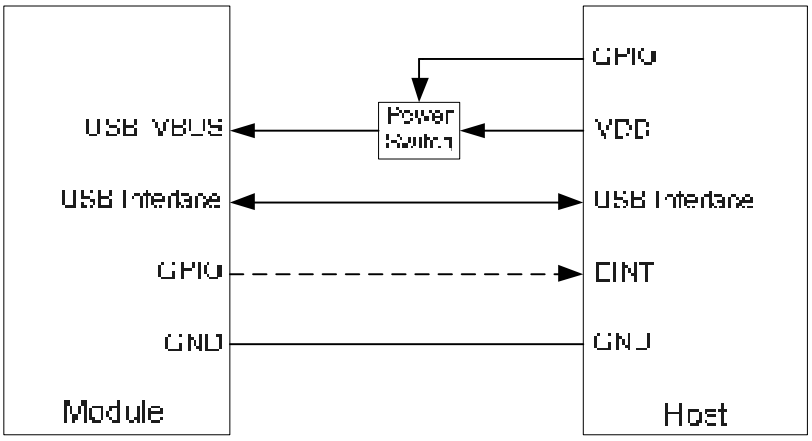

Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. The mode can be set via **AT+CFUN=<fun>** command. The parameter **<fun>** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides seven VBAT pins for connection with an external power supply.

- Three VBAT_BB pins for module's baseband part.
- Four VBAT_RF pins for module's RF part.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	241, 242, 244	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	109, 111, 112, 114	Power supply for the module's RF part	3.3	3.8	4.3	V
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124–131,133–135, 137, 138, 140, 141, 144–151,153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171–174,176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201–203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307–400					

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3 to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

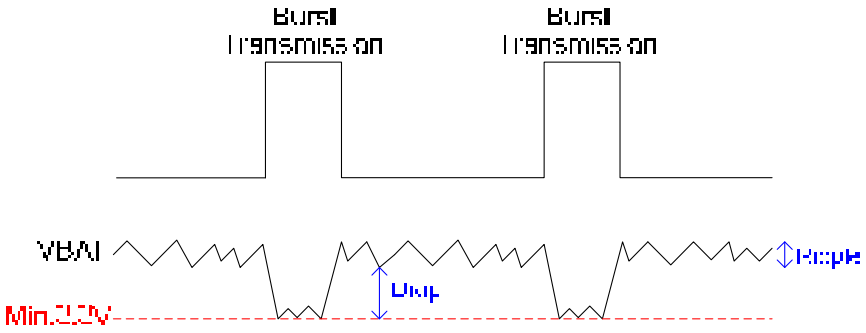

Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. DC_3V8 from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm. The width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use high power TVS diode to prevent static electricity, and place them as close to the VBAT pins as possible. The following figure shows a reference design of VBAT power supply pins.

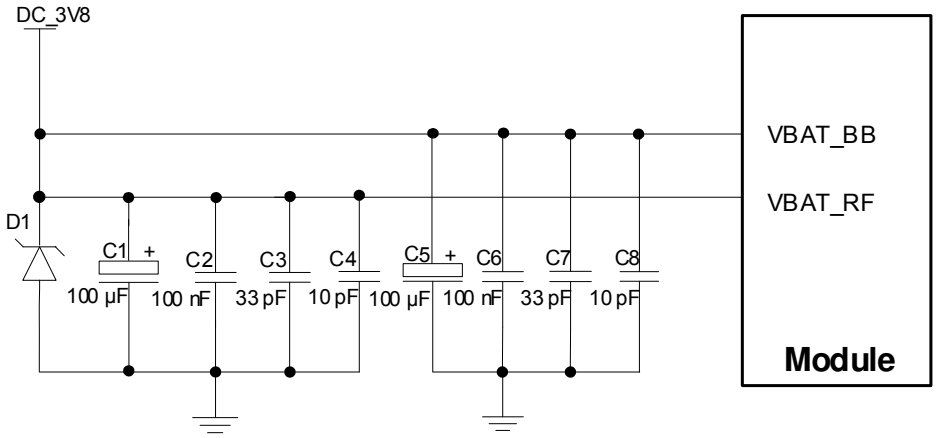

Figure 8: VBAT Reference Design

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for 12/24 V input power source. The designed output for the power supply is about 3.8 V and the maximum rated current is 5 A.

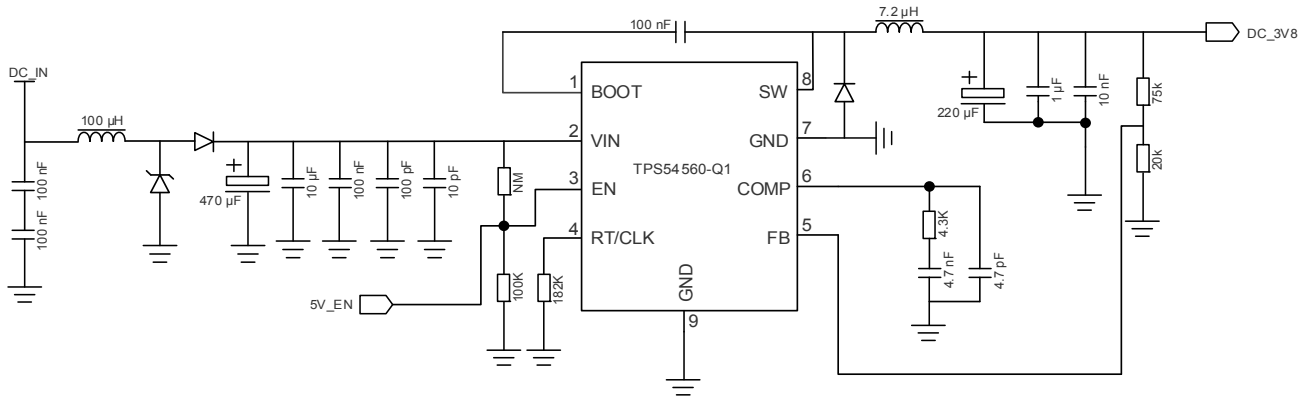

Figure 9: 12/24 V Power Supply System Reference Design

NOTE

To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after the module is turned off by PWRKEY, the power supply can be cut off.

3.6.4. Monitor the Power Supply

API can be used to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.7. Power on and off Scenarios

3.7.1. Turn on Module with PWRKEY

Table 8: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	7	Turn on/off the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	1.8 V power domain. Pulled-up internally. Active low.

When the module is in power-off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

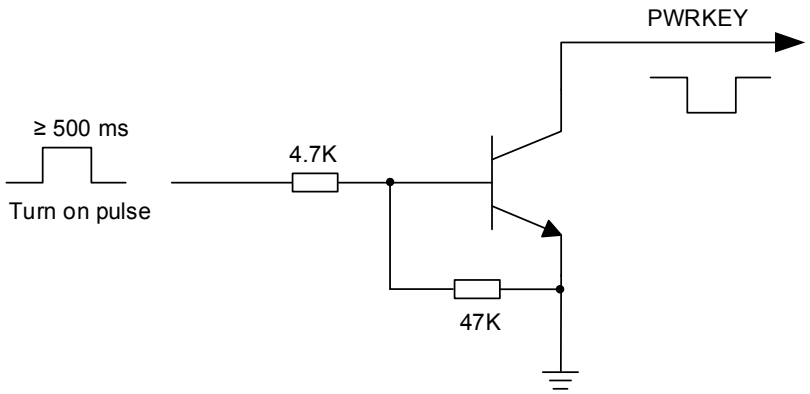

Figure 10: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

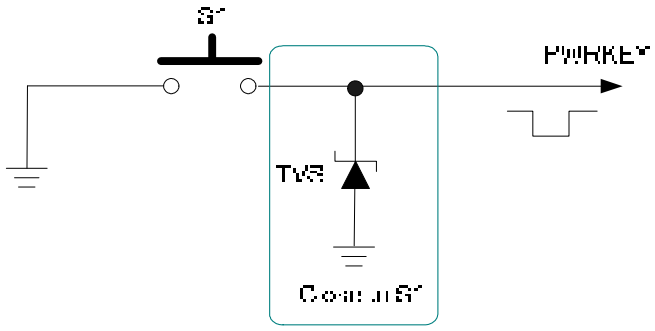

Figure 11: Turn on the Module Using Keystroke

The power on scenario is illustrated in the following figure.

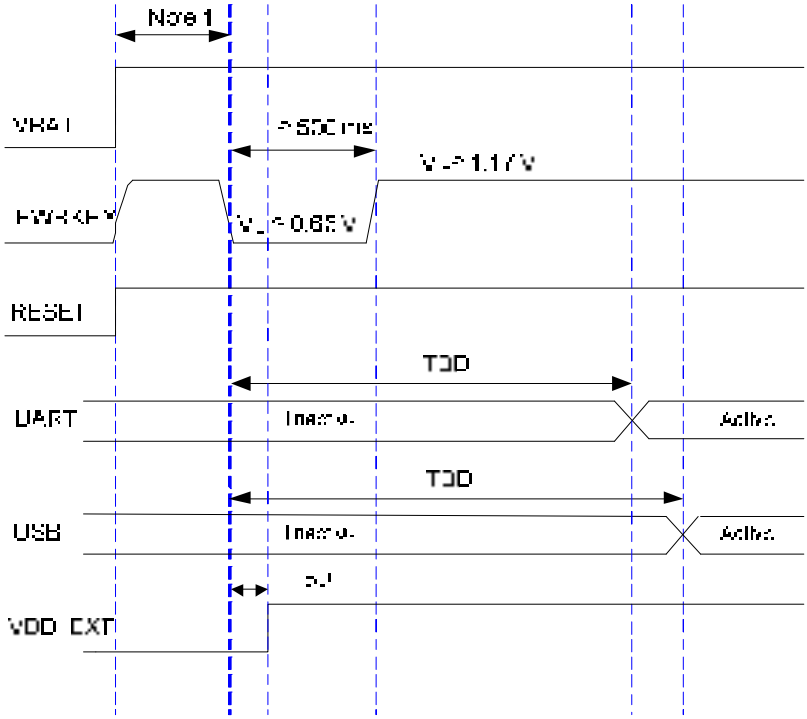

Figure 12: Power-on Timing

NOTES

1. Please make sure that VBAT is stable for at least 30 ms before pulling down PWRKEY pin.
2. It is recommended to use an external OD/OC circuit to control the PWRKEY pin.

3.7.2. Turn on Module with PON_1

Table 9: PON_1 Pin Description

Pin Name	Pin No.	Description	Comment
PON_1	248	Driving it high will turn on the module automatically	Valid trigger range: 0.78 V~1.89 V.

When the module is powered off, drive PON_1 high for at least 500 ms will turn on the module automatically. A simple reference circuit is illustrated in the following figure.

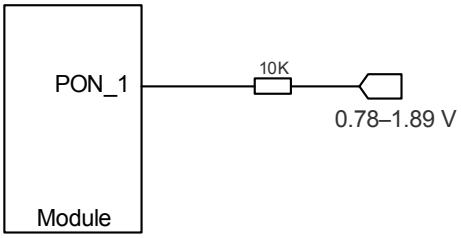

Figure 13: Turn on the Module using PON_1

NOTE

If PON_1 is not used, it is recommended to connect it to the ground.

3.7.3. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using API interface.

3.7.3.1. Turn off Module Using PWRKEY

Driving PWRKEY low for at least 2 s, the module will execute power-down procedure after PWRKEY is released. The power-off scenario is illustrated in the following figure.

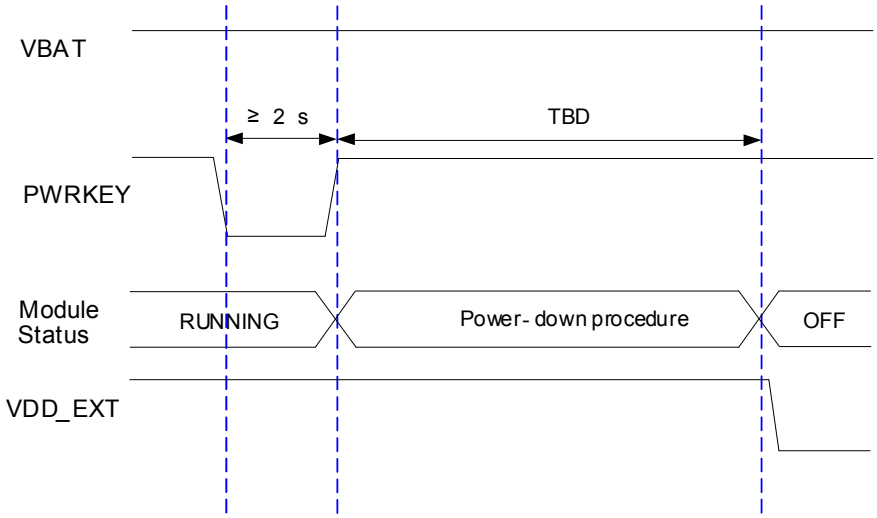

Figure 14: Power-off Timing

3.7.3.2. Turn off Module Using API Interface

It is also a safe way to use API interface to turn off the module, which is similar to turning off the module via PWRKEY Pin.

See ***document [2]*** for details about API function.

NOTES

1. To avoid damaging the internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or API interface, the power supply can be cut off.
2. When turn off module with API, please keep PWRKEY at high level after the execution of power off command. Otherwise the module will be turned on again after successfully turn-off.

3.8. Reset the Module

RESET can be used to reset the module. The module can be reset by driving RESET low for at least 370 ms. As the RESET pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground shielded.

Table 10: RESET Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET	8	Reset the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET.

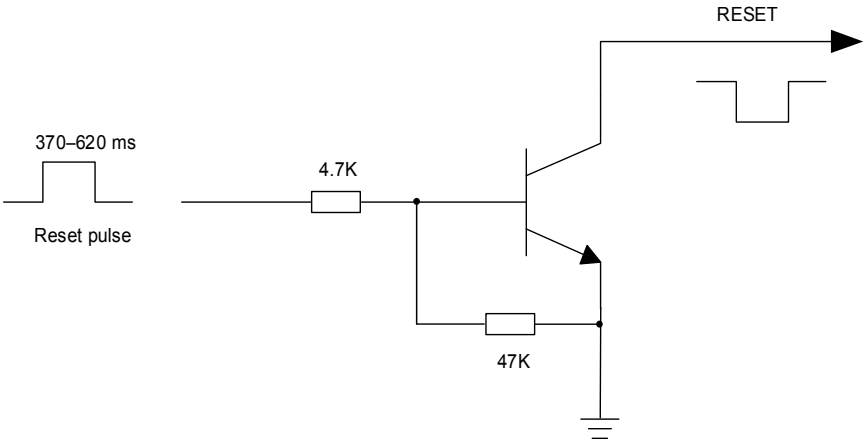

Figure 15: Reference Circuit of RESET by Using Driving Circuit

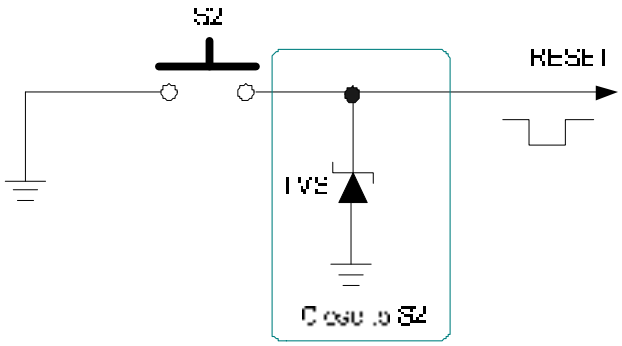

Figure 16: Reference Circuit of RESET by Using Button

The reset scenario is illustrated in the following figure.

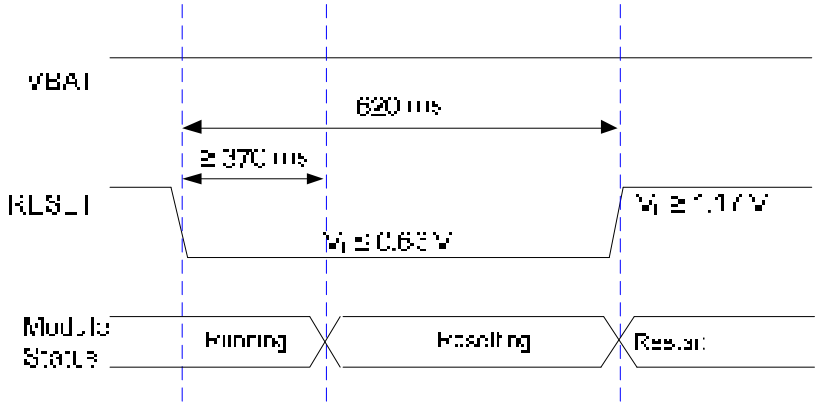

Figure 17: Timing of Resetting Module

NOTE

Please assure that there is no large capacitance on PWRKEY and RESET pins.

3.9. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 11: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	251	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	254	IO	(U)SIM1 card data	
USIM1_CLK	253	DO	(U)SIM1 card clock	
USIM1_RST	250	DO	(U)SIM1 card reset	
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	
USIM2_VDD	256	PO	(U)SIM2 card power supply	
USIM2_DATA	257	IO	(U)SIM2 card data	
USIM2_CLK	259	DO	(U)SIM2 card clock	
USIM2_RST	260	DO	(U)SIM2 card reset	

USIM2_DET	258	DI	(U)SIM2 card hot-plug detect

The module supports (U)SIM card hot-plug via the USIM_DET pin and either low level or high level detection is supported. The function is disabled by default and can be enabled by **AT+QSIMDET**. See ***document [3]*** for more details of the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

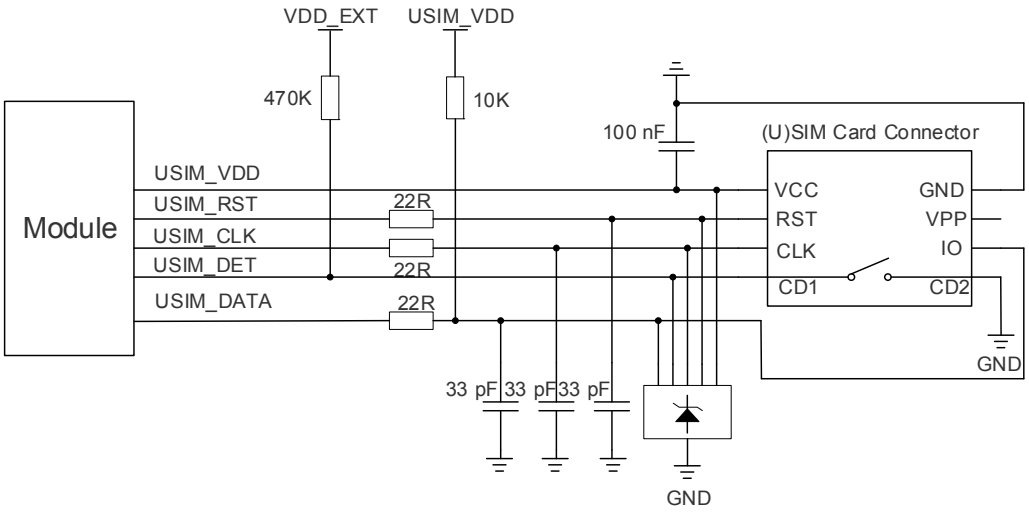

Figure 18: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET disconnected.

A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

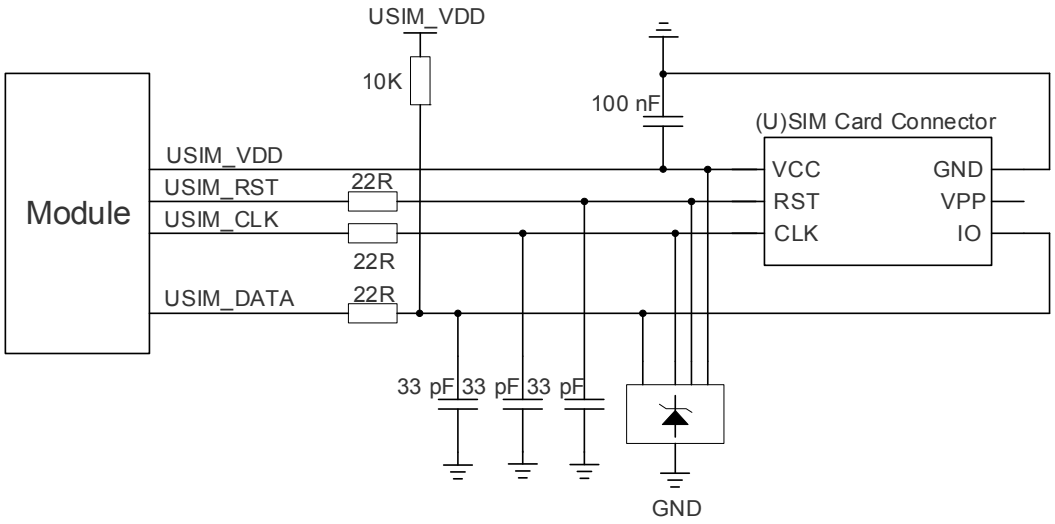

Figure 19: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card, follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the trace between the ground of the module and that of the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 10 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

NOTE

The load capacitance of (U)SIM interface will affect rise and fall time of the data exchange.

3.10. USB Interfaces

The module provides one USB 3.0 interface and one USB 2.0 interface which support SuperSpeed (5 Gbps on USB 3.0) and High-Speed (480 Mbps on USB 2.0) modes.

The USB 3.0 interface is used for data communication with AP by default. The USB 2.0 interface supports AT command communication, data transmission, software debugging, firmware upgrade and voice over USB*.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	84	DI	USB connection detect	
USB_DP	85	AI/AO	USB differential data bus (+)	Compliant with USB 2.0

USB_DM	87	AI/AO	USB differential data bus (-)	standard specification. Require differential impedance of 90 Ω.
USB_SS_TX_P	93	AO	USB 3.0 super-speed transmit (+)	Compliant with USB 3.0 standard specification. Require differential impedance of 90 Ω.
USB_SS_TX_M	91	AO	USB 3.0 super-speed transmit (-)	
USB_SS_RX_P	90	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	88	AI	USB 3.0 super-speed receive (-)	

It is recommended to reserve USB 2.0 for firmware upgrade in application design, and reserve test points for debugging purpose. The following are the reference circuits of USB 3.0 and 2.0 interfaces.

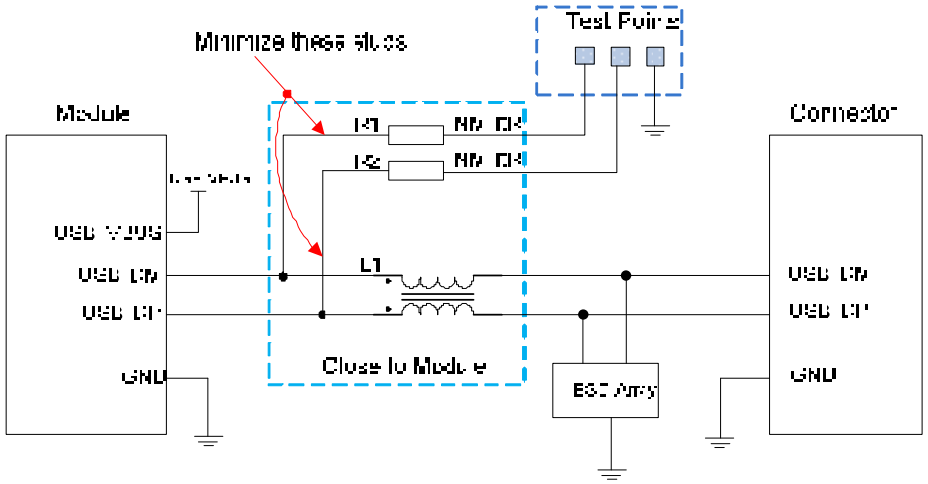

Figure 20: Reference Circuit of USB 2.0 Application

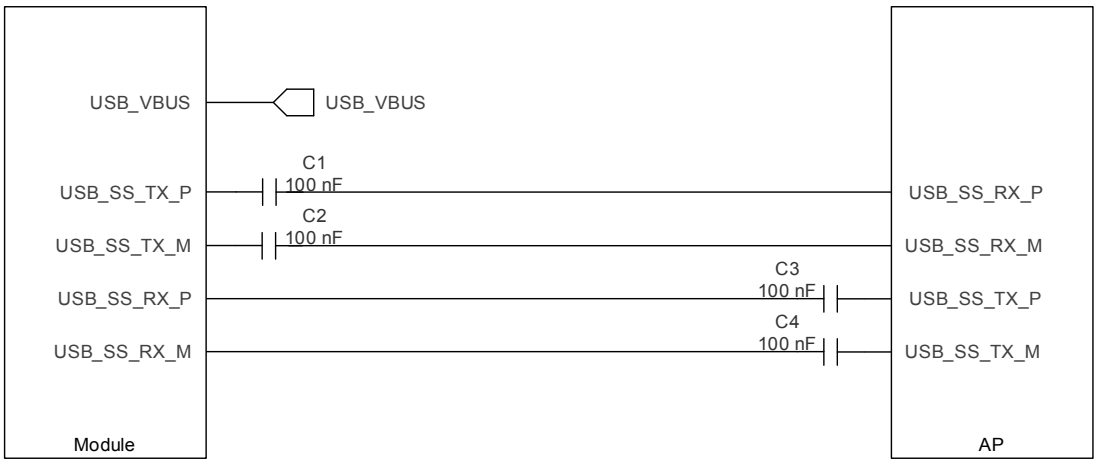

Figure 21: Reference Circuit of USB 3.0 Application

To ensure signal integrity of USB data lines, components R1, R2 and L1 must be placed close to the module, and also these resistors should be placed close to each other. The capacitors C1 and C2 should be placed near the module. The capacitors C3 and C4 should be placed near the AP. The extra stubs of trace must be as short as possible.

The following principles of USB interface should be complied with, so as to meet USB 2.0 and USB 3.0 specifications.

- It is important to route the USB 2.0 and 3.0 signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, the trace length should be less than 120 mm, and the differential data pair matching should be less than 0.7 mm (5 ps).
- For USB 3.0 signal traces, the maximum length of each differential data pair (Tx/Rx) is recommended to be less than 100 mm, and each differential data pair matching should be less than 0.7 mm (5 ps).
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- If a USB connector is used, please keep the ESD protection components as close to the USB connector as possible. Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.

NOTES

1. USB 2.0 and USB 3.0 share the same controller, therefore they cannot be used simultaneously.
2. “*” means under development.

3.11. UART Interfaces

The module provides three UART interfaces: UART1, BT UART and debug UART.

- UART1 and BT UART support RTS and CTS hardware flow control, and are used for data transmission with peripherals.
- UART1 and BT UART support 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 bps baud rates, and the default is 115200 bps.
- The debug UART interface supports 115200 bps baud rate, and is used for Linux console and log output.

Table 13: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Description	Comment
UART1_CTS	71	DO	UART1 clear to send	1.8 V power domain. Can be configured to GPIOs.
UART1_RTS	74	DI	UART1 request to send	
UART1_TXD	70	DO	UART1 transmit	
UART1_RXD	72	DI	UART1 receive	

Table 14: Pin Definition of BT UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_UART_TXD	59	DO	BT UART transmit	1.8 V power domain. Can be configured to GPIOs
BT_UART_RXD	63	DI	BT UART receive	
BT_UART_RTS	61	DI	BT UART request to send	
BT_UART_CTS	62	DO	BT UART clear to send	

Table 15: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	107	DO	Debug UART transmit	1.8 V power domain.
DBG_RXD	110	DI	Debug UART receive	1.8 V power domain.

Table 16: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.63	V
V_{IH}	1.17	2.1	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8 V UART interfaces. A level translator should be used if customers' application is equipped with a 3.3 V UART interface. A level translator TXS0104E-Q1 provided by *Texas Instruments* (visit http://www.ti.com for more information) is recommended. The following figure shows a reference design.

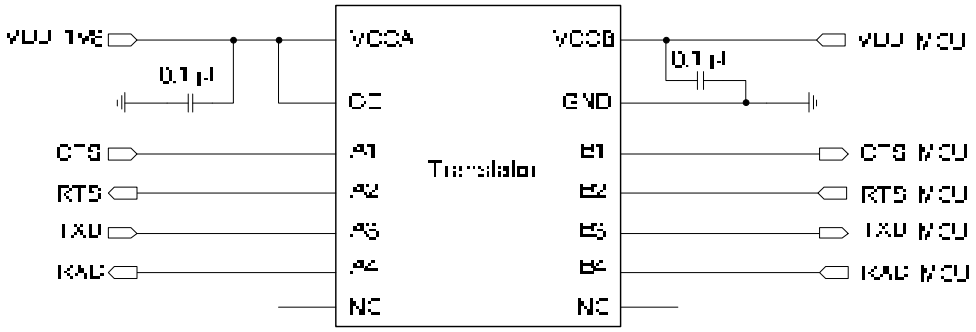

Figure 22: Reference Circuit with Translator Chip

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

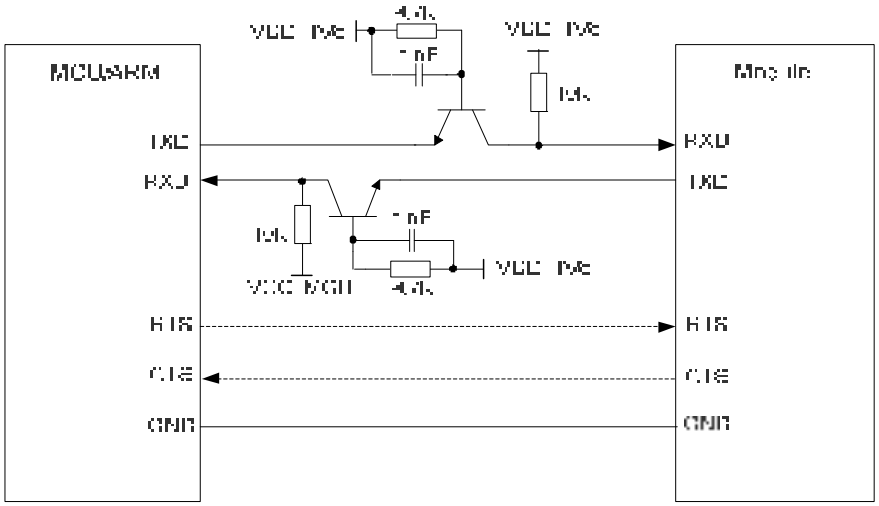

Figure 23: Reference Circuit with Transistor Circuit

NOTES

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. For the purpose of reducing power consumption, it is recommended to switch off the power supply for VDD_1V8 in sleep mode.
3. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

3.12. I2S and I2C Interfaces

The module provides I2S and I2C interfaces for audio function design.

Table 17: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
CDC_RST	77	DO	Codec reset	1.8 V power domain. Can be configured to GPIOs.
I2S_MCLK	81	DO	Clock output for codec	
I2S_WS	73	IO	I2S word select	
I2S_SCK	75	DO	I2S clock	
I2S_DIN	76	DI	I2S data in	
I2S_DOUT	78	DO	I2S data out	

Table 18: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	79	OD	I2C serial clock	Require external pull-up to 1.8 V.
I2C1_SDA	80	OD	I2C serial data	

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.

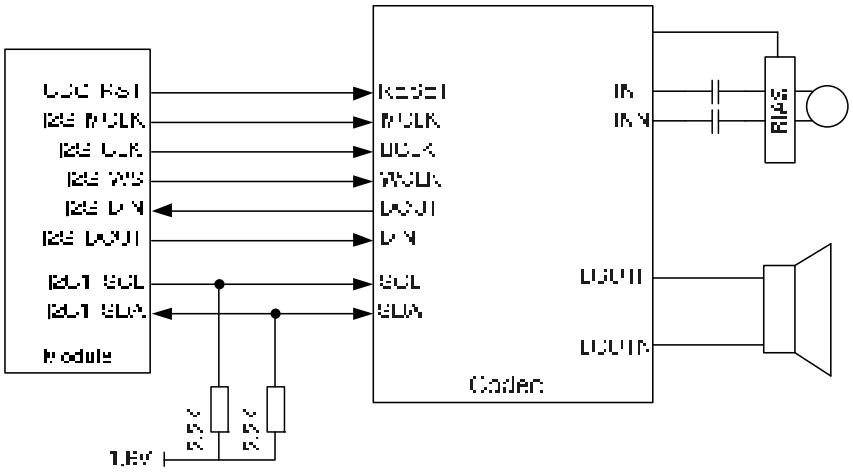

Figure 24: Reference Circuit of I2S and I2C Application with Audio Codec

NOTE

The module works as a master device pertaining to I2C interface.

3.13. SDIO Interface

The module provides an SDIO interface. It is recommended to use the interface for eMMC application.

Table 19: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_VDD	60	PI	SDIO power supply	Connect it to VDD_EXT.
SDC1_DATA_0	49	IO	SDIO data bit 0	1.8 V power domain for eMMC.
SDC1_DATA_1	50	IO	SDIO data bit 1	
SDC1_DATA_2	51	IO	SDIO data bit 2	
SDC1_DATA_3	52	IO	SDIO data bit 3	
SDC1_CMD	48	IO	SDIO command	
SDC1_DATA_4	53	IO	SDIO data bit 4	1.8 V power domain. For eMMC configuration by default. Can be configured to GPIO.
SDC1_DATA_5	55	IO	SDIO data bit 5	
SDC1_DATA_6	56	IO	SDIO data bit 6	
SDC1_DATA_7	58	IO	SDIO data bit 7	
SDC1_CLK	47	DO	SDIO clock	1.8 V power domain for eMMC.
EMMC_RST	54	DO	eMMC reset	1.8 V power domain.
EMMC_PWR_EN	45	DO	eMMC power supply enable control	

The following is a reference design of SDIO interface for eMMC application.

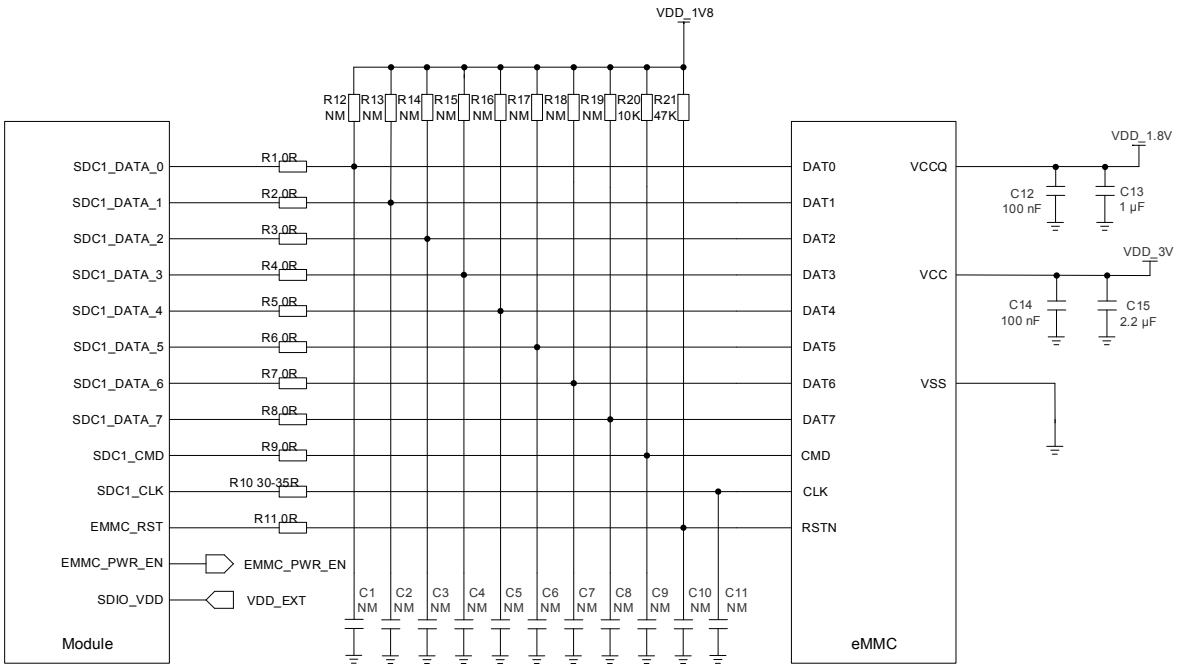

Figure 25: Reference Design of SDIO Interface for eMMC Application

Please follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve resistors R12–R21 for pulling up SDIOs to VDD_1.8 V. Resistors R12–R19 are not mounted by default, and the recommended resistor value is 10–100 kΩ.
- In order to improve signal quality, it is recommended to add 0 Ω resistors R1–R9 and R11 in series between the module and eMMC. Resistor R10 should be 30-35 Ω. The bypass capacitors C1–C11 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals as well as noisy signals such as clock signals and DC-DC signals.
- Spacing DATA to DATA/CLK bus is larger than two times of line width.
- Spacing DATA/CLK/CMD to other signals is larger than two times of line width.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 17 mm, so the exterior total trace length should be less than 33 mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 40 pF.

3.14. SPI Interfaces

The module provides two SPI interfaces supporting only master mode. The maximum clock frequency of SPI is up to 50 MHz.

Table 20: Pin Definition of SPI Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SPI1_CLK	216	DO	SPI1 clock	1.8 V power domain. Can be configured to GPIO. If unused, keep them open.
SPI1_CS	213	DO	SPI1 chip select	
SPI1_MISO	219	DI	SPI1 master-in salve-out	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	
SPI2_CLK	103	DO	SPI2 clock	
SPI2_CS	105	DO	SPI2 chip select	
SPI2_MISO	106	DI	SPI2 master-in salve-out	
SPI2_MOSI	108	DO	SPI2 master-out slave-in	

The following figure shows the timing relationship of SPI interfaces. The related parameters of SPI timing are shown in the table below.

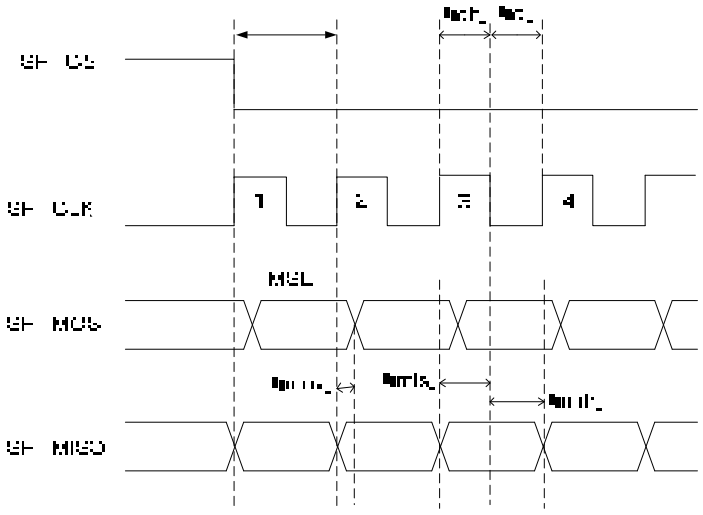

Figure 26: SPI Timing

Table 21: Parameters of SPI Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high-level time	9.0	-	-	ns
t(cl)	SPI clock low-level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides a 1.8 V SPI interface. A level translator should be used between the module and the host if customers' application is equipped with a 3.3 V processor or device interface.

3.15. RGMII Interface

The module includes an integrated Ethernet MAC with an RGMII interface. Key features of the RGMII interface are shown below:

- Support IEEE 1588-2008, IEEE 802.1AS-2011 and 802.1-Qav-2009
- Half/full duplex for 10/100/1000 Mbps
- Support VLAN tagging
- Can be used to connect to external Ethernet PHY like 88EA1512, or an external switch

Table 22: Pin Definition of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_MD_IO	10	IO	RGMII MDIO management data	Power domain determined by RGMII_PWR_IN
RGMII_MD_CLK	11	DO	RGMII MDC management clock	
RGMII_RX_0	13	DI	RGMII receive data bit 0	
RGMII_RX_1	14	DI	RGMII receive data bit 1	

RGMII_CTL_RX	15	DI	RGMII receive control	
RGMII_RX_2	16	DI	RGMII receive data bit 2	
RGMII_RX_3	17	DI	RGMII receive data bit 3	
RGMII_CK_RX	19	DI	RGMII receive clock	
RGMII_TX_0	20	DO	RGMII transmit data bit 0	
RGMII_CTL_TX	21	DO	RGMII transmit control	
RGMII_TX_1	22	DO	RGMII transmit data bit 1	
RGMII_TX_2	23	DO	RGMII transmit data bit 2	
RGMII_CK_TX	24	DO	RGMII transmit clock	
RGMII_TX_3	25	DO	RGMII transmit data bit 3	
RGMII_PWR_EN	27	DO	Enable external LDO to supply power to RGMII_PWR_IN	1.8 V power domain
RGMII_PWR_IN	28	PI	Power input for internal RGMII circuit	1.8/2.5 V power supply input. If RGMII interface is not used, please connect it to VDD_EXT.
RGMII_INT	29	DI	RGMII PHY interrupt output	1.8 V power domain
RGMII_RST	31	DO	Reset output for RGMII PHY	

The following figure shows the simplified block diagram for Ethernet application.

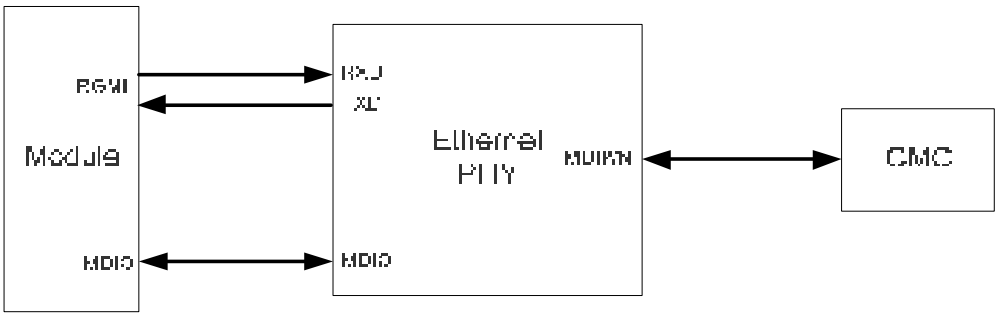

Figure 27: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of RGMII interface with PHY application.

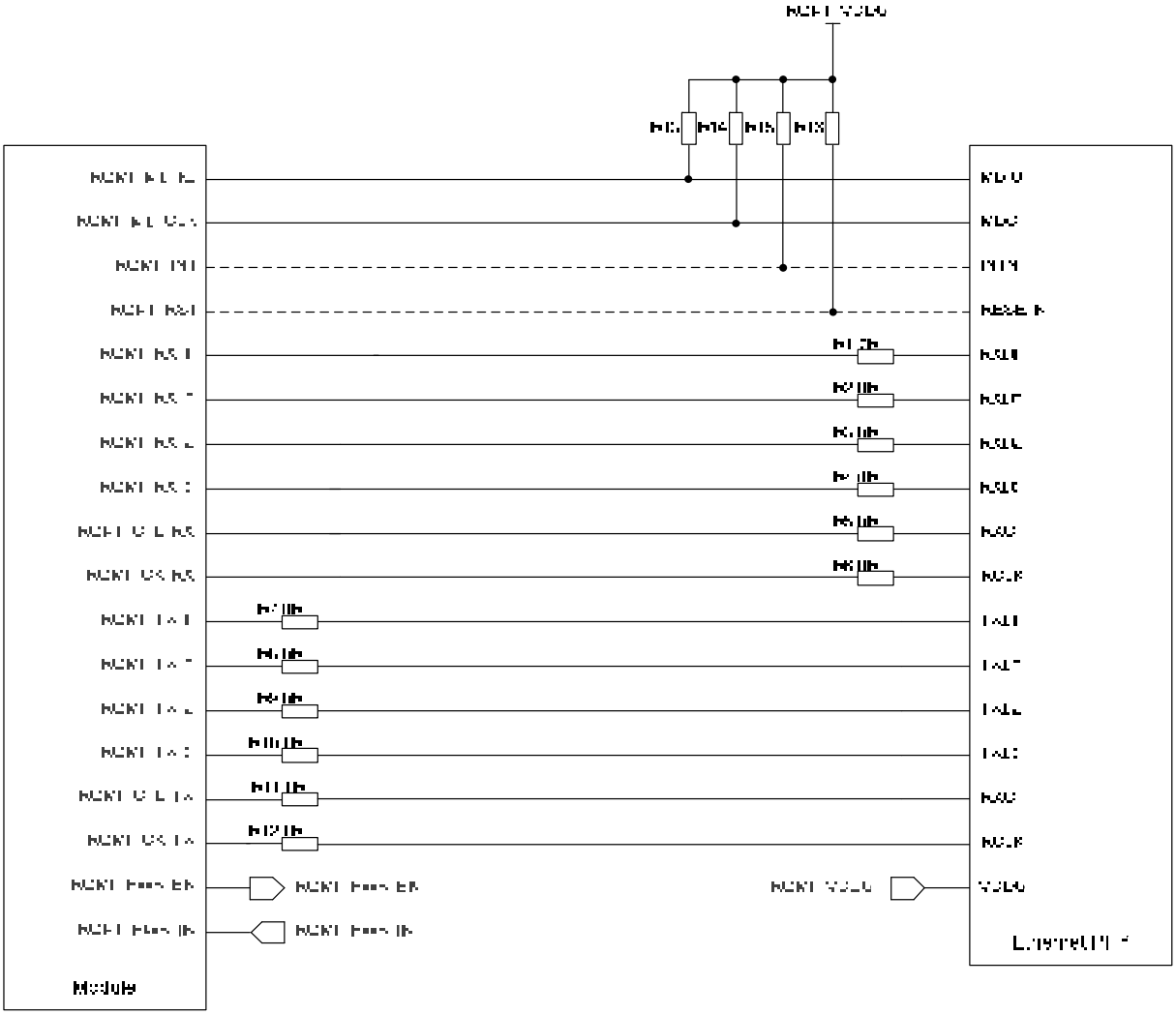

Figure 28: Reference Circuit of RGMII Interface with PHY Application

In order to enhance the reliability and availability of customers' application, please follow the criteria below in the Ethernet PHY circuit design:

- The I/O voltage of RGMII matches with that of PHY.
- The voltage of RGMII_INT and RGMII_RST matches with the I/O voltage of PHY.
- The typical power consumption of RGMII_PER_IN is 300 mA @ 1.8 V.
- Keep RGMII data and control signals away from RF and VBAT traces.
- Assure impedance of RGMII signals trace is 50 Ω ±20%.
- The length difference among CK_TX, CTL_TX and TX_[0-3] is less than 2 mm.
- The length difference among CK_RX, CTL_RX and RX_[0-3] is less than 2 mm.
- TX bus (CK_TX to CTL_TX/TX_[0-3]) spacing or RX bus (CK_RX to CTL_RX/RX_[0-3]) spacing is larger than two times of the line width.
- Spacing between TX bus and RX bus is larger than 2.5 times of line width.

- Spacing to all other signals is larger than three times of line width.
- Resistors R7–R12 should be placed near the module. Resistor R1–R6 should be placed near the Ethernet PHY. The value of R1–R16 varies with the selection of PHY.

3.16. WLAN and BT Interfaces*

The module provides a PCIe interface for WLAN function and UART & PCM interfaces for BT function.

Table 23: Pin Definition of WLAN and BT Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIe Interface				
PCIE_REFCLK_P	40	AO	PCIe reference clock (+)	Require differential impedance of 95 Ω.
PCIE_REFCLK_M	38	AO	PCIe reference clock (-)	
PCIE_TX_M	44	AO	PCIe transmit (-)	
PCIE_TX_P	46	AO	PCIe transmit (+)	
PCIE_RX_M	32	AI	PCIe receive (-)	
PCIE_RX_P	34	AI	PCIe receive (+)	
PCIE_CLKREQ	36	DIO	PCIe clock request	1.8 V power domain.
PCIE_RST	39	DO	PCIe reset	
PCIE_WAKE	30	DI	PCIe wakeup	
Coexistence Interface				
COEX_UART_RXD	67	DI	LTE&WLAN/BT coexistence receive	1.8 V power domain.
COEX_UART_TXD	69	DO	LTE&WLAN/BT coexistence transmit	
BT Interface				
BT_UART_TXD	59	DO	BT UART transmit	
BT_UART_RXD	63	DI	BT UART receive	

BT_UART_RTS	61	DI	BT UART request to send	1.8 V power domain. Can be configured to GPIOs.
BT_UART_CTS	62	DO	BT UART clear to send	
PCM_SYNC	265	IO	PCM data frame sync	
PCM_CLK	262	IO	PCM data bit clock	
PCM_IN	263	DI	PCM data input	
PCM_OUT	261	DO	PCM data output	
Others interfaces				
WLAN_PWR_EN2	225	DO	WLAN power supply enable control 2	1.8 V power domain.
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	
WLAN_EN	228	DO	WLAN enable	
BT_EN	66	DO	BT function enable	
WLAN_SLP_CLK	231	DO	WLAN sleep clock	
VDD_WIFI_VM	276	PO	Power supply for Wi-Fi	Vnorm = 1.35 V
VDD_WIFI_VH	277	PO	Power supply for Wi-FI	Vnorm = 1.95 V

NOTES

1. When WLAN or BT function is used, the coexistence interface must be used simultaneously.
2. When BT function is enabled on the module, PCM_SYNC and PCM_CLK pins will only be used to output signals.
3. It is recommended that the networks of PCIE_CLKREQ and PCIE_WAKE are pulled up to VDD_EXT.
4. “*” means under development.

The following figure shows a reference design for WLAN and BT interfaces application.

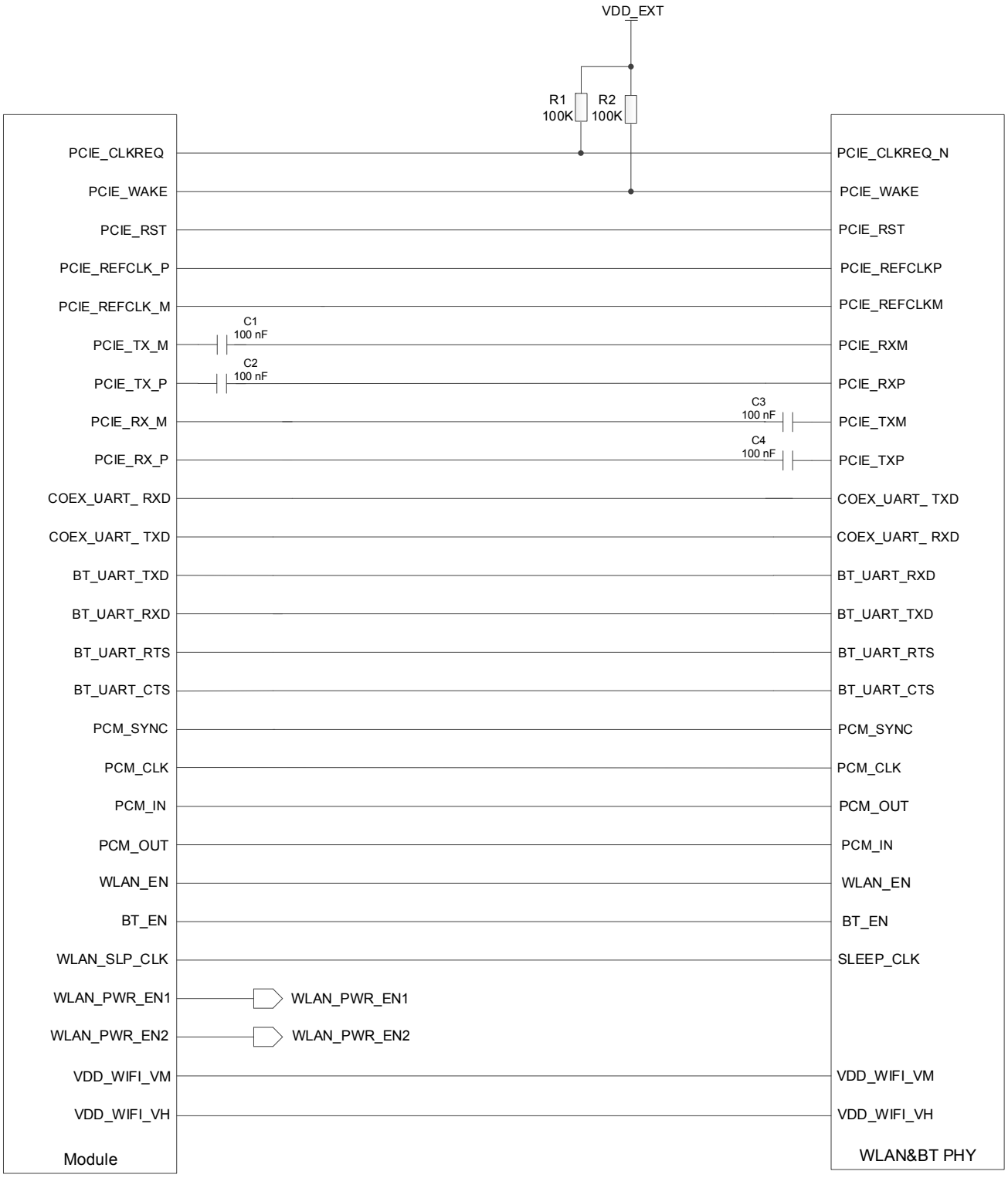

Figure 29: Reference Circuit for Connection with WLAN&BT PHY

To ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the module. C3 and C4 should be placed close to the PHY. The extra stubs of trace must be as short as possible.

The following principles of PCIe interface design should be complied with, so as to meet PCIe Gen2 specifications.

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. And the differential impedance is 95 Ω ±10%.
- For PCIe signal traces, the maximum length of each differential data pair (TX/RX/REFCLK) is recommended to be less than 270 mm, and each differential data pair matching should be less than 0.7 mm (5 ps).
- Spacing data lane-to-lane (intra-interface) is three times of line width.
- Spacing to all other signals (inter-interface) is four times of line width.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the PCIe differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.

3.17. ADC Interfaces

The module provides three analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read via **AT+QADC=<port>** command, through specifying **<port>** as 0, 1 or 2. For more details about the AT command, see ***document [3]***.

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=2**: read the voltage value on ADC2

In order to improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 24: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC1	245	General purpose ADC interface
ADC0	247	General purpose ADC interface
ADC2	139	General purpose ADC interface

Table 25: Characteristic of ADC Interface

Parameter	Min.	Typ.	Max.	Unit

ADC0 Voltage Range	0		1.875	V
ADC1 Voltage Range	0		1.875	V
ADC2 Voltage Range	0		1.875	V
ADC Resolution		14		bits
ADC Sample Rate		4.8		MHz

NOTES

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.18. USB_BOOT Interface

The module provides a USB_BOOT pin. Pulling up the USB_BOOT to VDD_EXT before powering on the module will force the module into emergency download mode when powered on. In emergency download mode, the module supports firmware upgrade over USB 2.0 interface.

Table 26: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	83	DI	Force the module into emergency download mode	1.8 V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

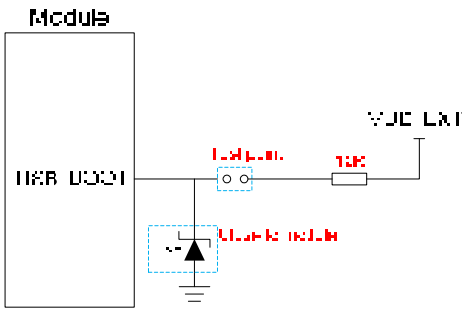

Figure 30: Reference Circuit of USB_BOOT Interface

3.19. GPIO Interfaces

The module provides 11 GPIOs.

Table 27: Pin Definition of GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	100	IO	General-purpose input/output	1.8 V power domain. If unused, keep them open.
GPIO2	101	IO		
GPIO3	102	IO		
GPIO4	104	IO		
GPIO5	116	IO		
GPIO6	243	IO		
GPIO7	246	IO		
GPIO8	249	DO		
GPIO9	264	IO		
GPIO10	267	IO		
GPIO11	289	IO		

4 Antenna Interfaces

The module includes one main antenna interface (ANT_MAIN) and one Rx-diversity antenna interface (ANT_DIV) which is used to resist the fall of signals caused by high speed movement and multipath effect. The antenna ports have an impedance of 50 Ω.

4.1. Main/Rx-diversity Antenna Interface

4.1.1. Pin Definition

The pin definition of Main/Rx-diversity antenna interfaces are shown below.

Table 28: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	143	AI/AO	Main antenna interface	50 Ω impedance
ANT_DIV	170	AI	Receive diversity antenna interface	50 Ω impedance

4.1.2. Operating Frequency

Table 29: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–850	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz

WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
WCDMA B9	1749.9–1784.9	1844.9–1879.9	MHz
WCDMA B19	830–845	875–890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B9	1749.9–1784.9	1844.9–1879.9	MHz
LTE-FDD B11	1427.9–1447.9	1475.9–1495.9	MHz
LTE-FDD B12	698–716	728–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B17	704–716	734–746	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B21	1447.9–1462.9	1495.9–1510.9	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B29 [1)]		717–728	MHz
LTE-FDD B30	2305–2315	2350–2360	MHz

LTE-FDD B32 [1)]		1452–1496	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2555–2655	2555–2655	MHz
LTE-TDD B66	1710–1780	2110–2200	MHz
LTE-TDD B71	663–698	617–652	MHz

NOTE

[1)] LTE-FDD B29, B30 and B32 support Rx only.

4.1.3. Reference Design of RF Antenna Interfaces

A reference design of main and Rx-diversity antenna interfaces is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2 and R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default.

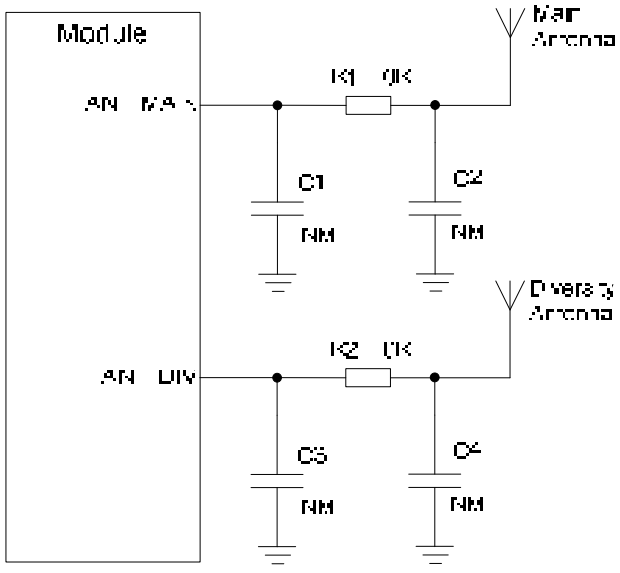

Figure 31: Reference Circuit of RF Antenna Interfaces

NOTES

ANT_DIV function is enabled by default. **AT+QCFG="diversity",0** command can be used to disable receive diversity. See ***document [3]*** for details of the command.

4.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

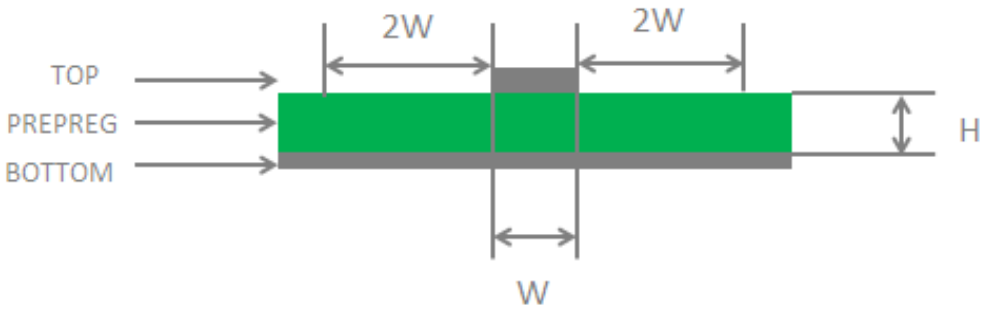

Figure 32: Microstrip Design on a 2-layer PCB

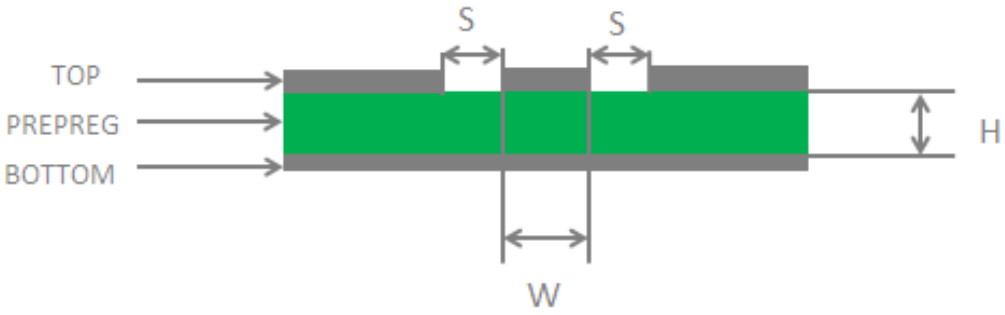

Figure 33: Coplanar Waveguide Design on a 2-layer PCB

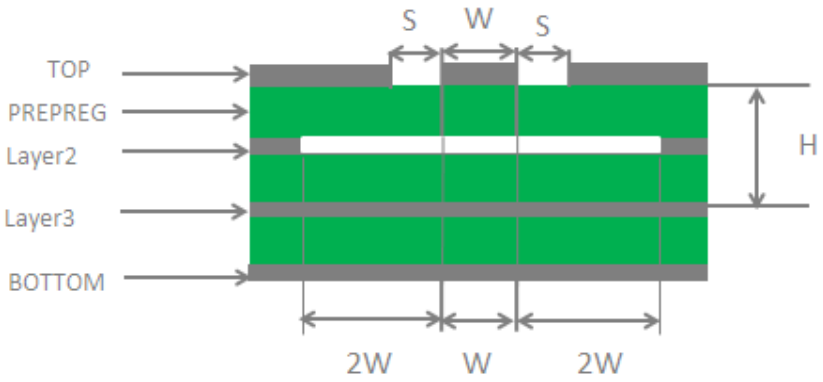

Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

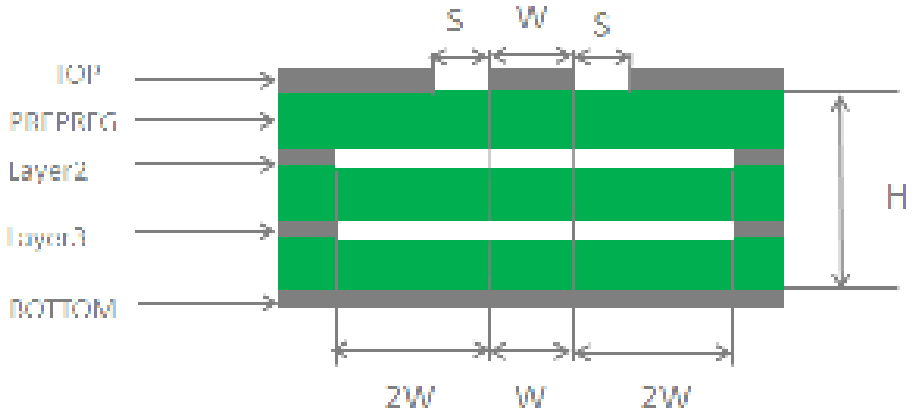

Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

4.2. Antenna Installation

4.2.1. Antenna Requirements

The following table shows the requirements on the main antenna and the Rx-diversity antenna.

Table 30: Antenna Requirements

Type	Requirements
GSM/UMTS/LTE	VSWR: ≤ 2 Efficiency: > 30% Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (GSM850, EGSM900, WCDMA B5/B8/B19, LTE-FDD B5/B8/B9/B12/B13/B17/B18/B19/B20/B26/B28/B29/B71) Cable insertion loss: < 1.5 dB (DCS1800, PCS1900, WCDMA B1/B2/B3/B4B9, LTE-FDD B1/B2/B3/B4/B9/B11/B21/B25/B32/B66, LTE-TDD B34/B39) Cable insertion loss: < 2 dB (LTE-FDD B7/B30, LTE-TDD B38/B40/B41)

4.2.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by *Rosenberger.*

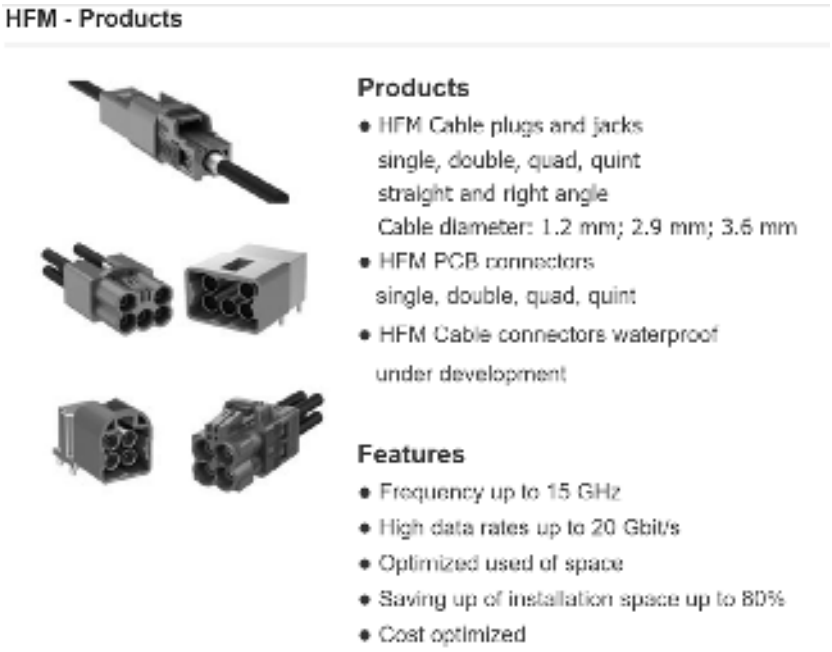

Figure 36: Description of the HFM Connector

For more details, visit https://www.rosenbergerap.com.

5 Reliability, Radio and Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	2.0	A
Voltage at Digital Pins	-0.3	2.04	V
Voltage at ADC0	0	1.91	V
Voltage at ADC1	0	1.91	V
Voltage at ADC2	0	1.91	V

5.2. Power Supply Ratings

Table 32: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

5.3. Operation and Storage Temperatures

Table 33: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
eCall Temperature Range [3)]	-40		+90	ºC
Storage Temperature Range	-40		+95	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant, and emergency call can be dialed out with a maximum power and data rate.
2. [2)] Within extended temperature range, the module remains fully functional and retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.
3. [3)] Within eCall temperature range, the emergency call function must be functional until the module is broken. When the ambient temperature is between 75 °C and 90 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of emergency call.

5.4. Current Consumption

Table 34: Module Current Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	0.021	mA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.144	mA
	GSM850 DRX = 2 (USB disconnected)	3.183	mA
	GSM850 DRX = 5 (USB disconnected)	2.128	mA
	GSM850 DRX = 5 (USB suspend)	TBD	mA
	GSM850 DRX = 9 (USB disconnected)	1.760	mA
	EGSM900 DRX = 2 (USB disconnected)	3.160	mA
	EGSM900 DRX = 5 (USB disconnected)	2.181	mA
	EGSM900 DRX = 5 (USB suspend)	TBD	mA
	EGSM900 DRX = 9 (USB disconnected)	1.868	mA
	DCS DRX = 2 (USB disconnected)	3.191	mA
	DCS DRX = 5 (USB disconnected)	2.157	mA
	DCS DRX = 5 (USB suspend)	TBD	mA
	DCS DRX = 9 (USB disconnected)	3.175	mA
	PCS DRX = 2 (USB disconnected)	3.156	mA
	PCS DRX = 5 (USB disconnected)	2.154	mA
	PCS DRX = 5 (USB suspend)	TBD	mA
	PCS DRX = 9 (USB disconnected)	3.886	mA
	WCDMA PF = 64 (USB disconnected)	3.295	mA
	WCDMA PF = 64 (USB suspend)	TBD	mA
	WCDMA PF = 128 (USB disconnected)	2.458	mA

	WCDMA PF = 256 (USB disconnected)	2.019	mA
	WCDMA PF = 512 (USB disconnected)	1.925	mA
	LTE-FDD PF = 32 (USB disconnected)	4.123	mA
	LTE-FDD PF = 64 (USB disconnected)	2.968	mA
	LTE-FDD PF = 64 (USB suspend)	TBD	mA
	LTE-FDD PF = 128 (USB disconnected)	3.208	mA
	LTE-FDD PF = 256 (USB disconnected)	2.541	mA
	LTE-TDD PF = 32 (USB disconnected)	5.170	mA
	LTE-TDD PF = 64 (USB disconnected)	3.849	mA
	LTE-TDD PF = 64 (USB suspend)	TBD	mA
	LTE-TDD PF = 128 (USB disconnected)	4.128	mA
	LTE-TDD PF = 256 (USB disconnected)	2.849	mA
Idle state	GSM DRX = 5 (USB connected)	29.93	mA
	GSM DRX = 5 (USB disconnected)	11.99	mA
	WCDMA PF = 64 (USB connected)	30.93	mA
	WCDMA PF = 64 (USB disconnected)	15.59	mA
	LTE-FDD PF = 64 (USB connected)	42.91	mA
	LTE-FDD PF = 64 (USB disconnected)	14.813	mA
	LTE-TDD PF = 64 (USB connected)	30.243	mA
	LTE-TDD PF = 64 (USB disconnected)	15.017	mA
GPRS data transfer (GNSS OFF)	GSM850 4DL/1UL @ 33 dBm	334.3	mA
	GSM850 3DL/2UL @ 32 dBm	553	mA
	GSM850 2DL/3UL @ 30dBm	586.7	mA
	GSM850 1DL/4UL @ 29 dBm	686.8	mA
	EGSM900 4DL/1UL @ 33 dBm	326.6	mA

	EGSM900 3DL/2UL @ 32 dBm	518.5	mA
	EGSM900 2DL/3UL @ 30dBm	618.1	mA
	EGSM900 1DL/4UL @ 29 dBm	690.5	mA
	DCS1800 4DL/1UL @ 29.5 dBm	236.8	mA
	DCS1800 3DL/2UL @ 29.0dBm	367.6	mA
	DCS1800 2DL/3UL @ 26.5 dBm	426.2	mA
	DCS1800 1DL/4UL @ 25.5 dBm	501.9	mA
	PCS1900 4DL/1UL @ 29.5 dBm	229.9	mA
	PCS1900 3DL/2UL @ 29.0dBm	362.5	mA
	PCS1900 2DL/3UL @ 26.5 dBm	412.4	mA
	PCS1900 1DL/4UL @ 25.5 dBm	469.3	mA
EDGE data transfer (GNSS OFF)	GSM850 4DL/1UL @ 27.0dBm	189.4	mA
	GSM850 3DL/2UL @ 26.0dBm	298.5	mA
	GSM850 2DL/3UL @ 24.0dBm	348.5	mA
	GSM850 1DL/4UL @ 23.0dBm	405.3	mA
	EGSM900 4DL/1UL @ 27.0dBm	187.3	mA
	EGSM900 3DL/2UL @ 26.0dBm	293	mA
	EGSM900 2DL/3UL @ 24.0dBm	343.5	mA
	EGSM900 1DL/4UL @ 23.0dBm	395.4	mA
	DCS1800 4DL/1UL @ 26.0dBm	173.9	mA
	DCS1800 3DL/2UL @ 25.0dBm	265.7	mA
	DCS1800 2DL/3UL @ 23.0dBm	325	mA
	DCS1800 1DL/4UL @ 22.0dBm	372.5	mA
	PCS1900 4DL/1UL @ 26.0dBm	179.4	mA
	PCS1900 3DL/2UL @ 25.0dBm	274.6	mA

	PCS1900 2DL/3UL @ 23.0dBm	322.2	mA
	PCS1900 1DL/4UL @ 22.0dBm	371.2	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @ 23.0 dBm	590.7	mA
	WCDMA B2 HSDPA @ 23.0 dBm	656.7	mA
	WCDMA B3 HSDPA @ 23.0 dBm	610.42	mA
	WCDMA B4 HSDPA @ 23.0 dBm	650.27	mA
	WCDMA B5 HSDPA @ 23.0 dBm	588.94	mA
	WCDMA B8 HSDPA @ 23.0 dBm	621.63	mA
	WCDMA B9 HSDPA @ 23.0 dBm	613.25	mA
	WCDMA B19 HSDPA @ 23.0 dBm	618.04	mA
	WCDMA B1 HSUPA @ 23.0 dBm	584.23	mA
	WCDMA B2 HSUPA @ 23.0 dBm	603.26	mA
	WCDMA B3 HSUPA @ 23.0 dBm	602.99	mA
	WCDMA B4 HSUPA @ 23.0 dBm	614.63	mA
	WCDMA B5 HSUPA @ 23.0 dBm	549.2	mA
	WCDMA B8 HSUPA @ 23.0 dBm	575.01	mA
	WCDMA B9 HSUPA @ 23.0 dBm	623.55	mA
	WCDMA B19 HSUPA @ 23.0 dBm	584.83	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 @ 23.0dBm	606.86	mA
	LTE-FDD B2 @ 23.0dBm	668.61	mA
	LTE-FDD B3 @ 23.0dBm	651.63	mA
	LTE-FDD B4 @ 23.0dBm	636.49	mA
	LTE-FDD B5 @ 23.0dBm	585.8	mA
	LTE-FDD B7 @ 23.0dBm	745.87	mA
	LTE-FDD B8 @ 23.0dBm	607.38	mA

	LTE-FDD B9 @ 23.0dBm	597.53	mA
	LTE-FDD B11 @ 23.0dBm	674.67	mA
	LTE-FDD B12 @ 23.0dBm	595.3	mA
	LTE-FDD B13 @ 23.0dBm	661.65	mA
	LTE-FDD B17 @ 23.0dBm	596.13	mA
	LTE-FDD B18 @ 23.0dBm	636.57	mA
	LTE-FDD B19 @ 23.0dBm	627.77	mA
	LTE-FDD B20 @ 23.0dBm	617.46	mA
	LTE-FDD B21 @ 23.0dBm	665.74	mA
	LTE-FDD B25 @ 23.0dBm	622.94	mA
	LTE-FDD B26 @ 23.0dBm	623.07	mA
	LTE-FDD B28 @ 23.0dBm	597.96	mA
	LTE-FDD B30 @ 23.0dBm	TBD	mA
	LTE-TDD B34 @ 23.0dBm	289.2	mA
	LTE-TDD B38 @ 23.0dBm	381.17	mA
	LTE-TDD B39 @ 23.0dBm	266.25	mA
	LTE-TDD B40 @ 23.0dBm	477.97	mA
	LTE-TDD B41 @ 23.0dBm	395.46	mA
	LTE-FDD B66 @ 23.0dBm	617.9	mA
	LTE-FDD B71 @ 23.0dBm	590.43	mA
GSM voice call	GSM850, PCL = 5 @ 32.dBm	340.3	mA
	GSM850, PCL = 12 @ 19.0dBm	155.6	mA
	GSM850, PCL = 19 @ 5.0dBm	127.5	mA
	EGSM900, PCL = 5 @ 32.dBm	327.3	mA
	EGSM900, PCL = 12 @ 19.0dBm	154.8	mA

	EGSM900, PCL = 19 @ 5.0dBm	125.1	mA
	DCS1800, PCL = 0 @ 30 dBm	248.9	mA
	DCS1800, PCL = 7 @ 16.0dBm	139.2	mA
	DCS1800, PCL = 15 @ 0dBm	132	mA
	PCS1900, PCL = 0 @ 30 dBm	255.6	mA
	PCS1900, PCL = 7 @ 16.0dBm	138.8	mA
	PCS1900, PCL = 15 @ 0dBm	129.8	mA
WCDMA voice call	WCDMA B1 @ 22.5 dBm	620.63	mA
	WCDMA B2 @ 22.5 dBm	666.99	mA
	WCDMA B3 @ 22.5 dBm	623	mA
	WCDMA B4 @ 22.5 dBm	659.48	mA
	WCDMA B5 @ 22.5 dBm	612.57	mA
	WCDMA B8 @ 23.0dBm	615.13	mA
	WCDMA B9 @ 23.0dBm	671.92	mA
	WCDMA B19 @ 23.0dBm	598.64	mA

5.5. RF Output Power

The following table shows the RF output power of the module.

Table 35: RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB

WCDMA B1	24dBm +1/-3 dB	< -49 dBm
WCDMA B2	24dBm +1/-3 dB	< -49 dBm
WCDMA B3	24dBm +1/-3 dB	< -49 dBm
WCDMA B4	24dBm +1/-3 dB	< -49 dBm
WCDMA B5	24dBm +1/-3 dB	< -49 dBm
WCDMA B8	24dBm +1/-3 dB	< -49 dBm
WCDMA B9	24dBm +1/-3 dB	< -49 dBm
WCDMA B19	24dBm +1/-3 dB	< -49 dBm
LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B2	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm
LTE-FDD B4	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm
LTE-FDD B9	23 dBm ±2 dB	< -39 dBm
LTE-FDD B11	23 dBm ±2 dB	< -39 dBm
LTE-FDD B12	23 dBm ±2 dB	< -39 dBm
LTE-FDD B13	23 dBm ±2 dB	< -39 dBm
LTE-FDD B17	23 dBm ±2 dB	< -39 dBm
LTE-FDD B18	23 dBm ±2 dB	< -39 dBm
LTE-FDD B19	23 dBm ±2 dB	< -39 dBm
LTE-FDD B20	23 dBm ±2 dB	< -39 dBm
LTE-FDD B21	23 dBm ±2 dB	< -39 dBm
LTE-FDD B25	23 dBm ±2 dB	< -39 dBm

LTE-FDD B26	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28	23 dBm ±2 dB	< -39 dBm
LTE-FDD B29	23 dBm ±2 dB	< -39 dBm
LTE-FDD B30	23 dBm ±2 dB	< -39 dBm
LTE-FDD B32	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38	23 dBm ±2 dB	< -39 dBm
LTE-TDD B39	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm
LTE-FDD B66	23 dBm ±2 dB	< -39 dBm
LTE-FDD B71	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.6. RF Receiving Sensitivity

Table 36: RF Receiving Sensitivity (Unit: dBm)

Frequency	Receive Sensitivity (Typ.)			
	Primary	Diversity	SIMO	3GPP (SIMO)
GSM850	-110.62	/	/	-102
EGSM900	-109.34	/	/	-102
DCS1800	-109.26	/	/	-102
PCS1900	-108.80	/	/	-102

WCDMA B1	-112	-112	-114	-106.7
WCDMA B2	-112	-112.5	-113	-106.7
WCDMA B3	-113	-113	-114.5	-106.7
WCDMA B4	-112.5	-113	-114	-106.7
WCDMA B5	-110	-113	-114.5	-106.7
WCDMA B8	-112	-113.5	-114.5	-106.7
WCDMA B9	-113.5	-112.5	-114	-103.7
WCDMA B19	-110	-113.5	-114	-103.7
LTE-FDD B1 (10 MHz)	-98.6	-99.4	-102.12	-96.3
LTE-FDD B2 (10 MHz)	-98.9	-98.8	-101.92	-94.3
LTE-FDD B3 (10 MHz)	-99.4	-99	-102.42	-93.3
LTE-FDD B4 (10 MHz)	-98.4	-99.4	-101.92	-96.3
LTE-FDD B5 (10 MHz)	-99.5	-99.4	-102.62	-94.3
LTE-FDD B7 (10 MHz)	-96.9	-99	-101.42	-94.3
LTE-FDD B8 (10 MHz)	-99.4	-99.8	-102.82	-93.3
LTE-FDD B9(10 MHz)	-99.5	-99.1	-102.44	-95.3
LTE-FDD B11 (10 MHz)	-99.5	-99.4	-102.62	-96.3
LTE-FDD B12 (10 MHz)	-98.9	-100.92	-103.12	-93.3
LTE-FDD B13 (10 MHz)	-99.2	-100.62	-103.3	-93.3
LTE-FDD B17 (10 MHz)	-98.8	-100.92	-103.12	-93.3
LTE-FDD B18 (10 MHz)	-99.5	-100.12	-102.92	-96.3
LTE-FDD B19 (10 MHz)	-99.4	-99.62	-102.52	-96.3
LTE-FDD B20 (10 MHz)	-98.8	-100.62	-102.62	-93.3
LTE-FDD B21 (10 MHz)	-98.82	-99.92	-102.42	-96.3
LTE-FDD B25 (10 MHz)	-98.7	-98.72	-101.72	-93.3

LTE-FDD B26(10 MHz)	-100	-100.12	-103.02	-94.3
LTE-FDD B28 (10 MHz)	-100.1	-100.02	-103.32	-94.8
LTE-FDD B29 (10 MHz)	-99.22	-100.22	-102.72	-93.3
LTE-FDD B30 (10 MHz)	-97.82	-98.82	-101.32	-95.3
LTE-FDD B32 (10 MHz)	-94.82	-96.82	-98.82	-95.3
LTE-TDD B34 (10 MHz)	-97.9	-97.82	-100.92	-96.3
LTE-TDD B38 (10 MHz)	-99.2	-98.12	-101.62	-96.3
LTE-TDD B39 (10 MHz)	-98.3	-99.02	-101.5	-96.3
LTE-TDD B40 (10 MHz)	-98.0	-98.22	-100.92	-96.3
LTE-TDD B41 (10 MHz)	-98.2	-98.32	-101.52	-94.3
LTE-FDD B66 (10 MHz)	-97.7	-99.12	-101.52	-95.8
LTE-FDD B71 (10 MHz)	-100.1	-98.82	-103.12	-93.5

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 37: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV
Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

5.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation. Through-holes will create better heat dissipation performance.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

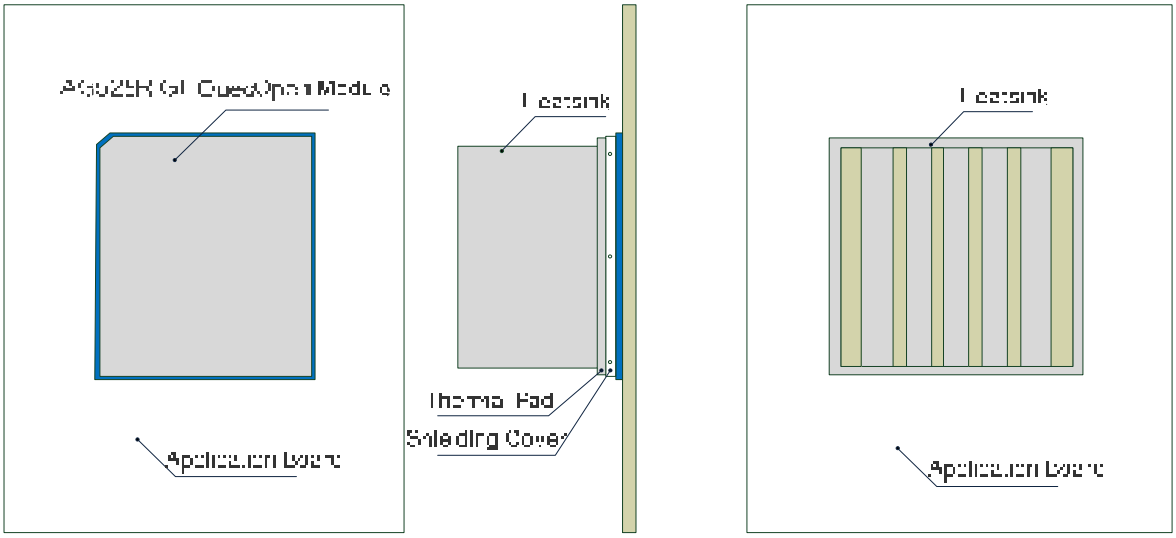

Figure 37: Referenced Heatsink Design (Heatsink at the Top of the Module)

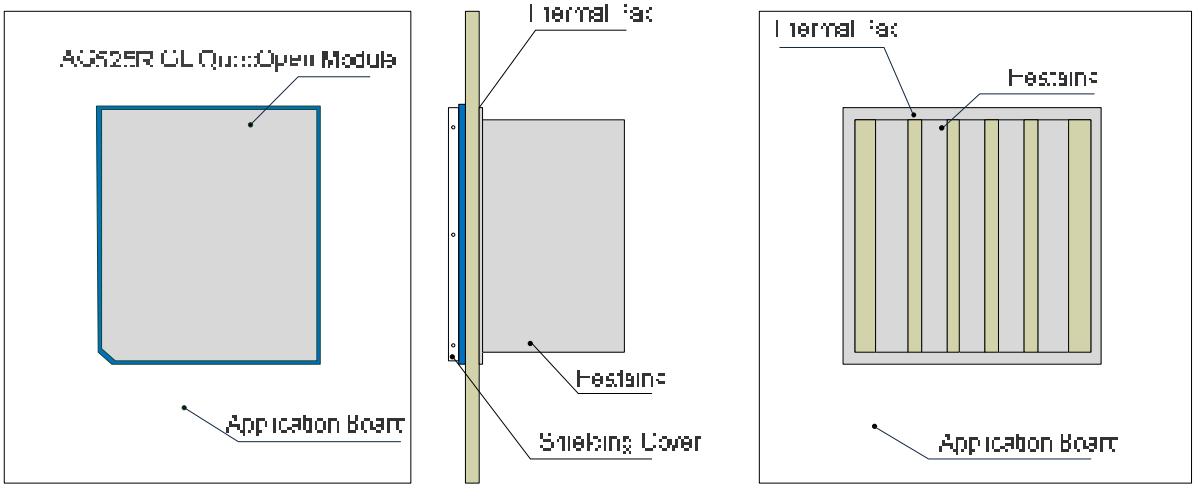

Figure 38: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTES

1. For better performance, the maximum temperature of the internal BB chip should be kept below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power and data rate). When the maximum BB chip temperature reaches or exceeds 118 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 118 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. Customers can execute **AT+QTEMP** command and get the maximum BB chip temperature from the first returned value.
2. For more detailed introduction on thermal design, see ***document [5]***.

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

6.1. Mechanical Dimensions

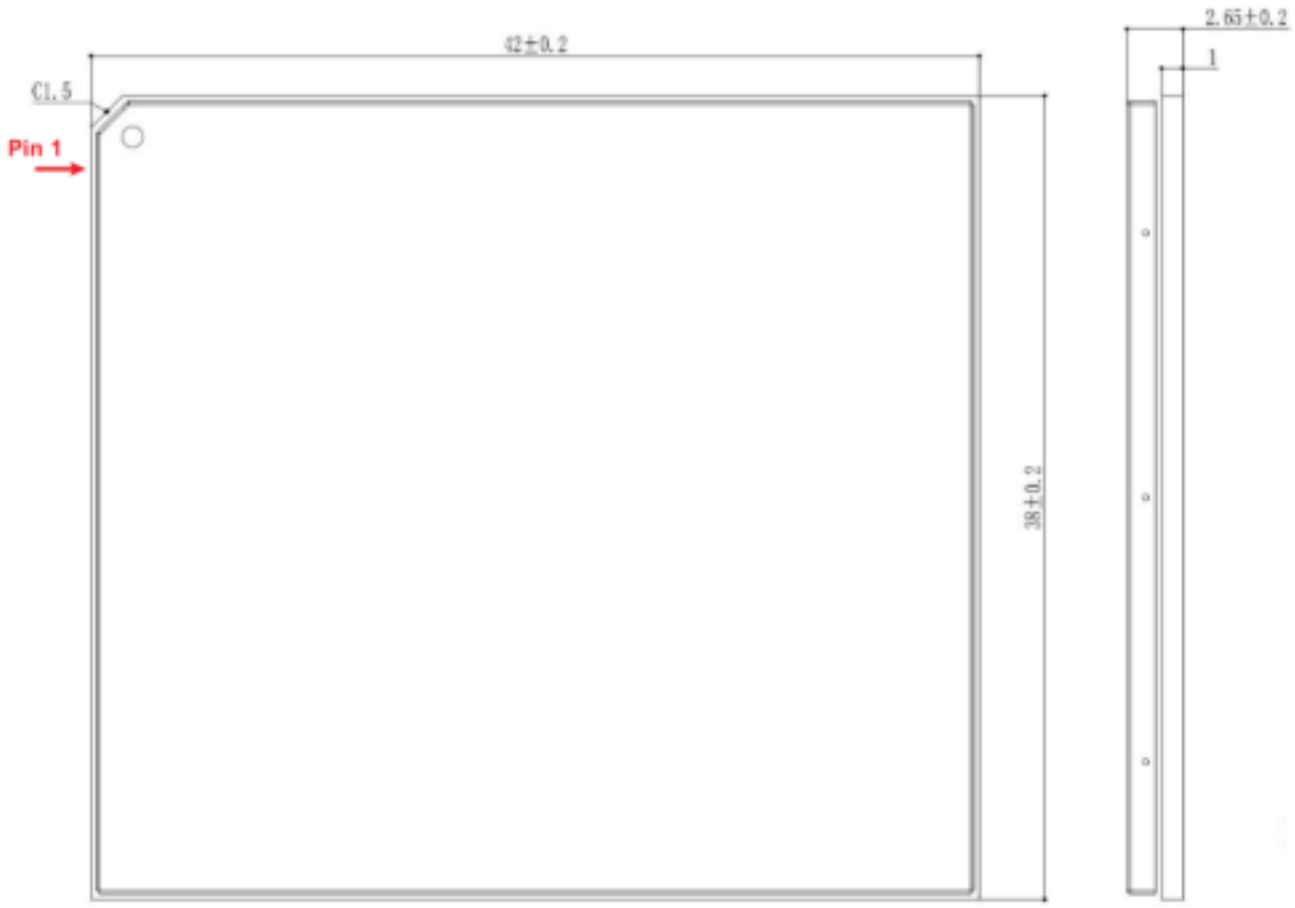

Figure 39: Module Top and Side Dimensions

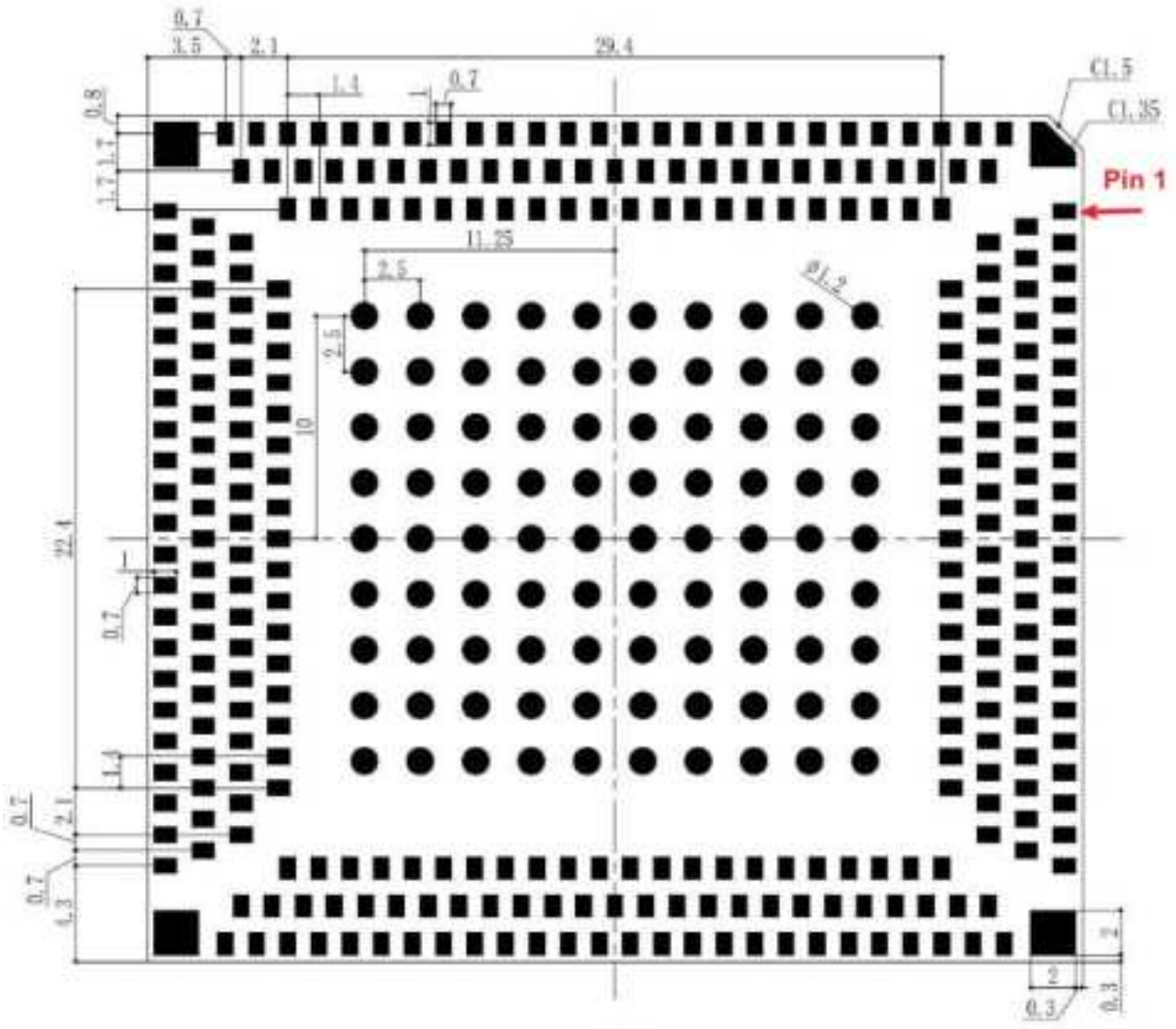

Figure 40: Module Bottom Dimensions (Top View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

6.2. Recommended Footprint

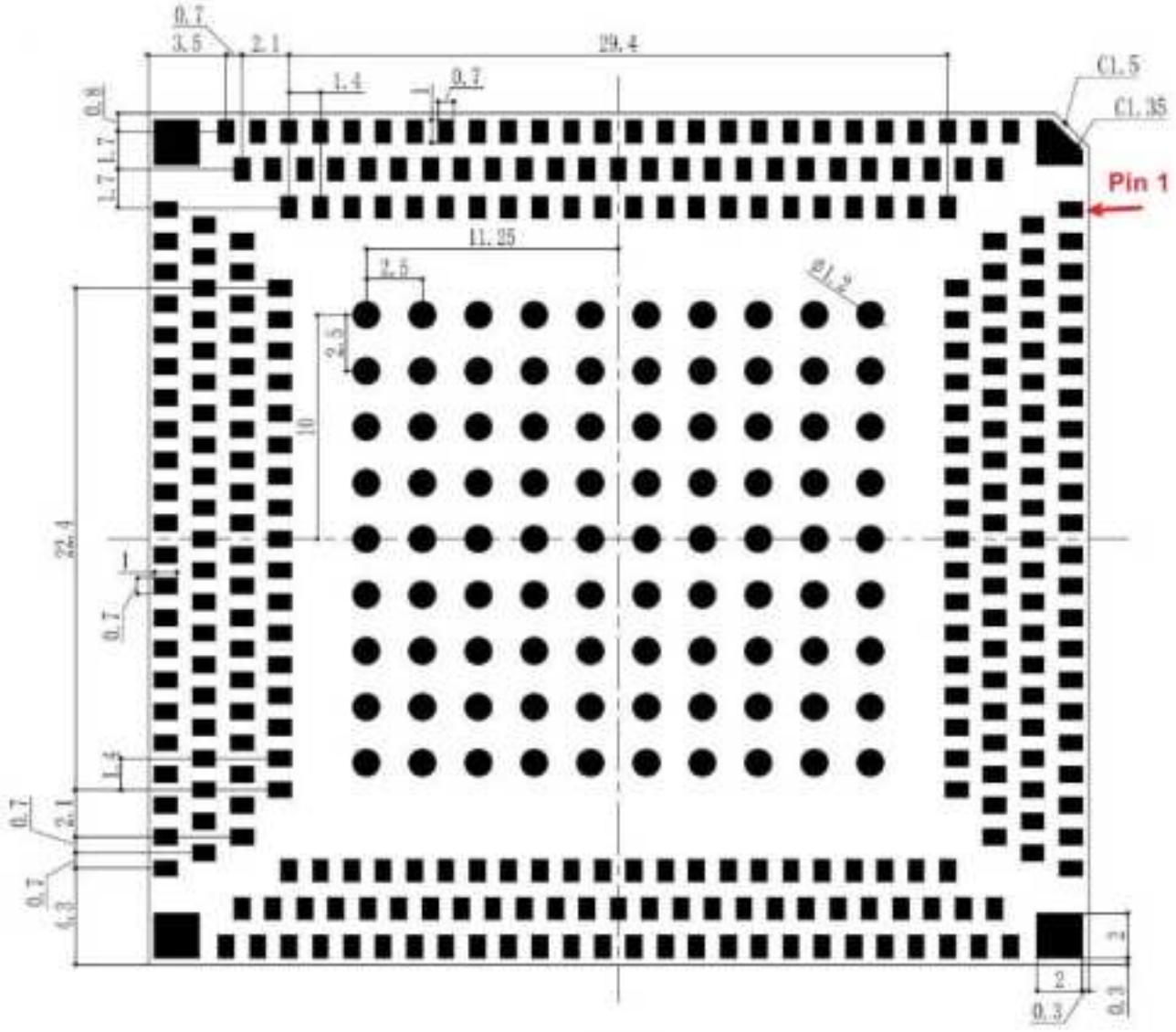

Figure 41: Recommended Footprint (Top View)

NOTE

For convenient maintenance of the module, please keep about 3 mm between the module and other components on the motherboard.

6.3. Top and Bottom Views

Figure 42: Top View of the Module

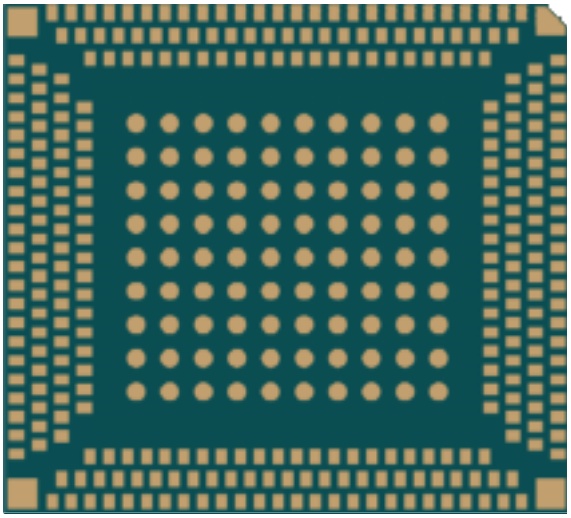

Figure 43: Bottom View of the Module

NOTE

These are renderings of the module. For authentic appearance, see the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 24 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10% (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTE

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [6]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

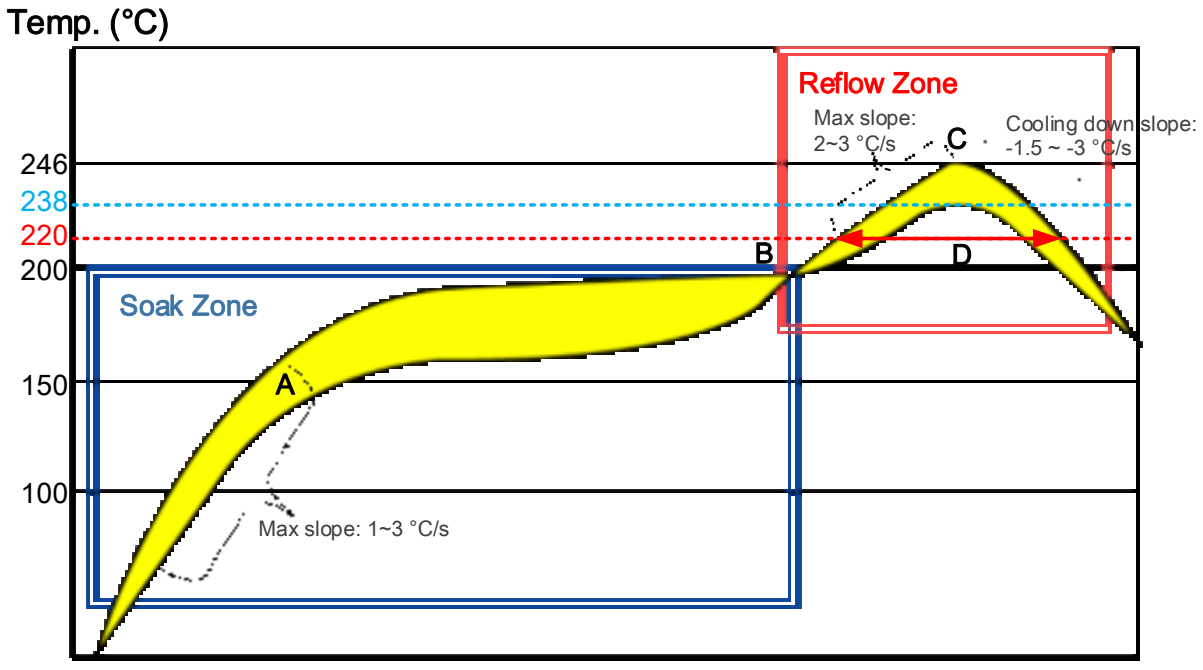

Figure 44: Recommended Reflow Soldering Thermal Profile

Table 38: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150°C and 200°C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220°C)	45–70 s
Max temperature	238–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

7.3. Packaging

The module is packaged in tape and reel carriers. One reel is 10.56 meters long and contains 220 modules. The figures below show the packaging details, measured in mm.

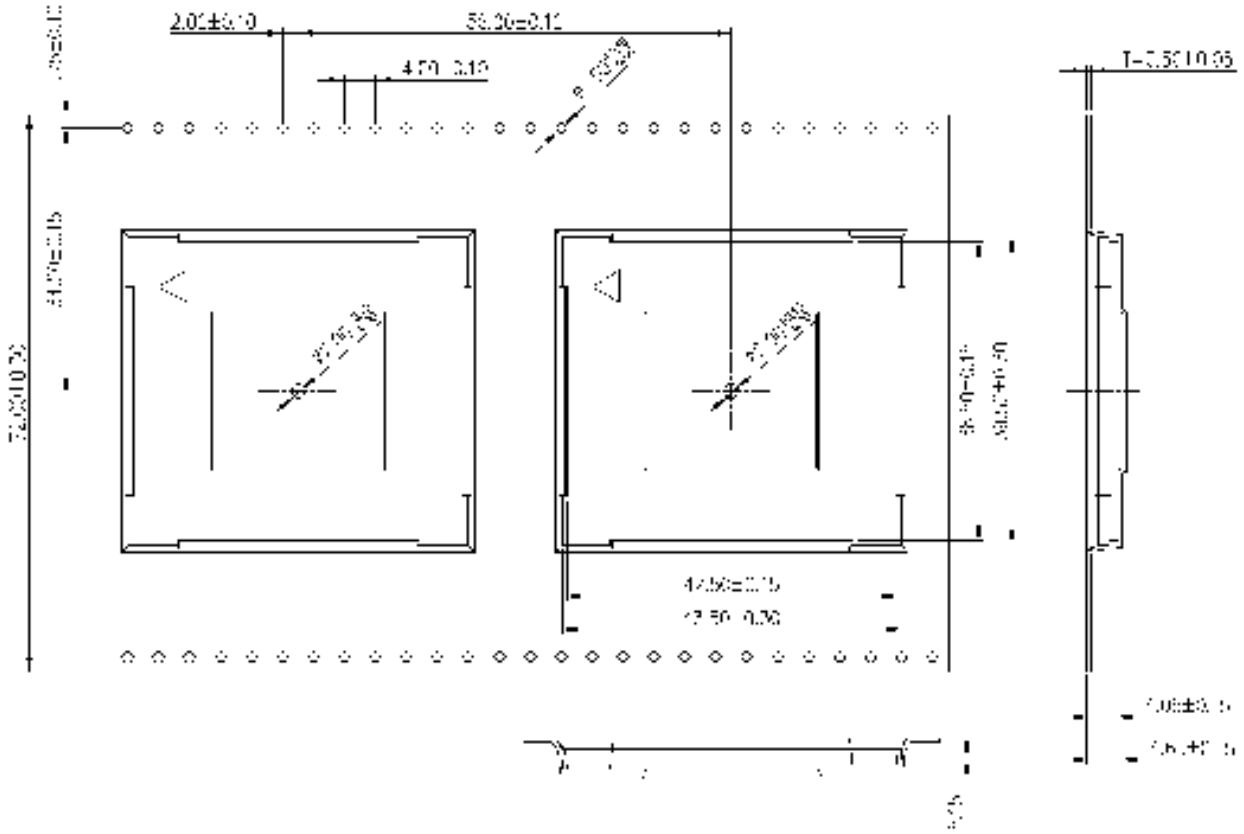

Figure 45: Tape Specifications

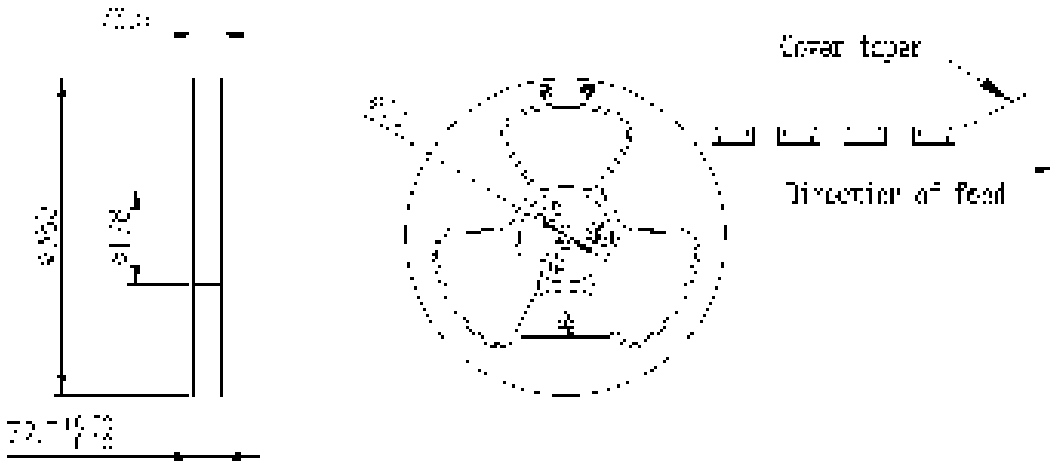

Figure 46: Reel Specifications

8 Appendix A References

Table 39: Related Documents

SN	Document Name	Remark
[1]	Quectel_V2X&5G_EVB_User_Guide	EVB User Guide for Automotive Modules
[2]	Quectel_AG525R-GL_QuecOpen_Developer_Guide	AG525R-GL QuecOpen Developer Guide
[3]	Quectel_AG525R-GL_AT_Commands_Manual	AG525R-GL AT Commands Manual
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal Design Guide for Quectel LTE (LTE Standard/LTE-A/Automotive) modules
[6]	Quectel_Module_Secondary_SMT_Application_Note	Quectel Module Secondary SMT Application Note
[7]	Quectel_AG525R-GL_QuecOpen_Reference_Design	AG525R-GL QuecOpen Reference Design

Table 40: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
API	Application Program Interface
bps	Bits Per Second
BT	Bluetooth
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data

CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
EVDO	Evolution-Data Optimized
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output

MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
Ppp	Peak Pulse Power
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value

Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
V_{RWM}	Reserve Stand-Off Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

9 Appendix B GPRS Coding Schemes

Table 41: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 42: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

11 Appendix D EDGE Modulation and Coding Schemes

Table 43: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05 kbps	18.1 kbps	36.2 kbps
CS-2:	GMSK	/	13.4 kbps	26.8 kbps	53.6 kbps
CS-3:	GMSK	/	15.6 kbps	31.2 kbps	62.4 kbps
CS-4:	GMSK	/	21.4 kbps	42.8 kbps	85.6 kbps
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps