EC600U Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-07-19	Mark YANG/ Frank WANG/ Ailsa WANG	Creation of the document
1.0	2021-08-18	Mark YANG/ Frank WANG/ Ailsa WANG	First official release
1.1	2021-12-20	Manli CHEN	1. Added notes on the use of pins 39, 40, 48–50 (i.e., MAIN_DTR, MAIN_RI, MAIN_DCD, WAKEUP_IN, and AP_READY). 2. Updated the information about USB serial drivers (Chapter 2.2). 3. Updated LCD interface to LCM interface (Chapters 2.2 & 2.3 & 3.1 & 3.3 & 3.14). 4. Updated the formation of matrix keypad interface (5 × 6) (Chapters 2.2 & 3.3 & 3.15). 5. Added note about the I2C interface (Chapter 3.22). 6. Updated the top and bottom views of the module (Chapter 6.3).
1.2	2022-08-26	Denny QIN/ Nathan LIU/ Ryan YI	1. Updated the information about USB serial drivers (Chapter 2.2). 2. Changed the external power supply for the VBAT_RF pin from 2.3 A to 3 A (Table 5). 3. Updated the pin description of HEADMIC_IN_DET (pin 93) (Table 5 & Chapter 3.13). 4. Updated the comment to ADC pins and the relevant note (Table 5 & Chapter 3.17). 5. Updated the external clock scheme for codec IC and added details for PCM interface, timing of PCM interface, as well as relevant notes (Chapter 3.12).

			6. Updated the max slope of reflow zone (Figure 45 & Table 43).
1.3	2023-05-15	Denny QIN/ Aaron ZHANG	1. Added applicable modules EC600U-EC and EC600U-CE. 2. Updated recommended value of the pull-down resistor required in the automatic turn-on scenario and added a note on power-on scenarios (Chapter 3.7.1). 3. Added a note on VBAT voltage requirement when VBAT power supply is disconnected and then restored (Chapter 3.7.2.2). 4. Updated I2C and PCM application reference design and the recommended resistance and capacitance on RC circuits (Chapter 3.12). 5. Updated the Rx sensitivity of EC600U-CN and EC600U-EU (Chapter 5.6). 6. Updated the recommended thickness of stencil for the module; updated the recommended ramp-to-soak, ramp-up, and cool-down slopes and added a related note (Chapter 7.2). 7. Added the module mounting direction (Chapter 7.3.3).
1.4	2023-11-06	Denny QIN/ Nick QIN/ Ryan YI	1. Added the applicable module EC600U-LA. 2. Updated the description of the optional Bluetooth and Wi-Fi Scan functions (Chapters 2.1 & 2.2 & 3.3 & 4). 3. Added notes about the bandwidth of B41 of EC600U-CN and EC600U-EU (Chapters 2.1 & 4.1.2). 4. Updated the information about USB serial drivers (Chapter 2.2). 5. Added emergency call function (Chapter 2.2 & Table 37). 6. Added a comment for USB_ID pin; Updated the power domain of PSM_EXT_INT; Added a note about USB_VBUS connecting to the power supply scenario (Chapter 3.3). 7. Updated the pin description of VBAT_SENSE (Chapters 3.3 & 3.16). 8. Updated the requirements of ESR for bypass capacitors (Chapter 3.6.2). 9. Added the note about PWRKEY (Chapter 3.7.2.2). 10. Added a note about test points for UART interface (Chapter 3.10).

	11. Updated the description of SPI interface (Chapter 3.11). 12. Updated the note for Tx Power (Chapter 5.5).

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1 Introduction

This document defines the EC600U series module and describes its air interface and hardware interface which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up wireless applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

2.1. Frequency Bands and Functions

EC600U series is an LTE Cat 1 module, which supports LTE-FDD, LTE-TDD, and GSM/GPRS network data connection. It provides voice functionality to meet your specific application demands as well as Bluetooth and Wi-Fi Scan [1] functions. EC600U series includes five models: EC600U-CN, EC600U-EU, EC600U-EC, EC600U-CE and EC600U-LA, from which you can choose according to the region or the operator. The following table shows the frequency bands of the module.

Table 2: Frequency Bands of EC600U Series

Mode	EC600U-CN	EC600U-EU	EC600U-EC	EC600U-CE	EC600U-LA
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8 /B20/B28	B1/B3/B5/B7/ B8/B20	B1/B3/B5/B8	B2/B3/B4/B5/ B7/B8/B28/B66
LTE-TDD	B34/B38/B39/ B40/B41	B38/B40/B41	B40	B38/B40/B41	-
GSM	-	GSM850/ EGSM900/ DCS1800/ PCS1900	GSM850/ EGSM900/ DCS1800/ PCS1900	EGSM900/ DCS1800	GSM850/ EGSM900/ DCS1800/ PCS1900
Bluetooth and Wi-Fi Scan [1]	2.4 GHz	2.4 GHz	-	2.4 GHz	-

NOTE

B41 of EC600U-CN and EC600U-EU only supports 140 MHz (2535–2675 MHz).

With a compact profile of 22.9 mm × 23.9 mm × 2.4 mm.EC600U series is an SMD type module which can be embedded into applications through its 148 pins, including 76 LCC pins and 72 LGA pins.

[1] EC600U-CN, EC600U-EU and EC600U-CE support Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.

2.2. Key Features

The following table describes the detailed features of EC600U series module.

Table 3: Key Features

Features	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands ● Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	● Supports up to Cat 1 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Max. transmission data rates: LTE-FDD: 10 Mbps (DL) /5 Mbps (UL) LTE-TDD: 8.96 Mbps (DL) /3.1 Mbps (UL) ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations
GSM Features (Only EC600U-CN not support)	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. transmission data rates: 85.6 kbps (DL) /85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/ FTPS/SSL/FILE/MQTT/MMS protocols ● Supports PAP and CHAP protocols, which are usually used for PPP connection
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
(U)SIM Interfaces	Supports USIM/SIM card: 1.8/3.0 V
USB Interface	● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, and firmware upgrade ● Supports USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–6.5,

	Android 4.x–13.x, etc.
UART Interfaces	● **Main UART:** Used for AT command communication and data transmission Baud rates: up to 921600 bps, 115200 bps by default Supports RTS and CTS hardware flow control ● **Debug UART:** Used for AP log output Baud rate: 921600 bps Cannot be used as a general-purpose UART ● **Auxiliary UART:** Baud rates: up to 921600 bps, 115200 bps by default Supports RTS and CTS hardware flow control
SPI	Supports only master mode
I2C Interface	Supports one I2C interface
PCM Interface	Supports one digital audio interface
Analog Audio Features	● Supports two analog audio input and three analog audio output channels ● HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
LCM Interface	Supports LCM interface with SPI mode
Matrix Keypad Interface	Supports 5 × 6 matrix keypad
ADC Interface	Supports four ADC interfaces
Network Status Indication	Two pins NET_MODE and NET_STATUS to indicate network status
USB_BOOT Interface	Supports one download control interface
Camera Interface	● Provides one camera interface supporting cameras up to 0.3 MP; I/O pins only support 1.8 V ● Supports the 2-data-line transmission of SPI
Antenna Interface	● Main antenna interface (ANT_MAIN) ● Bluetooth/Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) ● 50 Ω characteristic impedance
AT Commands	Compliant with *3GPP TS 27.007*, *27.005* and Quectel enhanced AT commands
Position Fixing	Supports Wi-Fi Scan [2]
Physical Characteristics	● Size: (22.9 ±0.15) mm × (23.9 ±0.15) mm × (2.4 ±0.2) mm ● Weight: approx. 2.6 g

[2] Only EC600U-CN, EC600U-EU and EC600U-CE support Wi-Fi Scan.

Temperature Range	● Operating temperature range: -35 °C to +75 °C [3] ● Extended temperature range: -40 °C to +85 °C [4] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Via USB interface or FOTA
RoHS	All hardware components are fully compliant with EU RoHS Directive

2.3. EVB Kit

Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

[3] Within this range, the module's performance complies with 3GPP requirements.
[4] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's performance will comply with 3GPP requirements again.

3 Application Interfaces

3.1. General Description

EC600U series module is equipped with 76 LCC pins and 72 LGA pins that can be connected to cellular application platform. The following interfaces are described in detail in subsequent chapters.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI
- I2C and PCM interfaces
- Analog audio interfaces
- LCM interface
- Matrix keypad interface
- Charging control interface*
- ADC interfaces
- PSM interface
- Network status indication
- USB_BOOT interface
- Camera interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

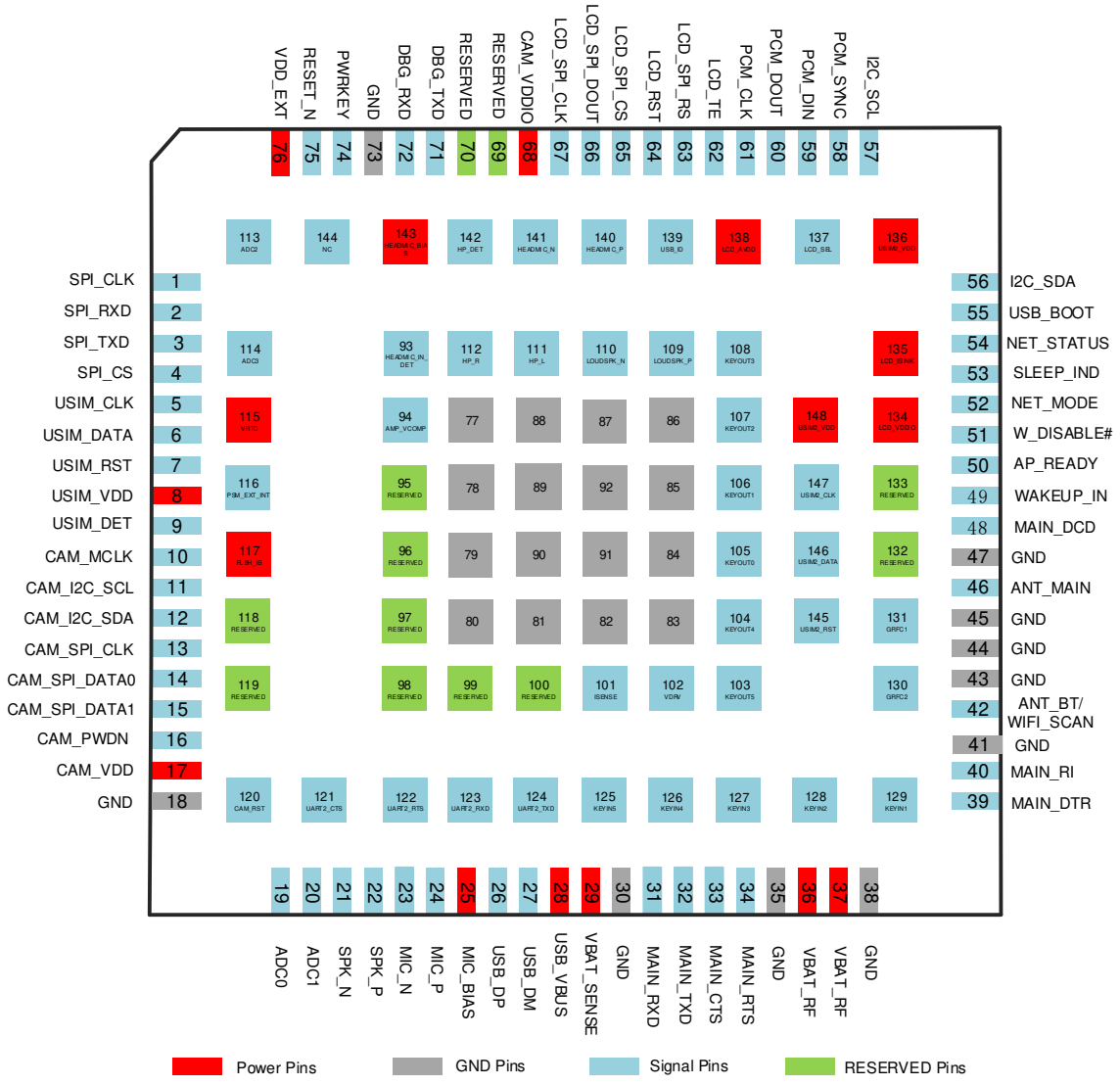


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep NC and RESERVED pins unconnected, and all GND pins should be connected to ground.
2. If the download function is not used, do not pull USB_BOOT to high level before turning on the module.
3. Before turning on the module, do not pull up KEYIN1 to high level.
4. There are hardware conflicts between pins 51–53 and 145–147. If pins 145–147 of (U)SIM2

interface are used, pins 51–53 must be kept unconnected; if pins 51–53 are used, that is, the (U)SIM2 interface is not used, pins 145–147 must be kept unconnected.

5. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for using dual (U)SIM operation. Please consult Quectel Technical Support for more information about how to use (U)SIM2.
6. When using pins 39, 40, 48–50, please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

3.3. Pin Description

The following tables show the pin definition and description of EC600U series module.

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current, etc.

Table 5: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_RF	36, 37	PI	Power supply for module's baseband part and RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of at least 3 A. A test point is recommended to be reserved.
GND	18, 30, 35, 38, 41, 43–45, 47, 73, 77–92				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	76	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Add a 2.2 μF capacitor and TVS components if used. A test point is recommended to be reserved.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	75	DI	Reset the module	V_{IL}max = 0.5 V	VBAT power domain. Active low. A test point is recommended to be reserved if unused.
PWRKEY	74	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain. A test point is recommended to be reserved.
Network Status Indication					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NET_MODE	52	DO	Indicate whether the module has registered on LTE network	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep them open.
NET_STATUS	54	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	26	AIO	USB 2.0 differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	27	AIO	USB 2.0 differential data (-)		
USB_VBUS	28	AI	USB connection detection	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typ. 5.0 V. If unused, keep it open. A test point must be reserved.
USB_ID*	139	DI	Reserved		Internally pulled up to 1.8 V by default. Keep it open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	9	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM_VDD	8	PO	(U)SIM card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported and can be identified by the module automatically.

USIM_DATA	6	DIO	(U)SIM card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	5	DO	(U)SIM card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_RST	7	DO	(U)SIM card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_VDD	136, 148	PO	(U)SIM2 card power supply	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported and can be identified by the module automatically. Use pin 148 as the power supply and keep pin 136 unconnected.
USIM2_DATA	146	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V	

				V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	147	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	145	DO	(U)SIM2 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	33	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	34	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_TXD	32	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
MAIN_RXD	31	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_DCD	48	DO	Main UART data carrier detection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_DTR	39	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	

				V_{IH}max = 2.0 V	
MAIN_RI	40	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	72	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Test points must be reserved.
DBG_TXD	71	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_RXD	123	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
UART2_TXD	124	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART2_CTS	121	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
UART2_RTS	122	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to MCU's RTS. 1.8 V power domain. Output CP log. Only 8 Mbps baud rate is supported. A test point must be reserved.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC3	114	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC2	113	AI			
ADC1	20	AI			
ADC0	19	AI			
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LOUDSPK_P	109	AO	Loudspeaker differential output (+)		With an internal PA. When configured as Class AB, the maximum drive power is 500 mW at 8 Ω load; when configured as Class D, the maximum drive power is 800 mW at 8 Ω load. If unused, keep them open.
LOUDSPK_N	110	AO	Loudspeaker differential output (-)		
AMP_VCOMP	94		Headset dedicated ground		It should be traced between the left and right channels, and connected to the GND of the headset jack, and then directly connected to the main GND layer. If unused, keep it open.
HP_L	111	AO	Headset left channel output		If unused, keep them open.
HP_R	112	AO	Headset right channel output		
HEADMIC_P	140	AI	Headset analog differential input (+)		
HEADMIC_N	141	AI	Headset analog differential input (-)		

HEADMIC_BIAS	143	PO	Bias voltage output for headset	Vo = 2.2–3.0 V Vnom = 2.6 V	
HP_DET	142	DI	Headset hot-plug detection		
HEADMIC_IN_DET	93	AI	Headset microphone and button detect		
SPK_P	22	AO	Analog audio differential output (+)		Used for earpiece interface. Without internal PA. The maximum drive power is 50 mW at 32 Ω load. If the output power cannot meet the demand, this pin can be used to drive an external PA. If unused, keep them open.
SPK_N	21	AO	Analog audio differential output (-)		
MIC_BIAS	25	PO	Bias voltage output for microphone	Vo = 2.2–3.0 V Vnom = 2.2 V	If unused, keep them open.
MIC_P	24	AI	Microphone analog input (+)		
MIC_N	23	AI	Microphone analog input (-)		
I2C and PCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	57	OD	I2C serial clock		Pull each of them up to 1.8 V with an external resistor. If unused, keep them open.
I2C_SDA	56	OD	I2C serial data		
PCM_DIN	59	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open. Only support slave mode.
PCM_DOUT	60	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	58	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	

				V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
PCM_CLK	61	DI	PCM clock	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	4	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open. Only support master mode.
SPI_TXD	3	DO	SPI master mode output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI_RXD	2	DI	SPI master mode input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_CLK	1	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_TE	62	DI	LCD tearing effect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
LCD_RST	64	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
LCD_SEL	137	DO	Reserved	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_CS	65	DO	LCD SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_CLK	67	DO	LCD SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_RS	63	DO	LCD SPI register select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SPI_DOUT	66	DIO	LCD SPI data output	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V	

				V_{OH}min = 1.35 V	
LCD_ISINK	135	PI	Sink current input; Backlight adjustment	Imax = 200 mA	It is driven by the current sink method and connected to the backlight cathode; the brightness can be adjusted with current control. If unused, keep it open.
LCD_VDDIO	134	PO	LCD digital power	Vnom = 1.8 V	LCD power supply. If unused, keep them open.
LCD_AVDD	138	PO	LCD analog power	Vnom = 3.0 V	
Matrix Keypad Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
KEYIN1	129	DI	Matrix keypad input 1		1.8 V power domain. If unused, keep them open.
KEYIN2	128	DI	Matrix keypad input 2		
KEYIN3	127	DI	Matrix keypad input 3		
KEYIN4	126	DI	Matrix keypad input 4		
KEYIN5	125	DI	Matrix keypad input 5		
KEYOUT0	105	DO	Matrix keypad output 0		
KEYOUT1	106	DO	Matrix keypad output 1		
KEYOUT2	107	DO	Matrix keypad output 2		
KEYOUT3	108	DO	Matrix keypad output 3		
KEYOUT4	104	DO	Matrix keypad output 4		
KEYOUT5	103	DO	Matrix keypad output 5		
Antenna Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_BT/ WIFI_SCAN [5]	42	AIO	The shared antenna interface for Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	46	AIO	Main antenna		50 Ω characteristic impedance.
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	55	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved. A test point is recommended to be reserved.
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	10	DO	Master clock of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
CAM_I2C_SCL	11	OD	I2C clock of camera		Pull each of them up to 1.8 V power domain with an external resistor.
CAM_I2C_SDA	12	OD	I2C data of camera		

[5] Only EC600U-CN, EC600U-EC and EC600U-CE support Bluetooth and Wi-Fi Scan functions.

					If unused, keep them open.
CAM_SPI_CLK	13	DI	SPI clock of camera	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	14	DI	SPI data0 of camera	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
CAM_SPI_DATA1	15	DI	SPI data1 of camera		
CAM_PWDN	16	DO	Power down of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
CAM_RST	120	DO	Reset of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
CAM_VDD	17	PO	Analog power supply of camera	Vnom = 2.8 V	Power supply of camera. If unused, keep them open.
CAM_VDDIO	68	PO	Digital power supply of camera	Vnom = 1.8 V	
Charging Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ISENSE	101	AI	Charging current detection		If unused, keep it open.
VBAT_SENSE	29	AI	Battery voltage and charging current (combines with ISENSE) detection		Regardless of whether the charging function is used, this pin must be connected to the VBAT power supply, otherwise the module will not be turned on normally.
USB_VBUS	28	AI	Charging voltage detect	Vmax = 5.25 V Vmin = 4.5 V Vnom = 5.0 V	Typ. 5.0 V. If unused, keep it open. A test point must be reserved.
VDRV	102	AO	Charging control pin		Used for driving the MOSFET in the external charging circuit to adjust the charging current. If unused, keep it open.

Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SLEEP_IND	53	DO	Indicate the module's sleep mode	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WAKEUP_IN	49	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
AP_READY	50	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
W_DISABLE#	51	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
VRTC*	115	PI	Power supply for RTC	Vnom = 3 V V_O = 2.8–3.2 V	If unused, keep it open.
PSM_EXT_INT	116	DI	External interrupt pin; Wake up the module from PSM when being pulled high externally		1.8 V power domain. Active high. If unused, keep it open.
FLSH_IB*	117	PI	Current sink input		If unused, keep it open.
GRFC2*	130	DO	Generic RF Controller		
GRFC1*	131	DO	Generic RF Controller		

RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	69, 70, 95–100, 118, 119, 132, 133, 136	Keep them open.

NC Pin

Pin Name	Pin No.	Comment
NC	144	Keep it open.

NOTE

1. There are hardware conflicts between pins 51–53 and 145–147. If pins 145–147 of (U)SIM2 interface are used, pins 51–53 must be kept unconnected; if pins 51–53 are used, that is, the (U)SIM2 interface is not used, pins 145–147 must be kept unconnected.
2. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for using dual (U)SIM operation. Please consult Quectel Technical Support for more information about how to use (U)SIM2.
3. When using pins 39, 40, 48–50, please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.
4. If the USB_VBUS is connected to the power supply and the VBAT is powered down, the USB_VBUS must be connected in series with a 1 kΩ resistor.

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred to in the following chapters.

Table 6: Overview of Operating Modes

Modes	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network, and is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or pulling down W_DISABLE# pin can set the module to airplane mode where the RF function is invalid.	
Sleep Mode	In this mode, the power consumption of the module is reduced to an ultra-low level. The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from the network normally.	

PSM	The power consumption of the module will be reduced to an extremely low level, and it is impossible to send AT commands to the module, but the module can still receive paging packets from the base station, and can be woken up to work.
Power Down Mode	In this mode, the module's power supply is cut off by its power management unit (PMU). The software is inactive and the serial interfaces are inaccessible, while the VBAT_RF pins are still powered.

NOTE

For more details about **AT+CFUN**, see ***document*** *错误!未找到引用源。*.

3.5. Power Saving

3.5.1. Sleep Mode

The module is able to reduce its power consumption to a an ultra-low level in the sleep mode. The following chapters describe power saving procedures of the module.

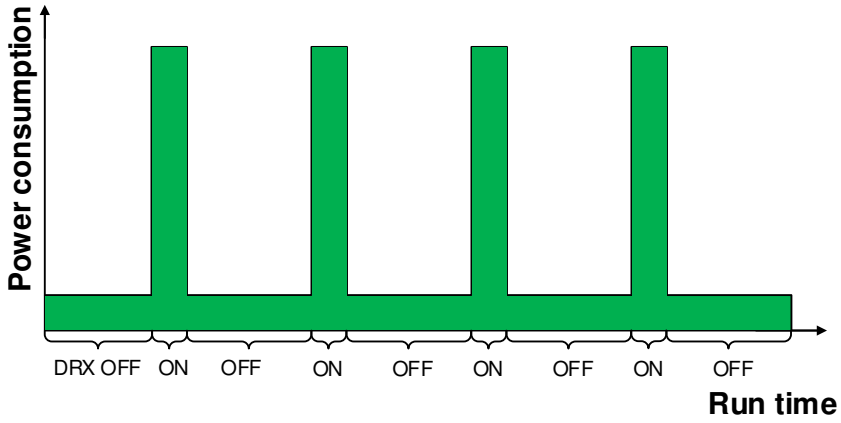


Figure 2: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.5.1.1. UART Application Scenario

If the MCU communicates with the module via UART interface, the following preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the MCU.

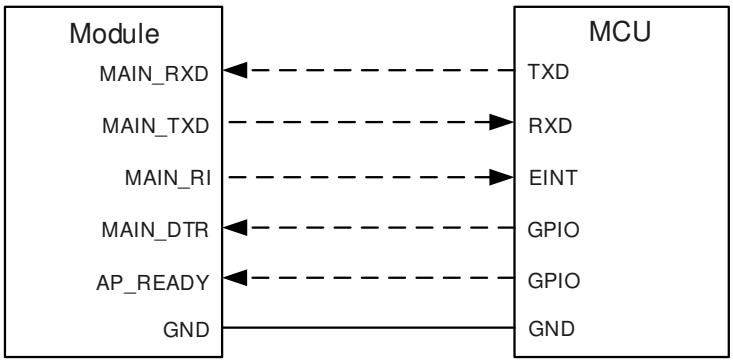


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR low will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 3.19*** for details about MAIN_RI behaviors.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

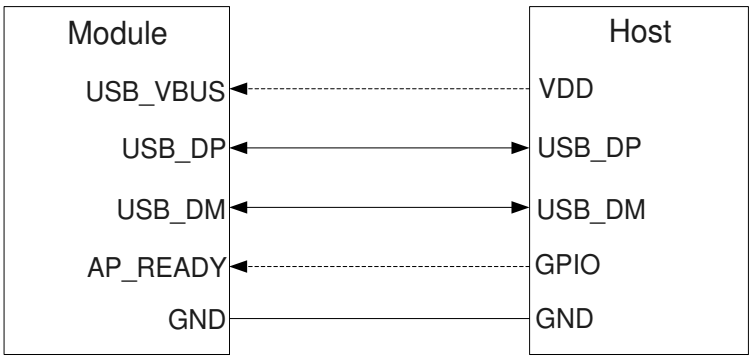


Figure 4: Sleep Mode Application with USB Remote Wakeup

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the module sends remote wake-up signals to wake up the host via the USB bus.

3.5.1.3. USB Application with USB Suspend/Resume and MAIN_RI Wakeup Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the MAIN_RI signal is needed to wake up the host.

In this case, three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

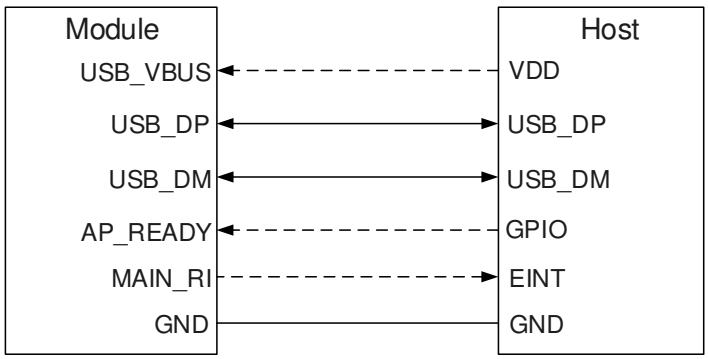


Figure 5: Sleep Mode Application with MAIN_RI

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the URC will trigger the behaviors of MAIN_RI pin. See ***Chapter 3.19*** for details about MAIN_RI behaviors.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to make the module enter into sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

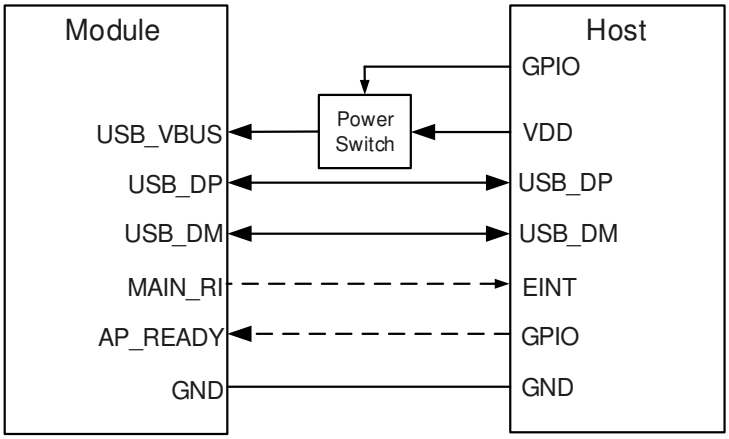


Figure 6: Sleep Mode Application without Suspend Function

You can wake up the module by switching on the power switch to supply power to USB_VBUS.

NOTE

1. Pay attention to the level matching shown in the dotted connection signal between the module and the MCU/host in ***Chapter 3.5.1***.
2. USB suspend is supported on the Linux system but not on the Windows system.
3. When using MAIN_DTR and MAIN_RI (pins 39 and 40), please note that the two pins will have a period of variable level state (not controllable by software) after the module is turned on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.
4. For more details about the AT commands, see ***document [3]***.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. You can set this mode via the following ways.

Hardware:

The pin W_DISABLE# is pulled up by default. Its control function for airplane mode, which is disabled by default in software, can be enabled through **AT+QCFG="airplanecontrol",1**. When such a control function is enabled, you can drive it to low level to make the module enter airplane mode.

Software:

AT+CFUN=<fun> provides the choice of functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (both RF and (U)SIM card functions are disabled).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** airplane mode (RF function is disabled).

NOTE

For more details about AT commands, see ***document*** *错误!未找到引用源。*.

3.5.3. PSM

The module supports power saving mode (PSM). It enters the PSM through the following AT commands when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling up the PSM_EXT_INT pin externally or setting the timer by software will enable the module to exit PSM.

Table 7: Pin Definition of PSM Interface

Pin Name	Pin No.	I/O	Description	Comment
PSM_EXT_INT	116	DI	External interrupt pin; Wake up the module from PSM when being pulled high externally	Active high. If unused, keep it open.

A reference circuit is shown in the following figure.

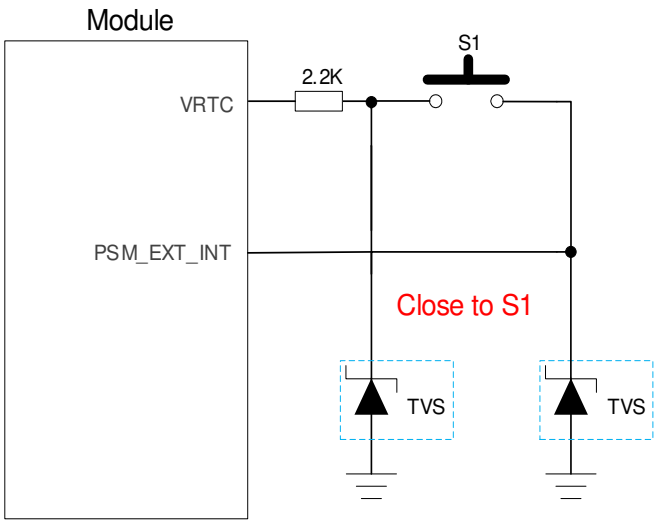


Figure 7: Reference Circuit of Waking Up Module from PSM

NOTE

For more details about AT commands, see ***document*** *错误!未找到引用源。* and ***document [3]***.

3.6. Power Supply

3.6.1. Power Supply Pins

The power supply pins of the module are used to connect an external power, supplying power to the RF and baseband circuits of the module.

Table 8: Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_RF	36, 37	PI	Power supply for the module's baseband part and RF part	3.3	3.8	4.3	V
VBAT_SENSE	29	AI	Battery voltage and charging current (combines with ISENSE) detection	3.3	3.8	4.3	V
GND	18, 30, 35, 38, 41, 43–45, 47, 73, 77–92						

NOTE

Whether or not the charging function is used, VBAT_SENSE must be connected to the VBAT power supply, otherwise the module will not be turned on normally.

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure the input voltage never drops below 3.3 V. The following figure shows the voltage drop during burst transmission.

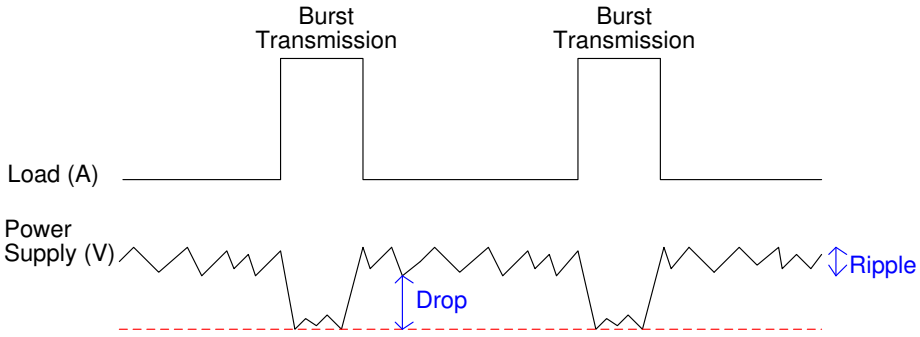


Figure 8: Power Supply Limits during Burst Transmission

To decrease the voltage drop, use bypass capacitors of about 100 μF with low ESR (ESR ≤ 0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to their ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_SENSE and VBAT_RF pins. When the external power supply is connected to the module, VBAT_SENSE and VBAT_RF need to be routed in star structure. The width of the VBAT_RF trace should not be less than 2.5 mm. When VBAT_SENSE is used as a power supply pin (that is, charging function is not used), its trace width should not be less than 1 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to avoid the surge, use a TVS of which reverse working voltage is 4.7 V and peak pulse power is up to 2550 W. The following figure shows the reference circuit with and without charging function.

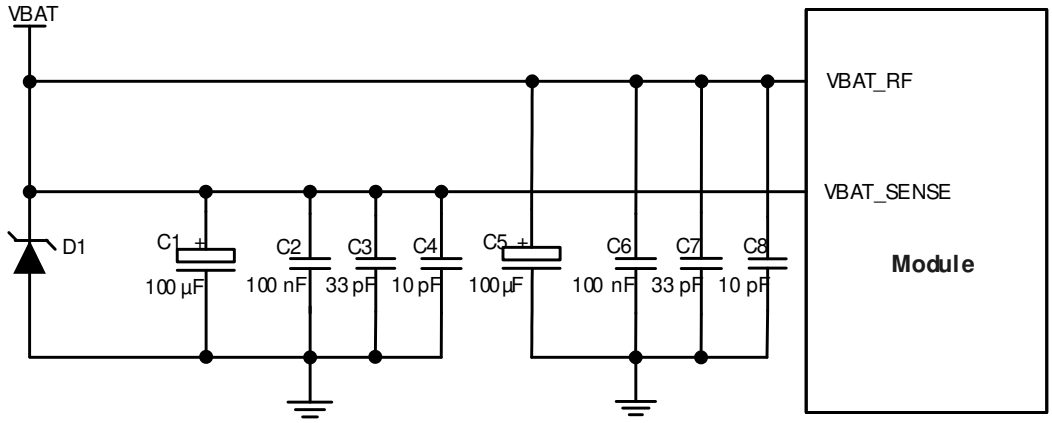


Figure 9: Power Supply (without Charging Function)

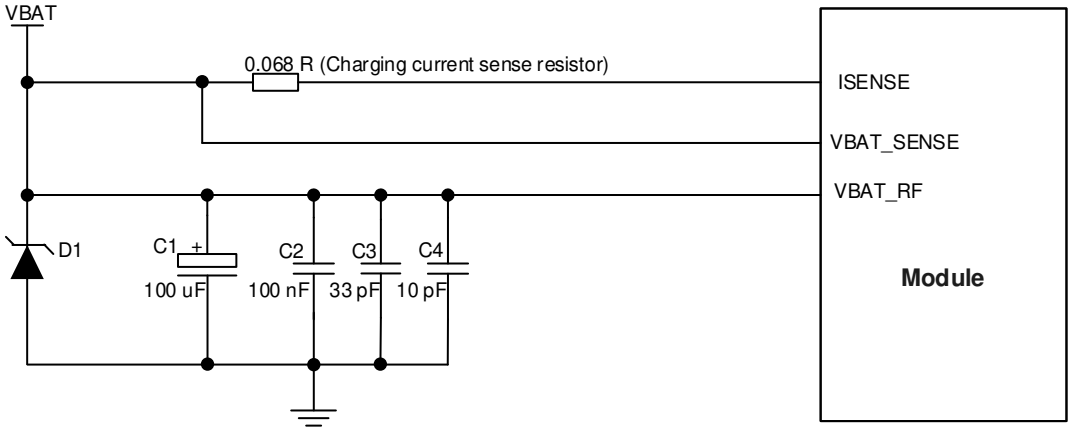


Figure 10: Power Supply (with Charging Function)

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current of 2.0 A at least for EC600U-CN and 3.0 A at least for EC600U-EU, EC600U-EC, EC600U-CE and EC600U-LA. If the voltage drop between the input and output is not too high, use an LDO to supply power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), use a buck converter as the power supply.

The following figure shows a reference design for +5 V input power source.

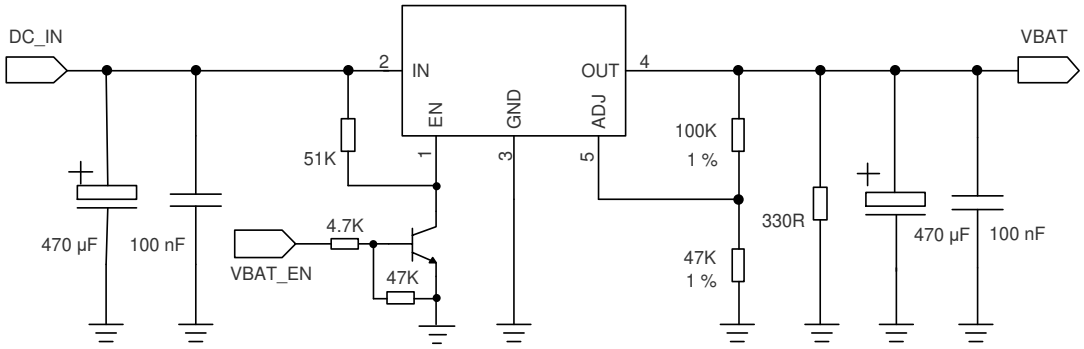


Figure 11: Reference Circuit of Power Supply

3.7. Turn On/Turn Off/Reset

3.7.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	74	DI	Turn on/off the module	VBAT power domain. A test point is recommended to be reserved.

When the module is in power down mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

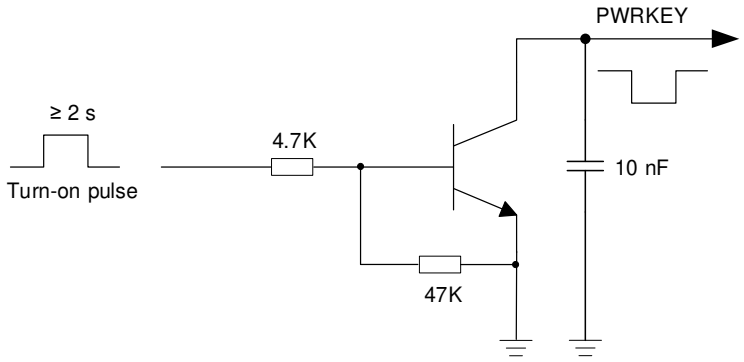


Figure 12: Turning On the Module Using Driving Circuit

If the module needs to be turned on automatically when powered up while turn-off function is not needed, PWRKEY can be driven low directly to ground with a resistor of less than 1 kΩ.

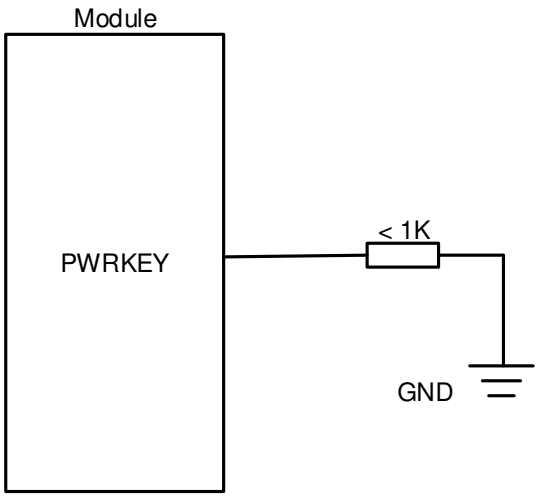


Figure 13: Reference Design of Automatic Turn-on upon Power-up

Another way to control the PWRKEY is using a button directly. When you are pressing the button, electrostatic strike may be generated from finger. Therefore, you must place a TVS nearby the button for ESD protection. A reference circuit is shown in the following figure.

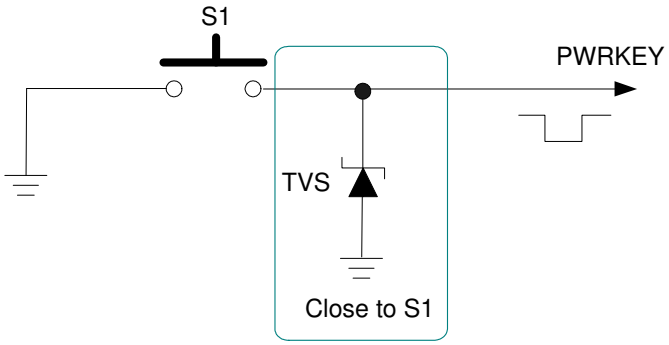


Figure 14: Turning On the Module Using Button

The power-up scenario is illustrated in the following figure.

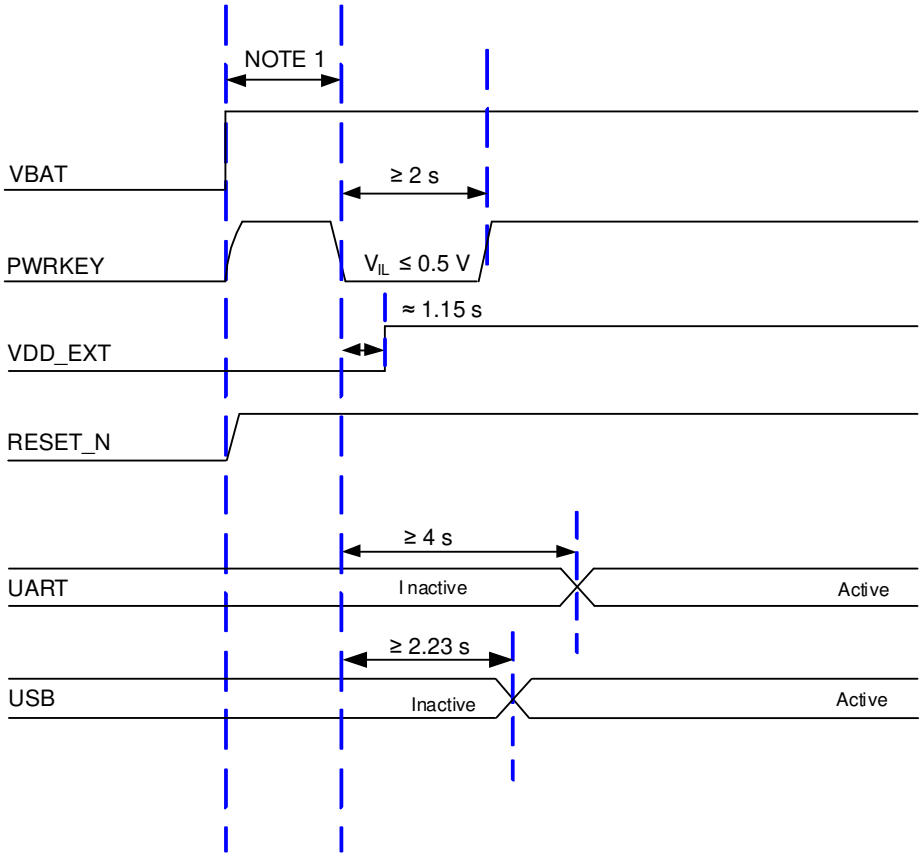


Figure 15: Power-up Timing

NOTE

1. Make sure that the VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a resistor of less than 1 kΩ, if the module needs to be turned on automatically and turn-off is not needed.
3. Pay attention to the following two turn-on scenarios:
   - In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is turned on later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered on stably for at least 2 s before PWRKEY is pulled down;
   - In the scenario where VBAT is turned on first (or has always been powered on), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.

3.7.2. Turn Off

The following methods can be used to turn off the module:

- Use the PWRKEY pin.
- Use **AT+QPOWD**.

3.7.2.1. Turn Off with PWRKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY. After this, the module executes power-down procedure. The power-down scenario is illustrated in the following figure.

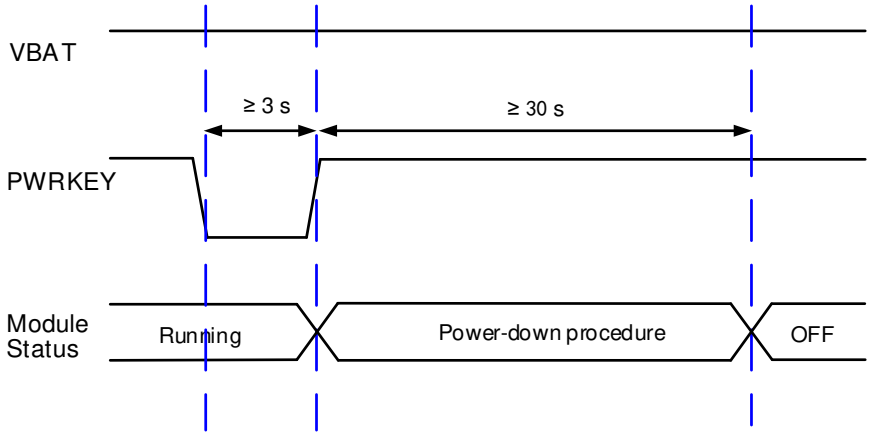


Figure 16: Power-down Timing

3.7.2.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When the PWRKEY pin has been kept pulled down directly to GND, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and turn on the module again. When the PWRKEY pin is long grounded, the VRTC pin is not allowed to connect to the power supply. Therefore, we recommend that you can use a control circuit to drive the PWEKEY high/low to turn on/off the module instead of

keeping the PWRKEY connected to GND.

3. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.
4. If you disconnect the VBAT power supply, ensure that the VBAT pins voltage is less than 0.5 V before powering it on again.

3.7.3. Reset

The RESET_N pin can be used to reset the module. You can reset the module by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	75	DI	Reset the module	VBAT power domain Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. You can use an open drain/collector driver or button to control the RESET_N.

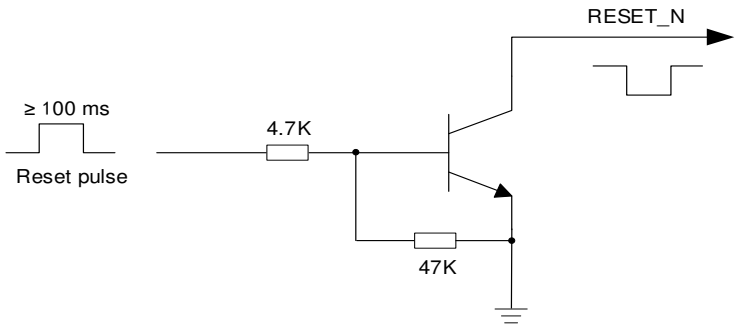


Figure 17: Reference Circuit of RESET_N by Using Driving Circuit

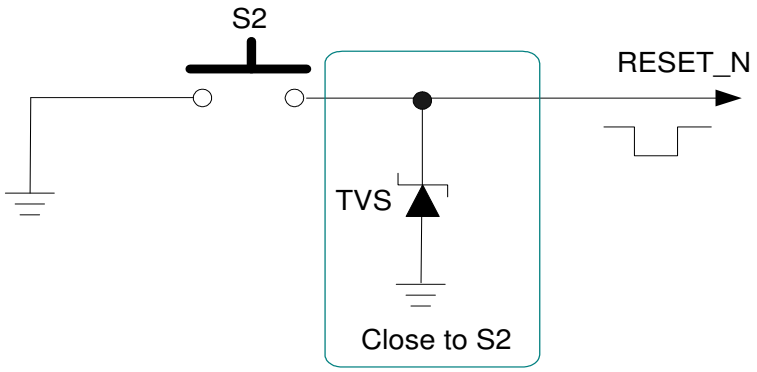


Figure 18: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

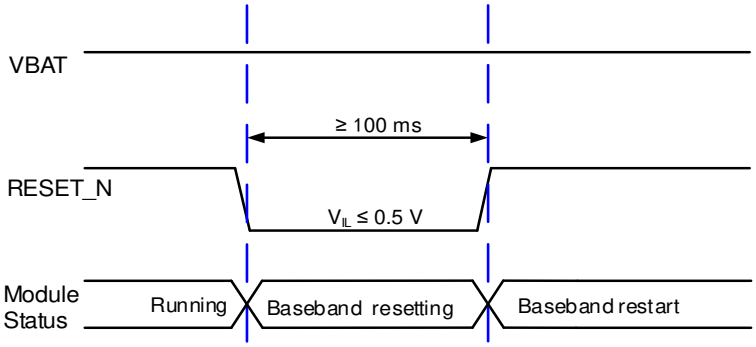


Figure 19: Timing of Resetting the Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when you fail to turn off the module with the **AT+QPOWD** or PWRKEY pin. For more details about AT command, see ***document*** *错误!未找到引用源。*.

3.8. (U)SIM Interfaces

The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	9	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_VDD	8	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	6	DIO	(U)SIM card data	
USIM_CLK	5	DO	(U)SIM card clock	
USIM_RST	7	DO	(U)SIM card reset	
USIM2_VDD	136, 148	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. It is recommended to use pin 148 as power supply and keep pin 136 unconnected.
USIM2_DATA	146	DIO	(U)SIM2 card data	
USIM2_CLK	147	DO	(U)SIM2 card clock	
USIM2_RST	145	DO	(U)SIM2 card reset	

The module supports (U)SIM card hot-plug via the USIM_DET pin and both high- and low-level detections are supported. By default, the function is disabled, and see **AT+QSIMDET** in ***document [2]*** for more details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

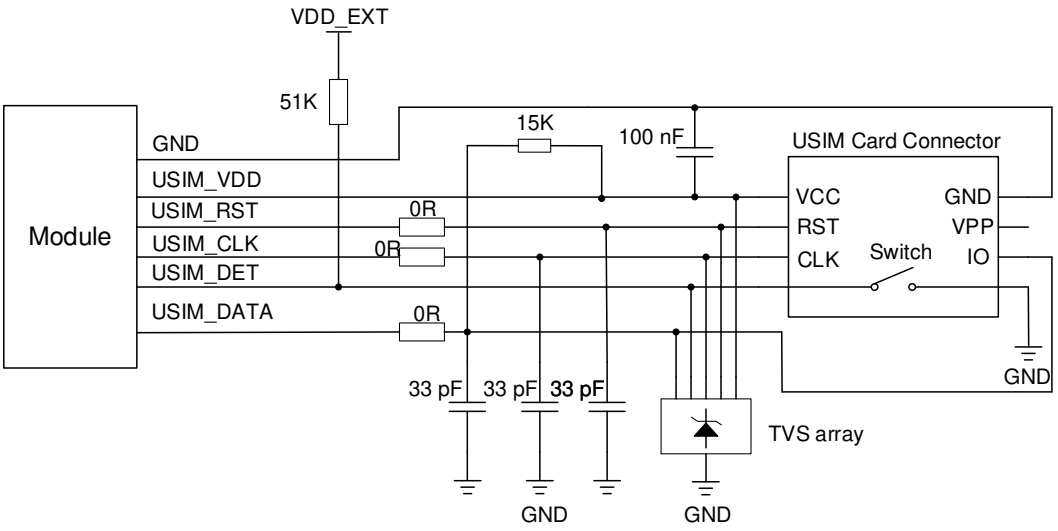


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the (U)SIM card detection function is not needed, keep USIM_DET disconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

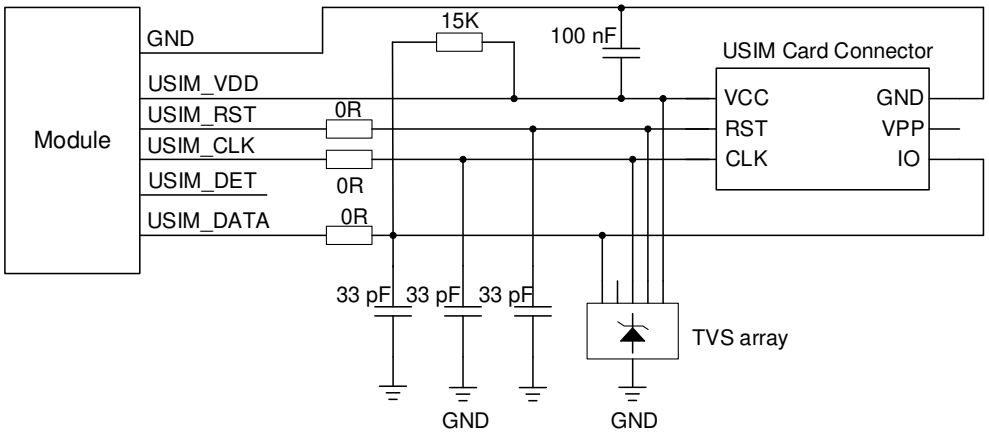


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure that the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.

- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering RF interference. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

NOTE

1. There are hardware conflicts between pins 51–53 and 145–147. If pins 145–147 of (U)SIM2 interface are used, pins 51–53 must be kept unconnected. If the pins 51–53 are used, that is, the (U)SIM2 interface is not used, the pins 145–147 must be kept unconnected.
2. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for using dual (U)SIM operation. Please consult Quectel Technical Support for more information about how to use (U)SIM2.

3.9. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full speed (12 Mbps) and high speed (480 Mbps) modes. The USB interface can only serve in the slave mode. It is used for AT command communication, data transmission, software debugging, and firmware upgrade. The following table shows the pin definition of USB interface.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	26	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	27	AIO	USB 2.0 differential data (-)	
USB_VBUS	28	AI	USB connection detection	Typ. 5.0 V, Min. 3.5 V. If unused, keep it open. A test point must be reserved.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

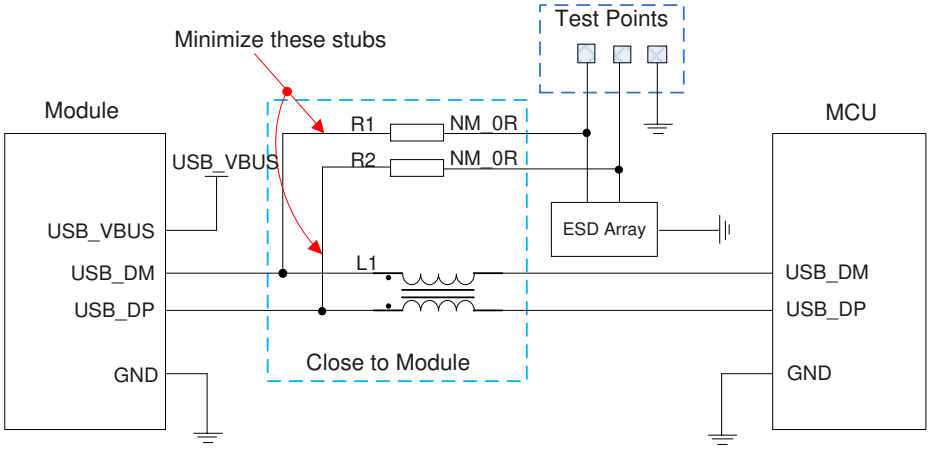


Figure 22: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R1 and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. The impedance of USB differential trace is 90 Ω.
- To preserve signal quality, do not route signal traces under or near crystals, oscillators, magnetic devices and RF signal traces.
- Pay attention to the selection of the ESD protection component on the USB data line. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

3.10. UART Interfaces

The module provides three UART interfaces: main UART, debug UART, and auxiliary UART. Their features are described below.

- Main UART interface supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps and so on, and the default setting is 115200 bps. This interface is used for data transmission and AT command communication. It supports RTS and CTS hardware flow control.
- Debug UART interface supports 921600 bps baud rate. It is used for log output.
- Auxiliary UART interface supports the same baud rates as the main UART interface. It supports RTS and CTS hardware flow control.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	33	DO	Clear to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	34	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_TXD	32	DO	Main UART transmit	1.8 V power domain. If unused, keep them open.
MAIN_RXD	31	DI	Main UART receive	
MAIN_DCD	48	DO	Main UART data carrier detection	
MAIN_DTR	39	DI	Main UART data terminal ready	
MAIN_RI	40	DO	Main UART ring indication	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	72	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	71	DO	Debug UART transmit	

Table 15: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
UART2_RXD	123	DI	Auxiliary UART receive	1.8 V power domain.

UART2_TXD	124	DO	Auxiliary UART transmit	If unused, keep them open.
UART2_CTS	121	DO	Clear to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
UART2_RTS	122	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. Output CP log. Only 8 Mbps baud rate is supported. A test point must be reserved.

The module provides 1.8 V UART interfaces. Use a voltage-level translator if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

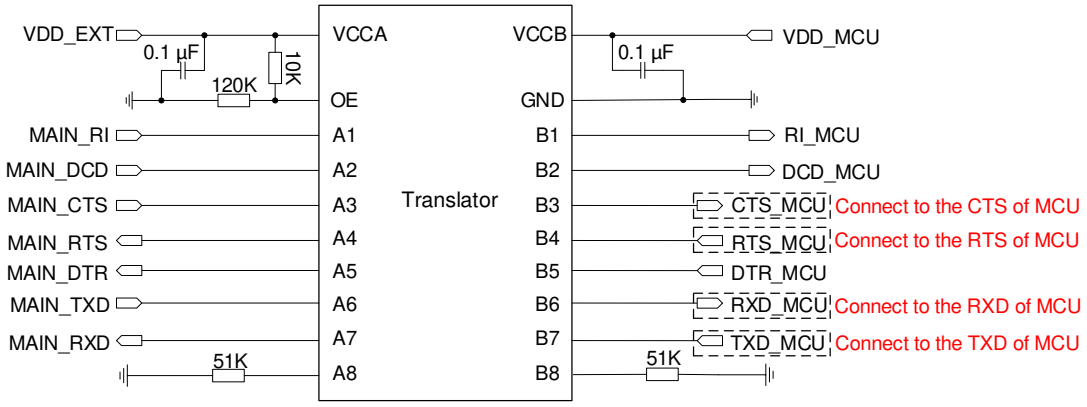


Figure 23: Reference Circuit with Translator

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

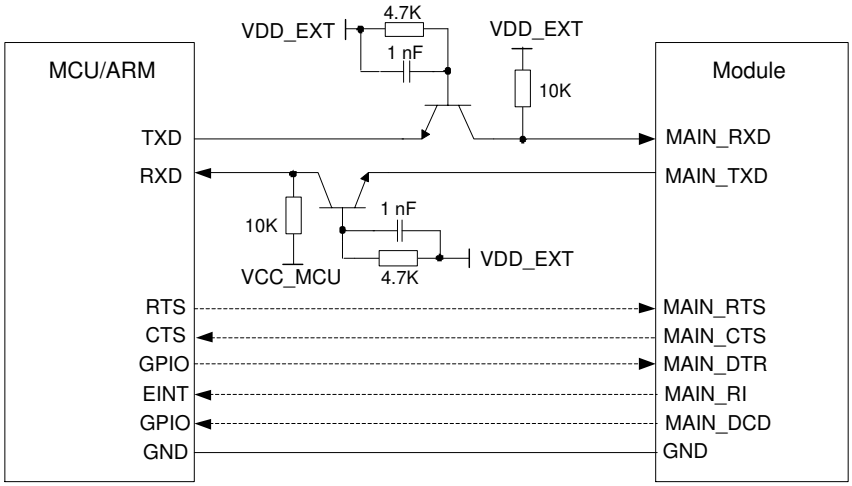


Figure 24: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. When using pins 39, 40, and 48, please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.
4. It is strongly recommended to reserve test points for DBG_RXD, DBG_TXD, and UART2_RTS to facilitate capturing AP log and CP log.

3.11. SPI*

The module provides one SPI that only supports master mode. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 16: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	4	DO	SPI chip select	1.8 V power domain. If unused, keep them open.
SPI_TXD	3	DO	SPI master mode output	

SPI_RXD	2	DI	SPI master mode input
SPI_CLK	1	DO	SPI clock

3.12. I2C and PCM Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface for an external codec IC. The PCM interface of the module only supports slave mode; therefore, the clock signal of the codec IC needs to be provided externally. It is recommended to use the module CAM_MCLK pin to provide the clock signal.

Table 17: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	57	OD	I2C serial clock	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
I2C_SDA	56	OD	I2C serial data	
PCM_DIN	59	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	60	DO	PCM data output	
PCM_SYNC	58	DI	PCM data frame sync	
PCM_CLK	61	DI	PCM clock	

PCM interface supports the short frame mode, in which PCM_CLK = Number of Channels × PCM_SYNC × Word Length. 1–4 channels are supported, but only data at the first channel will be used; PCM_SYNC equals the audio sampling frequency, which supports 8–44.1 kHz; the Word Length is 16-bit.

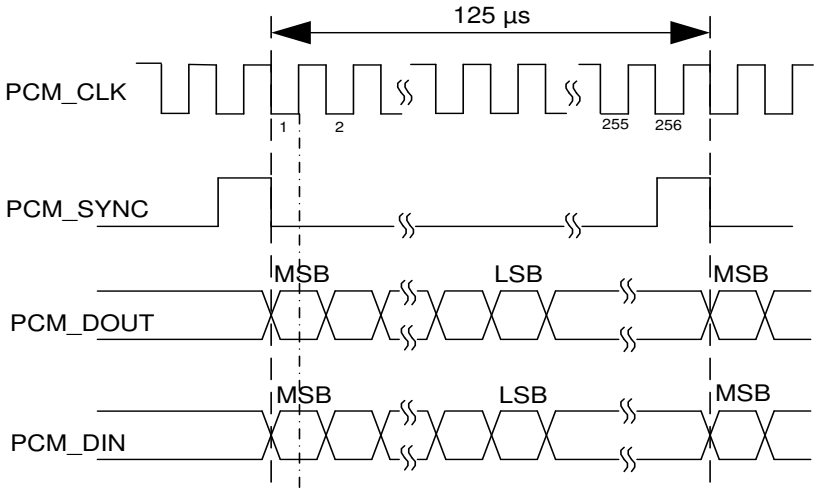


Figure 25: Timing of PCM Interface

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

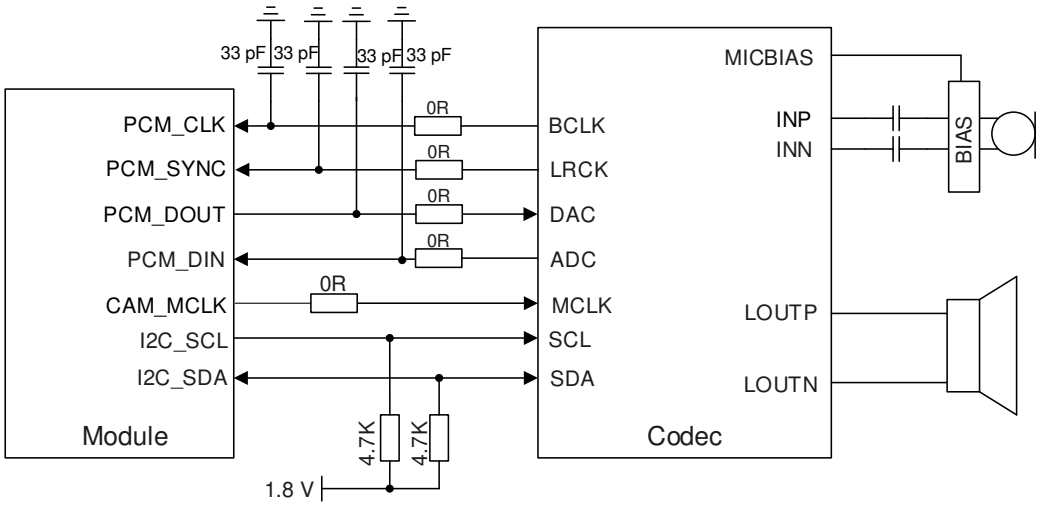


Figure 26: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. The clock signals of PCM_SYNC and PCM_CLK are provided by the codec of the master device, but the provided PCM_SYNC frequency must be equal to the sampling frequency of the audio file played by the module.
2. It is recommended to reserve a RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
3. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC. In

other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.

4. In this scheme, the CAM_MCLK pin is occupied on the hardware and therefore cannot be used for other interfaces.

3.13. Analog Audio Interfaces

The module provides two analog input and three analog output channels. The pin definition is shown in the following table.

Table 18: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS	25	PO	Bias voltage output for microphone	1.8 V power domain. If unused, keep them open.
MIC_P	24	AI	Microphone analog input (+)	
MIC_N	23	AI	Microphone analog input (-)	
HEADMIC_BIAS	143	PO	Bias voltage output for headset	
HEADMIC_P	140	AI	Headset analog differential input (+)	
HEADMIC_N	141	AI	Headset analog differential input (-)	
HP_L	111	AO	Headset left channel output	
HP_R	112	AO	Headset right channel output	
AMP_VCOMP	94		Headset dedicated ground	It should be traced between the left and right channels, and connected to the GND of the headset jack, and then a via directly to the main GND layer. 1.8 V power domain. If unused, keep them open.
HP_DET	142	DI	Headset hot-plug detection	1.8 V power domain.

HEADMIC_IN_DET	93	DI	Headset microphone and button detect	If unused, keep them open.
LOUDSPK_P	109	AO	Loudspeaker differential output (+)	With an internal PA. When configured as Class AB, the maximum drive power is 500 mW at 8 Ω load; when configured as Class D, the maximum drive power is 800 mW at 8 Ω load. If unused, keep them open.
LOUDSPK_N	110	AO	Loudspeaker differential output (-)	
SPK_P	22	AO	Analog audio differential output (+)	Used for receiver interface. Without internal PA. The maximum drive power is 50 mW at 32 Ω load. If the output power cannot meet the demand, this pin can be used to drive an external PA. If unused, keep them open.
SPK_N	21	AO	Analog audio differential output (-)	

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used) and headset.
- AO channels are differential output channels, which can be applied for output of loudspeaker, earpiece and headset.
- The module's internal PA is configured as Class AB by default.

3.13.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. Without placing this capacitor, TDD noise could be heard. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

For modules that support GSM, the severity of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitors on the PCB board should be placed as close to the audio devices or audio interfaces as possible, and the

traces should be as short as possible. They should go through the filter capacitors before arriving at other connection points.

To reduce radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces should not be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.13.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

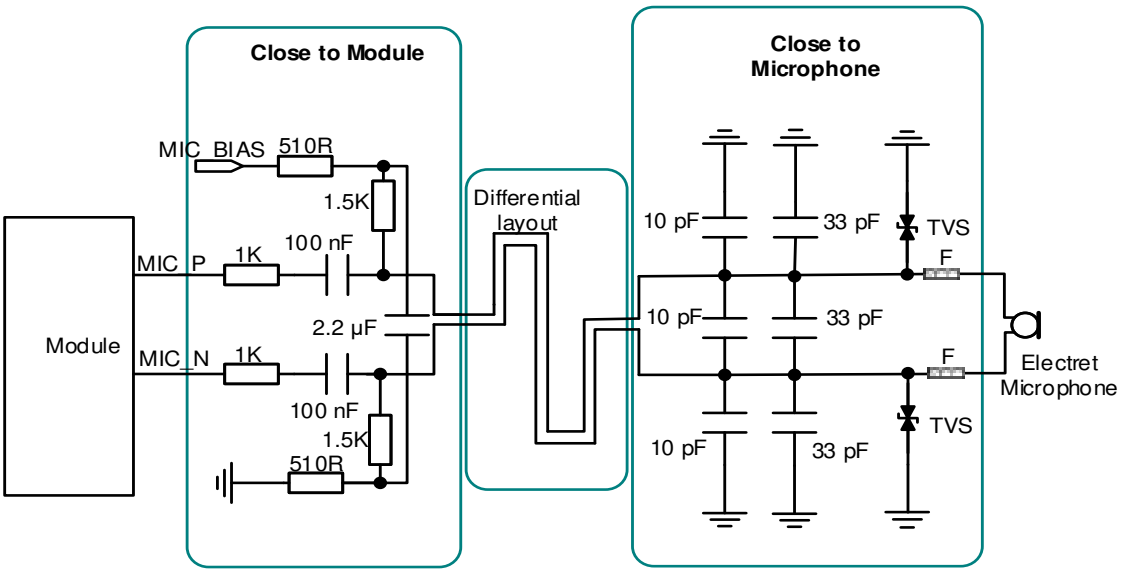


Figure 27: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components used for protecting the MIC.

3.13.3. Loudspeaker Interface Design

The loudspeaker interface reference circuit is shown in the following figure.

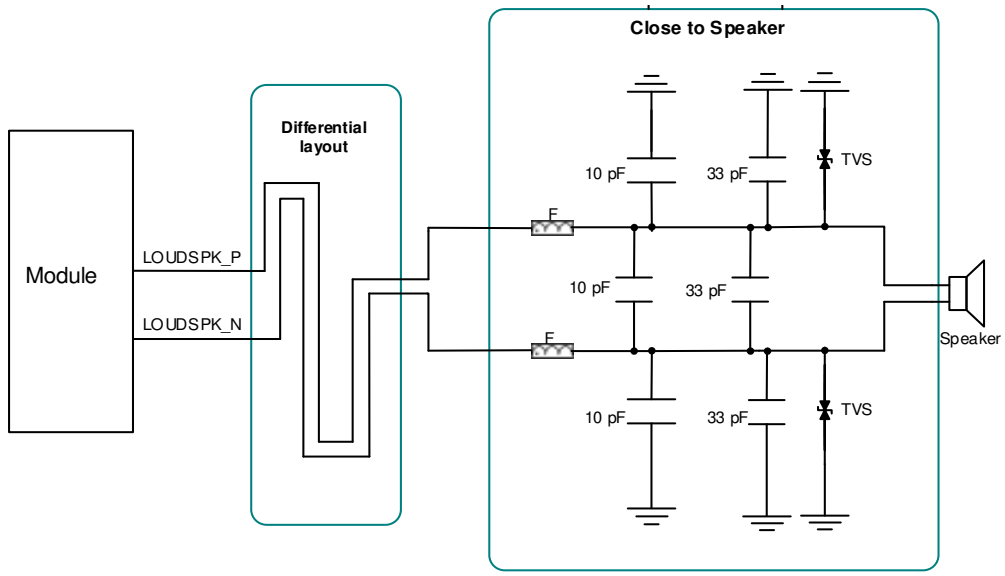


Figure 28: Reference Design for Loudspeaker Interface

3.13.4. Earpiece Interface Design

The earpiece interface reference circuit is shown in the following figure.

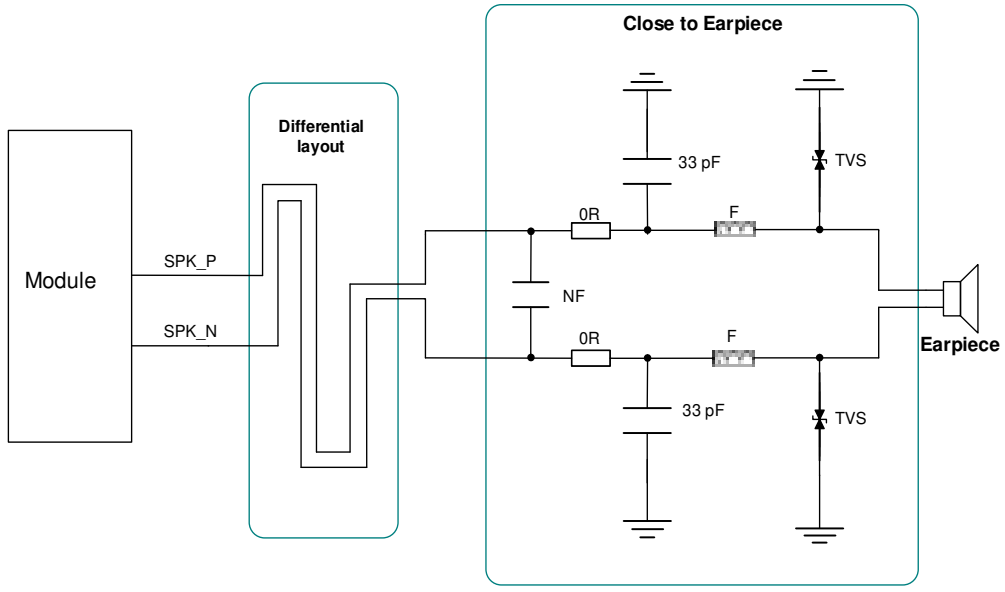


Figure 29: Reference Design for Earpiece Interface

3.13.5. Headset Interface Design

The reference design for headset interface circuit compatible with CTIA and OMTP is shown in the following figure.

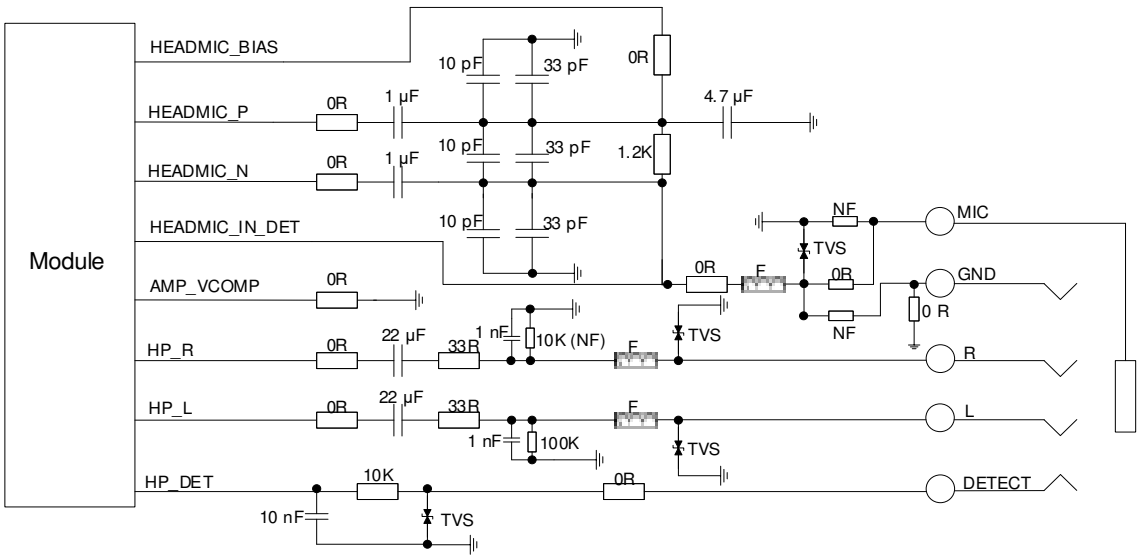


Figure 30: Reference Design for Headset Interface

3.14. LCM Interface

The LCM interface of the module supports the LCD display with a maximum resolution of 320 × 240, DMA transmission, as well as 16-bit RGB565 and YUV formats.

Table 19: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_TE	62	DI	LCD tearing effect	1.8 V power domain. If unused, keep them open.
LCD_RST	64	DO	LCD reset	
LCD_SEL	137	DO	Reserved	
LCD_SPI_CS	65	DO	LCD SPI chip select	
LCD_SPI_CLK	67	DO	LCD SPI clock	
LCD_SPI_RS	63	DO	LCD SPI register select	
LCD_SPI_DOUT	66	DIO	LCD SPI data output	
LCD_ISINK	135	PI	Sink current input. Backlight adjustment.	It is driven by the current sink method and connected to the

				backlight cathode; the brightness can be adjusted with current control.
LCD_VDDIO	134	PO	LCD digital power	LCD power supply, Vnom = 1.8 V. If unused, keep it open.
LCD_AVDD	138	PO	LCD analog power	LCD power supply, Vnom = 3.0 V. If unused, keep it open.

3.15. Matrix Keypad Interface

The module supports a 5 × 6 matrix keypad interface. Besides, USB_BOOT and KEYOUT0 can be designed as a scan button. Press the button composed of USB_BOOT + KEYOUT0 before powering up the module, which will enter the download mode when it is turned on. See ***Chapter 3.20*** for details.

Table 20: Pin Definition of Matrix Keypad Interface

Pin Name	Pin No.	I/O	Description	Comment
KEYIN1	129	DI	Matrix keypad input 1	1.8 V power domain. If unused, keep them open.
KEYIN2	128	DI	Matrix keypad input 2	
KEYIN3	127	DI	Matrix keypad input 3	
KEYIN4	126	DI	Matrix keypad input 4	
KEYIN5	125	DI	Matrix keypad input 5	
KEYOUT0	105	DO	Matrix keypad output 0	
KEYOUT1	106	DO	Matrix keypad output 1	
KEYOUT2	107	DO	Matrix keypad output 2	
KEYOUT3	108	DO	Matrix keypad output 3	
KEYOUT4	104	DO	Matrix keypad output 4	
KEYOUT5	103	DO	Matrix keypad output 5	

NOTE

Do not pull up KEYIN1 and USB_BOOT before turning on the module.

3.16. Charging Interface*

The module provides a charging interface that supports a minimum current of 300 mA and a maximum current of 1000 mA.

Table 21: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	28	AI	Charging voltage detect	Typ. 5.0 V. If unused, keep it open. A test point must be reserved.
VBAT_SENSE	29	AI	Battery voltage and charging current (combines with ISENSE) detection	Regardless of whether the charging function is used, this pin must be connected to the VBAT power supply, otherwise the module will not be turned on normally.
ISENSE	101	AI	Charging current detection	If unused, keep them open.
VDRV	102	AO	Charging control pin	Used for driving the MOSFET in the external charging circuit to adjust the charging current. If unused, keep them open.

To enhance the reliability and availability of the charging in your applications, please follow the criteria below in charging circuit design:

- The traces length between ISENSE and VBAT_SENSE from the module to the charging current detection resistor should be as short as possible, and they should be routed in a differential pair to avoid the influence of the trace impedance on the detection result.

- Pull out the VBAT_SENSE separately and connect it to one end of the charging current detection resistor (close to the positive electrode of the battery), and then connect the VBAT_RF to avoid affecting the detection of the battery voltage.
- The trace width of the charging path (from the USB_VBUS to the emitter electrode of the charging transistor, and from the collector of the charging transistor to the positive electrode of the battery) should not be less than 1.5 mm with sufficient margin.
- Charging circuit is a heat source when it is working. Pay attention to heat dissipation and keep it away from heat-sensitive devices.

3.17. ADC Interfaces

The module provides four analog-to-digital converter (ADC) interfaces. To improve the accuracy of ADC, surround the trace of ADC with ground.

The voltage on ADC pins can be read via **AT+QADC=<port>**:

- **AT+QADC=0**: read the voltage on ADC0.
- **AT+QADC=1**: the voltage on ADC1.
- **AT+QADC=2**: the voltage on ADC2.
- **AT+QADC=3**: the voltage on ADC3.

See ***document [2]*** for more details.

Table 22: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC3	114	General-purpose ADC interface	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC2	113		
ADC1	20		
ADC0	19		

Table 23: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage at ADC3	0	-	VBAT	V

Voltage at ADC2	0	-	VBAT	V
Voltage at ADC1	0	-	VBAT	V
Voltage at ADC0	0	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

Considering the possible difference between ADC voltage ranges, when using ADC pins, it is strongly recommended to reserve a voltage divider circuit for better compatibility with other Quectel modules. The value of the voltage divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. Connect the ADC pin in series with a 1 kΩ resistor when the divider circuit is not used.

3.18. Network Status Indication

The network status indication pins NET_MODE and NET_STATUS can drive the network status indicators. The following tables describe pin definition and logic level changes in different network status.

Table 24: Pin Definition of Network Status Indication Pins

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	52	DO	Indicate whether the module has registered on LTE network	1.8 V power domain. If unused, keep it open.
NET_STATUS	54	DO	Indicate the module's network activity status	

Table 25: Working State of Network Status Indication Pins

Pin Name	Status	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Registered on network and idle

	Flicker rapidly (63 ms low /62 ms high)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

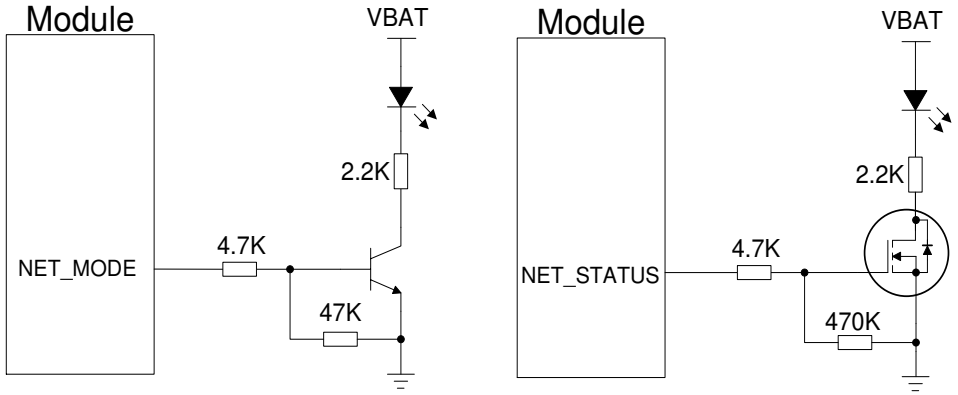


Figure 31: Reference Circuit of Network Status Indication

3.19. Behaviors of MAIN_RI

You can configure MAIN_RI behaviors with **AT+QCFG="risignaltype","physical"**. No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 26: Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The MAIN_RI behaviors can be changed via **AT+QCFG="urc/ri/ring"**. See ***document [2]*** for details.

NOTE

1. The **AT+QURCCFG** allows you to set the main UART, USB AT port, or USB modem port as the URC output port. The default setting is USB AT port.
2. When using MAIN_RI (pin 40), please note that the pin will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before it can be configured as 1.8 V output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.20. USB_BOOT Interface

The module provides a USB_BOOT interface. Pull up USB_BOOT to VDD_EXT before powering up the module, which will enter the download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Alternatively, pressing the scan button of USB_BOOT + KEYOUT0 before the module is powered up will also enable the module to enter the download mode when it is turned on.

Table 27: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	55	DI	Force the module into emergency download mode	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

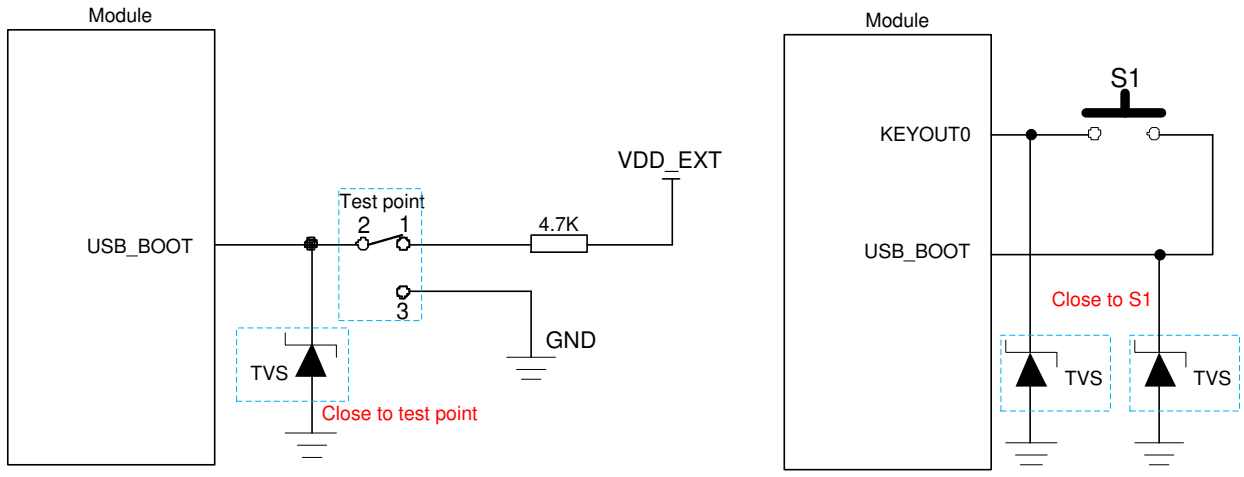


Figure 32: Reference Circuit of USB_BOOT Interface

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.

3.21. Camera Interface

The module provides one camera interface supporting camera up to 0.3 MP and the 2-data-line transmission of SPI.

Table 28: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	10	DO	Master clock of camera	1.8 V power domain. If unused, keep them open.
CAM_I2C_SCL	11	OD	I2C clock of camera	Pull each of them up to 1.8 V power domain with an external resistor. 1.8 V power domain. If unused, keep them open.
CAM_I2C_SDA	12	OD	I2C data of camera	
CAM_SPI_CLK	13	DI	SPI clock of camera	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	14	DI	SPI data0 of camera	

CAM_SPI_DATA1	15	DI	SPI data1 of camera	
CAM_PWDN	16	DO	Power down of camera	
CAM_RST	120	DO	Reset of camera	
CAM_VDD	17	PO	Analog power supply of camera	Power supply of camera. If unused, keep them open.
CAM_VDDIO	68	PO	Digital power supply of camera	

NOTE

If the camera interface is not required, the pins 11 and 12 can be used as an I2C interface to connect other peripherals.

4 Antenna Interfaces

EC600U series module provides a main antenna interface and a Bluetooth/Wi-Fi Scan [6] antenna interface. The impedance of antenna ports is 50 Ω.

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

4.1. Main Antenna and Bluetooth/Wi-Fi Scan Antenna Interfaces

4.1.1. Pin Definition

Table 29: Pin Definition of Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_BT/ WIFI_SCAN	42	AIO	The shared antenna interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	46	AIO	Main antenna	50 Ω characteristic impedance.

4.1.2. Operating Frequency

Table 30: EC600U-CN Operating Frequencies（Unit: MHz）

3GPP Band	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170

[6] EC600U-CN, EC600U-EU and EC600U-CE support Bluetooth and Wi-Fi Scan functions.

LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

B41 of EC600U-CN only supports 140 MHz (2535–2675 MHz).

Table 31: EC600U-EU Operating Frequencies（Unit: MHz）

3GPP Band	Transmit	Receive
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803

LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

B41 of EC600U-EU only supports 140 MHz (2535–2675 MHz).

Table 32: EC600U-EC Operating Frequencies（Unit: MHz）

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz

Table 33: EC600U-CE Operating Frequencies（Unit: MHz）

3GPP Band	Transmit	Receive
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880

LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

Table 34: EC600U-LA Operating Frequencies（Unit: MHz）

3GPP Band	Transmit	Receive
GSM850	824~849	869~894
EGSM900	880~915	925~960
DCS1800	1710~1785	1805~1880
PCS1900	1850~1910	1930~1990
LTE-FDD B2	1850~1910	1930~1990
LTE-FDD B3	1710~1785	1805~1880
LTE-FDD B4	1710~1755	2110~2155
LTE-FDD B5	824~849	869~894
LTE-FDD B7	2500~2570	2620~2690
LTE-FDD B8	880~915	925~960
LTE-FDD B28	703~748	758~803
LTE-FDD B66	1710~1780	2110~2180

NOTE

EC600U-CN does not support GSM frequency band.

4.1.3. Reference Design of Antenna Interface

A reference design of main antenna and Bluetooth/Wi-Fi Scan is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

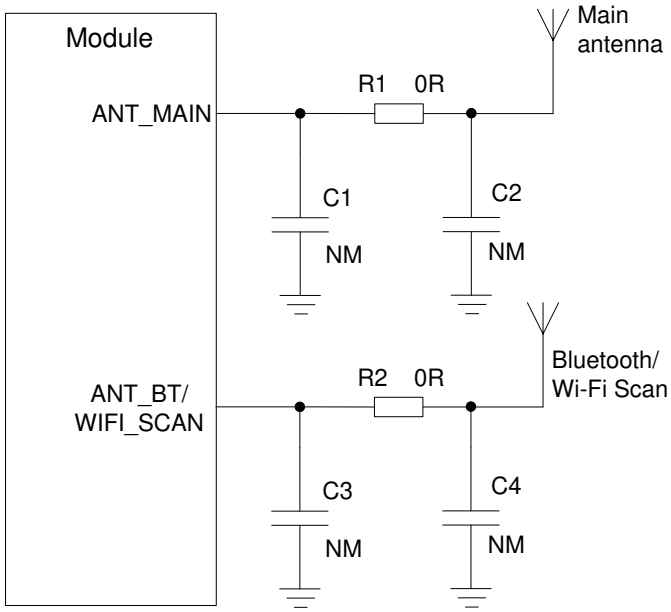


Figure 33: Reference Circuit of RF Antenna

NOTE

1. To improve the receiving sensitivity, ensure that the main antenna and the Bluetooth/Wi-Fi Scan receiving antenna are placed at a proper distance.
2. Place the π-type matching components (R1 & C1 & C2 and R2 & C3 & C4) as close to the antenna as possible.

4.1.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

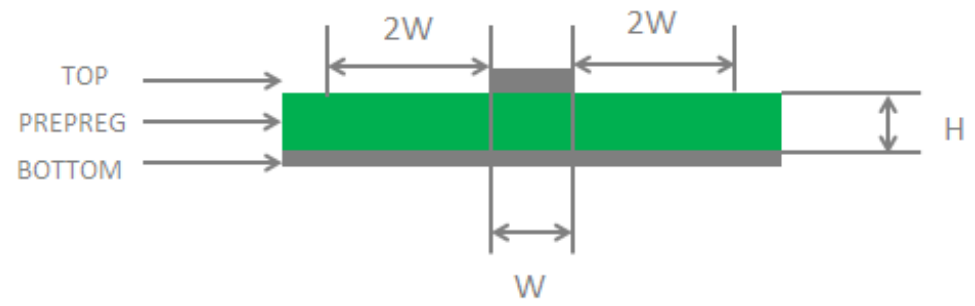


Figure 34: Microstrip Design on a 2-layer PCB

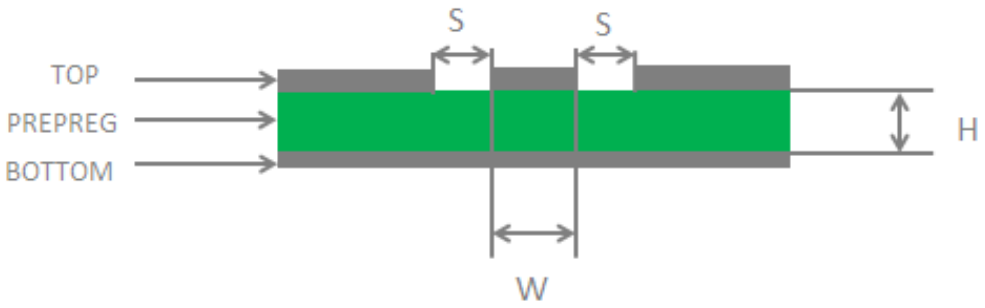


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

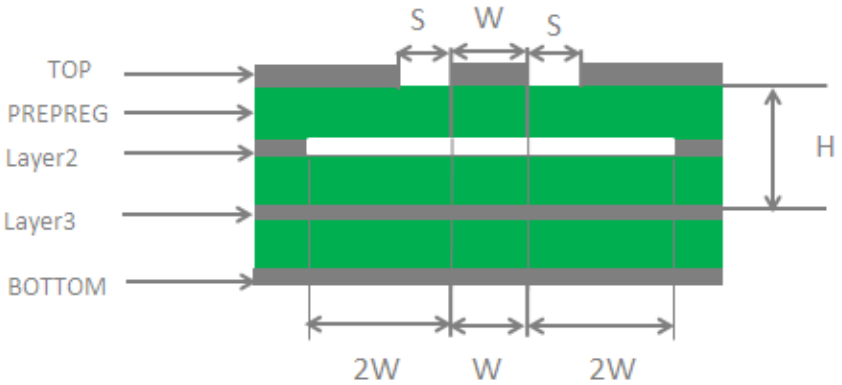


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

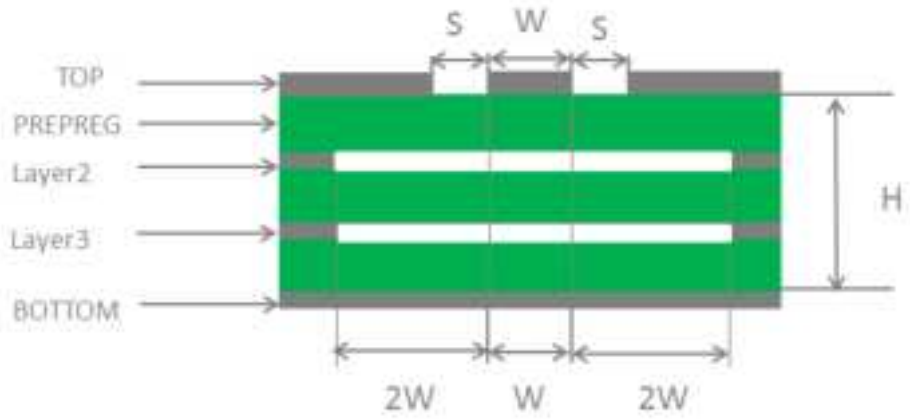


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

4.2. Antenna Installation

4.2.1. Antenna Design Requirement

Table 35: Antenna Requirements

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W

	Input impedance: 50 Ω Cable insertion loss: **< 1 dB**: LB (< 1 GHz) **< 1.5 dB**: MB (1–2.3 GHz) **< 2 dB**: HB (> 2.3 GHz)

4.2.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT receptacle provided by Hirose.

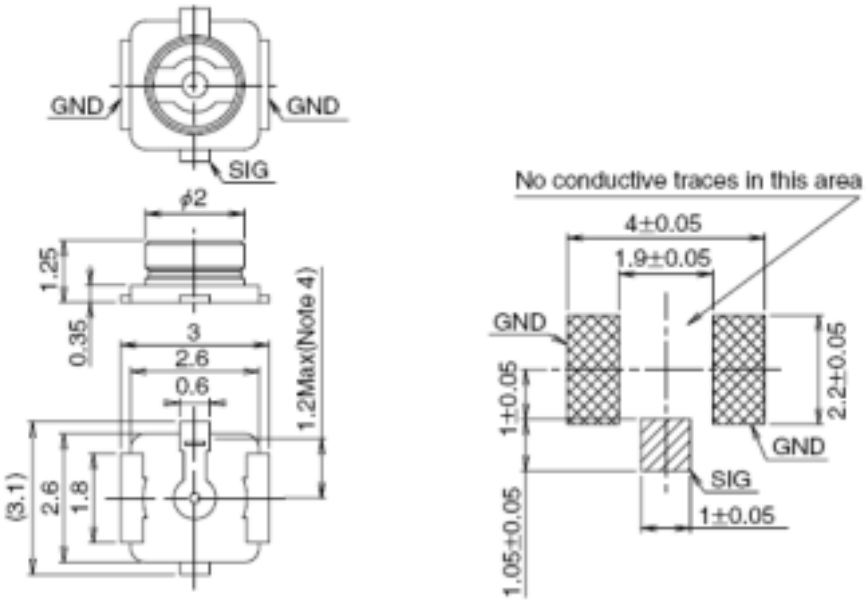


Figure 38: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

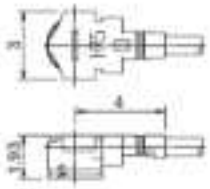
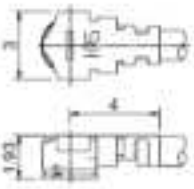
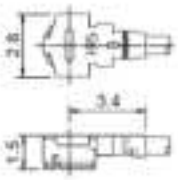
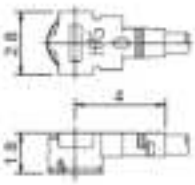
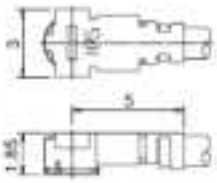
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

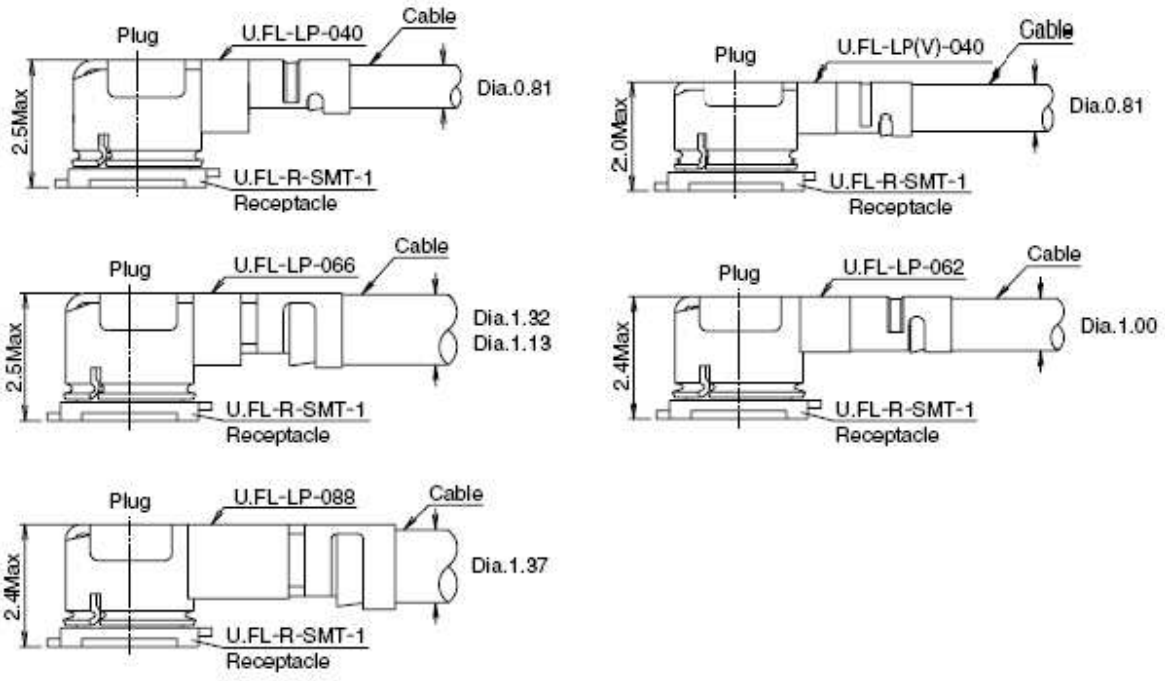


Figure 40: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

5 Reliability, Radio and Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_RF (EC600U-CN)	-	1.5	A
Peak Current of VBAT_RF (EC600U-EU/EC/CE/LA)	-	2.5	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC[0:3]	0	VBAT	V

5.2. Power Supply Ratings

Table 37: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_RF	The actual input voltages must be kept between the minimum	3.3	3.8	4.3	V

		and maximum values.				
	Voltage drop during burst transmission		-	-	400	mV
I_{VBAT}	EC600U-EU/EC/CE/LA peak supply current	At maximum power control level	-	2.3	2.5	A
	EC600U-CN peak supply current		-	1.2	1.5	A
USB_VBUS	USB connection detection		3.5	5.0	5.25	V

5.3. Operating and Storage Temperatures

Table 38: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [7]	-35	+25	+75	ºC
Extended Operation Range [8]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

5.4. Power Consumption

Table 39: EC600U-CN Power consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	33	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.29	mA

[7] Within this range, the module's performance complies with 3GPP requirements.
[8] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's performance will comply with 3GPP requirements again.

	AT+CFUN=4 (USB disconnected)	1.29	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.7	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.05	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.56	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.68	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.59	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.6	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.07	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.49	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.69	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.49	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	12.34	mA
	LTE-FDD @ PF = 64 (USB connected)	27.78	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.46	mA
	LTE-TDD @ PF = 64 (USB connected)	27.88	mA
LTE data transfer	LTE-FDD B1 @ 22.88 dBm	624	mA
	LTE-FDD B3 @ 22.97 dBm	623	mA
	LTE-FDD B5 @ 23.07 dBm	552	mA
	LTE-FDD B8 @ 22.85 dBm	510	mA
	LTE-TDD B34 @ 22.80 dBm	287	mA
	LTE-TDD B38 @ 23.15 dBm	332	mA
	LTE-TDD B39 @ 22.95 dBm	277	mA
	LTE-TDD B40 @ 23.64 dBm	301	mA
	LTE-TDD B41 @ 22.70 dBm	343	mA

Table 40: EC600U-EU Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	34	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.37	mA
	AT+CFUN=4 (USB disconnected)	1.37	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.87	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.37	mA
	EGSM900 @ DRX = 5 (USB suspended)	3.6	mA
	EGSM900 @ DRX = 9 (USB disconnected)	2.2	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.86	mA
	DCS1800 @ DRX = 5 (USB disconnected)	2.35	mA
	DCS1800 @ DRX = 5 (USB suspended)	3.6	mA
	DCS1800 @ DRX = 9 (USB disconnected)	2.2	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.68	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.06	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.27	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.73	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.57	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.72	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.07	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.52	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.74	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.58	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	13.21	mA
	EGSM900 @ DRX = 5 (USB connected)	28.67	mA

	LTE-FDD @ PF = 64 (USB disconnected)	12.9	mA
	LTE-FDD @ PF = 64 (USB connected)	28.38	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.85	mA
	LTE-TDD @ PF = 64 (USB connected)	28.34	mA
GPRS data transfer	GSM850 4DL/1UL @ 33.1 dBm	262	mA
	GSM850 3DL/2UL @ 30.9 dBm	397	mA
	GSM850 2DL/3UL @ 28.9 dBm	448	mA
	GSM850 1DL/4UL @ 26.7 dBm	464	mA
	EGSM900 4DL/1UL @ 32.5 dBm	254	mA
	EGSM900 3DL/2UL @ 30.9 dBm	386	mA
	EGSM900 2DL/3UL @ 28.9 dBm	440	mA
	EGSM900 1DL/4UL @ 26.8 dBm	464	mA
	DCS1800 4DL/1UL @ 29.4 dBm	169	mA
	DCS1800 3DL/2UL @ 27.9 dBm	249	mA
	DCS1800 2DL/3UL @ 25.8 dBm	273	mA
	DCS1800 1DL/4UL @ 23.7 dBm	286	mA
	PCS1900 4DL/1UL @ 29.8 dBm	183	mA
	PCS1900 3DL/2UL @ 27.9 dBm	267	mA
	PCS1900 2DL/3UL @ 25.8 dBm	296	mA
	PCS1900 1DL/4UL @ 23.7 dBm	315	mA
LTE data transfer	LTE-FDD B1 @ 22.99 dBm	693	mA
	LTE-FDD B3 @ 22.97 dBm	703	mA
	LTE-FDD B5 @ 23.86 dBm	627	mA
	LTE-FDD B7 @ 22.73 dBm	783	mA
	LTE-FDD B8 @ 22.73 dBm	702	mA

	LTE-FDD B20 @ 22.73 dBm	597	mA
	LTE-FDD B28 @ 22.73 dBm	655	mA
	LTE-TDD B38 @ 23.49 dBm	421	mA
	LTE-TDD B40 @ 23.77 dBm	391	mA
	LTE-TDD B41 @ 23.15 dBm	418	mA
GSM voice call	GSM850 PCL = 5 @ 33.0 dBm	293	mA
	GSM850 PCL = 12 @ 18.9 dBm	119	mA
	GSM850 PCL = 19 @ 5.2 dBm	91	mA
	EGSM900 PCL = 5 @ 32.4 dBm	269	mA
	EGSM900 PCL = 12 @ 19.1 dBm	121	mA
	EGSM900 PCL = 19 @ 5.5 dBm	82	mA
	DCS1800 PCL = 0 @ 29.4 dBm	185	mA
	DCS1800 PCL = 7 @ 16.1 dBm	96	mA
	DCS1800 PCL = 15 @ 0.9 dBm	79	mA
	PCS1900 PCL = 0 @ 29.8 dBm	199	mA
	PCS1900 PCL = 7 @ 16.1 dBm	98	mA
	PCS1900 PCL = 15 @ 0.9 dBm	79	mA

Table 41: EC600U-EC Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	29.65	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.09	mA
	AT+CFUN=4 (USB disconnected)	1.16	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.06	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.51	mA

	EGSM900 @ DRX = 5 (USB suspended)	3.08	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.32	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.06	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.52	mA
	DCS1800 @ DRX = 5 (USB suspended)	2.97	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.32	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.85	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.04	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.57	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.63	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.39	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.89	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.05	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.60	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.64	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.43	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	13.10	mA
	EGSM900 @ DRX = 5 (USB connected)	30.15	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.79	mA
	LTE-FDD @ PF = 64 (USB connected)	30.83	mA
	LTE-TDD @ PF = 64 (USB disconnected)	13.81	mA
	LTE-TDD @ PF = 64 (USB connected)	30.84	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.76 dBm	236	mA
	GSM850 3DL/2UL @ 31.78 dBm	381	mA
	GSM850 2DL/3UL @ 29.57 dBm	436	mA

	GSM850 1DL/4UL @ 28.52 dBm	505	mA
	EGSM900 4DL/1UL @ 32.70 dBm	241	mA
	EGSM900 3DL/2UL @ 31.61 dBm	385	mA
	EGSM900 2DL/3UL @ 29.56 dBm	449	mA
	EGSM900 1DL/4UL @ 28.46 dBm	514	mA
	DCS1800 4DL/1UL @ 29.54 dBm	158	mA
	DCS1800 3DL/2UL @ 28.54 dBm	236	mA
	DCS1800 2DL/3UL @ 26.57 dBm	268	mA
	DCS1800 1DL/4UL @ 25.45 dBm	304	mA
	PCS1900 4DL/1UL @ 29.83 dBm	165	mA
	PCS1900 3DL/2UL @ 28.79 dBm	249	mA
	PCS1900 2DL/3UL @ 26.79 dBm	287	mA
	PCS1900 1DL/4UL @ 25.78 dBm	329	mA
LTE data transfer	LTE-FDD B1 @ 22.61 dBm	611	mA
	LTE-FDD B3 @ 22.86 dBm	553	mA
	LTE-FDD B5 @ 22.69 dBm	571	mA
	LTE-FDD B7 @ 22.61 dBm	765	mA
	LTE-FDD B8 @ 22.48 dBm	560	mA
	LTE-FDD B20 @ 22.40 dBm	527	mA
	LTE-TDD B40 @ 22.60 dBm	321	mA
GSM voice call	GSM850 PCL = 5 @ 32.72 dBm	254	mA
	GSM850 PCL = 12 @ 18.90 dBm	101	mA
	GSM850 PCL = 19 @ 5.91 dBm	72	mA
	EGSM900 PCL = 5 @ 32.73 dBm	260	mA
	EGSM900 PCL = 12 @ 19.15 dBm	103	mA

	EGSM900 PCL = 19 @ 5.95 dBm	72	mA
	DCS1800 PCL = 0 @ 29.54 dBm	172	mA
	DCS1800 PCL = 7 @ 15.64 dBm	83	mA
	DCS1800 PCL = 15 @ 0.85 dBm	67	mA
	PCS1900 PCL = 0 @ 29.85 dBm	180	mA
	PCS1900 PCL = 7 @ 15.84 dBm	86	mA
	PCS1900 PCL = 15 @ 0.46 dBm	67	mA

Table 42: EC600U-CE Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	34.21	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.94	mA
	AT+CFUN=4 (USB disconnected)	1.03	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.68	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.16	mA
	EGSM900 @ DRX = 5 (USB suspended)	3.36	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.94	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.57	mA
	DCS1800 @ DRX = 5 (USB disconnected)	2.20	mA
	DCS1800 @ DRX = 5 (USB suspended)	3.28	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.89	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.55	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.81	mA
	LTE-FDD @ PF = 64 (USB suspended)	2.98	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.43	mA

	LTE-FDD @ PF = 256 (USB disconnected)	1.25	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.59	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.83	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.01	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.45	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.25	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	11.97	mA
	EGSM900 @ DRX = 5 (USB connected)	27.71	mA
	LTE-FDD @ PF = 64 (USB disconnected)	11.95	mA
	LTE-FDD @ PF = 64 (USB connected)	27.45	mA
	LTE-TDD @ PF = 64 (USB disconnected)	11.98	mA
	LTE-TDD @ PF = 64 (USB connected)	27.50	mA
GPRS data transfer	EGSM900 4DL/1UL @ 32.75 dBm	227	mA
	EGSM900 3DL/2UL @ 31.63 dBm	358	mA
	EGSM900 2DL/3UL @ 29.53 dBm	416	mA
	EGSM900 1DL/4UL @ 28.47 dBm	482	mA
	DCS1800 4DL/1UL @ 29.89 dBm	152	mA
	DCS1800 3DL/2UL @ 29.12 dBm	234	mA
	DCS1800 2DL/3UL @ 27.13 dBm	271	mA
	DCS1800 1DL/4UL @ 25.99 dBm	311	mA
LTE data transfer	LTE-FDD B1 @ 22.67 dBm	688	mA
	LTE-FDD B3 @ 22.46 dBm	737	mA
	LTE-FDD B5 @ 22.78 dBm	594	mA
	LTE-FDD B8 @ 23.00 dBm	582	mA
	LTE-TDD B38 @ 23.06 dBm	340	mA

	LTE-TDD B40 @ 23.15 dBm	300	mA
	LTE-TDD B41 @ 22.25 dBm	331	mA
GSM voice call	EGSM900 PCL = 5 @ 32.77 dBm	244	mA
	EGSM900 PCL = 12 @ 19.30 dBm	102	mA
	EGSM900 PCL = 19 @ 4.74 dBm	70	mA
	DCS1800 PCL = 0 @ 30.03 dBm	168	mA
	DCS1800 PCL = 7 @ 17.07 dBm	85	mA
	DCS1800 PCL = 15 @ 0.42 dBm	65	mA

Table 43: EC600U-LA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	28.54	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.85	mA
	AT+CFUN=4 (USB disconnected)	0.94	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.82	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.43	mA
	EGSM900 @ DRX = 5 (USB suspend)	2.35	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.26	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.80	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.29	mA
	DCS1800 @ DRX = 5 (USB suspend)	2.51	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.15	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.45	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.71	mA
	LTE-FDD @ PF = 64 (USB suspend)	2.97	mA

	LTE-FDD @ PF = 128 (USB disconnected)	1.36	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.17	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.10	mA
	EGSM900 @ DRX = 5 (USB connected)	28.55	mA
	DCS1800 @ DRX = 5 (USB disconnected)	12.10	mA
	DCS1800 @ DRX = 5 (USB connected)	28.33	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.14	mA
	LTE-FDD @ PF = 64 (USB connected)	29.48	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.51 dBm	226	mA
	GSM850 3DL/2UL @ 30.82 dBm	356	mA
	GSM850 2DL/3UL @ 29.22 dBm	437	mA
	GSM850 1DL/4UL @ 28.12 dBm	505	mA
	EGSM900 4DL/1UL @ 32.66 dBm	220	mA
	EGSM900 3DL/2UL @ 31.33 dBm	356	mA
	EGSM900 2DL/3UL @ 29.73 dBm	439	mA
	EGSM900 1DL/4UL @ 28.71 dBm	512	mA
	DCS1800 4DL/1UL @ 29.71 dBm	155	mA
	DCS1800 3DL/2UL @ 28.23 dBm	223	mA
	DCS1800 2DL/3UL @ 26.61 dBm	266	mA
	DCS1800 1DL/4UL @ 25.64 dBm	308	mA
	PCS1900 4DL/1UL @ 29.43 dBm	151	mA
	PCS1900 3DL/2UL @ 28.03dBm	225	mA
	PCS1900 2DL/3UL @ 26.55 dBm	272	mA
	PCS1900 1DL/4UL @ 25.34 dBm	309	mA
LTE data transfer	LTE-FDD B2 @ 23.43 dBm	712	mA

	LTE-FDD B3 @ 23.00 dBm	683	mA
	LTE-FDD B4 @ 23.16 dBm	671	mA
	LTE-FDD B5 @ 23.36 dBm	713	mA
	LTE-FDD B7 @ 23.2 dBm	896	mA
	LTE-FDD B8 @ 23.2 dBm	724	mA
	LTE-FDD B28 @ 23.29 dBm	678	mA
	LTE-TDD B66 @ 23.18 dBm	713	mA
GSM voice call	GSM850 PCL = 5 @ 32.30 dBm	234	mA
	GSM850 PCL = 12 @ 19.27 dBm	99	mA
	GSM850 PCL = 19 @ 5.41 dBm	69	mA
	EGSM900 PCL = 5 @ 32.54 dBm	237	mA
	EGSM900 PCL = 12 @ 19.47 dBm	102	mA
	EGSM900 PCL = 19 @ 5.59 dBm	70	mA
	DCS1800 PCL = 0 @ 29.7 dBm	171	mA
	DCS1800 PCL = 7 @ 16.14 dBm	82	mA
	DCS1800 PCL = 15 @ 0.39 dBm	67	mA
	PCS1900 PCL = 0 @ 29.97 dBm	165	mA
	PCS1900 PCL = 7 @ 16.45 dBm	83	mA
	PCS1900 PCL = 15 @ 0.93 dBm	66	mA

5.5. Tx Power

Table 44: EC600U-CN RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm

LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 45: EC600U-EU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 46: EC600U-EC RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40	23 dBm ±2 dB	< -39 dBm

Table 47: EC600U-CE RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 48: EC600U-LA RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is up to 6.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.

5.6. Rx Sensitivity

Table 49: EC600U-CN Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO) Primary + Diversity
	Primary	
LTE-FDD B1 (10 MHz)	-98.5	-96.3
LTE-FDD B3 (10 MHz)	-98.5	-93.3
LTE-FDD B5 (10 MHz)	-99.5	-94.3
LTE-FDD B8 (10 MHz)	-99.5	-93.3
LTE-TDD B34 (10 MHz)	-99.0	-96.3
LTE-TDD B38 (10 MHz)	-99.0	-96.3
LTE-TDD B39 (10 MHz)	-99.0	-96.3
LTE-TDD B40 (10 MHz)	-99.0	-96.3
LTE-TDD B41 (10 MHz)	-98.5	-94.3

Table 50: EC600U-EU Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO) Primary + Diversity
	Primary	
GSM850	-108.0	-102
EGSM900	-108.0	-102
DCS1800	-107.5	-102
PCS1900	-107.5	-102
LTE-FDD B1 (10 MHz)	-98.0	-96.3
LTE-FDD B3 (10 MHz)	-99.0	-93.3
LTE-FDD B5 (10 MHz)	-99.5	-94.3
LTE-FDD B7 (10 MHz)	-96.5	-94.3
LTE-FDD B8 (10 MHz)	-98.5	-93.3
LTE-FDD B20 (10 MHz)	-99.0	-93.3
LTE-FDD B28 (10 MHz)	-99.0	-94.8
LTE-TDD B38 (10 MHz)	-97.5	-96.3
LTE-TDD B40 (10 MHz)	-98.0	-96.3
LTE-TDD B41 (10 MHz)	-97.5	-94.3

Table 51: EC600U-EC Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO) Primary + Diversity
	Primary	
GSM850	-108.5	-102
EGSM900	-108.5	-102
DCS1800	-108.5	-102
PCS1900	-108.5	-102

LTE-FDD B1 (10 MHz)	-98.0	-96.3
LTE-FDD B3 (10 MHz)	-98.0	-93.3
LTE-FDD B5 (10 MHz)	-99.0	-94.3
LTE-FDD B7 (10 MHz)	-96.5	-94.3
LTE-FDD B8 (10 MHz)	-99.0	-93.3
LTE-FDD B20 (10 MHz)	-99.0	-93.3
LTE-TDD B40 (10 MHz)	-99.0	-96.3

Table 52: EC600U-CE Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO) Primary + Diversity
	Primary	
EGSM900	-108.5	-102
DCS1800	-108.5	-102
LTE-FDD B1 (10 MHz)	-97.5	-96.3
LTE-FDD B3 (10 MHz)	-97.5	-93.3
LTE-FDD B5 (10 MHz)	-98.5	-94.3
LTE-FDD B8 (10 MHz)	-99.0	-93.3
LTE-TDD B38 (10 MHz)	-98.0	-96.3
LTE-TDD B40 (10 MHz)	-99.0	-96.3
LTE-TDD B41 (10 MHz)	-97.5	-94.3

Table 53: EC600U-LA Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO) Primary + Diversity
	Primary	
GSM850	-108.7	-102

EGSM900	-108.7	-102
DCS1800	-108.2	-102
PCS1900	-107.8	-102
LTE-FDD B2 (10 MHz)	-98	-96.3
LTE-FDD B3 (10 MHz)	-98.2	-93.3
LTE-FDD B4 (10 MHz)	-97.8	-96.3
LTE-FDD B5 (10 MHz)	-98.6	-94.3
LTE-FDD B7 (10 MHz)	-96.5	-94.3
LTE-FDD B8 (10 MHz)	-99	-93.3
LTE-FDD B28 (10 MHz)	-99.5	-94.8
LTE-FDD B66 (10 MHz)	-97.7	-96.5

5.7. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatics discharge characteristics of the module.

Table 54: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %, Unit: kV)

Tested Interfaces	Contact Discharge	Air Discharge
VBAT, GND	±5	±10
Antenna Interfaces	±4	±8
Other Interfaces	±0.5	±1

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

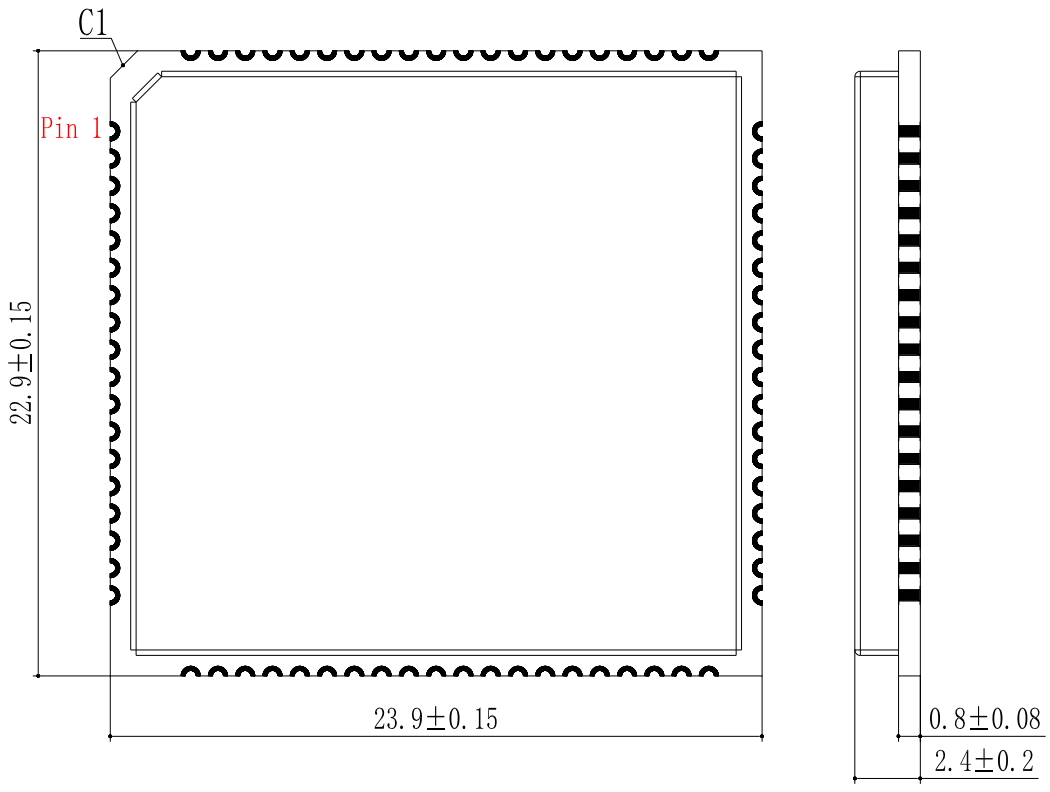


Figure 41: Top and Side Dimensions

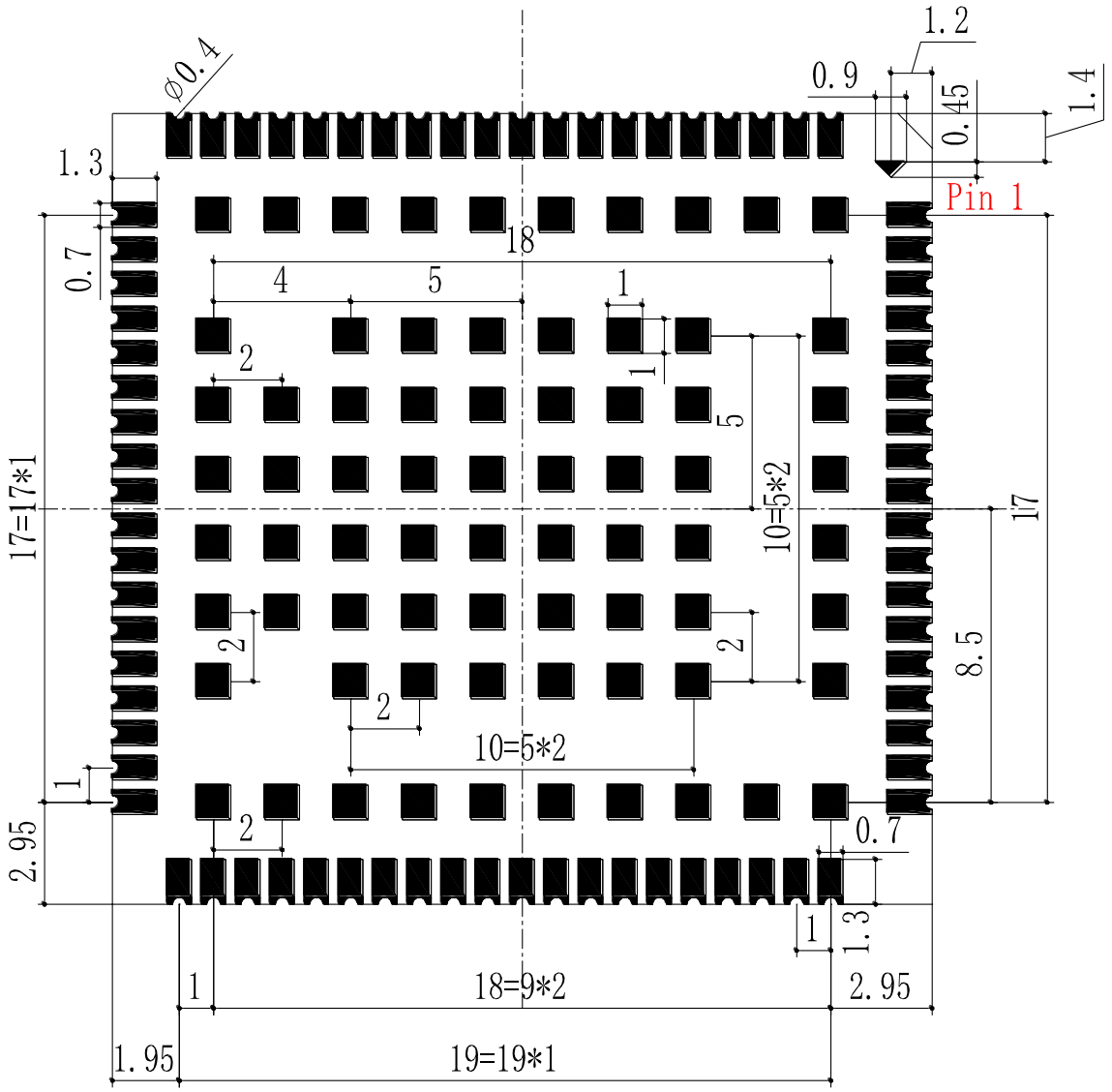


Figure 42: Bottom Dimension

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

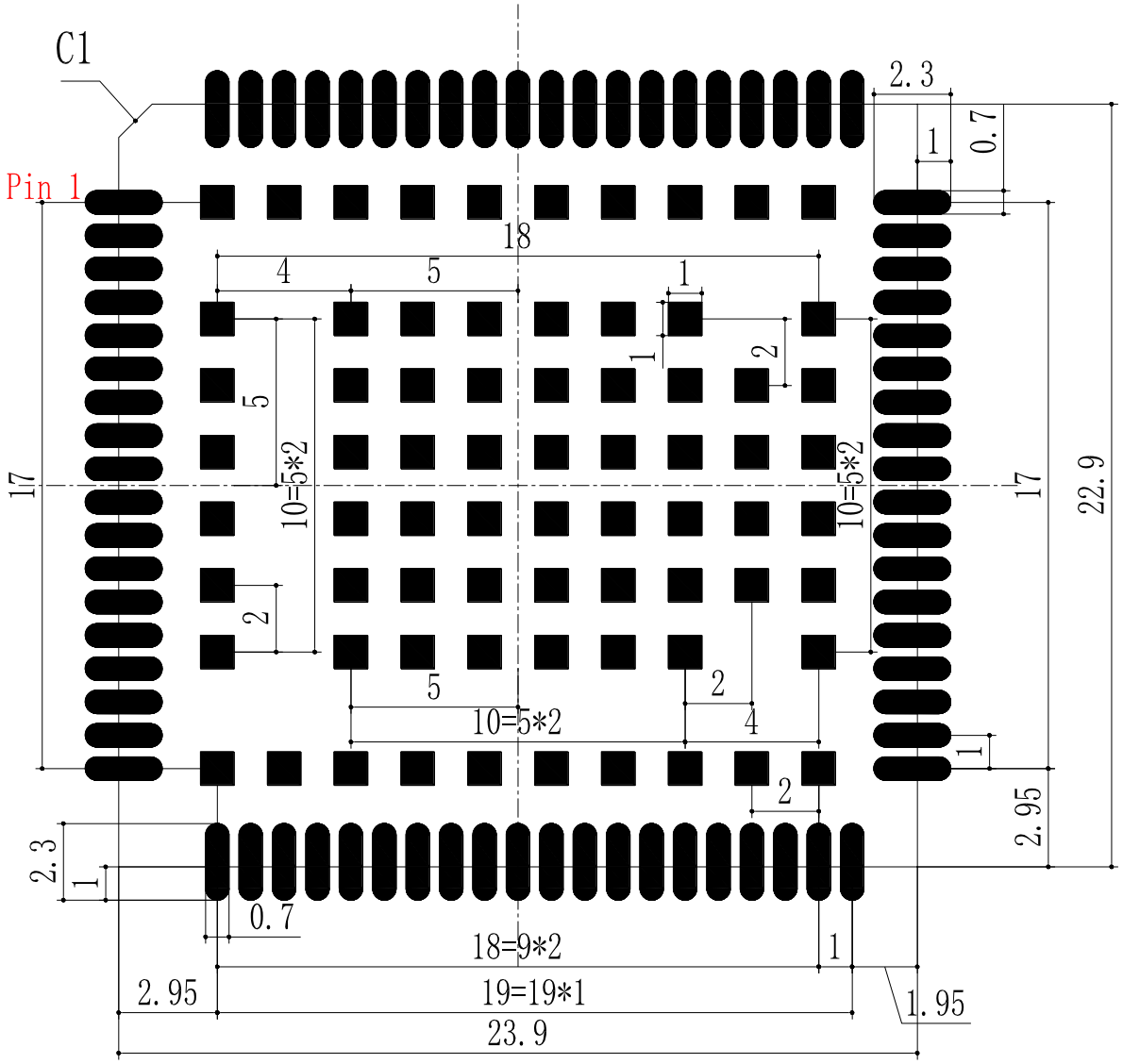


Figure 43: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

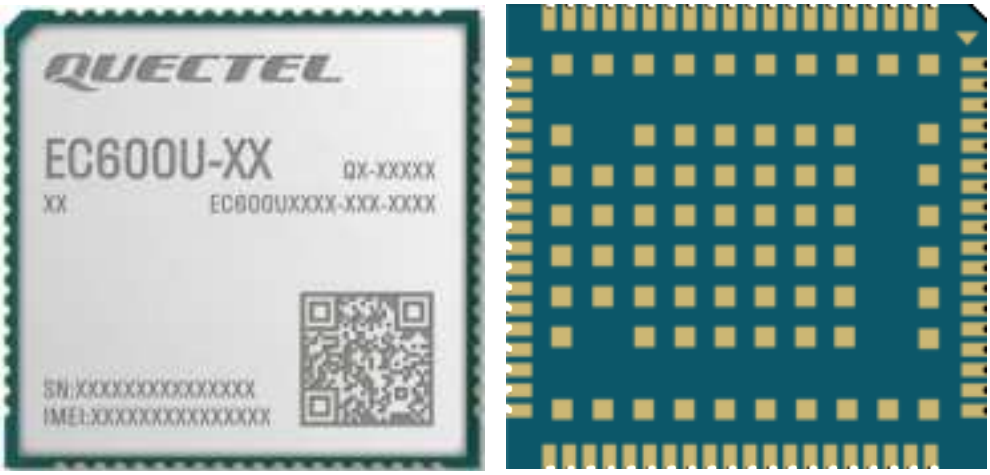


Figure 44: Top and Bottom Views of Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing & Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [9] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a dry cabinet.

[9] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.20 mm. For more details, see ***document [5]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

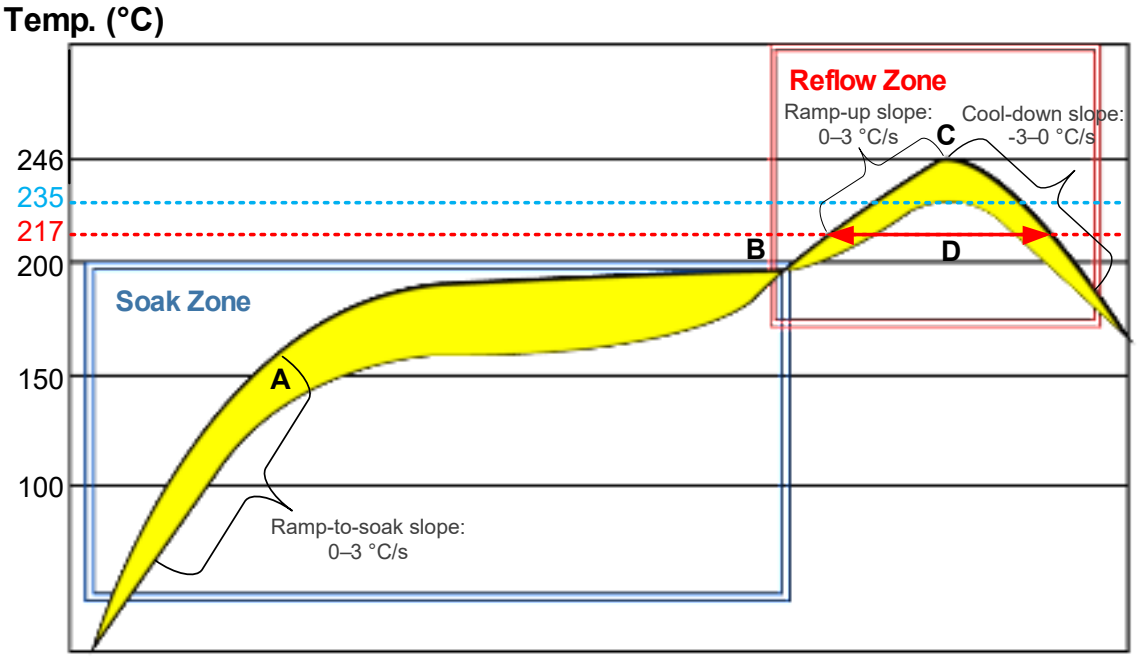


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 55: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, and trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

7.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

7.3.1. Carrier Tape

Dimension details are as follow:

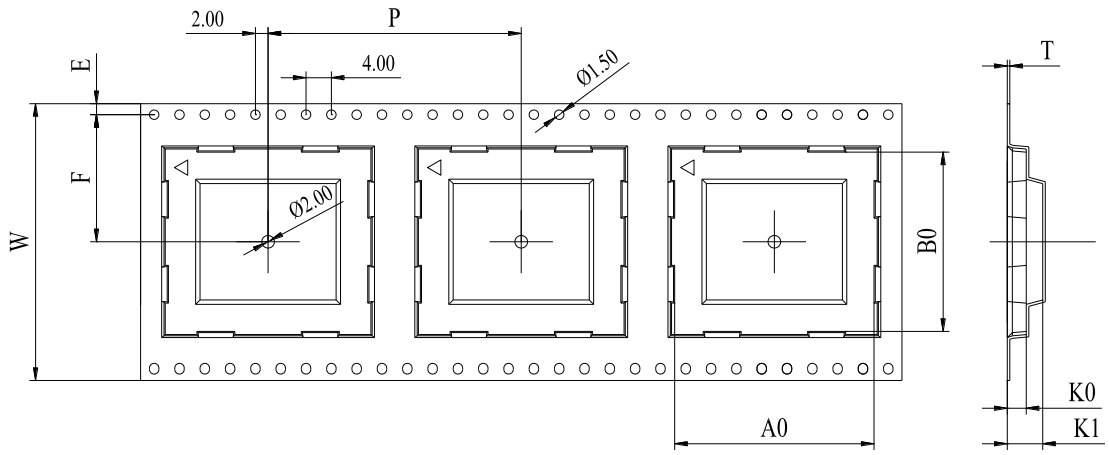


Figure 46: Carrier Tape Dimension Drawing

Table 56: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	24.4	23.4	3.1	6.5	20.2	1.75

7.3.2. Plastic Reel

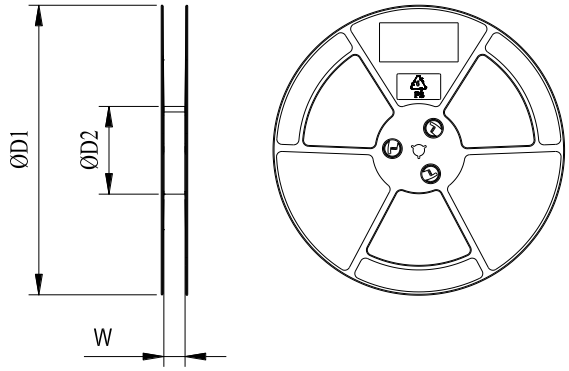


Figure 47: Plastic Reel Dimension Drawing

Table 57: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

7.3.3. Mounting Direction

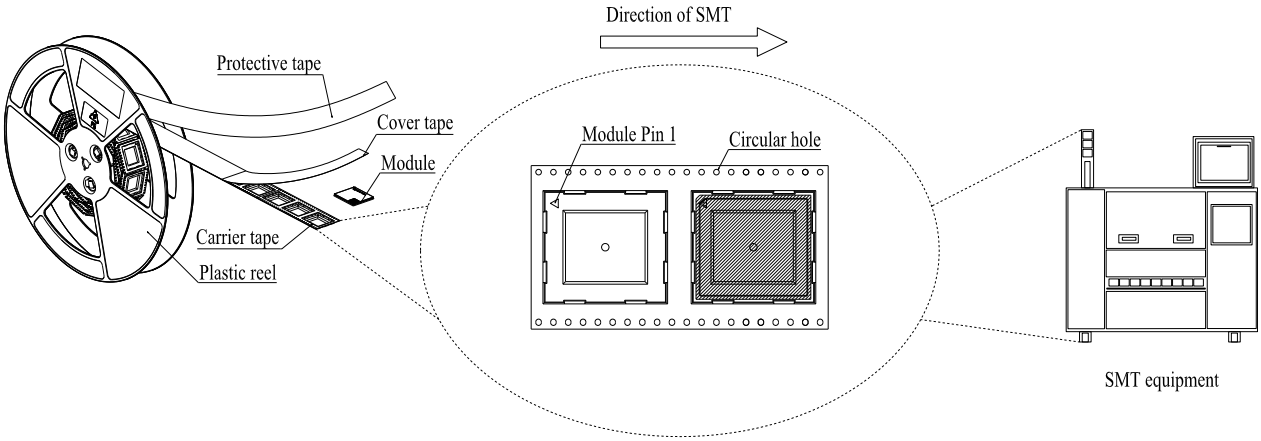
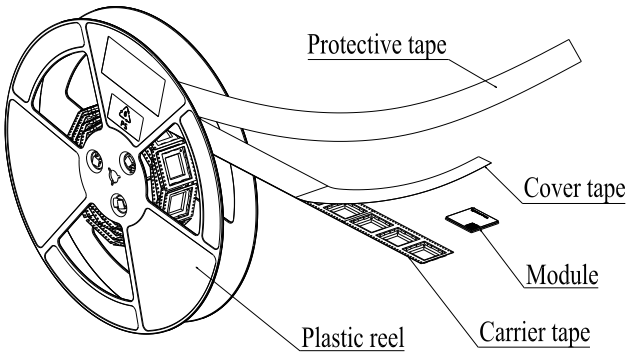


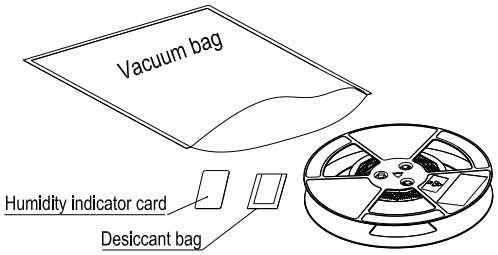
Figure 48: Mounting Direction

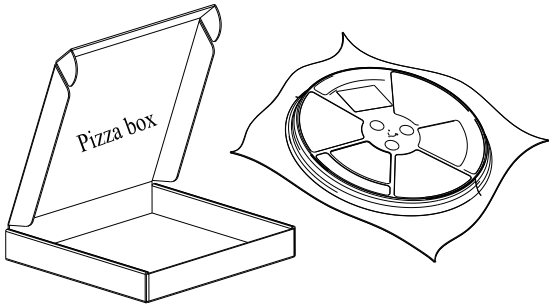
7.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

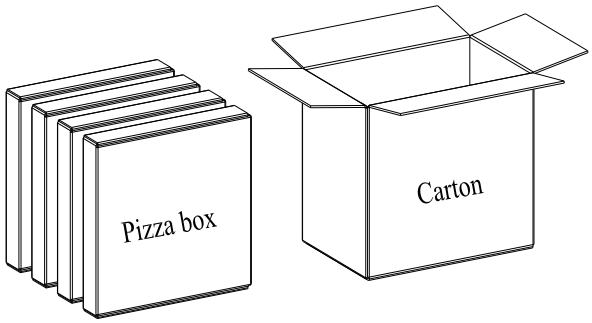


Figure 49: Packaging Process

8 Appendix References

Table 58: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200D&ECx00G&EC600U&EG800G_Series_AT_Commands_Manual
[3] Quectel_ECx00G&EC600U&EG800G_Series_Low_Power_Mode_Application_Note
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_SMT_Application_Note

Table 59: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Channel Multiplexer
CS	Coding Scheme
CTIA	Cellular Telecommunications And Internet Association
CTS	Clear to Send
DL	Downlink
DMA	Direct Memory Access

DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FDD	Frequency Division Duplex
FOTA	Firmware Over-The-Air
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL/FTP Secure
GSM	Global System for Mobile Communications
HB	High Band
HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000
LB	Low Band
LCC	Leadless Chip Carrier (package)
LCD	Liquid Crystal Display
LCM	LCD Module/liquid crystal monitor
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array

LTE	Long Term Evolution
M2M	Machine to Machine
MB	Mid Band
MCU	Microcontroller Unit
ME	Mobile Equipment
MMS	Multimedia Messaging Service
MO	Mobile Originating/Originated
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
MT	Mobile Terminating/Terminated
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
OMTP	Open Mobile Terminal Platform
PA	Power Amplifier
PAP	Password Authentication Protocol
PAM	Power Amplifier Module
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMIC	Power Management IC
PMU	Power Management Unit
POS	Point of Sale

PPP	Point-to-Point Protocol
P_{PP}	Peak Pulse Power
PSM	Power Saving Mode
PRx	Primary Receive
RF	Radio Frequency
RGB	Red, Green, Blue
RTS	Ready To Send/Request to Send
SAW	Surface Acoustic Wave
SMS	Short Message Service
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
Tx	Transmit/Transmission
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage

$V_{IL}max$	Maximum Low-level Input Voltage
$V_{IL}min$	Minimum Low-level Input Voltage
Vnom	Nominal Voltage
V_O	Voltage Output
$V_{OH}max$	Maximum High-level Output Voltage
$V_{OH}min$	Minimum High-level Output Voltage
$V_{OL}max$	Maximum Low-level Output Voltage
$V_{OL}min$	Minimum Low-level Output Voltage
V_{RWM}	Peak Reverse Working Voltage
VSWR	Voltage Standing Wave Ratio

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID XMR2024EC600ULA procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2024EC600ULA”
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Gain	LTE Band 2: 1.59dBi LTE Band 3: 2.00dBi LTE Band 4: 2.00dBi LTE Band 5: 2.13dBi LTE Band 7: 3.00dBi LTE Band 8: 2.98dBi	LTE Band 28: 3.95dBi LTE Band 66: 2.00dBi

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.247 & 15.209 &15.407.

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 4.84dBi antenna. The host manufacturer installing this module into their product must ensure that the final compos it product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Not applicable The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable The module has its own antenna, and doesn't need a hosts printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users" body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application The FCC ID of the module cannot be used on the final product In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: External Antenna

Gain: 3.6 dBi Max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a "unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2024EC600ULA" with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15 209 &15.407 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator

digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.