Name	Type	Initial Condition	Absolute Maximum Ratings		Description
			Minimum Voltage	Maximum Voltage	
Digital Processor Interface (22 terminals)					
Master Clock & Timing					
MCLK	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	master clock
MCLKEN	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	master clock enable: idle (low) or active (high)
Interrupt Logic					
INT	digital output	low	DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	processor interrupt: idle (low) or active (high)
Baseband Transmit & Receive Sections					
TXON	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	baseband transmit section: idle (low) or active (high)
RXON	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	baseband receive section: idle (low) or active (high)
ASM	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	advance state machine
Control Serial Port					
CSFS	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	control serial port framing signal: idle (low) or active (high)
CSDI	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	control serial port data input
CSDO	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	control serial port data output
Baseband Serial Port					
BSIFS	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	baseband serial port input framing signal: idle (low) or active (high)
BSDI	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	baseband serial port data input
BSOFS	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	baseband serial port output framing signal: idle (low) or active (high)
BSDO	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	baseband serial port data output
Audio Serial Port					
ASFS	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	audio serial port framing signal: idle (low) or active (high)
ASDI	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	audio serial port data input
ASDO	digital output	low	DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	audio serial port data output
Ring Tone Input					
GPI	digital input		DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	ring tone input
Register Reset					
ABBRESET	digital input		DGND - 0.3 V	min(2.75 V, VCORE + 0.3 V)	reset input: active (low) or idle (high)

Name	Type	Initial Condition	Absolute Maximum Ratings		Description
			Minimum Voltage	Maximum Voltage	
Power Management Section					
RESET	digital output	low	DGND - 0.3 V	min(5.5 V, VMEM + 0.3 V)	reset output: active (low) or idle (high)
DBBON	digital input		AGND4 - 0.3 V	min(5.5 V, VRTC + 0.3 V)	digital supply regulators: idle (low) or active (high)
VCXOEN	digital input		DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	voltage-controlled crystal oscillator supply regulator: idle (low) or active (high)
Digital Ground					
DGND	digital ground				digital ground
Test Access Port (4 terminals)					
TCK	digital input		DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	test clock
TMS	digital input w/ pull-up		DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	test mode select
TDI	digital input w/ pull-up		DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	test data input
TDO	digital output	low	DGND - 0.3 V	min(5.5 V, VEXT + 0.3 V)	test data output
Substrate (1 terminals)					
AGND0	analog ground				substrate ground
Thermal (36 terminals)					
AGND0 (36)	thermal / analog ground				thermal terminals arranged to form four 3 x 3 arrays in the center of the package

Pins Description of AD6525:

PIN FUNCTIONALITY (NORMAL MODE)					
Group	**[3]Pin Name (Reset)**	**Pins**	**{I/O}**	**Supply**	**Default (Alternative Function)**
CONTROL	CLKIN	1	I	V_{CC}	13 MHz or 26 MHz XTAL System Clock Input (Auto Detect)
	CLKON (H)	1	O	V_{EXT}	Oscillator Power Control Signal (on/off)
	nRESET	1	I	V_{MEM}	System Reset Input
	OSCIN	1	I	V_{DDRTC}	32.768 kHz Crystal Input - Inverted (GND if no Crystal)
	OSCOUT (n/a)	1	O	V_{DDRTC}	32.768 kHz Oscillator Output and Feedback to Crystal
	PWRON (L)	1	O	V_{DDRTC}	Power ON/OFF Control
EBUS I/F	nDISPLAYCS (H)	1	I/O	V_{MEM}	Processor Address - 8M Words (GPO_14 | ADD[23] | LCDCTL | µSM-14)
	ADD[22] (L)	1	I/O	V_{MEM}	Processor Address - 4M Words (GPO_15 | LCDCTL | LCDCTL | µSM-15)
	ADD[21] (L)	1	I/O	V_{MEM}	Processor Address - 2M Words (GPO_27 | µSM-21)
	ADD[20:1] (L)	20	I/O	V_{MEM}	Processor Address Bus
	ADD[0] (L)	1	I/O	V_{MEM}	Processor Address Bus (GPO_28 | LCDCTL)
	DATA[15:8] (L)	8	I/O	V_{MEM}	Processor Data Bus
	DATA[7:0] (L)	8	I/O	V_{MEM}	Processor Data Bus
	nRD (H)	1	I/O	V_{MEM}	Processor Read Strobe
	nHWR / nUBS (H)	1	I/O	V_{MEM}	Processor High Write Strobe (GPO_29)
	nLWR / nLBS (H)	1	I/O	V_{MEM}	Processor Low Write Strobe (GPO_30)
	nWE (H)	1	Tri-O	V_{MEM}	Processor Write Strobe (nWR)
	nROMCS (H)	1	O	V_{MEM}	External ROM Chip Select
	nRAMCS (H)	1	Tri-O	V_{MEM}	(GPO_31)
	nGPCS0 (H)	1	Tri-O	V_{MEM}	(GPO_12 | RNGOUT[0] | µSM-12)
	nGPCS1 (H)	1	Tri-O	V_{MEM}	(GPO_13 | RNGOUT[1] | nDISPLAYCS | µSM-13)
	GPIO_32	1	I/O	V_{MEM}	(DBGACK {O} | µSM-31 {O})
SIM	SIMDATAOP (L)	1	I/O	V_{SIM}	SIM Data Output
	GPIO_22	1	I/O	V_{SIM}	SIM Data Input SIMDATAIP/SIMPROG {I} (µSM-22 {O})
	SIMCLK (L)	1	O	V_{SIM}	SIM Clock
	GPIO_23 (L)	1	I/O	V_{SIM}	SIM Reset SIMRESET {O} (µSM-23 {O})
	GPIO_24 (L)	1	I/O	V_{MEM}	SIM Supply Enable SIMSUPPLY {O} (µSM-24 {O})

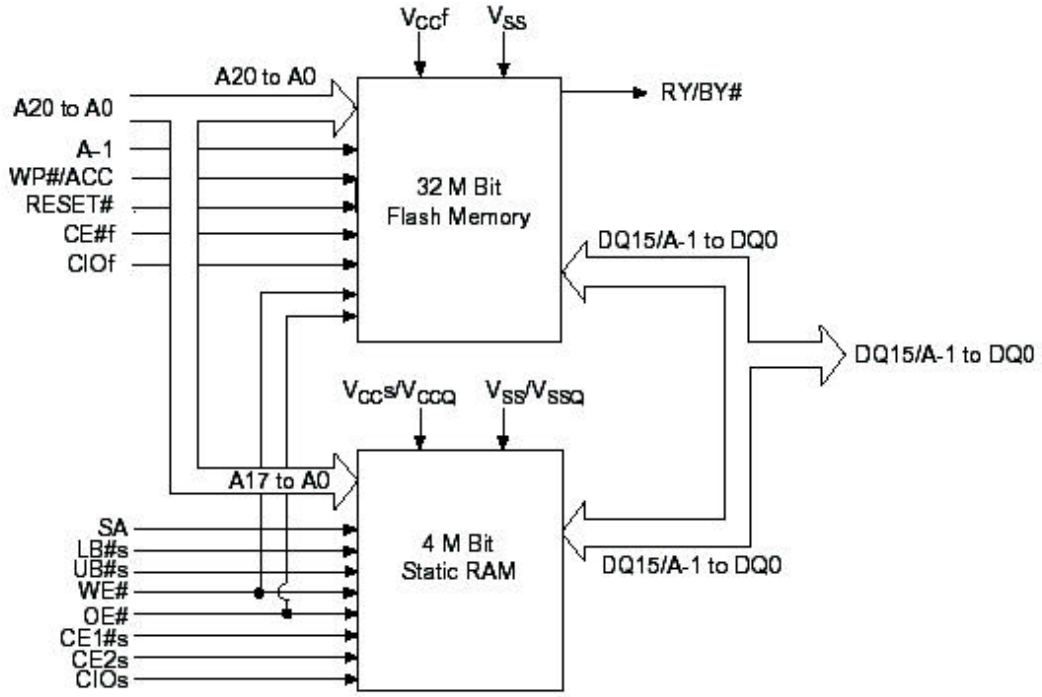
PIN FUNCTIONALITY (NORMAL MODE)					
Group	**[3]Pin Name (Reset)**	**Pins**	**{I/O}**	**Supply**	**Default (Alternative Function)**
RADIO	GPO_0 (L)	1	O	V_{PEG}	Receiver On RxOn (µSM-0)
	GPO_1 (L)	1	O	V_{PEG}	TxOn (µSM-1)
	GPO_2 (L)	1	O	V_{EXT}	OTH_TX_PA | TXEN (µSM-2)
	GPO_3 (L)	1	O	V_{EXT}	RXON1(PONRX1) (µSM-3)
	GPO_4 (L)	1	O	V_{EXT}	OTH_PA_NEGBIAS | RXON2(PONRX2) (µSM-4)
	GPO_5 (L)	1	O	V_{PEG}	ARMSM (µSM-5)
	GPO_6 (L)	1	O	V_{PEG}	ATSM (µSM-6)
	GPO_7 (H)	1	O	V_{EXT}	TXPHASE (µSM-7)
	GPO_8 (H)	1	O	V_{EXT}	OTH_DCS_SWITCH (µSM-8)
	GPO_9 (L)	1	O	V_{EXT}	OTH_DCS_SWITCH | VSYNTHEN (not(GPO_8) | µSM-9)
	GPO_10 (H)	1	O	V_{EXT}	OTH_GSM_SWITCH (µSM-10)
	GPO_11 (L)	1	O	V_{EXT}	OTH_GSM_SWITCH | TxPA (not(GPO_9) | µSM-11)
(Synths)	GPO_16 (L)	1	I/O	V_{EXT}	OTH_TX_GSM | BSEL1/GSMSEL (GSPe_EN2 | DSP PF[5] {I/O} | µSM-16)
	GPO_17 (L)	1	O	V_{EXT}	OTH_TX_DCS | BSEL2/DCSSEL (GSPe_EN3 | µSM-17)
	GPO_18 (L)	1	O	V_{EXT}	OTH_EN | B3-LE/SYNTHEN (GSPe_EN0 | µSM-18)
	GPO_19 (L)	1	O	V_{EXT}	OTH_VLO_EN | AGCEN (GSPe_EN1)
	GPO_20 (L)	1	I/O	V_{EXT}	OTH_DATA | B3-DATA/SDATA (GSPe_DATA | DSP PF[6] {I/O})
	GPO_21 (L)	1	I/O	V_{EXT}	OTH_CLK | B3-CLK/SCLK (GSPe_CLK | DSP PF[7] {I/O})
(VBC)	CLKOUT (L)	1	I/O	V_{PEG}	Clock Output to VBC
	CLKOUT_GATE	1	I	V_{PEG}	Hardware CLKOUT On/Off Switching
	GPO_24 (L)	1	I/O	V_{PEG}	Reset Output VBCRESET
(A-Sport)	ASDI	1	I	V_{PEG}	Auxiliary Serial Port Data Input
	ASFS (L)	1	O	V_{PEG}	Auxiliary Serial Port Framing Signal
	ASDO (L)	1	Tri-O	V_{PEG}	Auxiliary Serial Port Data Output
(B-Sport)	BSDO (L)	1	I/O	V_{PEG}	Baseband Serial Port Data Output
	BSOFS	1	I/O	V_{PEG}	Baseband Serial Port Output Framing Signal
	BSDI	1	I	V_{PEG}	Baseband Serial Port Data Input
	BSIFS	1	I/O	V_{PEG}	Baseband Serial Port Input Framing Signal
(V-Sport)	VSDO (L)	1	I/O	V_{PEG}	Voiceband Serial Port Data Output
	VSDI	1	I/O	V_{PEG}	Voiceband Serial Port Data Input
	VSFS	1	I/O	V_{PEG}	Voiceband Serial Port Framing Signal
Universal	USC[0]	1	I/O	V_{EXT}	See USC Pin Out Table (HSLCLK {O} | TCK {I})
System	USC[1]	1	I/O	V_{EXT}	See USC Pin Out Table (HSLD[0] {O} | TDI {I})
Connector	USC[2]	1	I/O	V_{EXT}	See USC Pin Out Table (HSLD[1] {O} | TDO {O})
	USC[3]	1	I/O	V_{EXT}	See USC Pin Out Table (HSLD[2] {O} | TMS / TCK {I})
	USC[4]	1	I/O	V_{EXT}	See USC Pin Out Table (HSLD[3] {O} | TDI {I} | PF[0] {O})
	USC[5]	1	I/O	V_{EXT}	See USC Pin Out Table (HSLD[4] {O} | TDO {O} | PF[1] {O})
	USC[6]	1	I/O	V_{EXT}	See USC Pin Out Table (TMS {I} | PF[2] {I})

PIN FUNCTIONALITY (NORMAL MODE)					
Group	**[3]Pin Name (Reset)**	**Pins**	**{I/O}**	**Supply**	**Default (Alternative Function)**
MMI	GPIO_0	1	I/O	V_{EXT}	USC7 (GSPb_CLK | MONITOR[0] {O} | µSM-32 {O})
	GPIO_1	1	I/O	V_{EXT}	USC8/(b_RX) (GSPb_OUT/DI | MONITOR[1] {O} | µSM-33 {O})
	GPIO_2	1	I/O	V_{EXT}	(GSPb_EN/FS | BUZZER1{O} | MONITOR[2] {O} | µSM-34 {O})
	GPIO_3	1	I/O	V_{EXT}	USC9/(b_TX / DATA) (GSPb_DO/DI | MONITOR[3] | µSM-35)
	GPIO_4	1	I/O	V_{EXT}	(µSM-TimeOut {O} | MONITOR[4] {O} | µSM-36 {O})
	GPIO_5	1	I/O	V_{EXT}	(CLK17ON {O} | MONITOR[5] {O} | µSM-37 {O})
	GPIO_6	1	I/O	V_{EXT}	(GSPdb_RX) (GSPdb_OUT/DI | MONITOR[6] {O} | µSM-38 {O})
	GPIO_7	1	I/O	V_{EXT}	(GSPdb_CLK | µSM-TimerIn {I} | MONITOR[7] {O} | µSM-39 {O})
	GPIO_8	1	I/O	V_{EXT}	(GSPdb_EN/FS | BUZZER2 {O} | MONITOR[8] {O} | µSM-40 {O})
	GPIO_9	1	I/O	V_{EXT}	(GSPdb_TX / DATA) (GSPdb_DO/DI | MONITOR[9] | µSM-41)
	GPIO_10	1	I/O	V_{EXT}	GPIO or E2-CLK (GSPda_CLK | CacheMiss {O} | MONITOR[10] | µSM-42)
	GPIO_11	1	I/O	V_{EXT}	Digital Temp (GSPda_DATA) or E2-DATA (GSPda_OUT/DI | MONITOR[11] | µSM-43)
	GPIO_12 (L)	1	I/O	V_{EXT}	Service Light or E2-EN (GSPda_EN/FS | BACKLIGHT2 {O} | MONITOR[12] | µSM-44)
	GPIO_13	1	I/O	V_{EXT}	BATDI (GSPda_DATA) (GSPda_DO/DI)
	GPIO_14 (L)	1	I/O	V_{EXT}	DISPCLK {O} (GSPc_CLK | µSM-45 {O})
	GPIO_15 (L)	1	I/O	V_{EXT}	DISPA0 {O} (GSPc_OUT/DI | µSM-46 {O})
	GPIO_16 (L)	1	I/O	V_{EXT}	DISPEN {O} (GSPc_EN/FS | µSM-47 {O})
	GPIO_17 (L)	1	I/O	V_{EXT}	DISPD0 (GSPc_DO/DI)
	GPO_22 (L)	1	Tri-O	V_{EXT}	Backlight Display (BACKLIGHT0)
	GPO_23 (L)	1	I/O	V_{EXT}	Backlight Keyboard (BACKLIGHT1) | DBGRQ {I}
	KEYPADROW[4]	1	I	V_{EXT}	(GPI)
	KEYPADROW[3]	1	I/O	V_{EXT}	(GPI) (GSPda_CLK {I/O})
	KEYPADROW[2]	1	I/O	V_{EXT}	(GPI) (GSPda_OUT/DI {I/O})
	KEYPADROW[1]	1	I/O	V_{EXT}	(GPI) (GSPda_EN/FS {I/O})
	KEYPADROW[0]	1	I/O	V_{EXT}	(GPI) (GSPda_DO/DI {I/O})
	KEYPADCOL[4] (T)	1	I/O	V_{EXT}	(GPO)
	KEYPADCOL[3] (T)	1	I/O	V_{EXT}	(GPO) (GSPdb_CLK {I/O})
	KEYPADCOL[2] (T)	1	I/O	V_{EXT}	(GPO) (GSPdb_OUT/DI {I/O})
	KEYPADCOL[1] (T)	1	I/O	V_{EXT}	(GPO) (GSPdb_EN/FS {I/O})
	KEYPADCOL[0] (T)	1	I/O	V_{EXT}	(GPO) (GSPdb_DO/DI {I/O})

PIN FUNCTIONALITY (NORMAL MODE)					
Group	**[3]Pin Name (Reset)**	**Pins**	**{I/O}**	**Supply**	**Default (Alternative Function)**
JTAG	JTAGEN	1	I	V_{EXT}	JTAG Enable Pull Down
	GPIO_18	1	I/O	V_{EXT}	JTAG Test Clock (TCK {I})
	GPIO_19	1	I/O	V_{EXT}	JTAG Test Mode Select (TMS {I} | DAIRESET)
	GPIO_20	1	I/O	V_{EXT}	JTAG Test Data Input (TDI {I} | DAI[1])
	GPIO_21	1	I/O	V_{EXT}	JTAG Test Data Output (TDO {O} | DAI[0])
POWER	V_{CC}[4:1]	4	PWR	N/A	Core Power Supply Voltage 1.7V to 1.9V
	V_{DDRTC}	1	PWR	N/A	RTC Power Supply 1.0V to 2.0V
	V_{SSRTC}	1	PWR	N/A	RTC Power Supply Return
	V_{SIM}	1	PWR	N/A	SIM Power Supply 1.7V to 3.3V
	V_{MEM}[4:1]	4	PWR	N/A	Memory Power Supply 1.7V to 1.9V and 2.7V to 3.15V Memory Support
	V_{EXT}[4:1]	4	PWR	N/A	External Device Power Supply 2.4V to 3.3V
	V_{PEG1}	1	PWR	N/A	AD6521 Interface Power Supply 1.7V to 3.3V
	GND[11:1]	11	PWR	N/A	Ground (7 Periphery and 4 Core)

D501: Memory chip adopts K5A3240YTCT755. It integrates with 32M Bit Flash Memory and 4M Bit SRAM.

BLOCK DIAGRAM



Pins description is as below:

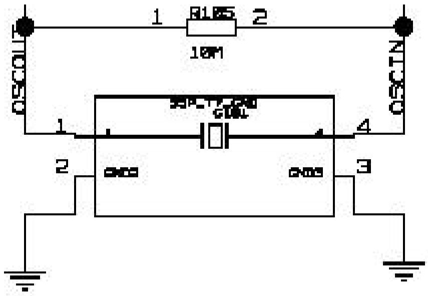
BALL DESCRIPTION

Ball Name	Description
A_0 to A_{17}	Address Input Balls (Common)
A-1, A_{18} to A_{20}	Address Input Balls (Flash Memory)
DQ_0 to DQ_{15}	Data Input/Output Balls (Common)
$\overline{RESET}$	Hardware Reset (Flash Memory)
$\overline{WP}$/ACC	Write Protection / Acceleration Program (Flash Memory)
Vcc_S	Power Supply (SRAM)
Vcc_F	Power Supply (Flash Memory)
Vss	Ground (Common)
$\overline{UB}$	Upper Byte Enable (SRAM)
$\overline{LB}$	Lower Byte Enable (SRAM)
$\overline{BYTE_S}$	$\overline{BYTE_S}$ Control (SRAM)
$\overline{BYTE_F}$	$\overline{BYTE_F}$ Control (Flash Memory)
SA	Address Inputs (SRAM)
$\overline{CE_F}$	Chip Enable (Flash Memory)
$\overline{CS1_S}$	Chip Enable (SRAM Low Active)
$CS2_S$	Chip Enable (SRAM High Active)
$\overline{WE}$	Write Enable (Common)
$\overline{OE}$	Output Enable (Common)
RY/$\overline{BY}$	Ready/Busy (Flash memory)
N.C	No Connection

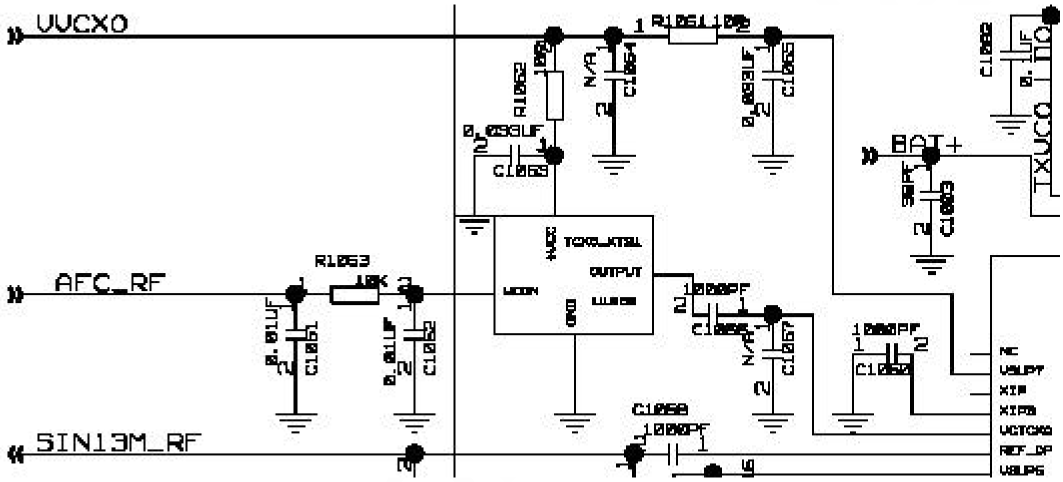
3.3.2 Logic circuit tuning up:

Cannot power on

a. Turn on power supply, test the pin-VBAT of D201, if the voltage is not co rrect, chick the battery or the power supply voltage.
b. Check the battery contacts and see if it was cold soldered or unsoldered.
c. Check the Baseband supply and RF power supply of D201, change another D201 if necessary.
d. Test if 32KHz crystal oscillator clock works, otherwise change G101, and c heck R105.



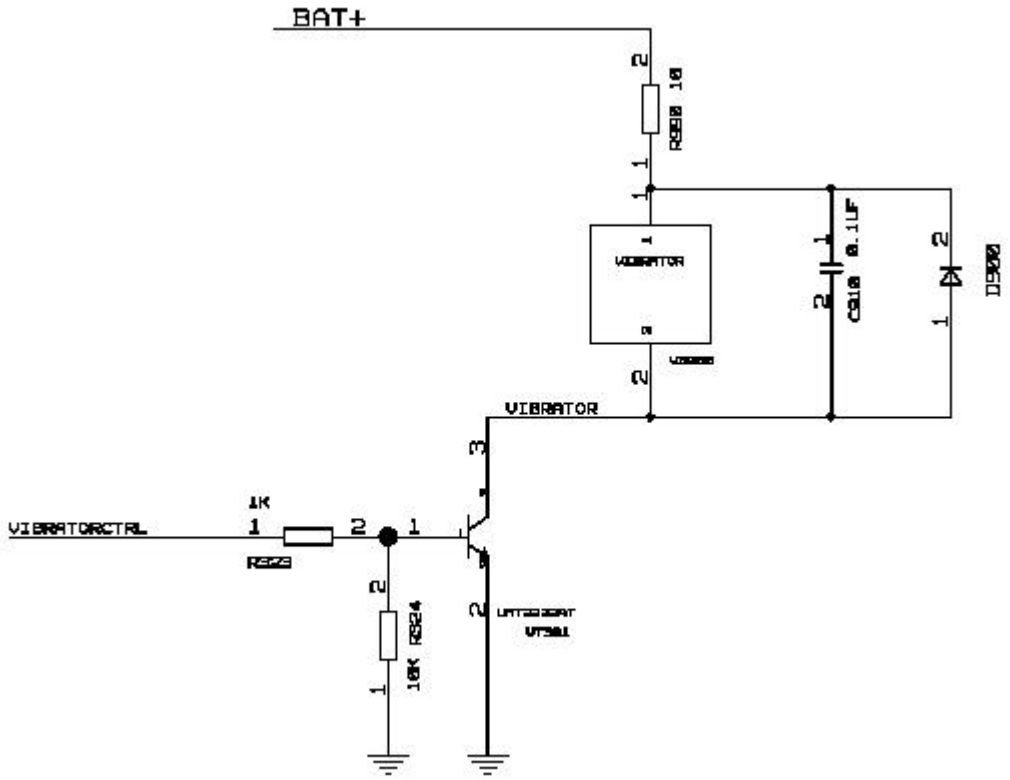
e. Check if 26M oscillator works, otherwise change U1060 and check with C1066, C1068, L1061 and C135; Check VVCXO signal; change another U1060 if necessary.



f. Check the signal from Memory or change another D101, D201, D501 step by step.

<u>Do not vibrate</u>

1. Check with the vibrator. And change it, if necessary.
2. Check if R323, R324, C910, D900, VT301 are cold soldered or unsoldered.
3. Check with the supply voltage VBAT; Check the VIB of D900.



No keypad function:

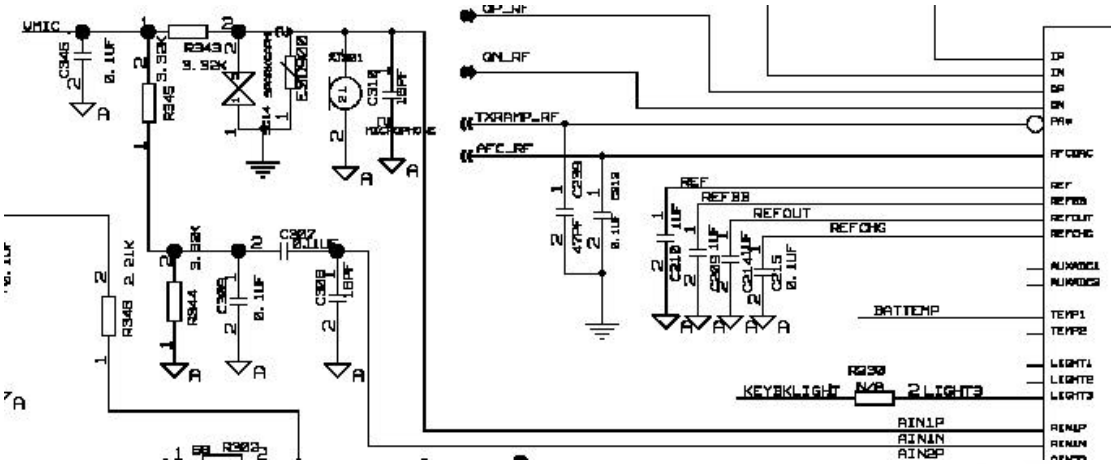
1. Check the signals on the main PCB.
2. Check if the contacts of the keypad are being oxygenated or not smooth.
3. If the signal is incorrect, it might be the problem of the D101.

No hands free function

1. Check if the pieces are cold soldered? unsoldered or damaged.
2. Check with the control signals.
3. Check with the relevant chipset.
4. Check if the problem with earpiece's contact or other component.

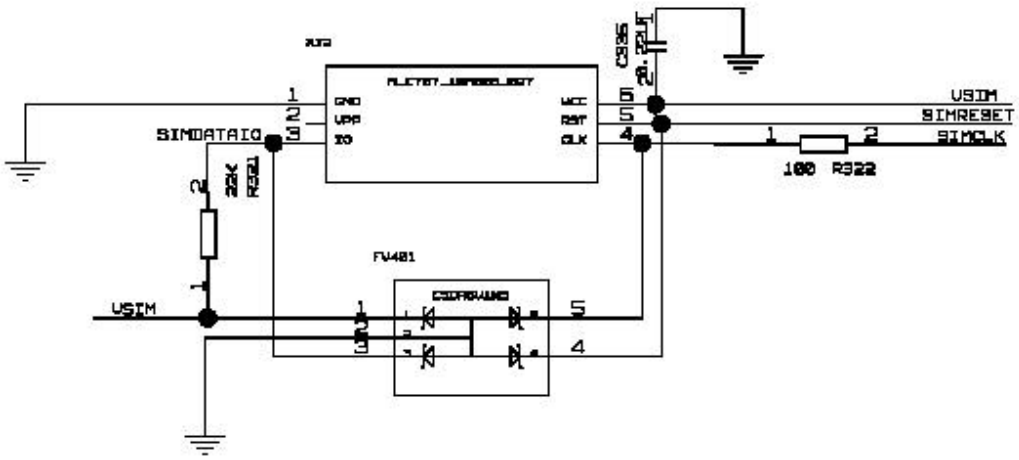
MIC does not work

1. Check if the MIC is place nicely.
2. Test if the signal of MIC contact is right or not.
3. If the signal is incorrect, check the component of the path are soldered wel l or not.
4. Check if voltage of MIC-BIAS is correct or not.
5. In the end check with the relevant chipset.



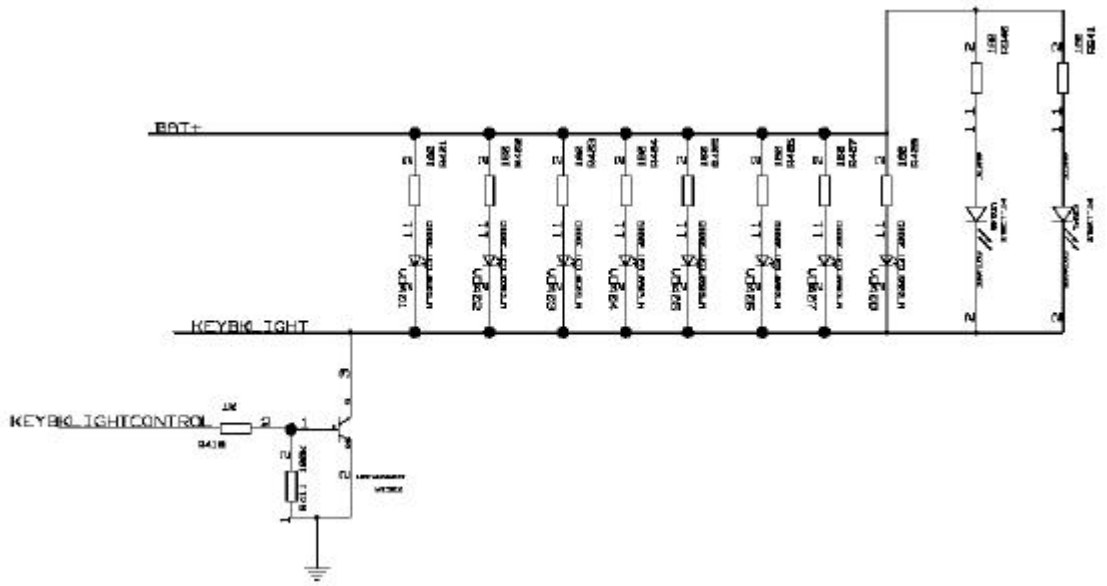
SIM card invalid

1. Check if the SIM can work.
2. Check if the SIM holder is soldered well.
3. Check if the contacts of the SIM can be touched.
4. Check if the contacts of the SIM with the same level.
5. Check the signal of the power supply.
6. Check the clock of the SIM.
7. Check if the data information is correct



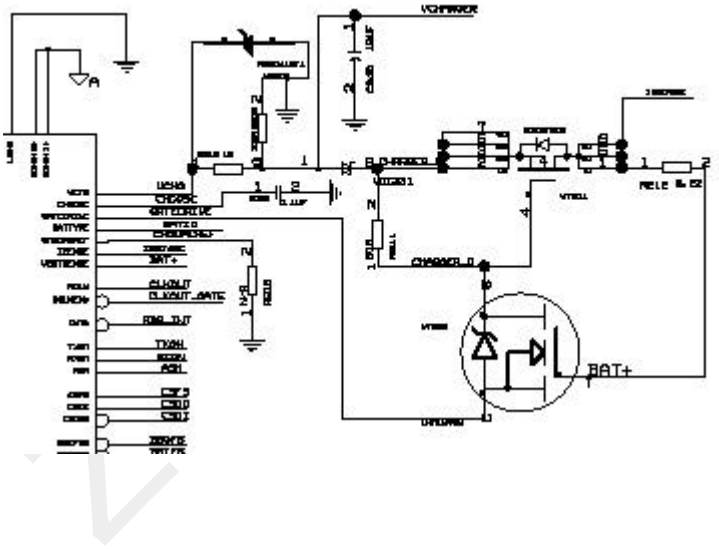
No key backlight or LCD backlight:

1. Check if the backlight is a good one.
2. Check with the revelant component, R410, R411, VT302.

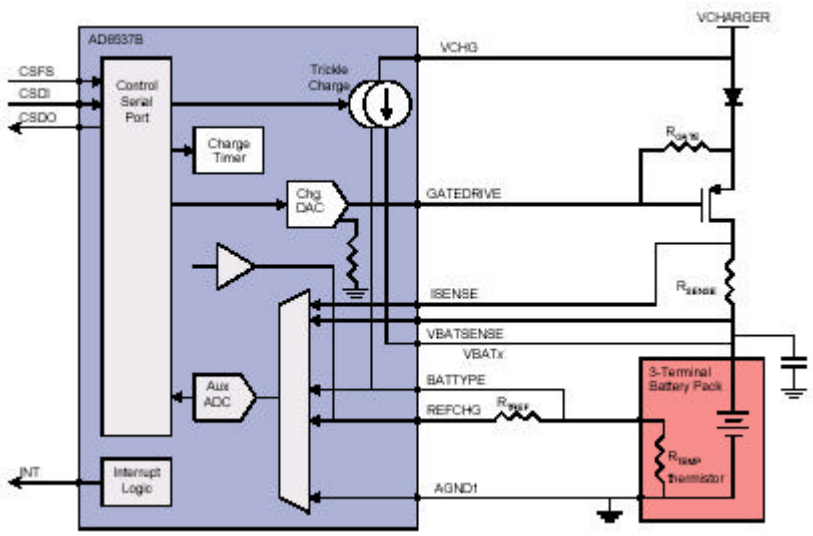


Can not charge:

1. Check with the battery contacts.
2. Check with the charge control chipset D201.
3. Check with the relevant components.



Block diagram of the charging circuit:



冷焊	CS（Cold Solder）	多余焊锡	ES（Excess Solder）	元件歪斜	SP（Skewed Part）
连焊	SS（Solder Short）	元件翘起	TP（Tombstone Part）	元件移动	MP（Misaligned Part）
开路	OT（Open Trace）	元件放反	RP（Reversed Part）	元件丢失	PM（Part Missing）
短路	DS（Direct Short）	多余元件	EP（Extra Part）	元件损坏	DP（Damaged Part）
错件	WP（Wrong Part）	管脚弯曲	BP（Bent Pin）	元件缺陷	CD（Component Defect）
虚焊	PS（Pretense Solder）	焊锡不足	IS（Insufficient Solder）		

4. Antenna Feature of A12

Return Loss

Frequency	**880MHz**	**1880MHz**
Return Loss	-4.11	-12.18

Gain

Frequency(MHZ)	**A12 Antenna**		
	E1	**E2**	**H**
824MHz	-2.56	-1.37	-1.33
880MHz	-0.74	0.14	0.13
1880MHz	1.86	-1.54	0.98
1990MHz	1.39	-1.38	0.39

XY plane is the **E1** plane, that means the Theta=90 degree.
XZ plane is the **E2** plane, that means the Phi = 0 degree.
YZ plane is the **H** plane, that means the Phi = 90 degree.

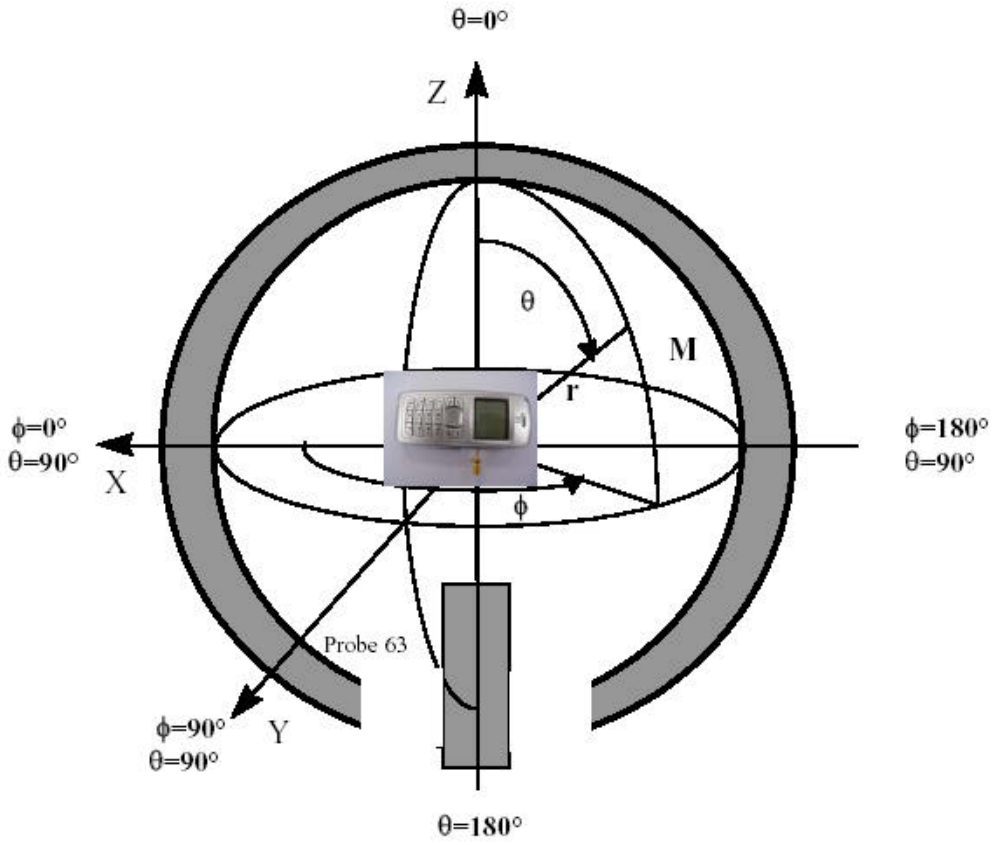


Figure 3: Coordinate System

Efficiency

Frequency (MHz)	**824**	**880**	**1880**	**1990**
Efficiency	34%	51%	61%	57%