Fibocom

PERFECT WIRELESS EXPERIENCE

FIBOCOM SU806-LA

Hardware Guide

Version: V2.0.2

Date: 2022-04-02

Copyright

Notice

The document is subject to update from time to time owing to the product version upgrade or other reasons. Unless otherwise specified, the document only serves as the user guide. All the statements, information and suggestions contained in the document do not constitute any explicit or implicit guarantee.

Trademark

The trademark is registered and owned by Fibocom Wireless Inc.

FCC Regulatory Compliance

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

Notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom wires Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOSU806LA”.
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the ZMOSU806LA cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15C, part 22, part 24, part 27, part 90 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

1 Introduction

1.1 Instruction

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SU806 series module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the SU806 series module and develop products.

1.2 Reference Standards

The design of product refers to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124V10.3.0: ElectroMagnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- IEEE 802.11n WLAN MAC and PHY, October 2009+ IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i:
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0+EDR/2.1/2.1+EDR/3.0/3.0+HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009

1.3 Related Document

FIBOCOM Sx806 Series SMT Design Guide

2 Product Overview

2.1 Product Introduction

SU806 series smart module integrates core components such as Baseband, eMCP, PMU, Transceiver, PA; it supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, GSM and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. SU806 series module is embedded with Android operating system and support various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows. Among them, the production models SU806-CN-01 and SU806-CN-11 support WCDMA Band5.

Table 2-1 Bands supported of SU806-LA

Mode	Band	Note
GSM/GPRS/EDGE	GSM850/EGSM900/DCS1800/PCS1900	-
WCDMA	Band 2/4/5/8	-
FDD-LTE	Band2/3/4/5/7/12/17/28	-
TDD-LTE	Band40/41 (2496-2690MHz)	-
WIFI 802.11b/g/n	2402-2482 MHz	-
BT4.2 LE	2402-2480 MHz	-
GNSS	GPS/BeiDou	-

2.2 Product Specification

SU806 series module is available in 262 LCC+LGA package that includes 146 LCC pins and 116 LGA pins. The dimension is 40.5mm×40.5mm×2.8mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring and multimedia terminals. Its detailed performance is shown in the following table.

Table 2-3 Main performance

Performance	Description

Performance	Description
Power Supply	DC:3.5~4.2V, typical:3.8V
Application processor	Quad-core ARM® Cortex™ A53 MP processor, up to 1.4GHz
Memory	8GB e.MMC+8Gb LPDDR3 16GB e.MMC+16Gb LPDDR3
Power class	Class 4 (33dBm±2dB) for GSM850/EGSM900 Class 1 (30dBm±2dB) for DCS1800/PCS1900 Class E2 (27dBm±3dB) for GSM850/EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800/PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands
GSM/GPRS/EDGE features	R99: CSD transmission rate:9.6kbps,14.4kbps GPRS: Support GPRS multi-slot class 12 Coding formats:CS-1/CS-2/CS-3 and CS-4 4 Rx time slots per frame maximum EDGE: Support EDGE multi-slot class 12 Support GMSK and 8-PSK Uplink encoding formats: CS 1-4 and MCS 1-9 Uplink encoding formats: CS 1-4 and MCS 1-9
WCDMA features	Support 3GPP R9 Support 16-QAM, 64-QAM and QPSK modulation CAT7 HSUPA: Maximum uplink rate 11Mbps CAT14 HSDPA: Maximum downlink rate 21Mbps
LTE features	Support 3GPP R10 Support FDD/TDD CAT4 Support 1.4-20M RF bandwidth Downlink support 2 × 2 MIMO Maximum uplink rate 50Mbps, maximum downlink rate 150Mbps
WLAN features	Support 2.4G WLAN wireless communication, support 802.11b,

Performance	Description
	802.11g, 802.11n, the maximum rate up to 72.2Mbps
Bluetooth	BT4.2 (BR/EDR+BLE)
Satellite positioning	GPS/BeiDou
SMS	Text and PDU modes Point-to-Point MO and MT SMS cell broadcast SMS storage: stored in the module by default
LCD interface	One 4 lane MIPI_DSI interface Support maximum HD+ 60fps (1440x720)
Camera interface	Two 4 lane MIPI_CSI interface, can support three cameras; Main camera can support 13M 30fps at maximum
Audio interface	Audio Input: 3 analog microphone inputs Integrated internal bias Audio output: Class AB stereo headphone output Class AB differential handset output Class D differential speaker amplifier output
USB interface	USB2.0 HS interface, with data transfer rate up to 480 Mbps Supports USB OTG (additional 5V power supply is required), and does not support HUB expansion when serving as USB master device
(U)SIM interface	Two (U)SIM card interfaces supporting (U)SIM card: 1.8/3V adaptive Support dual (U)SIM dual standby single pass, support hot plug (closed by default)
UART interface	Three UART serial interfaces: One 4-line serial interface supporting RTS and CTS hardware flow control One 2-line serial interface (reserved) One 2 line debug serial interface
SDIO interface	Support SD3.0, 4bit SDIO; SD card supports hot plug

Performance	Description
I2C interface	Multiple I2C interfaces, can be used for peripherals such as TP, camera, and sensor
ADC interface	One universal 12bits ADC
RTC	Support
Antenna interface	MAIN antenna, DRX antenna, GNSS antenna, WIFI/BT antenna
Physical characteristics	Dimension: 40.5mm×40.5mm×2.8mm Encapsulation: 146 LCC pin + 116 LGA pin Weight: about 9.0g
Temperature range	Operating temperature: -20°C~75°C Storage temperature: -40°C~95°C
Software update	USB/OTA/SD
RoHS	Comply with RoHS standard

Note:

When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Functional Block Diagram

Functional diagram shows the main hardware features of the SU806 series module：

- Baseband
- Wireless transceiver
- PMU
- Memory
- Peripheral interface

  --Communication expansion interface (USB/UART/I2C/SDIO/SPI)

  --(U)SIM card interface

  --MIPI DSI interface

  --MIPI CSI Interface

  -- Analog audio interface

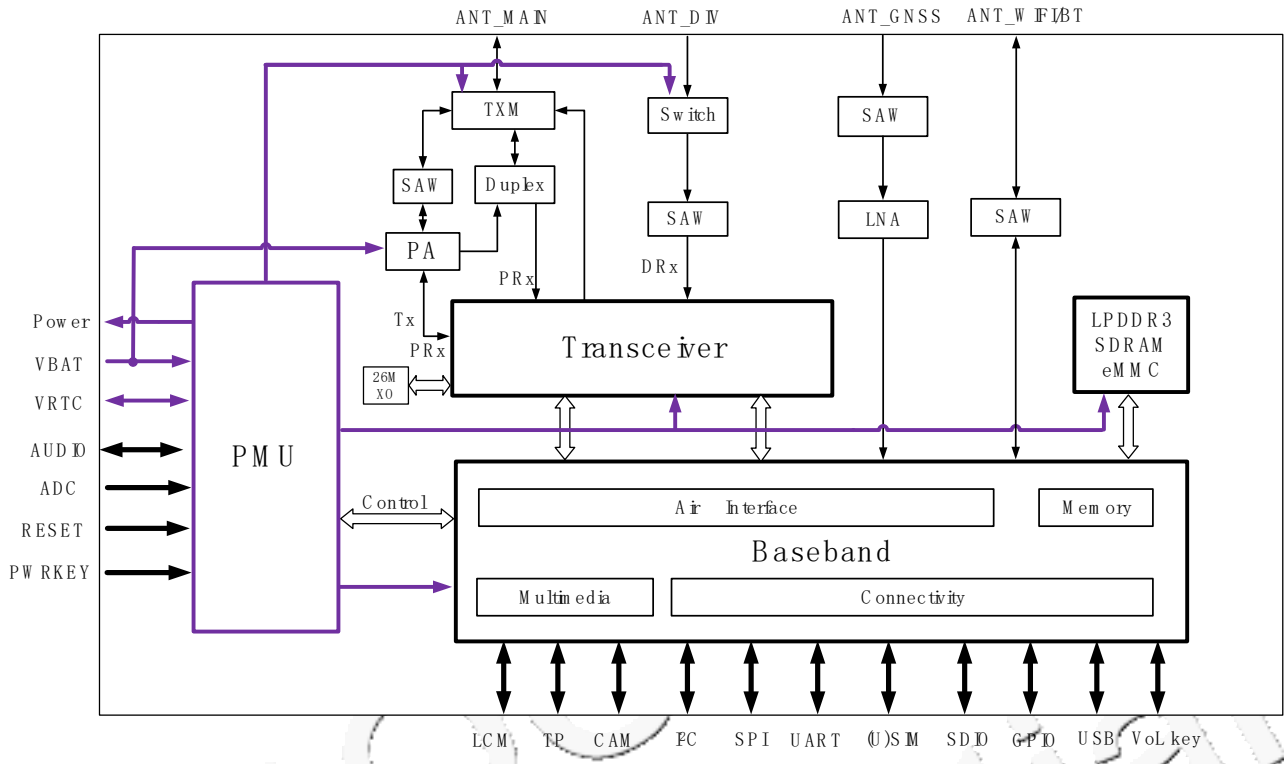

Figure 2-1 Functional block diagram

2.4 Pin Definition

2.4.1 Pin Assignment

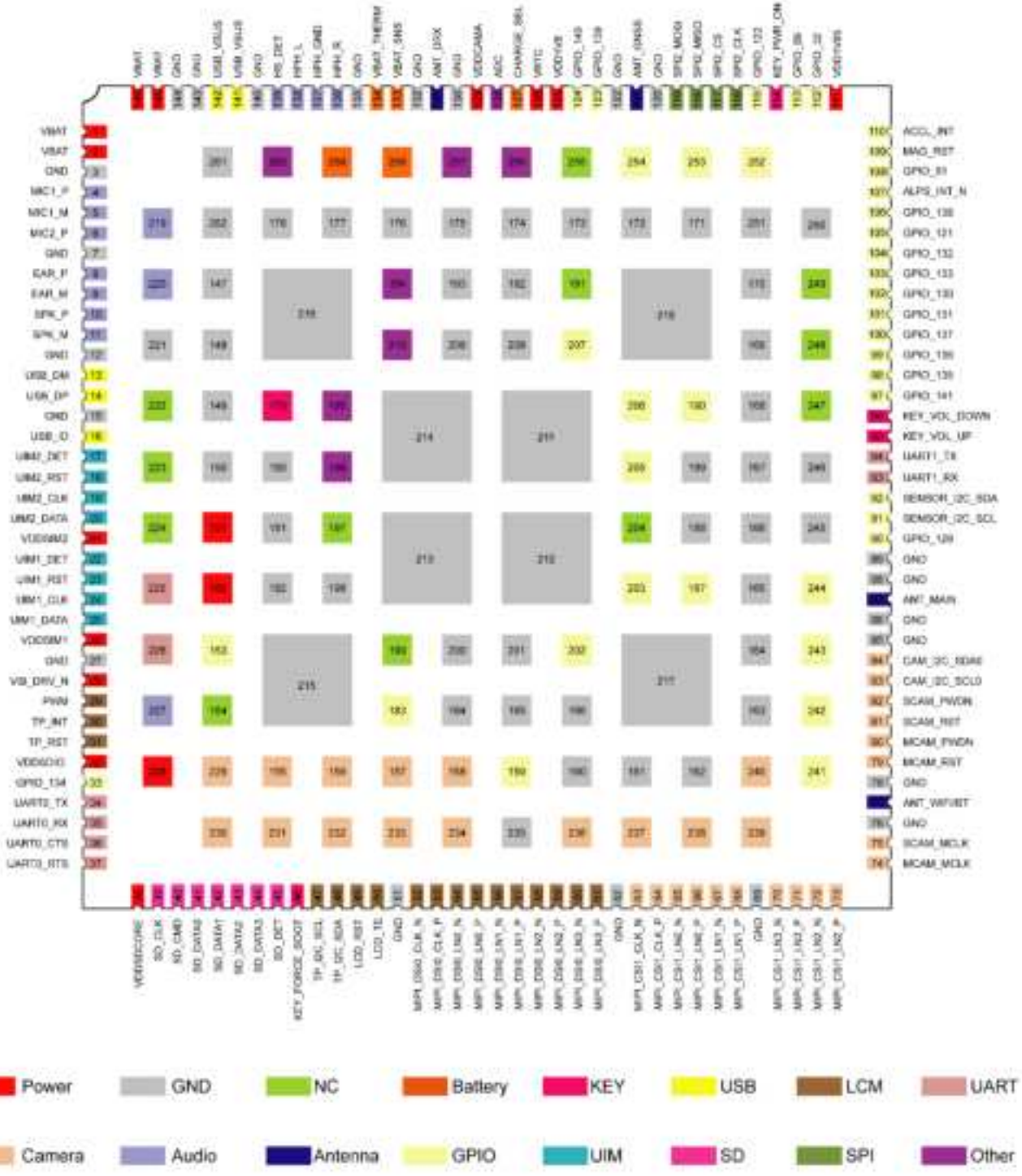

Figure 2-2 Pin assignment (top view)

Note:

"NC" represent No Connect, the pin of this position is reserved and does not need to be connected.

2.4.2 Pin Descriptions

Table 2-4 Parameter and acronym definitions

Symbol	Description
IO	Input/Output
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain

Pin descriptions of SU806 series module are presented in the following table:

Table 2-5 Pin description

Pin Name	Pin Number	I/O	Functional Description	Note
Power supply				
VBAT	1,2,145, 146	PI	Main power input	-
VRTC	126	PI/PO	RTC clock power supply	-
VDD1V85	111	PO	IO voltage output	-
VDD1V8	125	PO	Camera IO voltage output	-
VDDCAMMOT	152	PO	Power output for camera moto	-
VDDSDCORE	38	PO	Power output for SD card	-
VDDSDIO	32	PO	Power output for SD IO	-
VDDSIM1	26	PO	Power output for (U)SIM card 1	-
VDDSIM2	21	PO	Power output for (U)SIM card 2	-

Pin Name	Pin Number	I/O	Functional Description	Note
VDDCAMA	129	PO	Output for camera analog power, 2.8V by default	-
VDDCAMCORE	151	PO	Output for camera digital power	-
VDD2V8	228	PO	2.8V voltage output	-
VIB_DRV_N	28	PO	Vibrator drive output	Can be configured as or LDO mode
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 147, 148, 149, 150, 160-178, 180-182, 184-186, 188, 189, 192, 193, 198, 200, 201, 208, 209, 211-218, 221, 235, 245, 246, 250, 251, 262			Ground
Battery supply interface				
CHARGE_SEL	127	DI	Charge modes select	Use internal charging when it's floating, and turn off internal charging when it's grounded
VBAT_SNS	133	AI	Battery voltage sense	-
VBAT_THERM	134	AI	Battery thermistor output	-
SENSE_N	258	AI	Battery fuel gauge negative input	Reserved
SENSE_P	259	AI	Battery fuel gauge positive input	Reserved
Key				
KEY_FORCE_BOOT	46	DI	Force download	Active low
KEY_VOL_UP	95	DI	Volume+ key	Active low
KEY_VOL_DOWN	96	DI	Volume- key	Active low
KEY_PWR_ON	114	DI	Power key 1	Active low
KEY_RESIN_N	179	DI	Reset key	Active low, support two key(KEY_PWR_ON&

Pin Name	Pin Number	I/O	Functional Description	Note
				KEY_RESIN_N)reset and one key(KEY_PWR_ON) reset
CBL_PWR_N	261	DI	Power on key 2, just have power on function	Active low
(U)SIM card interface				
UIM2_DATA	20	I/O	(U)SIM card 2 data	-
UIM2_CLK	19	DO	(U)SIM card 2 clock	-
UIM2_RST	18	DO	(U)SIM card 2 reset	-
UIM2_DET	17	DI	(U)SIM card 2 hot plug detection	Disabled by default, cannot used as general GPIO
UIM1_DATA	25	I/O	(U)SIM card 1 data	-
UIM1_CLK	24	DO	(U)SIM card 1 clock	-
UIM1_RST	23	DO	(U)SIM card 1 reset	-
UIM1_DET	22	DI	(U)SIM card 1 hot plug detection	Disabled by default, cannot used as general GPIO
SDIO interface				
SD_DET	45	DI	SD card detect	Active low
SD_DATA3	44	I/O	SD card data 3	-
SD_DATA2	43	I/O	SD card data 2	-
SD_DATA1	42	I/O	SD card data 1	-
SD_DATA0	41	I/O	SD card data 0	-
SD_CMD	40	I/O	SD card command	-
SD_CLK	39	DO	SD card clock	-
I2C interface				
SENSOR_I2C_SCL	91	DO	I2C clock	For sensor by default

Pin Name	Pin Number	I/O	Functional Description	Note
SENSOR_I2C_SDA	92	I/O	I2C data	For sensor by default
TP_I2C_SCL	47	DO	I2C clock	For touch panel by default
TP_I2C_SDA	48	I/O	I2C data	For touch panel by default
CAM_I2C_SCL0	83	DO	I2C clock	For rear camera by default
CAM_I2C_SDA0	84	I/O	I2C data	For rear camera by default
CAM_I2C_SCL1	239	DO	I2C clock	For front/depth camera by default
CAM_I2C_SDA1	240	I/O	I2C data	For front/depth camera by default
USB interface				
USB_VBUS	141,142	PI	USB 5V input	-
USB_DP	14	AI/AO	USB HS data+	-
USB_DM	13	AI/AO	USB HS data-	-
USB_ID	16	DI	USB OTG detection	-
UART interface				
UART0_TX	34	DO	UART0 data transmission	-
UART0_RX	35	DI	UART0 data reception	-
UART0_CTS	36	DI	UART0 clear to send	-
UART0_RTS	37	DO	UART0 request to send	-
UART1_TX	94	DO	UART1 data transmission	Debug_UART serial port
UART1_RX	93	DI	UART1 data reception	
UART2_TX	226	DO	UART2 data transmission	Reserved
UART2_RX	225	DI	UART2 data reception	Reserved
SPI interface				
SPI_CLK	116	DO	SPI clock	-

Pin Name	Pin Number	I/O	Functional Description	Note
SPI_CS	117	DO	SPI chip selects	-
SPI_MISO	118	DI	SPI master input slave output	-
SPI_MOSI	119	DO	SPI master output slave input	-
LCD interface				
MIPI_DSI0_CLK_N	52	AO	MIPI display serial interface clock	-
MIPI_DSI0_CLK_P	53	AO		-
MIPI_DSI0_LN0_N	54	AO	MIPI display serial interface lane	-
MIPI_DSI0_ LN0_P	55	AO		-
MIPI_DSI0_ LN1_N	56	AO		-
MIPI_DSI0_ LN1_P	57	AO		-
MIPI_DSI0_LN2_N	58	AO		-
MIPI_DSI0_LN2_P	59	AO		-
MIPI_DSI0_LN3_N	60	AO		-
MIPI_DSI0_LN3_P	61	AO		-
LCD_RST	49	DO	LCD reset signal	-
PWM	29	DO	LCD backlight PWM	-
LCD_TE	50	DI	LCD tearing effect	Keep floating if unused
GPIO_25	190	DO	LCD backlight enable	-
Touch panel interface				
TP_INT	30	DI	LCD TP interrupt signal	-
TP_RST	31	DO	LCD TP reset signal	-
Camera interface				
MIPI_CSI0_CLK_P	229	AI	MIPI rear camera serial interface clock	-
MIPI_CSI0_CLK_N	230	AI		
MIPI_CSI0_LN0_P	155	AI	MIPI rear camera serial	-

Pin Name	Pin Number	I/O	Functional Description	Note
MIPI_CSI0_LN0_N	231	AI	interface lane	
MIPI_CSI0_LN1_P	156	AI		
MIPI_CSI0_LN1_N	232	AI		
MIPI_CSI0_LN2_P	157	AI		
MIPI_CSI0_LN2_N	233	AI		
MIPI_CSI0_LN3_P	158	AI		
MIPI_CSI0_LN3_N	234	AI		
MCAM_MCLK	74	DO	Rear camera master clock	-
MCAM_RST	79	DO	Rear camera reset signal	-
MCAM_PWDN	80	DO	Rear camera power down	-
MIPI_CSI1_CLK_N	63	AI	MIPI front camera serial interface clock	-
MIPI_CSI1_CLK_P	64	AI		-
MIPI_CSI1_LN0_N	65	AI	MIPI front camera serial interface lane	
MIPI_CSI1_LN0_P	66	AI		
MIPI_CSI1_LN1_N	67	AI		
MIPI_CSI1_LN1_P	68	AI		
SCAM_MCLK	75	AI	Front camera master clock	-
SCAM_RST	81	AI	Front camera reset signal	
SCAM_PWDN	82	AI	Front camera power down	
MIPI_CSI1_LN3_N	70	AI	MIPI depth camera serial interface clock	
MIPI_CSI1_LN3_P	71	AI		
MIPI_CSI1_LN2_N	72	AI	MIPI depth camera serial interface lane	-
MIPI_CSI1_LN2_P	73	AI		-
DCAM_MCLK	238	DO	Depth camera master clock	-
DCAM_RST	237	DO	Depth camera reset signal	-

Pin Name	Pin Number	I/O	Functional Description	Note
DCAM_PWDN	236	DO	Depth camera power down	-
Audio interface				
SPK_P	10	AO	Speaker amp + output	-
SPK_M	11	AO	Speaker amp - output	-
EAR_P	8	AO	Earpiece PA + output	-
EAR_M	9	AO	Earpiece PA - output	-
HPH_L	138	AO	Headphone PA left channel output	-
HPH_GND	137	-	Headphone PA ground sensing	-
HPH_R	136	AO	Headphone PA right channel output	-
HPH_DET	139	AI	Headset detection	-
MIC2_P	6	AI	Headset MIC difference input +	-
MIC1_M	5	AI	MIC1 difference input -	-
MIC1_P	4	AI	MIC1 difference input +	-
MIC_BIAS1	219	AO	MIC bias1	-
MIC3_P	220	AI	Sub-MIC difference input +	-
MIC_BIAS2	227	AO	MIC bias2	-
Antenna interface				
ANT_MAIN	87	AI/AO	2G/3G/4G main antenna	-
ANT_DRX	131	AI	Diversity reception antenna	-
ANT_WIFI/BT	77	AI/AO	WIFI/BT antenna	-
ANT_GNSS	121	AI	GNSS antenna	-
Interrupt interface				
ALPS_INT_N	107	DI	Ambient light sensor and proximity sensor interrupt	-

Pin Name	Pin Number	I/O	Functional Description	Note
MAG_RST	109	DO	Magnetic sensor reset	-
ACCL_INT	110	DI	Accelerometer sensor interrupt	-
Other interface				
ADC	128	AI	ADC detection	-
LED_B	194	AI	RGB LED input2	-
LED_G	195	AI	RGB LED input1	-
LED_R	196	AI	RGB LED input0	-
CHG_EN	210	AO	Charge enable	-
ADC4_BAT_ID	260	AI	BAT_ID detection	The PIN260 is NC which product models support internal charging
NFC_CLK	256	DO	NFC clock	Reserved
NFC_DWL_REQ	257	DI	NFC power reset control	Reserved
GPIO interface				
GPIO_134	33	I/O	General Purpose Input and Output.1.8V power domain	INPUT (WPD)
GPIO_129	90	I/O		INPUT (WPD)
GPIO_135	98	I/O		INPUT (WPU)
GPIO_136	99	I/O		INPUT (WPU)
GPIO_137	100	I/O		INPUT (WPU)
GPIO_131	101	I/O		INPUT (WPD)
GPIO_130	102	I/O		INPUT (WPD)
GPIO_133	103	I/O		INPUT (WPD)
GPIO_132	104	I/O		INPUT (WPD)
GPIO_121	105	I/O		OUTPUT
GPIO_138	106	I/O		INPUT (WPU)
GPIO_91	108	I/O		INPUT (WPD)

Pin Name	Pin Number	I/O	Functional Description	Note
GPIO_32	112	I/O		INPUT (WPD)
GPIO_89	113	I/O		OUTPUT
GPIO_122	115	I/O		WPD
GPIO_139	123	I/O		INPUT (WPU)
GPIO_140	124	I/O		INPUT (WPU)
GPIO_88	153	I/O		INPUT (WPU)
GPIO_30	159	I/O		INPUT (WPD)
GPIO_29	183	I/O		INPUT (WPD)
GPIO_27	187	I/O		INPUT (WPD)
GPIO_85	202	I/O		OUTPUT
GPIO_154	203	I/O		INPUT (WPD)
GPIO_155	205	I/O		INPUT (WPD)
GPIO_28	206	I/O		INPUT (WPD)
GPIO_24	207	I/O		INPUT (WPD) Boot configuration doesn't add pull-up
GPIO_11	241	I/O		INPUT (WPD)
GPIO_7	242	I/O		INPUT (WPD)
GPIO_143	243	I/O		INPUT (WPU)
GPIO_10	244	I/O		INPUT (WPD)
GPIO_141	97	I/O		INPUT (WPU)
GPIO_26	252	I/O		INPUT (WPD)
GPIO_22	253	O		INPUT (WPD)
GPIO_23	254	I/O		INPUT (WPD)
NC interface				

Pin Name	Pin Number	I/O	Functional Description	Note
NC	154, 191, 197, 199, 204, 222 to 224, 247 to 249, 255			Keep floating

Note：

H: High-voltage tolerant

L: Low-voltage tolerant

Hiz: High impedance

WPU: Weak pull up

WPD: Weak pull down

The GPIOs with “WPU” aren’t recommended as the enable control of default highly efficient devices. For example, backlight enable of LCM and audio amplifier enable.

3 Application Interface

3.1 Power Supply

The SU806 series module provides four VBAT pins for connecting to external power supply source. The input range of power is 3.5V to 4.2V and the recommended value is 3.8V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. In extreme cases, the peak current of the module can reach 3A instantly and if the power supply capacity is insufficient that VBAT voltage drop below 3.0V instantly, the module may be powered off or restarted. The VBAT voltage drop is shown as the following figure:

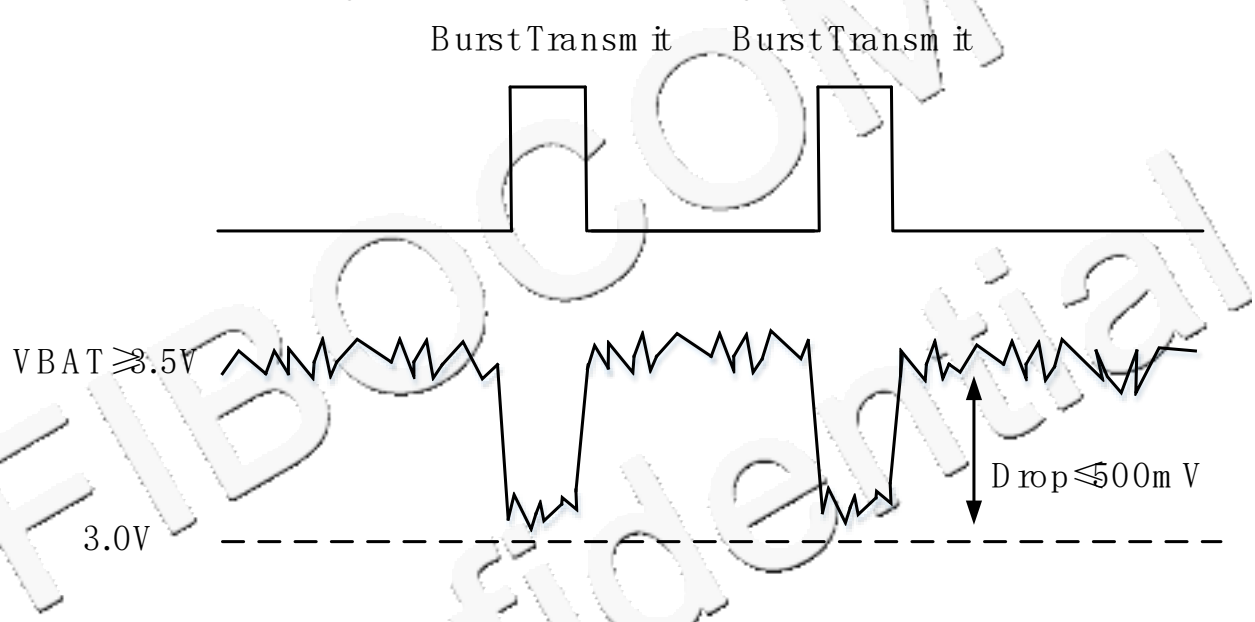

Figure 3-1 VBAT voltage drop

3.1.1 Power Input

External power source supplies the module by VBAT pins. To ensure the instant power voltage is no less than 3.5V, it is recommended to connect two 220μF tantalum capacitors with low ESR and decoupling capacitors of 1uF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides the PCB trace of VBAT should as short and wide as possible (no narrow than 3 mm) and the ground plane of the power section should be flat. That can reduce the equivalent impedance of the VBAT trace and ensure at maximum transmit power, significant voltage drop will not occur at high currents.

Table 3-1 Power supply

Parameter	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.2	V

The reference design of power supply is shown as the following figure:

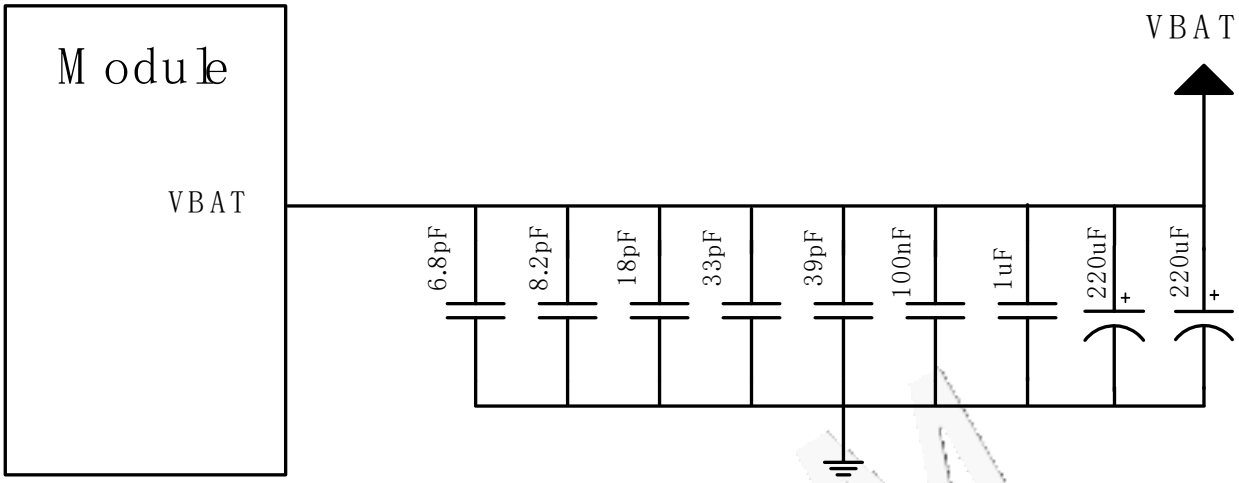

Figure 3-2 Power supply reference design

Table 3-2 Power supply decoupling capacitor design

Recommended Capacitor	Application	Description
220uF x 2	Voltage stabilizing capacitor	To reduce power fluctuations during module operation, it is required to adopt low ESR capacitor LDO or DCDC power requires not less than 440uF capacitor Battery power can be properly reduced to 100 - 220uF capacitor
1uF,100nF	Filter capacitor	Filter clock and digital signal interference
39pF,33pF,18pF,8.2pF,6.8pF	Filter capacitor	Filter high frequency interference

3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When VBAT no power supply, the real time clock is not correct, it is recommended to update system clock from network. The VRTC parameters are as follows:

Table 3-3 VRTC parameters

Parameter	Minimum	Typical	Maximum	Unit
VRTC output voltage	-	3.0	3.35	V

VRTC input voltage	-	3.0	-	V
VRTC input current	-	40	-	uA

The reference design of VRTC pin powered by external power source is shown the following figure:

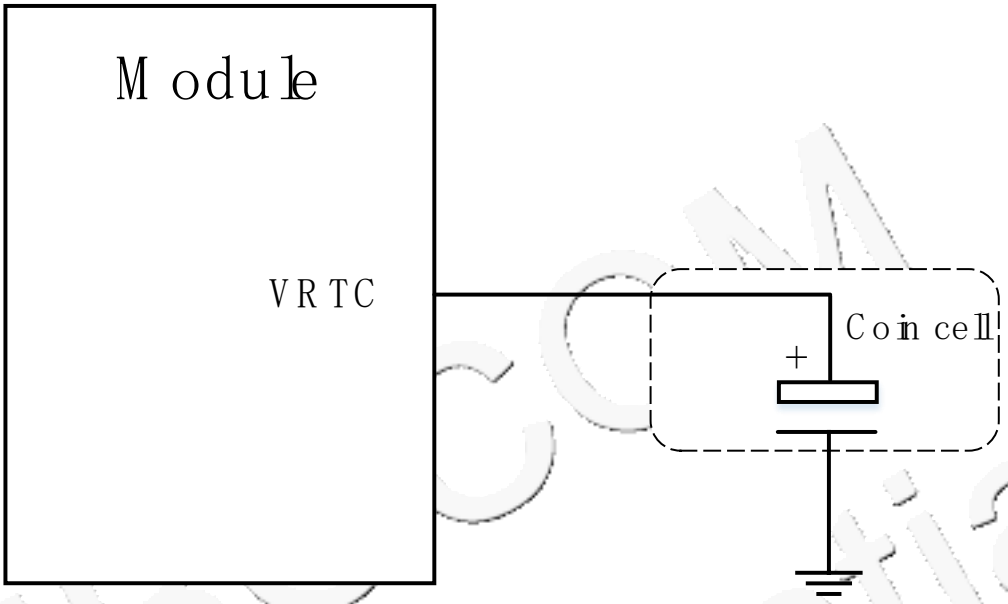

Figure 3-3 VRTC reference design

3.1.3 Power Output

The SU806 series module provides multiple power outputs for peripheral circuits. It is recommended to connect 33pF and 10pF capacitors in parallel with every power to avoid high frequency interference effectively.

Table 3-4 Power output

Pin Name	Programmable Voltage Range (V)	Default Voltage (V)	Drive Current (mA)
VDD1V85	1.75-2.1	1.85	200
VDD1V8	1.10625-1.9	1.8	200
VDDCAMMOT	1.8-3.3	2.8	100
VDDSDCORE	1.8-3.3	3.0	400
VDDSDIO	1.8-3.3	1.8/3	100
VDDSIM1	1.8-3.3	1.8/3	50
VDDSIM2	1.8-3.3	1.8/3	50
VDDCAMA	1.8-3.3	2.8	150

VDDCAMCORE	1.00625-1.4	1.2	400
VDD2V8	1.8-3.3	2.8	200
VIB_DRV_N	1.8-3.3	3.3	100

3.2 Control Signal

3.2.1 Power on/off

SU806 series module provides one-way power on/off control signal to module's power on/off, restart and sleep/wake up. Its pin definition is shown as follow table:

Table 3-5 Power on/off signal

Pin Name	Pin Number	I/O	Description	Note
KEY_PWR_ON	114	DI	Active low, module power on/off, restart, sleep/wake up the module	-
CBL_PWR_N	261	DI	Active low, just have module power on function	-

3.2.1.1 Power on

After module's VBAT pin is powered, pull down KEY_PWR_ON or CBL_PWR_N pin for 3.5s~6s can trigger module power on. The button control and OC drive power on reference design is shown as follows:

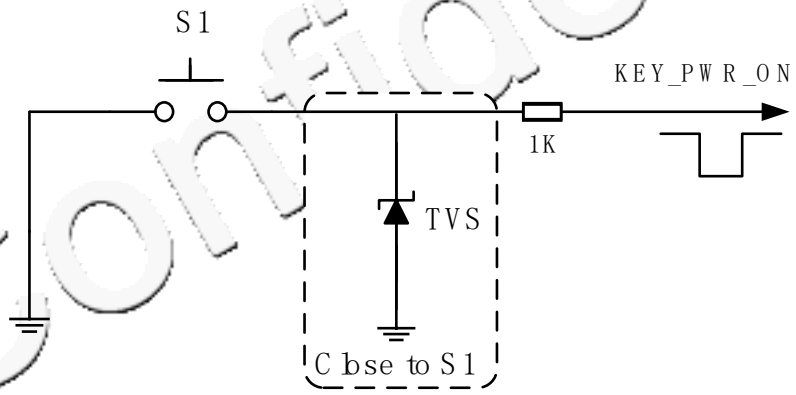

Figure 3-4 Button power on reference design

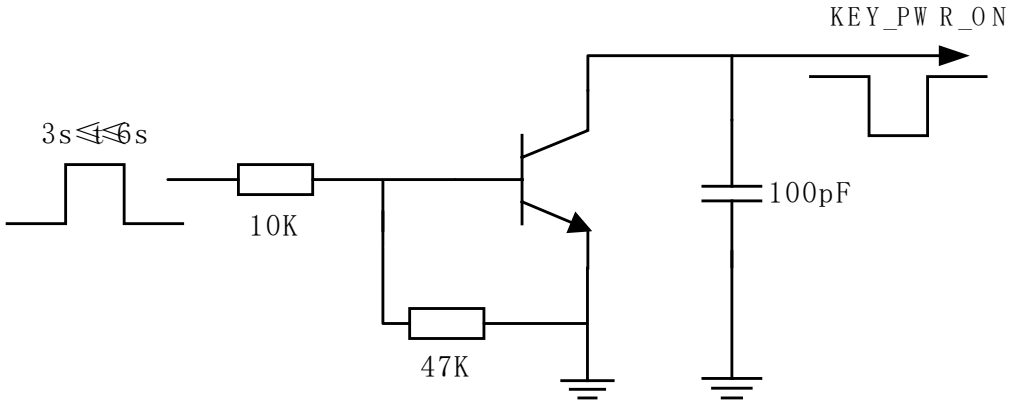

Figure 3-5 OC drive power on reference design

The power on timing is shown as follows:

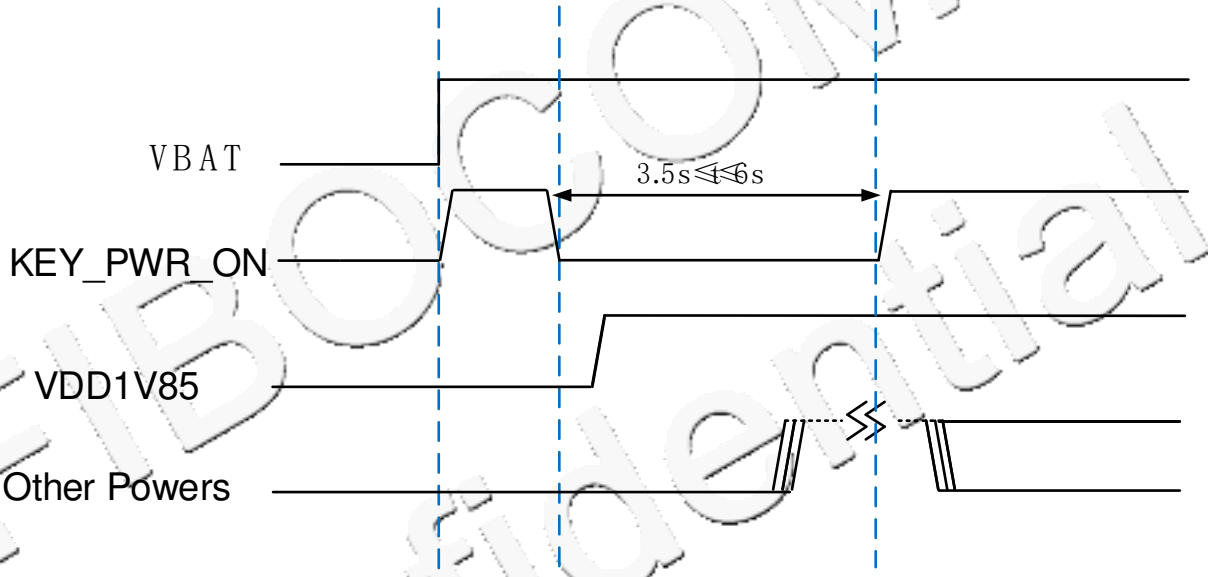

Figure 3-6 Power on timing

3.2.1.2 Power off

Normal power off: when module in operating mode, pull down KEY_PWR_ON pin 0.6s~6s, user interface will display selection box (select power off or restart).

Note:

When the system is abnormal or shutdown, can use force power off method to power off the module, please use normal method generally, otherwise may cause data loss and other anomalies.

3.2.1.3 Sleep/Wake up

When module in standby mode, pull down KEY_PWR_ON pin 0.1s~0.5s and then release it, module will

enter sleep mode. When module in sleep mode, pull down KEY_PWR_ON pin 0.1s~0.5s and then release it, module can be waked up.

3.2.2 Reset

Support one key (KEY_PWR_ON) reset and two key (KEY_PWR_ON & KEY_RESIN_N) reset; and two key reset mode is default.

One key (KEY_PWR_ON) reset: when module in operating mode, pull down KEY_PWR_ON pin 0.6s~6s, user interface will display selection box (select power off or restart); pull down KEY_PWR_ON pin 7s~10s module will be forced reset. The reset timing is shown as follows:

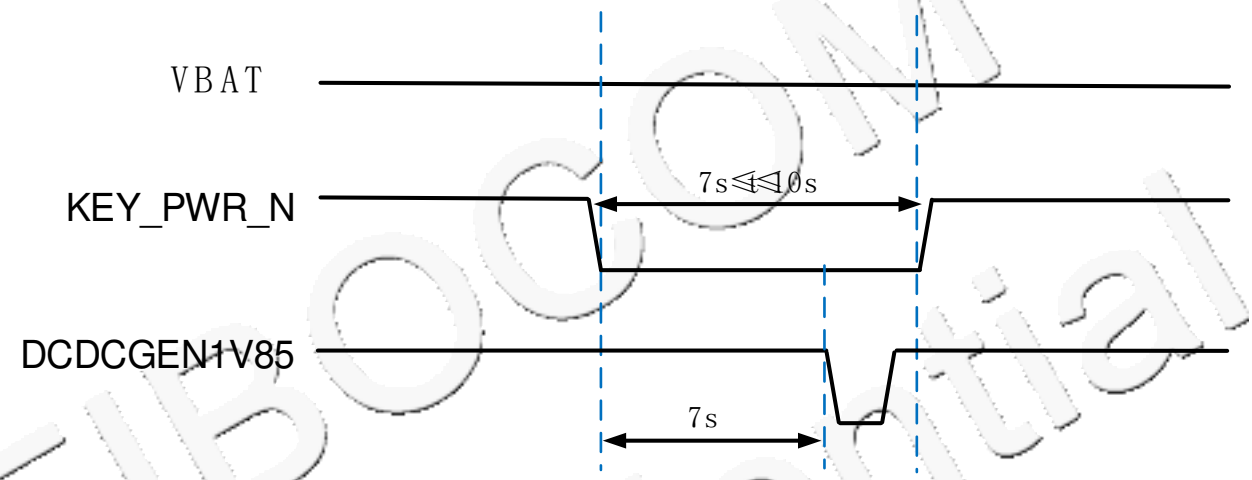

Figure 3-7 Force reset timing

Two key (KEY_PWR_ON & KEY_RESIN_N) reset: when module in operating mode, pull down KEY_PWR_ON and KEY_RESIN_N pin 7s~10s at the same time, module will be forced reset. The reset reference circuit please refer to power on circuit design.

3.2.3 Volume Control

KEY_VOL_UP and KEY_VOL_DOWN is the volume up and volume down control; its circuit design can refer to the power on keypad circuit.

3.3 USB

The SU806 series module supports one USB 2.0 interface; USB2.0 supports HS (480Mbps) modes and compatible USB1.1 FS (12Mbps). Supports USB OTG (additional 5V power supply is required), and does not support HUB expansion when serving as USB master device. Its pin definition is shown in the following table:

Table 3-6 USB 2.0 pin definition

Pin Name	Pin Number	I/O	Description	Note
USB_VBUS	141,142	PI	USB VBUS 5V input	-
USB_DP	14	AI/AO	USB HS data +	-
USB_DM	13	AI/AO	USB HS data -	-
USB_ID	16	DI	USB OTG detection	-

The reference design of USB 2.0 is show as follow figure:

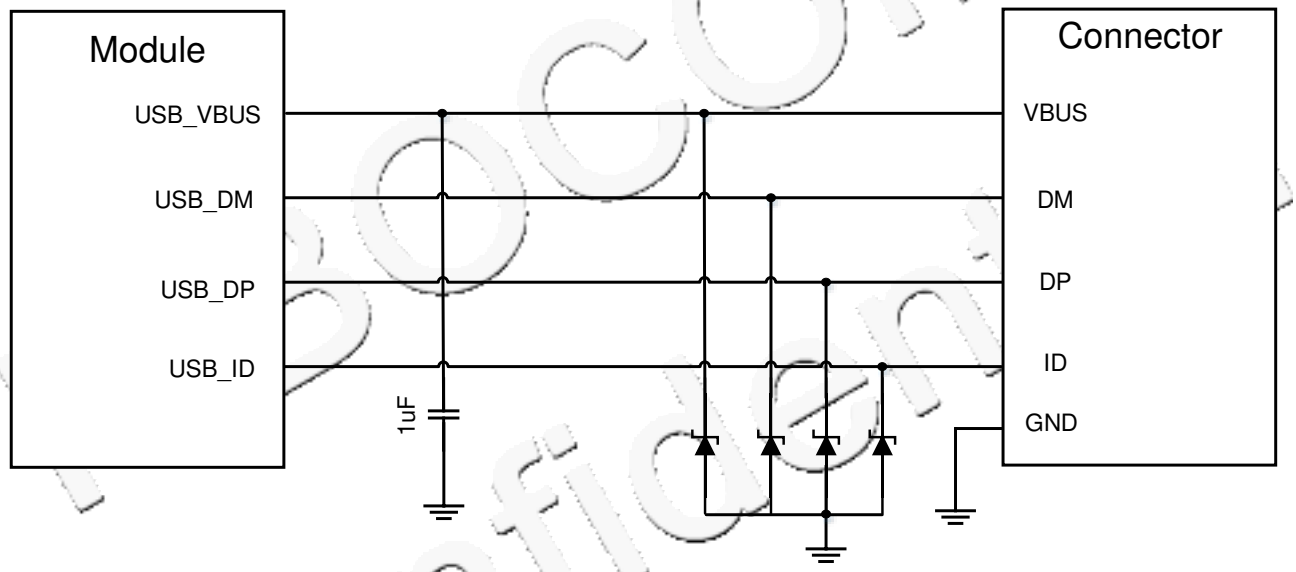

Figure 3-8 USB 2.0 reference design

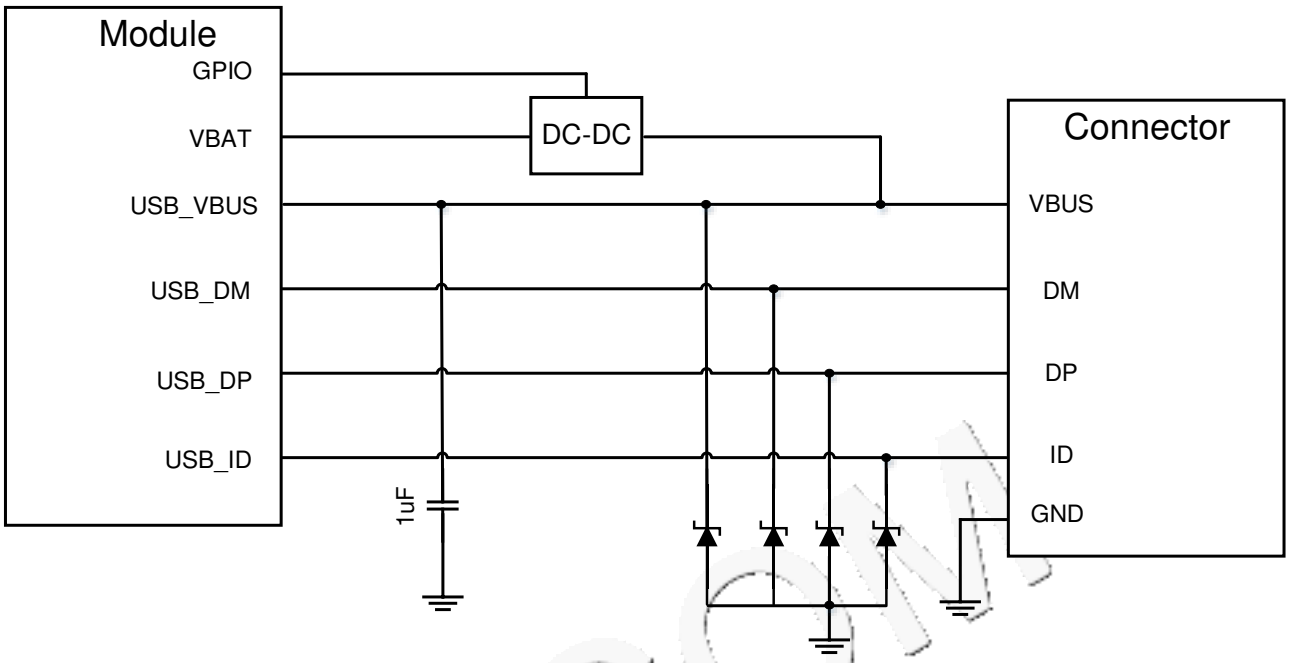

Figure 3-9 USB 2.0 reference design (with OTG function)

Note:

1) Please choose junction capacitor less than 1pF for ESD protection device of USB_DP/DM

2) USB_DP and USB_DM are high-speed differential signal. The highest transmission rate is 480Mbps. Please pay attention to the following requirements in PCB layout:

- USB_DP and USB_DM signal cables are required to be parallel and equal in length (differential cable length controlled within 2 mm), while the right-angle route shall be avoided, and differential 90Ω impedance shall be controlled.
- USB2.0 differential signal cable laid on the signal layer nearest to the ground, with well grounded.

3) Please choose DC-DC that satisfy output is 5V when support OTG function.

Table 3-7 Length of USB differential signal line in module

Pin Name	Pin Number	Length (mm)	Length Difference (DP-DM) mm
USB_DP	14	11.33134	0.40037
USB_DM	13	10.93097	

3.4 UART

SU806 series module defines three UART ports，all are 1.8V voltage domain ,the function of UART2 has not achieve at present. Its pin definition is shown in the following table:

Table 3-8 UART interface pin definition

Pin Name	Pin Number	I/O	Description	Note
UART0_TX	34	DO	UART0 data transmission	-
UART0_RX	35	DI	UART0 data reception	-
UART0_CTS	36	DI	UART0 clear to send	-
UART0_RTS	37	DO	UART0 request to send	-
UART1_TX	94	DO	UART1 data transmission	Debug_UART serial port by default
UART1_RX	93	DI	UART1 data reception	
UART2_TX	226	DO	UART2 data transmission	Reserved
UART2_RX	225	DI	UART2 data reception	Reserved

Note:

Please do not pull down UART1_TX before module power on, otherwise module will not be powered on normally.

All series ports are 1.8V voltage domain, if the peripheral is other voltage domain, please add level shift.

Level shift reference design is show in the following figure:

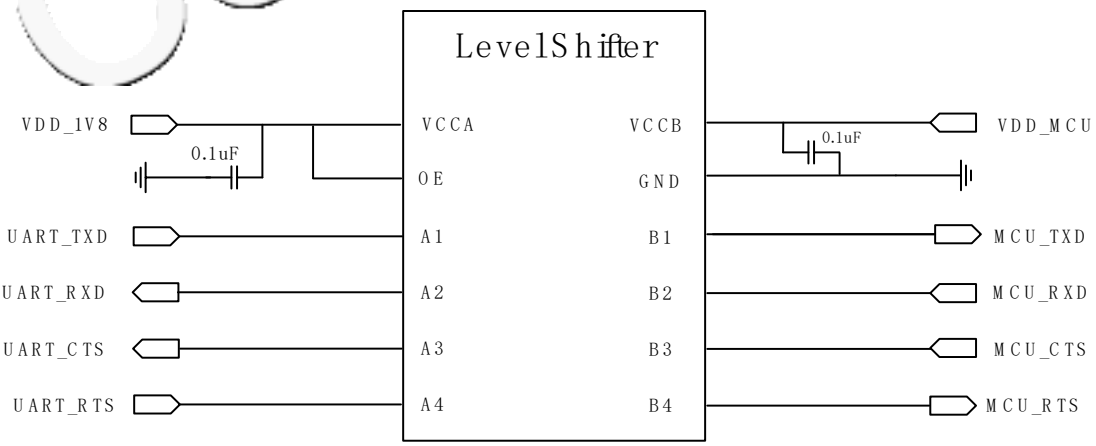

Figure 3-10 Level shift reference design

The other level translator circuit is shown as Figure 3-11, The rest input and output circuit design of dotted line please refer to solid line part, but pay attention to signal connection direction.

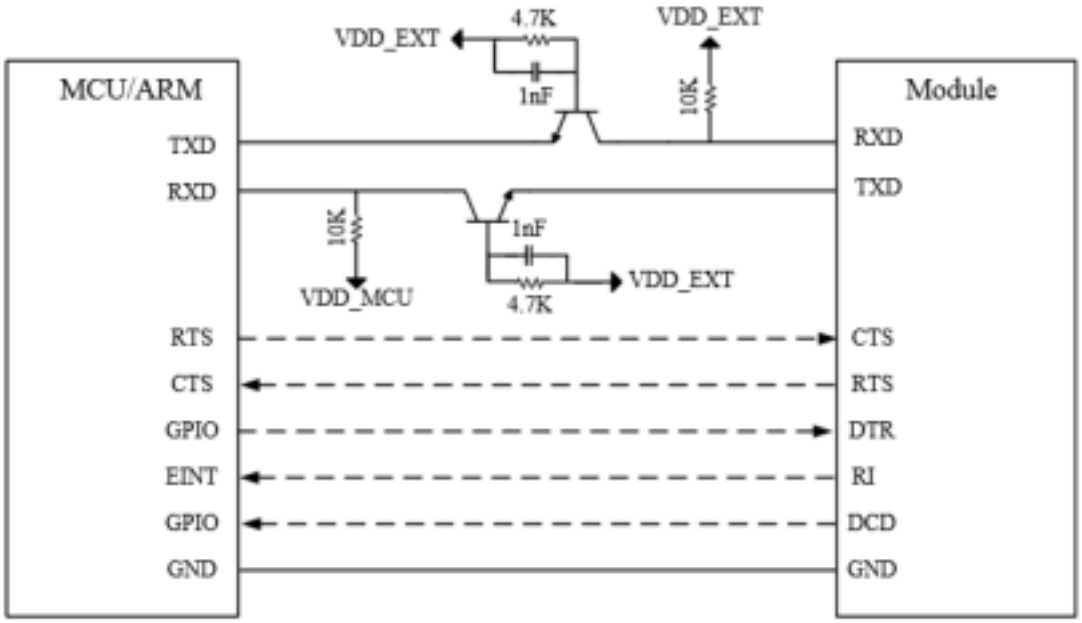

Figure 3-11 Level shift reference design 2

3.5 SPI

SU806 series module provides one master only SPI interface, the pin definition is shown in the following table:

Table 3-9 SPI pin definition

Pin Name	Pin Number	I/O	Description	Note
SPI_CLK	116	DO	SPI clock	-
SPI_CS	117	DO	SPI chip selects	-
SPI_MISO	118	DI	SPI master input slave output	-
SPI_MOSI	119	DO	SPI master output slave input	-

3.6 (U)SIM

The SU806 series module supports two (U)SIM cards, dual-SIM dual-standby single-active (default double) and both support hot plug (default off).

Table 3-10 (U)SIM pin definition

Pin Name	Pin Number	I/O	Description	Note
UIM1_DATA	25	I/O	(U)SIM 1 data signal	-
UIM1_CLK	24	DO	(U)SIM 1 clock signal	-
UIM1_RST	23	DO	(U)SIM 1 reset signal	-
UIM1_DET	22	DI	(U)SIM 1 plug detection	Disabled by default, cannot used as general GPIO
UIM2_DATA	20	I/O	(U)SIM 2 data	-
UIM2_CLK	19	DO	(U)SIM 2 clock	-
UIM2_RST	18	DO	(U)SIM 2 reset	-
UIM2_DET	17	DI	(U)SIM 2 plug detection	Disabled by default, cannot used as general GPIO
VDDSIM1	26	PO	(U)SIM 1 power supply	-
VDDSIM2	21	PO	(U)SIM 2 power supply	-

(U)SIM reference design is shown as the following figure:

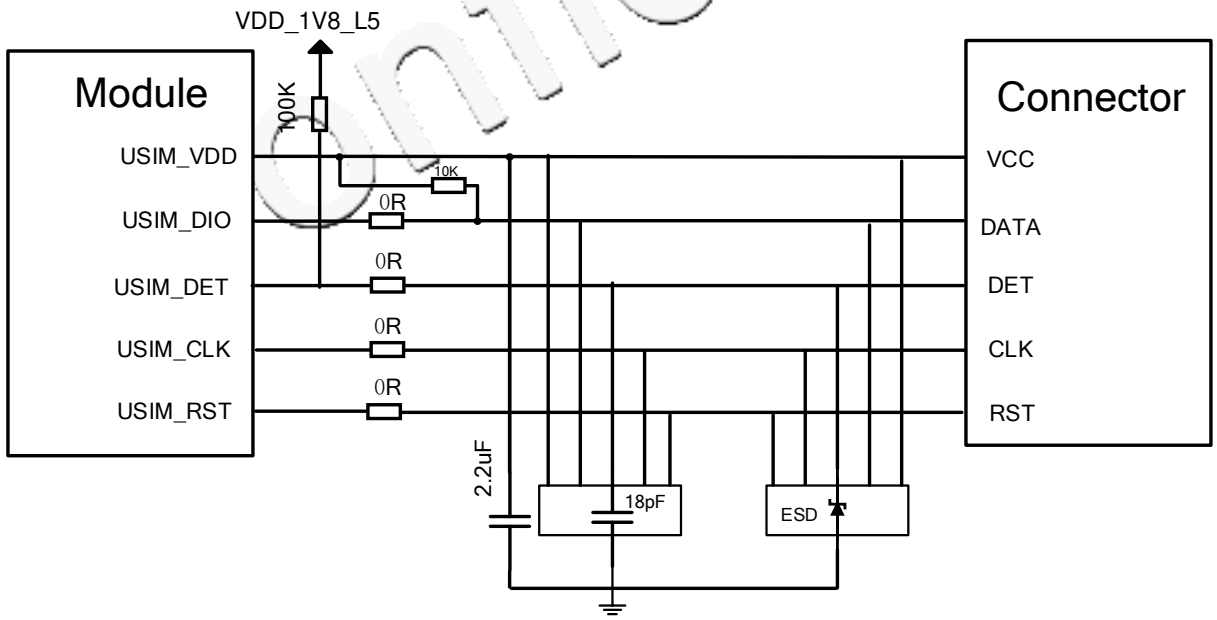

Figure 3-12 (U)SIM reference design

(U)SIM card design notice:

1) The length from the (U)SIM card holder to module should less than 100mm.

2) The layout and routing of the (U)SIM card must be kept away from EMI interference sources such as RF antenna and digital switch power.

3) The decoupling capacitors of the (U)SIM card signal and the ESD device should be placed close to the card holder.

3.7 SDIO

SU806 series module supports one SDIO interface. The pin definition is shown in the following table:

Table 3-11 SDIO pin definition

Pin Name	Pin Number	I/O	Description	Note
SD_DET	45	DI	SD card detect	Active low
SD_DATA3	44	I/O	SD card data3	-
SD_DATA2	43	I/O	SD card data2	-
SD_DATA1	42	I/O	SD card data1	-
SD_DATA0	41	I/O	SD card data0	-
SD_CMD	40	I/O	SD card command	-
SD_CLK	39	DO	SD card clock	-
VDDSDCORE	38	PO	Power for SD card	-
VDDSDIO	32	PO	Power for SDIO interface	-

SDIO interface reference design is show in the following figure:

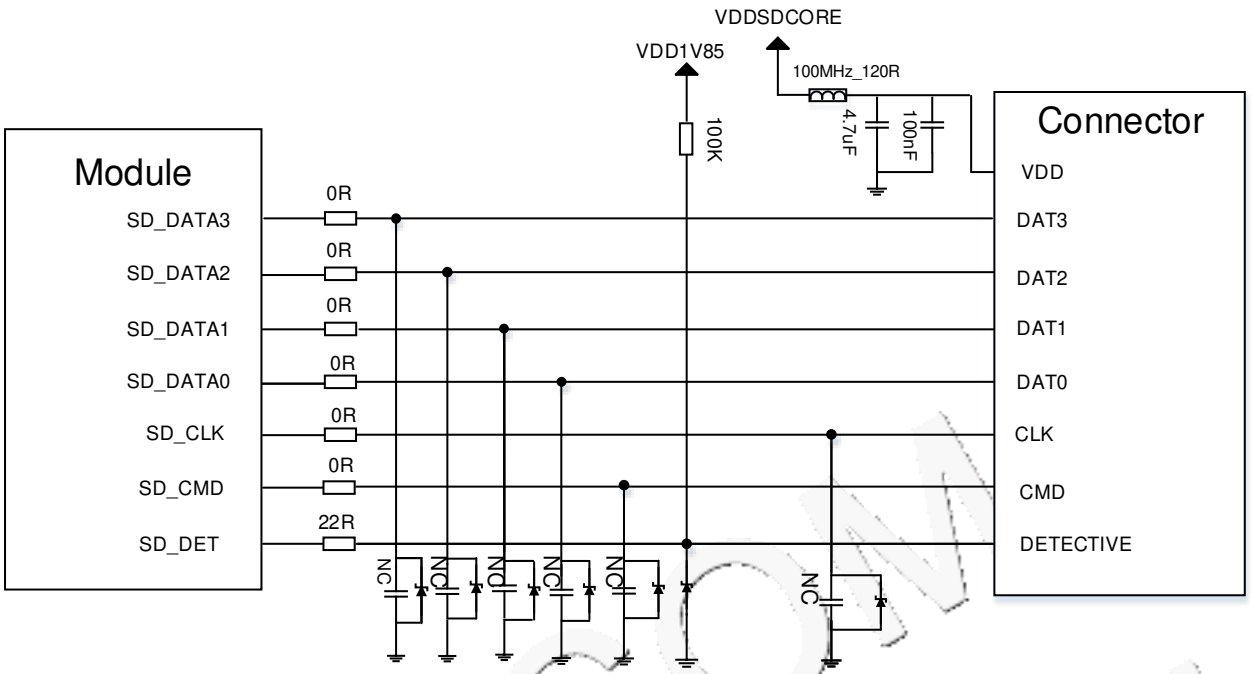

Figure 3-13 SDIO reference design

SDIO design notice:

1) VDDSDCORE is the SD card peripheral driving power and can provide about 400mA current. SD3.0 need external LDO with power driver ability more than 800mA.
2) Match all SD signals length and pay attention to controlling the width of trace.
3) Pull up SD_DET with VDD1V85.
4) SDIO is a high-speed digital signal cable, needs to be shielded.

3.8 GPIO

SU806 series module have rich GPIOs and the interface level is 1.8V. The pin definition is shown in the following table:

Table 3-12 GPIO list

Pin Name	Pin Number	H/L/Hiz After Reset	After Reset	Interrupt Function
GPIO_134	33	L	INPUT(WPD)	YES
GPIO_129	90	L	INPUT(WPD)	YES
GPIO_135	98	H	INPUT(WPU)	YES
GPIO_136	99	H	INPUT(WPU)	YES
GPIO_137	100	H	INPUT(WPU)	YES

Pin Name	Pin Number	H/L/Hiz After Reset	After Reset	Interrupt Function
GPIO_131	101	L	INPUT(WPD)	YES
GPIO_130	102	L	INPUT(WPD)	YES
GPIO_133	103	L	INPUT(WPD)	YES
GPIO_132	104	L	INPUT(WPD)	YES
GPIO_121	105	L	OUTPUT	YES
GPIO_138	106	H	INPUT(WPU)	YES
GPIO_91	108	L	INPUT(WPD)	YES
GPIO_32	112	L	INPUT(WPD)	YES
GPIO_89	113	L	OUTPUT	YES
GPIO_122	115	Hiz	WPD	YES
GPIO_139	123	H	INPUT(WPU)	YES
GPIO_140	124	H	INPUT(WPU)	YES
GPIO_88	153	H	INPUT(WPU)	YES
GPIO_30	159	L	INPUT(WPD)	YES
GPIO_29	183	L	INPUT(WPD)	YES
GPIO_27	187	L	INPUT(WPD)	YES
GPIO_85	202	Hiz	OUTPUT	YES
GPIO_154	203	L	INPUT(WPD)	YES
GPIO_155	205	L	INPUT(WPD)	YES
GPIO_28	206	L	INPUT(WPD)	YES
GPIO_24	207	L	INPUT(WPD) Boot configuration doesn't add pull-up	YES

Pin Name	Pin Number	H/L/Hiz After Reset	After Reset	Interrupt Function
GPIO_11	241	L	INPUT(WPD)	YES
GPIO_7	242	L	INPUT(WPD)	YES
GPIO_143	243	H	INPUT(WPU)	YES
GPIO_10	244	L	INPUT(WPD)	YES
GPIO_141	97	H	INPUT(WPU)	YES
GPIO_26	252	L	INPUT(WPD)	YES
GPIO_22	253	L	INPUT(WPD)	YES
GPIO_23	254	L	INPUT(WPD)	YES

Note：

H: High-voltage tolerant

L: Low-voltage tolerant

Hiz: High impedance

WPU: Weak pull up

WPD: Weak pull down

3.9 I²C

SU806 series module provides four I2C interfaces for TP, camera, sensor, etc. And four I2C interfaces are all internal pull up, when in use, please reserve pull-up resistors to 1.8V power domain. The pin definition is shown in the following table:

Table 3-13 I2C pin definition

Pin Name	Pin Number	I/O	Description	Note
SENSOR_I2C_SCL	91	DO	I2C clock	For sensor by default
SENSOR_I2C_SDA	92	I/O	I2C data	For sensor by default
TP_I2C_SCL	47	DO	I2C clock	For touch panel by default

TP_I2C_SDA	48	I/O	I2C data	For touch panel by default
CAM_I2C_SCL0	83	DO	I2C clock	For rear/front camera by default
CAM_I2C_SDA0	84	I/O	I2C data	For rear/front camera by default
CAM_I2C_SCL1	239	DO	I2C clock	For depth camera by default
CAM_I2C_SDA1	240	I/O	I2C data	For depth camera by default

Note:

When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address.

3.10 RBG

SU806 series module provides three RGB LED inputs, its pin definition is shown in the following table:

Table 3-14 RGB pin definition

Pin Name	Pin Number	I/O	Description	Note
LED_B	194	AI	RGB LED input 2	-
LED_G	195	AI	RGB LED input 1	-
LED_R	196	AI	RGB LED input 0	-

3.11 ADC

SU806 series module provides one ADC interface and its maximum resolution is 12 bits. It provides one ADC4_BAT_ID which is use for charging temperature detection. Its pin definition is shown in the following table:

Table 3-15 ADC pin definition

Pin Name	Pin Number	I/O	Description	Note

ADC	128	AI	ADC detection	Detection voltage range is 0.1V~1.2V with maximum 50mV accuracy and 0.1V~3.0V with maximum 150mV test accuracy, software configurable
ADC4_BAT_ID	260	AI	BAT_ID detection	The PIN260 is NC which product models support internal charging

3.12 Battery Power Supply Interface

SU806 series module just support circuit modes coulomb counter fuel gauge, if use coulomb counter IC externally, please connect SENSE_P and SENSE_N pin to GND.

Table 3-16 Battery power supply pin definition

Pin Name	Pin No.	I/O	Description	Note
CHARGE_SEL	127	DI	Charge modes select	Use internal charging when it's floating, and turn off internal charging when it's grounded
VBAT_SNS	133	AI	Battery voltage sense	-
VBAT_THERM	134	AI	Battery thermal detect input	NTC resistor is 47K
SENSE_N	258	AI	Battery fuel gauge negative input	Reserved
SENSE_P	259	AI	Battery fuel gauge positive input	Reserved

Fuel gauge reference design is shown in the following figure:

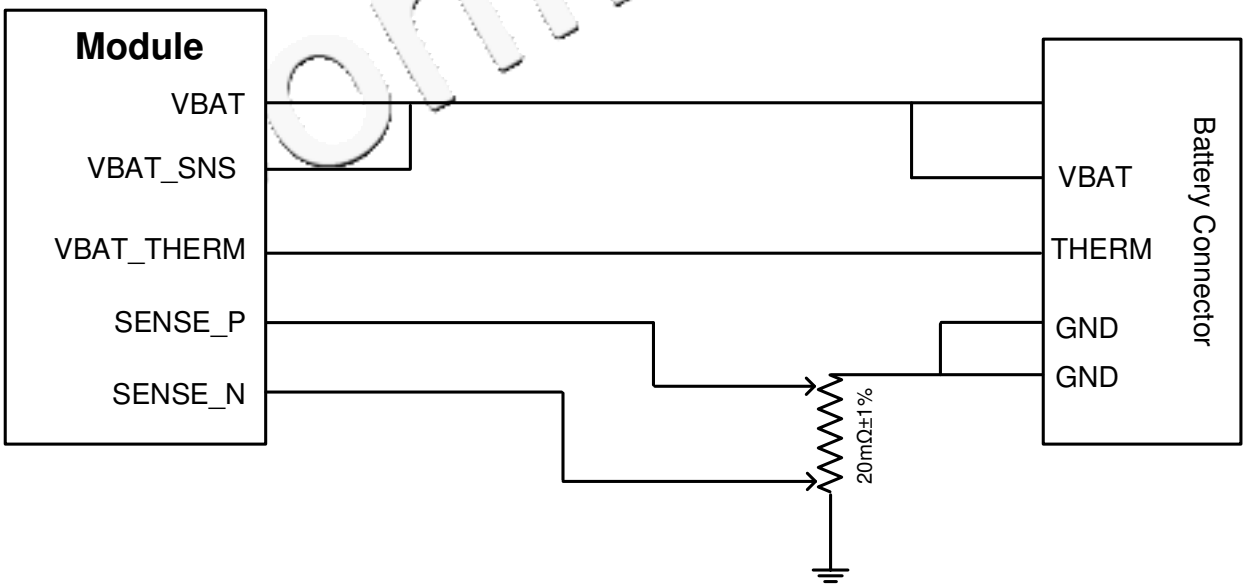

Figure 3-14 Fuel gauge reference design

Note:

Trace routing of SENSE_P and SENSE_N should follow differential rule.

The impedance of VBAT_SNS pin varies with the use scenario, if VBAT_SNS not connect with battery directly, recommend add isolators between VBAT_SNS pin and battery.

3.13 Charge Enable Interface

Table 3-17 Charge enable interface pin definition

Pin Name	Pin Number	I/O	Description	Note
CHG_EN	210	AO	Charge enable output	-

3.14 Vibration Motor Driver Interface

Table 3-18 Vibration motor driver pin definition

Pin Name	Pin Number	I/O	Description	Note
VIB_DRV_N	28	PO	Vibration motor driver output	Can be configured as LDO mode and connect with Vibration motor +

3.15 LCM

The video output of SU806 series module can support single-screen display. Its screen interface is based on MIPI_DSI standard and supports 4 sets of high-speed differential data transmit, and supports HD+ maximum.

Table 3-19 LCM pin definition

Pin Name	Pin Number	I/O	Description	Note
VDD1V85	111	PO	LCD IO voltage	-
VDD2V8	228	PO	LCD analog power VDD	-
MIPI_DSI0_CLK_N	52	AO	MIPI display serial interface clock -	-
MIPI_DSI0_CLK_P	53	AO	MIPI display serial interface clock +	-

Pin Name	Pin Number	I/O	Description	Note
MIPI_DSI0_LN0_N	54	AO	MIPI display serial interface Lane0 -	-
MIPI_DSI0_LN0_P	55	AO	MIPI display serial interface Lane0 +	-
MIPI_DSI0_LN1_N	56	AO	MIPI display serial interface Lane 1-	-
MIPI_DSI0_LN1_P	57	AO	MIPI display serial interface Lane 1+	-
MIPI_DSI0_LN2_N	58	AO	MIPI display serial interface Lane 2-	-
MIPI_DSI0_LN2_P	59	AO	MIPI display serial interface Lane 2+	-
MIPI_DSI0_LN3_N	60	AO	MIPI display serial interface Lane 3 -	-
MIPI_DSI0_LN3_P	61	AO	MIPI display serial interface Lane 3 +	-
LCD_RST	49	DO	LCD reset	-
PWM	29	DO	LCD backlight PWM	-
LCD_TE	50	DI	LCD tearing effect	Keep floating if unused
GPIO_25	190	DO	LCD backlight enable	-

The reference design of LCD interface circuit is shown as follows:

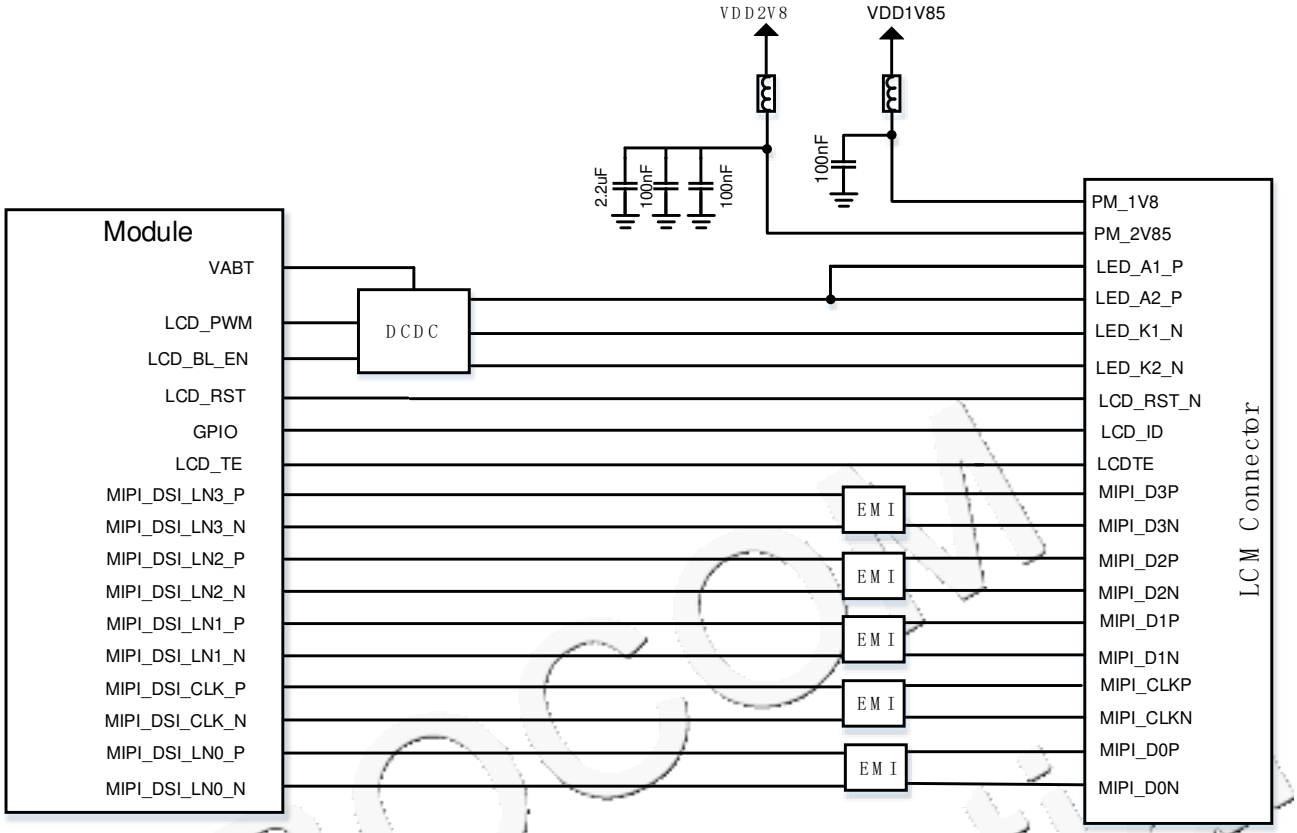

Figure 3-15 LCM reference design

LCM design notice:

1) MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the electromagnetic interference of the circuit.
2) MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;
3) The MIPI signal needs to be controlled with a differential impedance of 100Ω tolerance ±10%;
4) The total length of the trace must ≤ 70 mm, VIAs ≤ 4;
5) The intra lane match of MIPI differential pair signal must ≤ 0.5 mm;
6) The inter lane match of MIPI signal must ≤ 2 mm;
7) It is recommended that the space of intra lane should be 1.5 times trace width and the differential cable should keep 3 times trace width from other cable;
8) The parasitic capacitance of differential signal must not exceed 1.0pF;

Table 3-20 Length of MIPI_DSI differential signal line in module

Pin Name	Pin Number	Length (mm)	Length Difference (DP-DM) mm
MIPI_DSI0_CLK_N	52	62.96494	0.03838

Pin Name	Pin Number	Length (mm)	Length Difference (DP-DM) mm
MIPI_DSI0_CLK_P	53	63.00332	
MIPI_DSI0_LN0_N	54	62.71304	-0.27227
MIPI_DSI0_LN0_P	55	62.44077	
MIPI_DSI0_LN1_N	56	62.22446	0.32383
MIPI_DSI0_LN1_P	57	62.54829	
MIPI_DSI0_LN2_N	58	62.8235	0.1031
MIPI_DSI0_LN2_P	59	62.9266	
MIPI_DSI0_LN3_N	60	63.84148	-0.39457
MIPI_DSI0_LN3_P	61	63.44691	

3.16 TP

SU806 series module provides one I2C interface can be used to connect the touch panel and it provides power, interrupt, reset pins. The pin definition of the module is shown in the follow table:

Table 3-21 TP pin definition

Pin Name	Pin Number	I/O	Description	Note
TP_INT	30	DI	LCD TP interrupt signal	-
TP_RST	31	DO	LCD TP reset signal	-
VDD1V85	111	PO	LCD TP IO voltage output	-
VDD2V8	228	PO	LCD TP VDD voltage output	-
TP_I2C_SCL	47	DO	LCD TP I2C clock	-
TP_I2C_SDA	48	I/O	LCD TP I2C data	-

TP reference design circuit is shown as follows:

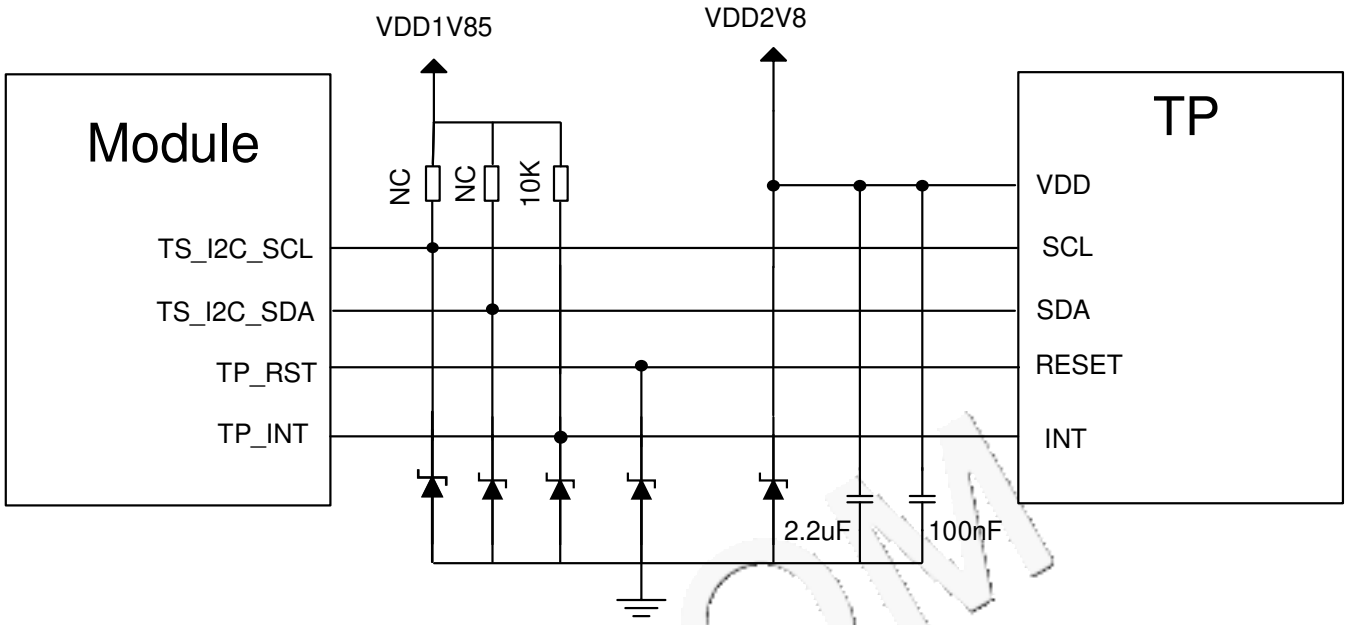

Figure 3-16 TP reference design

3.17 Camera

The camera interface is based on the MIPI_CSI standard and can support three (4-lane+2-lane+1-lane) cameras, maximum 13MP. The pin definition of camera interface is shown in the following table:

Table 3-22 Camera interface pin definition

Pin Name	Pin Number	I/O	4-Lane+2-Lane+1-Lane	Note
VDD1V8	125	PO	DOVDD power supply, 1.8V	-
VDDCAMA	129	PO	AVDD power supply, 2.8V	-
VDDCAMMOT	152	PO	Camera focus motor drive AFVDD power supply, 2.8V	-
VDDCAMCORE	151	PO	DVDD power supply, 1.2V	-
MIPI_CSI0_CLK_P	229	AI	MIPI rear camera serial interface clock+	-
MIPI_CSI0_CLK_N	230	AI	MIPI rear camera serial interface clock+	-
MIPI_CSI0_LN0_P	155	AI	MIPI rear camera serial interface lane 0+	-
MIPI_CSI0_LN0_N	231	AI	MIPI rear camera serial interface lane 0-	-
MIPI_CSI0_LN1_P	156	AI	MIPI rear camera serial interface lane 1+	-

Pin Name	Pin Number	I/O	4-Lane+2-Lane+1-Lane	Note
MIPI_CSI0_LN1_N	232	AI	MIPI rear camera serial interface lane 1-	-
MIPI_CSI0_LN2_P	157	AI	MIPI rear camera serial interface lane 2+	-
MIPI_CSI0_LN2_N	233	AI	MIPI rear camera serial interface lane 2-	-
MIPI_CSI0_LN3_P	158	AI	MIPI rear camera serial interface lane3+	-
MIPI_CSI0_LN3_N	234	AI	MIPI rear camera serial interface lane 3-	-
MCAM_MCLK	74	DO	Rear camera master clock	-
MCAM_RST	79	DO	Rear camera reset	-
MCAM_PWDN	80	DO	Rear camera power down	-
CAM_I2C_SCL0	83	DO	Rear camera I2C clock	-
CAM_I2C_SDA0	84	I/O	Rear camera I2C data	-
MIPI_CSI1_CLK_N	63	AI	MIPI front camera serial interface clock +	-
MIPI_CSI1_CLK_P	64	AI	MIPI front camera serial interface lane 0 -	-
MIPI_CSI1_LN0_N	65	AI	MIPI front camera serial interface lane 0 +	-
MIPI_CSI1_LN0_P	66	AI	MIPI front camera serial interface lane 0 -	-
MIPI_CSI1_LN1_N	67	AI	MIPI front camera serial interface lane 1 +	-
MIPI_CSI1_LN1_P	68	AI	MIPI front camera serial interface lane 1 -	-
SCAM_MCLK	75	DO	Front camera master clock	-
SCAM_RST	81	DO	Front camera reset	-
SCAM_PWDN	82	DO	Front camera power down	-
MIPI_CSI1_LN3_N	70	AI	MIPI depth camera serial interface clock -	-
MIPI_CSI1_LN3_P	71	AI	MIPI depth camera serial interface clock +	-
MIPI_CSI1_LN2_N	72	AI	MIPI depth camera serial interface lane 0 -	-

Pin Name	Pin Number	I/O	4-Lane+2-Lane+1-Lane	Note
MIPI_CSI1_LN2_P	73	AI	MIPI depth camera serial interface lane 0 +	-
DCAM_MCLK	238	DO	Depth camera master clock	-
DCAM_RST	237	DO	Depth camera reset	-
DCAM_PWDN	236	DO	Depth camera power down	-
CAM_I2C_SCL1	239	DO	Front/depth camera I2C clock	-
CAM_I2C_SDA1	240	I/O	Front/depth camera I2C data	-

3.17.1 Rear Camera

Reference design of rear camera is shown as follows:

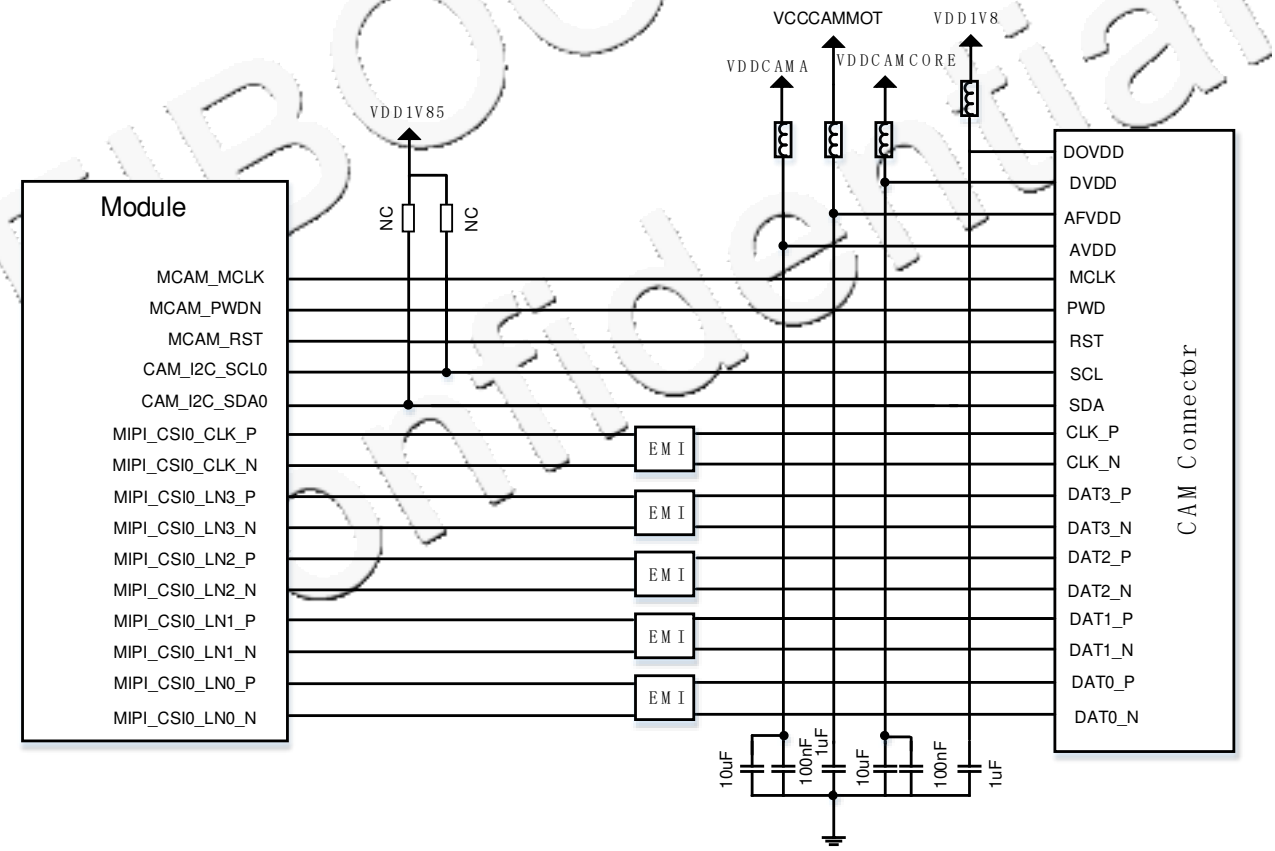

Figure 3-17 Rear camera reference design

3.17.2 Front Camera

Reference design of front camera is shown as follows:

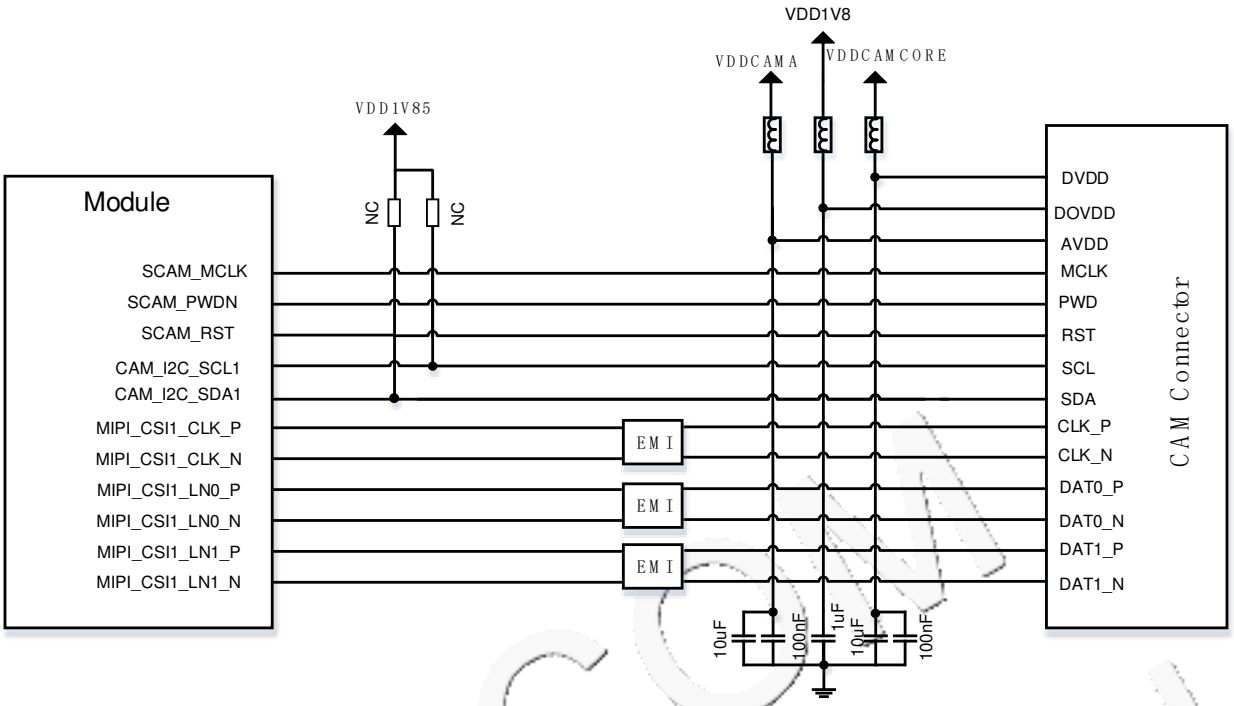

Figure 3-18 Front camera reference design

3.17.3 Depth Camera

Pin definition of depth camera is shown as follow:

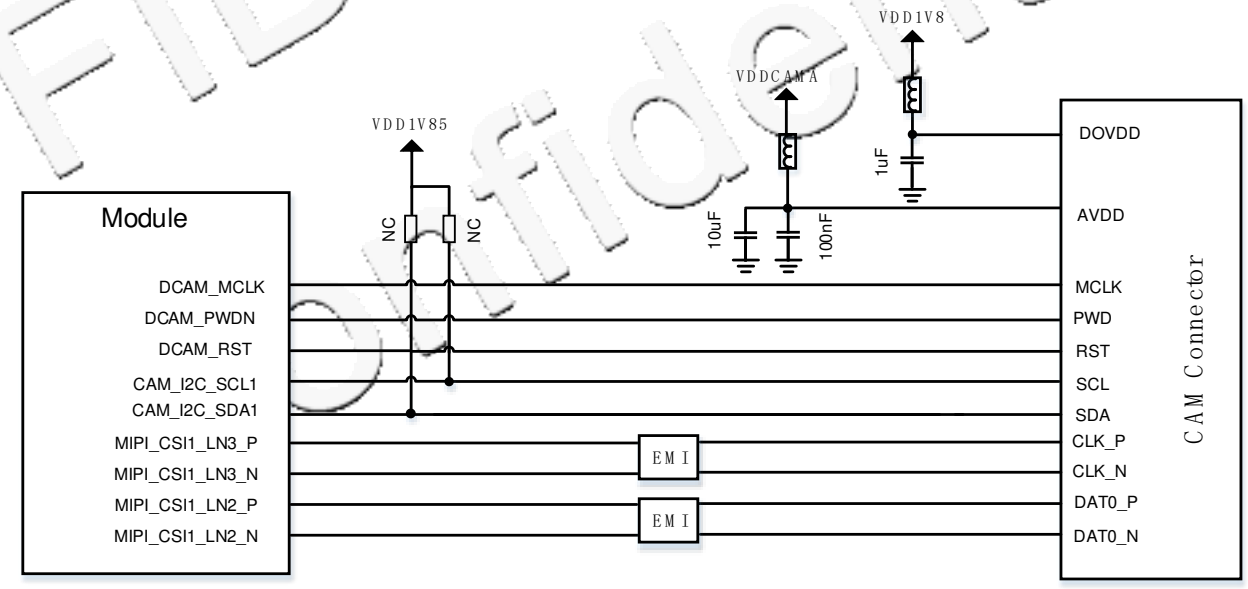

Figure 3-19 Depth camera reference design

3.17.4 Design Notice

MIPI_CSI is a high-speed signal which has relatively high requirement for routing and must be prioritized when PCB layout.

1) MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series

near the LCD connector to reduce the electromagnetic interference of the circuit.

2) MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;
3) The MIPI signal needs to be controlled with a differential impedance of 100Ω tolerance ±10%;
4) The total length of the trace must ≤ 70mm, VIAs ≤ 4;
5) The intra lane match of MIPI differential pair signal must ≤ 0.5 mm;
6) The inter lane match of MIPI signal must ≤ 2 mm;
7) It is recommended that the space of intra lane should be 1.5 times trace width and the differential cable should keep 3 times trace width from other cable;
8) The parasitic capacitance of differential signal must not exceed 1.0pF;

The matters need attention of another camera signal:

9) CAM_CLK is a high-speed clock signal and requires three-dimensional grounding
10) If two cameras share the same I2C interface, please confirm the I2C addresses of the two cameras do not conflict;
11) The analog voltage VDDCAMA routing should be away from interference sources, otherwise it is easy to bring interference of power noise;
12) Camera analog power supply suggest to add LDO with high PSRR ability and place it near camera.

Table 3-23 Length of MIPI_CSI differential signal in module

Pin Name	Pin Number	Length (mm)	Length Difference (DP-DM) mm
MIPI_CSI0_CLK_P	229	24.6976	0.2409
MIPI_CSI0_CLK_N	230	24.4567	
MIPI_CSI0_LN0_P	155	24.59549	0.09393
MIPI_CSI0_LN0_N	231	24.50157	
MIPI_CSI0_LN1_P	156	24.65386	0.021
MIPI_CSI0_LN1_N	232	24.63286	
MIPI_CSI0_LN2_P	157	23.86664	0.13116
MIPI_CSI0_LN2_N	233	23.73548	
MIPI_CSI0_LN3_P	158	23.60038	-0.04674
MIPI_CSI0_LN3_N	234	23.64712	

Pin Name	Pin Number	Length (mm)	Length Difference (DP-DM) mm
MIPI_CSI1_CLK_P	64	10.74214	0.04892
MIPI_CSI1_CLK_N	63	10.69322	
MIPI_CSI1_LN0_P	66	11.22924	-0.10242
MIPI_CSI1_LN0_N	65	11.33166	
MIPI_CSI1_LN1_P	68	11.73285	0.28125
MIPI_CSI1_LN1_N	67	11.4516	
MIPI_CSI1_LN2_P	73	19.19065	-0.18467
MIPI_CSI1_LN2_N	72	19.37532	
MIPI_CSI1_LN3_P	71	19.95271	0.07975
MIPI_CSI1_LN3_N	70	19.87296	

3.18 Sensor

SU806 series module supports I2C interface to communicate with various types of sensors, such as accelerometer sensor, ambient light sensor and magnetic sensor etc.

Table 3-24 Sensor interface pin definition

Pin Name	Pin Number	I/O	Description	Note
SENSOR_I2C_SCL	91	DO	I2C clock	-
SENSOR_I2C_SDA	92	I/O	I2C data	-
ALPS_INT_N	107	DI	Ambient light and proximity sensor interrupt	-
MAG_RST	109	DO	Magnetic sensor reset	-
ACCL_INT	110	DI	Accelerometer sensor interrupt	-

3.19 Audio

3.19.1 Audio Interface Pin Definition

SU806 series module supports analog audio, have 3 input and 3 output. Pin definition is shown in the following table:

Table 3-25 Audio interface pin definition

Pin Name	Pin Number	I/O	Description	Note
SPK_P	10	AO	Speaker amp+ output	Power consumption 800mW in 8Ω load
SPK_M	11	AO	Speaker amp- output	
EAR_P	8	AO	Earpiece output+	Power consumption 25mW in 32Ω load
EAR_M	9	AO	Earpiece output-	
HPH_L	138	AO	Headset left channel output	-
HPH_GND	137	AI	Headset ground sensing	-
HPH_R	136	AO	Headset right channel output	-
HPH_DET	139	AI	Headset detection	-
MIC2_P	6	AI	Headset mic input	-
MIC1_M	5	AI	Main mic difference input-	-
MIC1_P	4	AI	Main mic difference input+	-
MIC3_P	220	AI	Sub-mic input	-

Design notice:

1) SU806 series module has MIC bias circuit internally, and no external addition is required.
2) The SPK is configured as class D amplifier output, cannot connect with amplifier externally, it is recommended to connect 8Ω speakers. Note that the route width must meet the power rating requirements; If an external audio amplifier is required, please use the output of headphone as the input of external audio amplifier.
3) The reference ground of the headphone has already grounded in the module. The external circuit is recommended not to be grounded and resistor can be reserved.
4) It is recommended to use earpiece with 32Ω impendence.

5) Reduce noise and improve audio quality, the following approaches are recommended.

- Keep audio PCB routing away from the antenna and high-frequency digital signal.
- Reserve LC filter circuit in audio circuit to reduce EMI.
- Audio routing needs to be masked.

3.19.2 Microphone Circuit Design

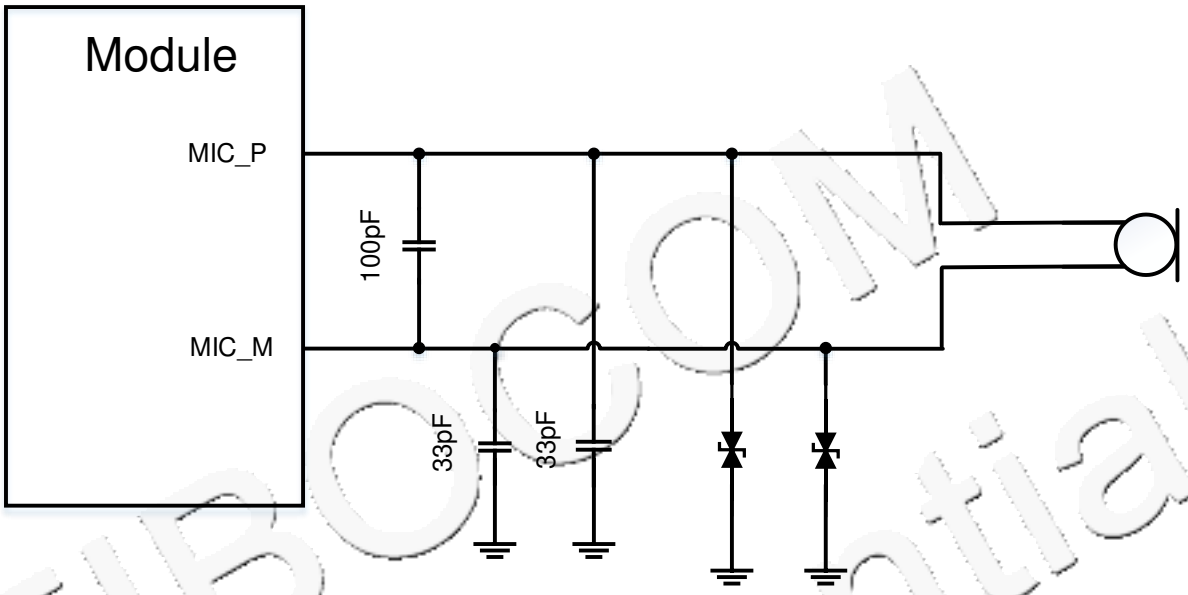

Figure 3-20 Microphone reference design

3.19.3 Earpiece Circuit Design

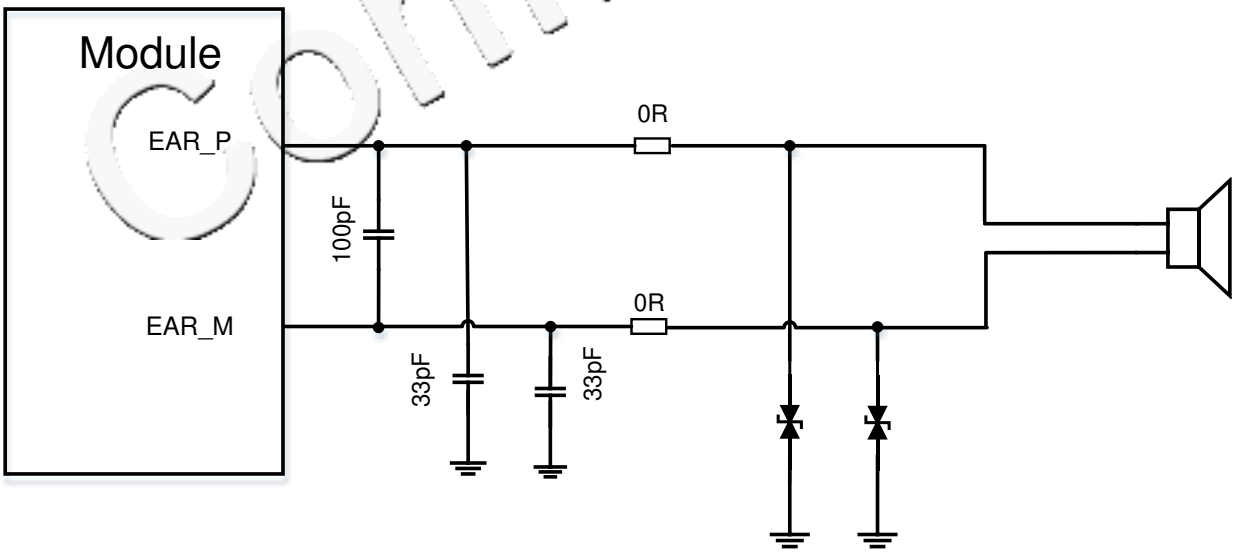

Figure 3-21 Earpiece reference design

3.19.4 Headset Circuit Design

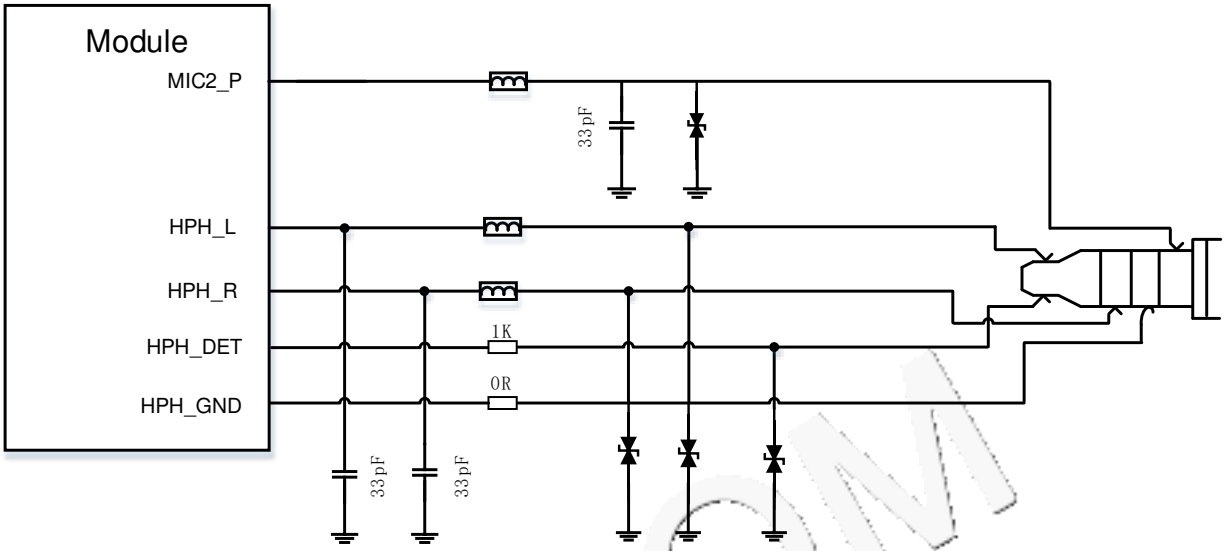

Figure 3-22 Headset reference design

Note：

Please choose bidirectional TVS for headset ESD protection.

3.19.5 Speaker Circuit Design

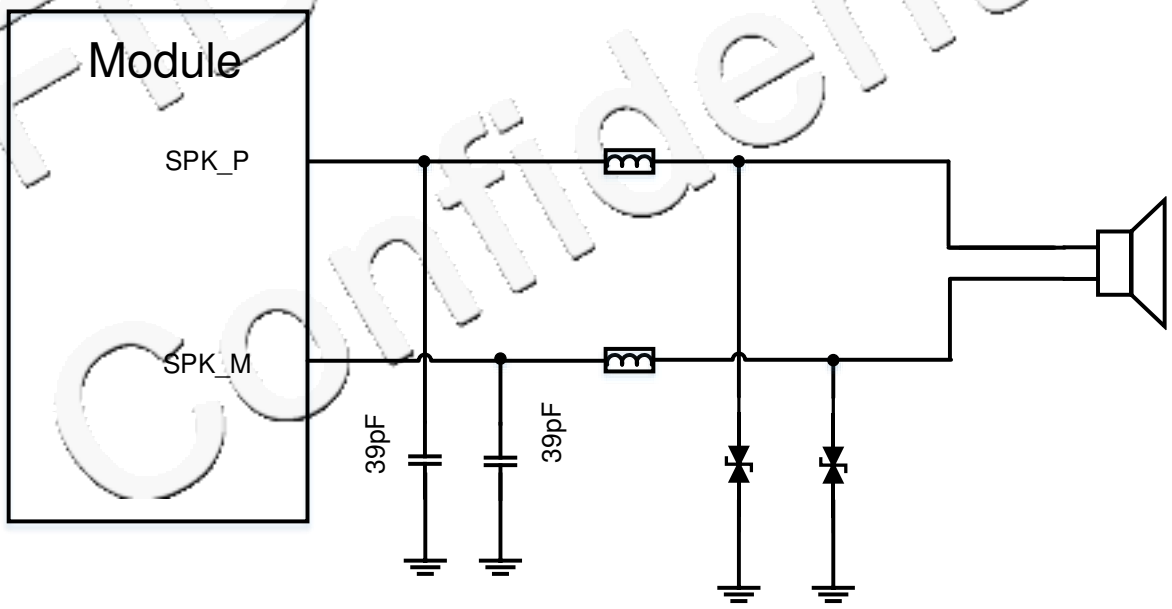

Figure 3-23 Speaker reference design

3.20 Force Download Interface

SU806 series module provides KEY_FORCE_BOOT pin as an emergency download interface. Connect the KEY_FORCE_BOOT with GND when power on, the module can enter the emergency download mode which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve the test pin of this pin. Reference design is shown in the following figure:

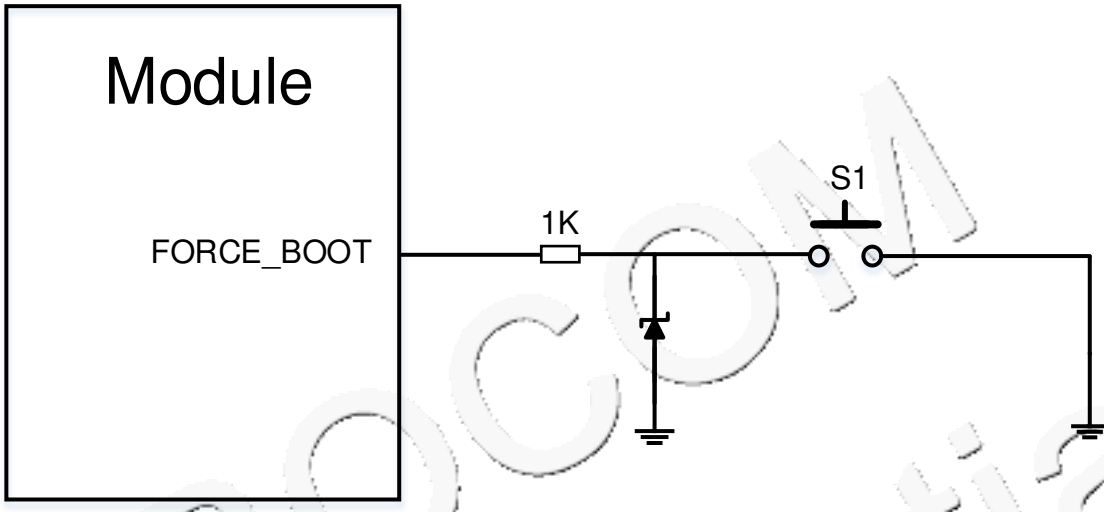

Figure 3-24 Force download reference design

4 Antenna Interface

SU806 series module support 2/3/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 MAIN/DRX Antenna

SU806 series module provides two 2G/3G/4G antenna interfaces. The ANT_MIAN is used to receive and transmit RF signal, the ANT_DRX is used for diversity reception.

Table 4-1 Main/DRX pin definition

Pin Name	Pin Number	I/O	Description	Note
ANT_MAIN	87	AI/AO	2G/3G/4G main antenna	-
ANT_DRX	131	AI	Diversity reception antenna	-

4.1.1 Operating Band

Table 4-2 Module operating band of SU806-LA

Mode	Band	Tx (MHz)	Rx (MHz)
GSM	850	824-849	869-894
	900	880-915	925-960
	1800	1710-1785	1805-1880
	1900	1850-1910	1930-1990
WCDMA	Band 2	1850-1910	1930-1990
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 8	880-915	925-960
LTE FDD	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 4	1710-1755	2110-2155

Mode	Band	Tx (MHz)	Rx (MHz)
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 12	699-716	729-746
	Band 17	704-716	734-746
	Band 28	703-748	758-803
LTE TDD	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690

4.1.2 Antenna Reference Design

When use the SU806 series module, it is necessary to connect the antenna pin with the RF connector or antenna feed point on the main board via an RF trace. Microstrip trace is recommended for RF trace, with insertion loss within 0.2dB and impedance at 50Ω.A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel components are directly connected across the RF trace and should not pull out a branch, as the figure shows:

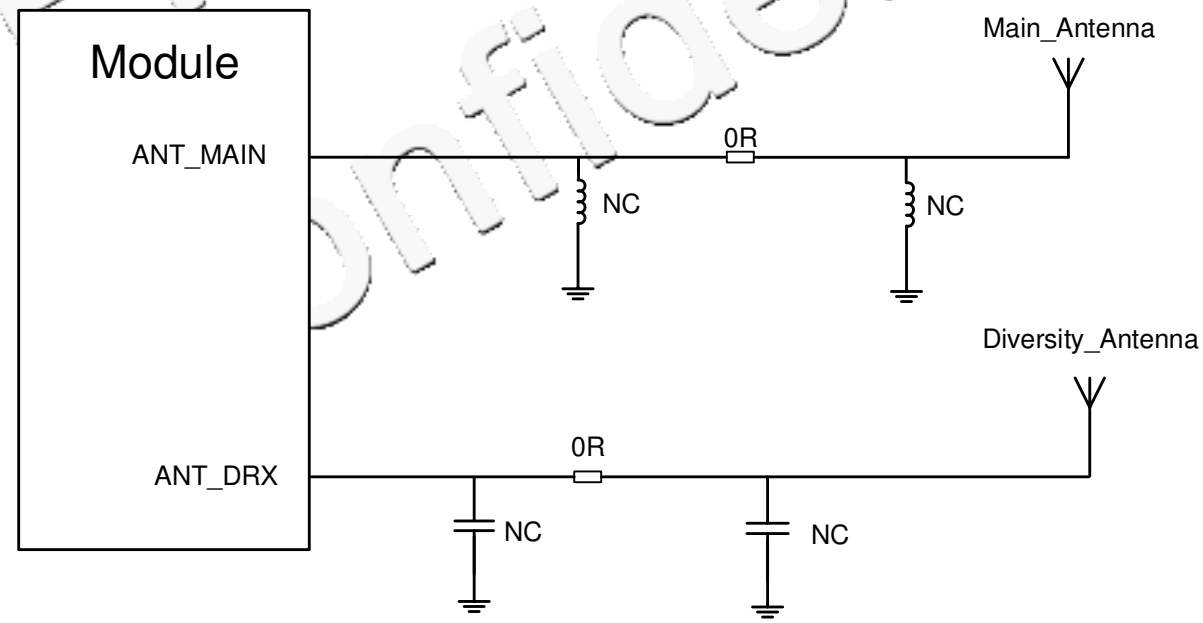

Figure 4-1 MAIN/DRX antenna reference design

4.2 WIFI/BT Antenna

Microstrip trace is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50Ω.

Table 4-5 WIFI/BT antenna interface definition

Pin Name	Pin Number	I/O	Description	Note
ANT_WIFI/BT	77	AI/AO	WIFI/BT antenna	-

4.2.1 WIFI/BT Operating Frequency

Table 4-6 WIFI/BT operating frequency

Mode	Frequency	Unit
WIFI	2402-2482	MHz
BT4.2	2402-2480	MHz

4.2.2 WIFI/BT Antenna Reference Design

WIFI/BT antenna reference design is shown in the following figure:

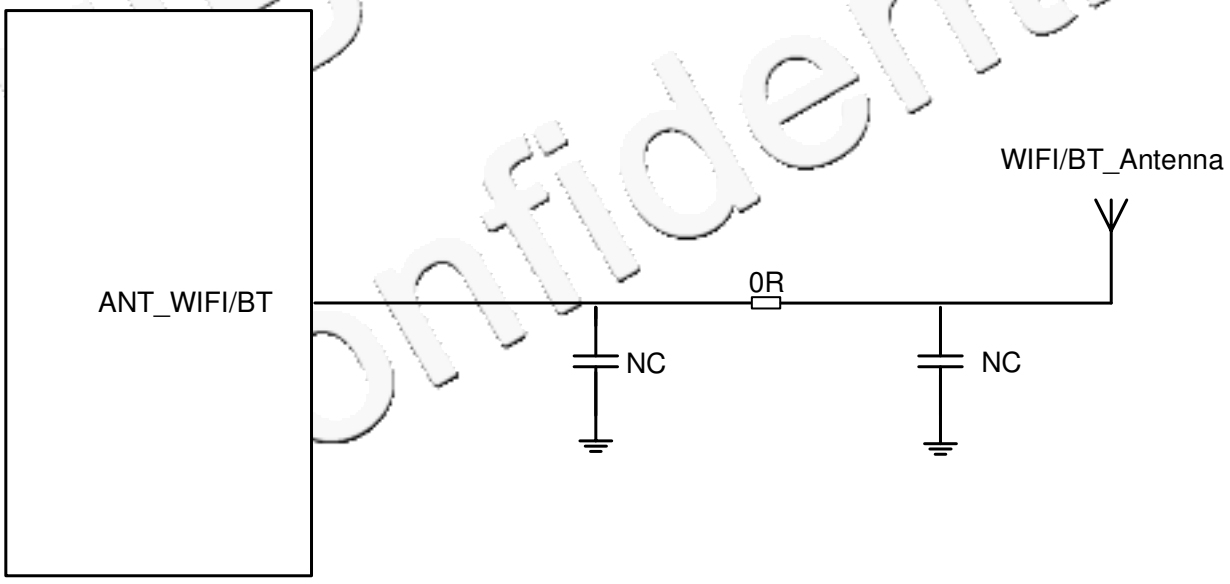

Figure 4-2 WIFI/BT antenna reference design

4.3 GNSS Antenna

GNSS supports GPS/BeiDou.

Table 4-7 GNSS antenna interface definition

Pin Name	Pin Number	I/O	Description	Note
ANT_GNSS	121	AI	GNSS antenna	-

4.3.1 Operating Frequency

Table 4-8 GNSS operating frequency

Mode	Frequency	Unit
GPS	1575.42±1.023	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 GNSS Antenna Reference Design

4.3.2.1 Passive Antenna Reference Design:

SU806 series module have a built-in LNA. The passive antenna is used in the design of the device. Microstrip trace is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50Ω.

The GNSS antenna reference design is shown in the following figure:

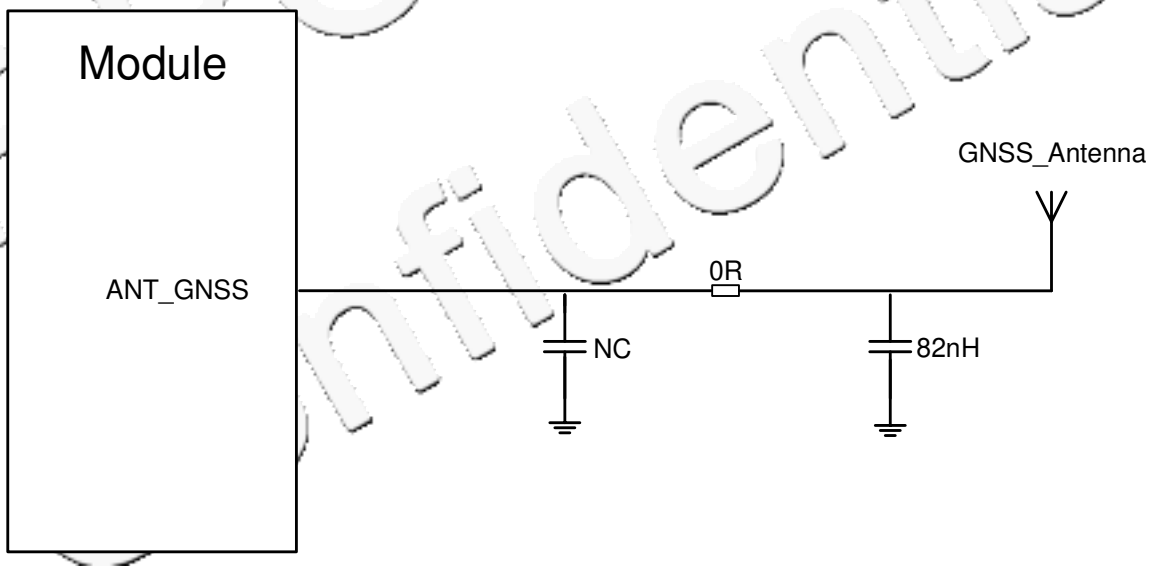

Figure 4-3 GNSS passive antenna reference design

Note：

For GNSS passive antenna, it is recommended to add an 82nH indictor near antenna connector to improve GNSS antenna's ability of resist ESD. For better ability of resist ESD, please choose TVS that junction capacitance less than 0.5pF, recommended type: ESD9D5U, with 0.5pF junction capacitance and 5.0V embedded voltage.

4.3.2.2 Active Antenna Reference Design

The power of the active antenna is fed from the antenna's signal line through a 56nH inductor. Common active antennas supply power from 3.3V to 5.0V. The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-performance LDO be used to power the antenna.

The active antenna reference circuit is shown in the following figure:

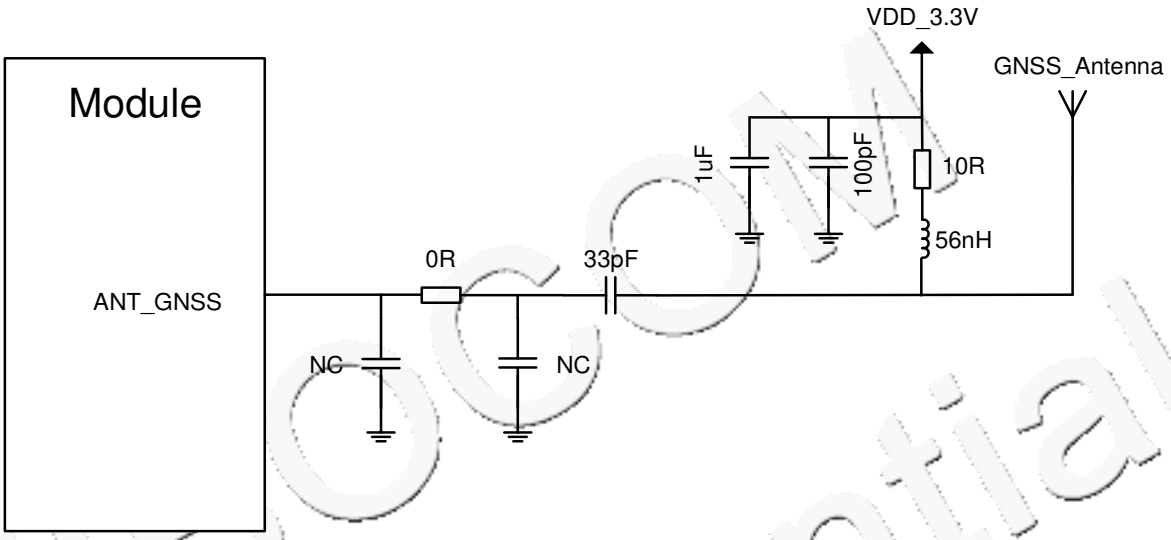

Figure 4-4 GNSS active antenna reference design

4.4 Antenna Requirement

SU806 series module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 4-9 Antenna requirements

SU806 Series Module Antenna Requirement	
Standard	**Antenna Requirement**
GSM/WCDMA /LTE	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB (0.7-1GHz) Insertion loss: < 1.5dB(1.4-2.2GHz)

SU806 Series Module Antenna Requirement	
Standard	**Antenna Requirement**
	Insertion loss: < 2dB (2.3-2.7GHz)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB
GNSS	Frequency range: 1559MHz~1607MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) Passive antenna gain: > 0dBi Active antenna NF: < 15dB (typical) Active antenna gain: > -2dBi

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal traces should be within 50Ω. In general, the impedance of the RF signal trace is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually in two ways: microstrip trace and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip trace and coplanar waveguide when the impedance cable is at 50Ω.

- Microstrip trace entirety structure

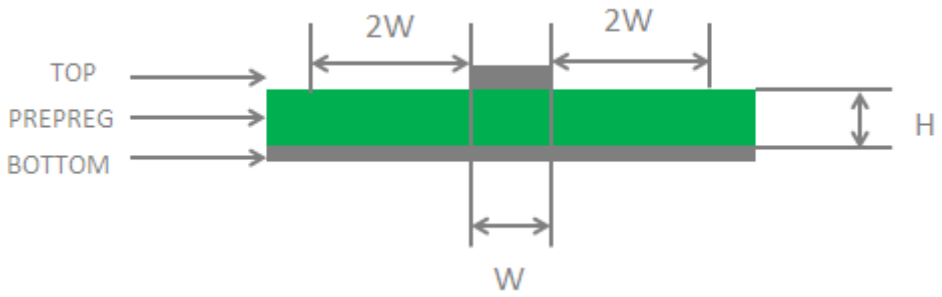

Figure 5-1 Two-layer PCB microstrip cable structure

- Coplanar waveguide entirety structure

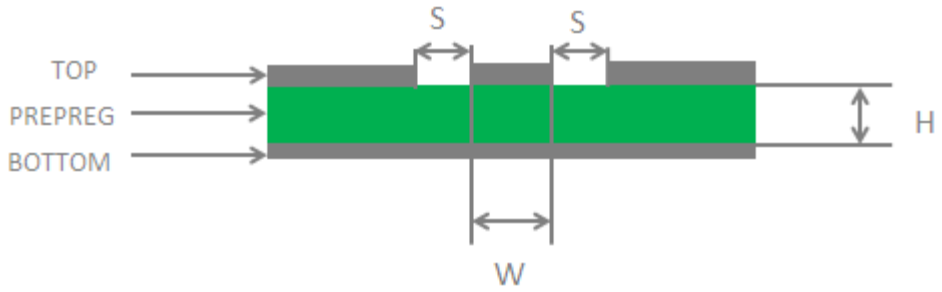

Figure 5-2 Two-layer PCB coplanar waveguide structure

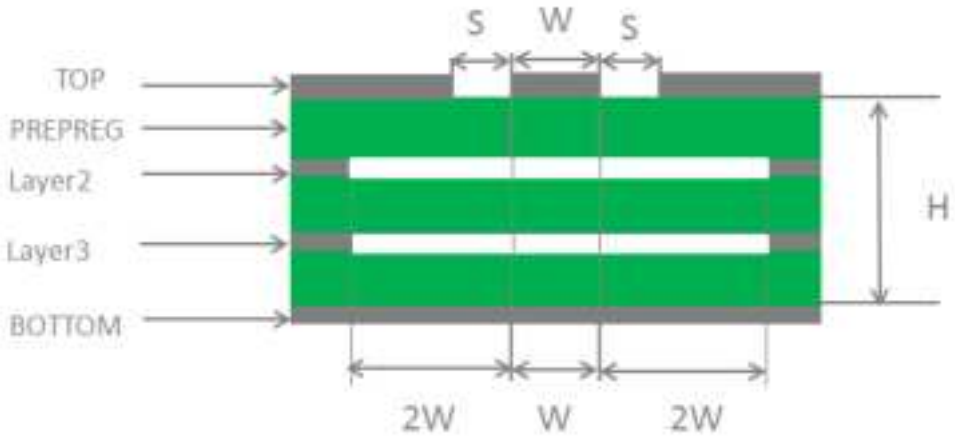

Figure 5-3 Four-layer PCB coplanar waveguide structure (reference ground layer3)

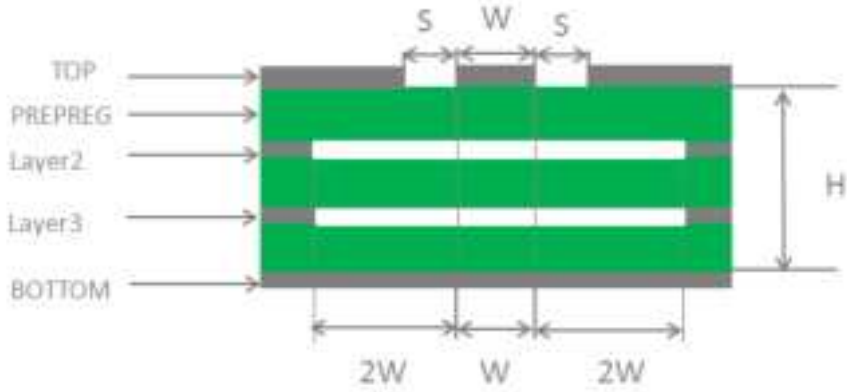

Figure 5-4 Four-layer PCB coplanar waveguide structure (reference ground layer4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degrees.
- Attention should be paid to the establishment of the component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal trace should be entirety; adding a certain amount of ground holes around the signal and the reference ground can help improve the RF performance; the distance between the ground hole and the signal trace should be at least 2 times the trace width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

SU806 series module supports 2.4G WLAN wireless communications and 802.11b, 802.11g, 802.11n standards, with a maximum speed up to 72.2Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20

6.2 WIFI Performance

Test condition: 3.8V power supply, environment temperature 25°C

Table 6-1 WIFI transmit power

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17±3
		11Mbps	20	17±3
	802.11g	6Mbps	20	16±3
		54Mbps	20	13±3
	802.11n	MCS0	20	15±3
		MCS7	20	13±3

Table 6-2 WIFI RX sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-88
		11Mbps	20	-84
	802.11g	6Mbps	20	-86
		54Mbps	20	-74

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
	802.11n	MCS0	20	-85
		MCS7	20	-70

6.3 Bluetooth Overview

SU806 series module supports BT4.2 (BR/EDR+BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1MHz and can accommodate 79 channels. The BLE channel bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 6-3 BT rate and version information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	-
BT2.0+EDR	3Mbit/s	> 80Kbit/s	-
BT3.0+HS	24Mbit/s	Refer 3.0+HS	-
BT4.2 LE	24Mbit/s	Refer 4.2 LE	-

6.4 Bluetooth Performance

Table 6-4 BT performance index

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitter	8±2	7.5±2	7.5±2	2±2.5	dBm
Sensitivity	-86	-88	-82	-90	dBm

Note:

The sensitivity here is a typical value.

7 GNSS

7.1 Overview

SU806 series smart module supports GPS/BeiDou positioning systems. The module is embedded with LNA which can effectively improve the sensitivity of GNSS.

7.2 Performance

Test condition: 3.8V power supply, environment temperature 25°C

Table 7-1 GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-146	dBm
	Tracking	-155	dBm
C/No	-130dBm	39.5	dB/Hz
TTFF	Cold Start	40	s
	Warm Start	32	s
	Hot Start	3	s
CEP	Static accuracy (95% @-130dbm)	5	m

8 Electrical, Reliability and RF Performance

8.1 Recommended Parameters

Table 8-1 Recommended parameters

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.2	V
USB_VBUS	4.75	5	5.25	V
VRTC	-	3.0	3.35	V
Operating Temperature	-20	25	65	℃
Storage Temperature	-40	25	95	℃

8.2 Absolute Maximum Ratings

The functionality of SU806 series module is subject to the absolute maximum/minimum values listed in the following table. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 8-2 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
VBAT	Power supply	-0.3	5	V
USB_VBUS	VBUS 5V input	-0.3	17	V

8.3 Power Consumption

Test condition: 3.8V power supply, environment temperature 25°C

Table 8-3 Power consumption of SU806-LA

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Power supply, not power on	120	uA

Parameter	Description	Condition	Typical Result	Unit
	Software power off current	By AT command or select the power off menu in LCM selection box	230	
I_{sleep}	GSM	MFRMS=5	3.3	mA
	WCDMA	DRX=8	3.4	
	TDD LTE	DPC (Default Paging Cycle)=#256	3.2	
	FDD LTE	DPC (Default Paging Cycle)=#256	3.2	
	Radio Off	AT+CFUN=4 Flight Mode	2.5	
$I_{GSM-RMS}$	GSM voice RMS Current	GSM850@ PCL=5	267	mA
		GSM850@ PCL=19	98	
		EGSM900@ PCL=5	277	
		EGSM900@ PCL=19	103	
		DCS1800@ PCL=0	203	
		DCS1800@ PCL=15	101	
		PCS1900@ PCL=0	185	
		PCS1900@ PCL=15	95	
$I_{GSM-MAX}$	GSM voice Peak current	GSM850@ PCL=5	1900	mA
		EGSM900@ PCL=5	1950	
		DCS1800@ PCL=0	1420	
		PCS1900@ PCL=0	1350	
$I_{GPRS-RMS}$	GPRS data RMS Current	GSM850@ Gamma=3(1UL/4DL)	277	mA
		GSM850@ Gamma=3(4UL/1DL)	477	
		EGSM900@ Gamma=3(1UL/4DL)	242	
		EGSM900@ Gamma=3(4UL/1DL)	463	

Parameter	Description	Condition	Typical Result	Unit
		DCS1800@ Gamma=3(1UL/4DL)	186	
		DCS1800@ Gamma=3(4UL/1DL)	315	
		PCS1900@ Gamma=3(1UL/4DL)	183	
		PCS1900@ Gamma=3(4UL/1DL)	298	
$I_{EGPRS-RMS}$	EGPRS data RMS Current	GSM850@ Gamma=6(1UL/4DL)	178	mA
		GSM850@ Gamma=6(4UL/1DL)	312	
		EGSM900@ Gamma=6(1UL/4DL)	173	
		EGSM900@ Gamma=6(4UL/1DL)	315	
		DCS1800@ Gamma=5(1UL/4DL)	162	
		DCS1800@ Gamma=5(4UL/1DL)	318	
		PCS1900@ Gamma=5(1UL/4DL)	161	
		PCS1900@ Gamma=5(4UL/1DL)	311	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band2@ max power	588	mA
		Band4@ max power	650	
		Band5@ max power	590	
		Band8@ max power	610	
$I_{LTE-RMS}$	FDD data RMS Current	Band2@ max power(10MHz,1RB)	600	mA
		Band3@ max power(10MHz,1RB)	695	
		Band4@ max power(10MHz,1RB)	650	
		Band5@ max power(10MHz,1RB)	625	
		Band7@ max power(10MHz,1RB)	718	
		Band12@ max power(10MHz,1RB)	670	

Parameter	Description	Condition	Typical Result	Unit
		Band17@ max power(10MHz,1RB)	670	
		Band28@ max power(10MHz,1RB)	689	
	TDD data RMS Current	Band40@ max power(10MHz,1RB)	319	
		Band41@ max power(10MHz,1RB)	357	

8.4 RF Transmit Power

The transmit power of each band of the SU806 module is shown in the following table:

Test condition: 3.8V power supply, environment temperature 25°C, maximum power test of LTE 10M 12RB.

Table 8-4 RF Transmit power of SU806-LA

Mode	Band	Max Power (dBm)	Min Power (dBm)
GSM	850 (GMSK)	33±2	5±5
	900 (GMSK)	33±2	5±5
	1800 (GMSK)	30±2	0±5
	1900 (GMSK)	30±2	0±5
GSM	850 (8PSK)	27.0±3	5±5
	900 (8PSK)	27.0±3	5±5
	1800 (8PSK)	26.0±3	0±5
	1900 (8PSK)	26.0±3	0±5
WCDMA	Band 2	24+1/-3	< -49
	Band 4	24+1/-3	< -49
	Band 5	24+1/-3	< -49
	Band 8	24+1/-3	< -49
LTE FDD	Band 2	23.0±2	< -39
	Band 3	23.0±2	< -39

Mode	Band	Max Power (dBm)	Min Power (dBm)
	Band 4	23.0±2	< -39
	Band 5	23.0±2	< -39
	Band 7	23.0±2	< -39
	Band 12	23.0±2	< -39
	Band 17	23.0±2	< -39
	Band 28	23.0±2	< -39
LTE TDD	Band 40	23.0±2	< -39
	Band 41	23.0±2	< -39

8.5 RF Receiver Sensitivity

The sensitivity of each frequency band of the SU806 series module is shown in the following table:

Test condition: 3.8V power supply, environment temperature 25°C. The test bandwidth of LTE sensitivity LTE is 10M, RB configuration please refer to 3GPP standard.

Table 8-5 RF receiver sensitivity of SU806-LA

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
GSM	850	-109.2	-	-	-102	dBm
	900	-108.7	-	-	-102	dBm
	1800	-108.5	-	-	-102	dBm
	1900	-108.5	-	-	-102	dBm
WCDMA	Band 2	-110.5	-	-	-104.7	dBm
	Band 4	-110	-	-	-106.7	dBm
	Band 5	-110.8	-	-	-104.7	dBm
	Band 8	-111.3	-	-	-103.7	dBm
LTE FDD	Band 2	-98	-	-	-94.3	dBm
	Band 3	-99	-	-	-93.3	dBm
	Band 4	-98.5	-	-	-96.3	dBm

	Band 5	-99	-	-	-94.3	dBm
	Band 7	-98	-	-	-94.3	dBm
	Band 12	-98.5	-	-	-93.3	dBm
	Band 17	-98.5	-	-	-93.3	dBm
	Band 28	-99	-	-	-94.8	dBm
LTE TDD	Band 40	-97.1	-	-	-96.3	dBm
	Band 41	-97	-	-	-94.3	dBm

8.6 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, so ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

ESD performance parameters are shown in the following table (Temperature: 25°C, Humidity: 45%)

Table 8-6 ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	KV
Antenna interface	±4	±8	KV
Other interface	±0.5	±1	KV

9 Structural Specification

9.1 Product Appearance

SU806 series module product appearance is shown in the following figure:

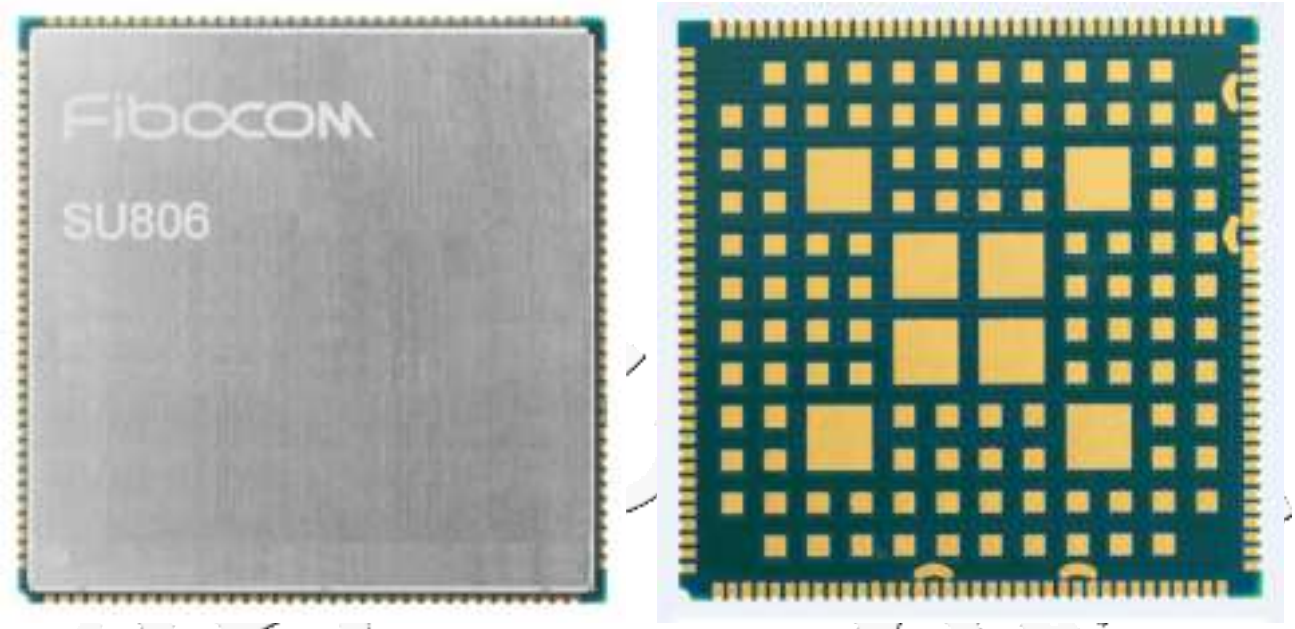

Figure 9-1 Module product appearance

9.2 Structural Dimension

The structural dimension of SU806 series module is shown in the following figure:

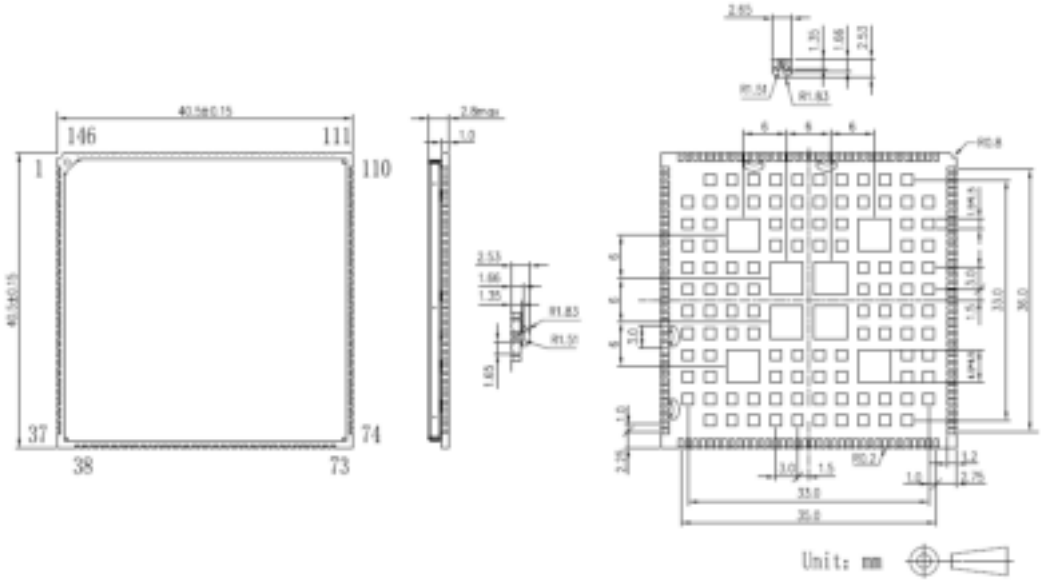

Figure 9-2 Structural dimension

9.3 PCB Soldering Pad and Stencil Design

PCB soldering pad and stencil design please refer to *FIBOCOM Sx806 Series SMT Design Guide*.

10 Production and Storage

10.1 SMT

SMT production process parameters and related requirements please refer to *FIBOCOM Sx806 Series SMT Design Guide*.

10.2 Carrier and Storage

Carrier and storage please refer to *FIBOCOM Sx806 Series SMT Design Guide*.

Appendix A Terms and Acronyms

Table A-0-1 Terms and acronyms

Term	Definition
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
EGSM	Extended GSM900 Band
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated

Term	Definition
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly PolarizedRMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value

Term	Definition
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Appendix B GPRS Encoding Scheme

Table B-0-1 GPRS encoding scheme

Encoding method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

Appendix C GPRS Multislot

In the GPRS standard, 29 types of GPRS multislot modes are defined and can be used by mobile stations. The multislot class defines the maximum rate of uplink and downlink. The expression is 3+1 or 2+2, the first number represents the number of downlink timeslots and the second number represents the number of uplink timeslots. Active timeslot represents the total number of timeslots that the GPRS device can use for both uplink and downlink communications.

Table C-0-1 Multilevel multislot allocation

Multislot Class	Downlink Slot	Uplink Slot	Active Slot
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

Appendix D EDGE Modulation and Encoding Method

Table D-0-1 EDGE modulation and encoding method

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	-	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	-	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	-	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	-	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps