# AIROCTM Bluetooth® & Bluetooth® LE module

## General description

The CYW30739B2-P5TAI051 module is a multi-protocol solution wireless module solution with an integrated 2.4 GHz transceiver that is Matter 1.2, Thread 1.3, and Bluetooth® 5.3-compliant. The CYW30739B2-P5TAI051 includes onboard crystal oscillators, 2 MB flash, passive components, and the CYW30739 silicon device.

The CYW30739B2-P5TAI051 supports a number of peripheral functions (ADC, PWM), as well as multiple serial communication protocols (UART, SPI, I2C, I2S/PCM). The device is intended for use in smart home applications such as thermostats, sensors, smart lighting and smart door locks. The CYW30739B2-P5TAI051 is the optimal solution for applications in smart home, industrial and Internet of Things (IoT) devices, with the flexibility to address the increasing size of protocol stacks and applications. The CYW30739B2-P5TAI051 includes a royalty-free stack compatible with Bluetooth® core specification v5.1 with Bluetooth® LE 2 Mbps and IEEE 802.15.4-2015 in a small module form-factor.

The CYW30739B2-P5TAI051 has 2MB external flash memory and qualified by Bluetooth® SIG and Matter v1.3, and includes regulatory certification approval for FCC, ISED, and CE.

## Module description

- Module size: 13.47 mm × 15.83 mm × 1.95 mm
- Complies with Bluetooth® Core specification version 5.3 supporting BR, EDR 2/3 Mbps, eSCO, Bluetooth® LE, and LE 2 Mbps.
  - QDID: **D068835**
  - Declaration ID: **243084**
- Certified for FCC ISED and CE
- Up to 13 GPIOs
- External 2048-KB flash memory. And Internal 1024-KB flash memory, 512-KB SRAM memory
- Industrial temperature range: –30 °C to +85 °C
- Integrated Arm® Cortex®-M4 microprocessor core with floating point unit (FPU)

## RF characteristics

- Maximum TX output power: +5.0 dBm
- Bluetooth® LE RX receive sensitivity: –92.0 dBm
- Received signal strength indicator (RSSI) with 1-dB resolution

## Power consumption

- TX current consumption
  - Bluetooth® LE silicon: 5.6 mA (MCU + radio only, 0 dBm)
- RX current consumption
  - Bluetooth® silicon: 5.9 mA (MCU + radio only)
- CYW30739 silicon low power mode support
  - PDS: 6.1 µA with 512 KB SRAM retention
  - SDS: 1.6 µA
  - HIDOFF (external interrupt): 400 nA

## Functional capabilities

- 1x ADC with (12-bit ENoB for DC measurement and 13-bit ENoB for Audio measurement) with 10 channels
- 1x HCI UART for programming and HCI
- 1x peripheral UART (PUART)
- 1x SPI (master or slave) blocks (SPI, Quad SPI, MIPI DBI-C)
- 1x I2C master/slave and 1x I2C master only
- I2S/PCM audio interfaces
- Up to 6 16-bit PWMs
- Watchdog timer (WDT)
- Bluetooth® Basic Rate (BR) and Enhanced Data Rate (EDR) Support
- Bluetooth® LE protocol stack supporting generic access profile (GAP) central, peripheral, or broadcaster roles
- Features are subject to support in the Bluetooth® SDK.
- Matter-ready SDK and Bluetooth® LE SDK: Check the latest version of the Bluetooth® SDK technical brief for supported features
- Hardware security engine

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# 1 Benefits

CYW30739B2-P5TAI051 is fully integrated and certified solution that provides all necessary components required to operate Bluetooth® and Matter communication standards.

- Proven hardware design ready to use
- Ultra-flexible supermux I/O design allows maximum flexibility for GPIO function assignment
- Large nonvolatile memory (1MB Internal + 2MB External) for complex application development
- Over-the-Air (OTA) update capable for development or field updates
- Bluetooth® SIG qualified with QDID and declaration ID

IEEE 802.15.4 architecture

- CYW30739 has 2 MB ROM, where stable software that requires little or no ongoing updates can be stored, thus freeing up much of the 1 MB internal flash on the part for application usage. The ROM currently includes the Bluetooth® LE software stack as well as support for hardware peripherals and the lower layers of the IEEE 802.15.4 MAC. Any updates to software in ROM can be implemented via patch code stored in flash and executed from RAM.
- CYW30739 supports the Thread networking standard for wireless mesh networking, which runs on top of the IEEE 802.15.4 MAC layer. It also supports the Matter protocol for interoperable device to device communications running on top of Thread. The Thread and Matter software stacks are maintained in flash currently, and executed from RAM.

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# 2 More information

Infineon provides a wealth of data at **www.infineon.com** to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

## 2.1 References

- Overview: **EZ-BLE/EZ-BT Module Portfolio**, **Module Roadmap**
- Development kits:
  - **CYW30739B2-P5TAI051** CYW30739 Base Module w/ 2 MB external flash
  - **CYW30739B2-P5-EVK**, Evaluation Kit for CYW30739 silicon device
- Test and debug tools:
  - **CYSmart**, Bluetooth® LE Test and Debug Tool (Windows)
  - **CYSmart Mobile**, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge base article
  - **KBA97095** - EZ-BLETM Module Placement
  - **KBA224516** - RF Regulatory Certifications for CYBT-483039-02 EZ-BTTM WICED Modules
  - **KBA213976** - FAQ for Bluetooth® LE and Regulatory Certifications with EZ-BLE modules
  - **KBA210802** - Queries on Bluetooth® LE Qualification and Declaration Processes
  - **KBA218122** - 3D Model Files for EZ-BLE/EZ-BT Modules
  - **KBA223428** - Programming an EZ-BT WICED Module
  - **KBA225450** - Putting 2073x, 2070x, and 20719 based devices or modules in HCI Mode

## 2.2 Technical support

- **Infineon Community:** Whether you're a customer, partner or a developer interested in the latest Infineon innovations, the Infineon Developer Community offers you a place to learn, share and engage with both Infineon experts and other embedded engineers around the world.
- **Frequently Asked Questions (FAQs)**: Learn more about our Bluetooth® ecosystem.
- Visit our **support** page and create a **technical support case** or contact a **local sales representatives**.

# 3 Overview

## Functional block diagram

**Figure 1** Figure 1 illustrates the CYW30739B2-P5TAI051 functional block diagram.

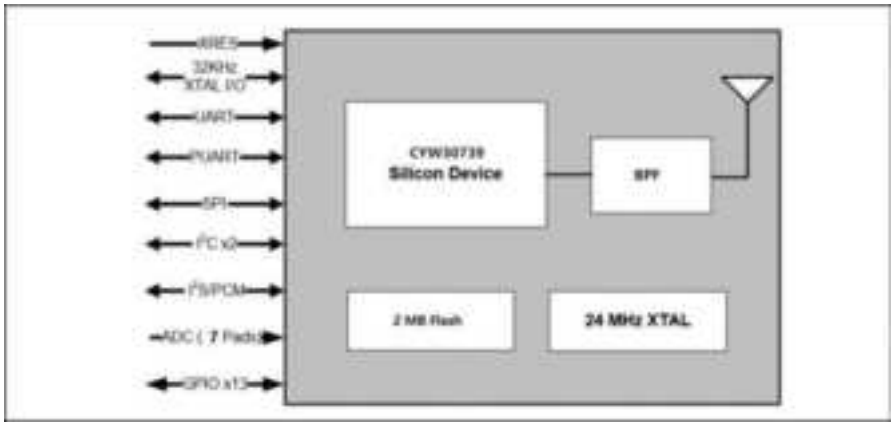



**Figure 1 Functional block diagram**

**Note** General purpose input/output pins shown in **Figure 1** are configurable to any specified input or output function in the SuperMux table detailed in **Table 4** in the **Module connections** section.

**Note** Connections shown in the above block diagram are maximum number of connections per function. The total number of GPIOs available on the CYW30739B2-P5TAI051 is 13.

## 3.1 Module description

The CYW30739B2-P5TAI051 module is a complete module designed to be soldered to the applications main board.

### 3.1.1 Module dimensions and drawing

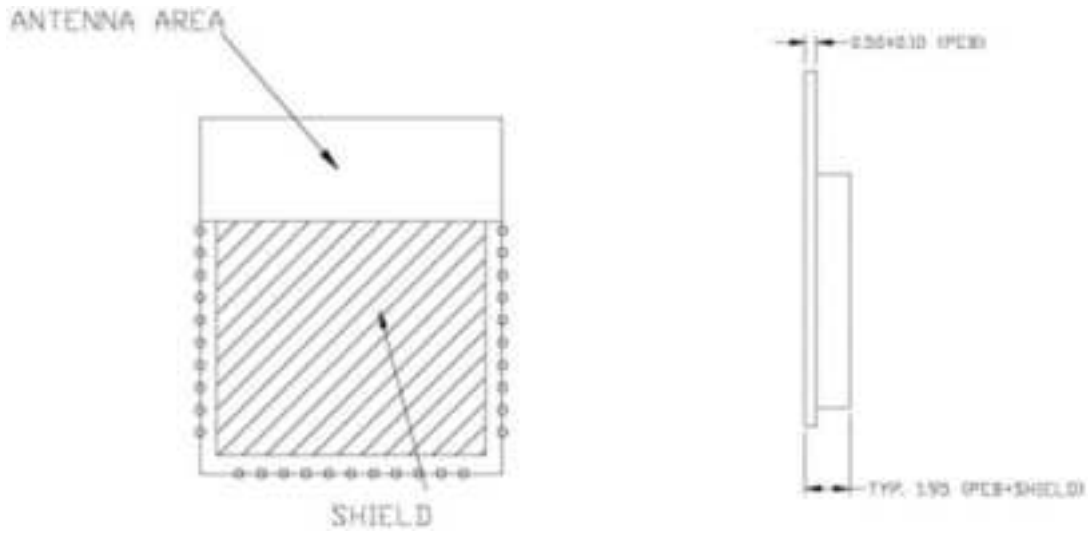
Infineon reserves the right to select components from various vendors to achieve the Bluetooth® module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Any changes to the current BOM for the CYW30739B2-P5TAI051 will not be made until approval is provided by the end customer for this product. The CYW30739B2-P5TAI051 will be held within the physical dimensions shown in the mechanical drawings in **Figure 2**. All dimensions are in millimeters (mm).

**Table 1. Module design dimensions**

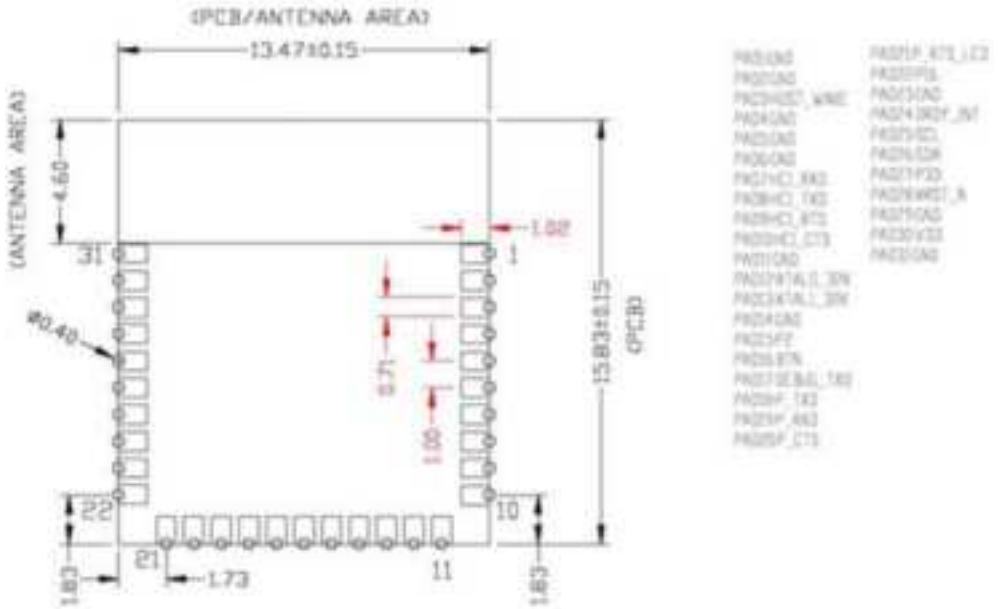
| Dimension item | Unit | Specification |
|---|---|---|
| Module dimensions | Length (X) | 13.47 ± 0.15 mm |
| | Width (Y) | 15.83 ± 0.15 mm |
| Antenna location dimensions | Length (X) | 13.47 mm |
| | Width (Y) | 4.60 mm |
| PCB thickness | Height (H) | 0.50 ± 0.10 mm |
| Shield height | Height (H) | 1.45 mm |
| Maximum component height | Height (H) | 0.95 mm typical (inductor) |
| Total module thickness (bottom of module to top of shield) | Height (H) | 1.95 mm typical |

Overview

See **Figure 2** for the mechanical reference drawing for CYW30739B2-P5TAI051.




**Top view (Seen from top)** **Side View**




**Bottom view (Seen from bottom)**

**Figure 2 Module mechanical drawing[1]**

**Note**
1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see **Recommended host PCB layout**.

# 4 Pad connection interface

As shown in the bottom view of **Figure 2**, the CYW30739B2-P5TAI051 has 31 connections to a host board via solder pads (SP). **Table 2** and **Figure 3** detail the solder pad length, width, and pitch dimensions of the CYW30739B2-P5TAI051 module.

**Table 2 Connection description**

| Name | Connections | Connection type | Pad length dimension | Pad width dimension | Pad pitch |
|---|---|---|---|---|---|
| SP | 31 | Solder pad | 1.02 mm | 0.71 mm | 1.00 mm |

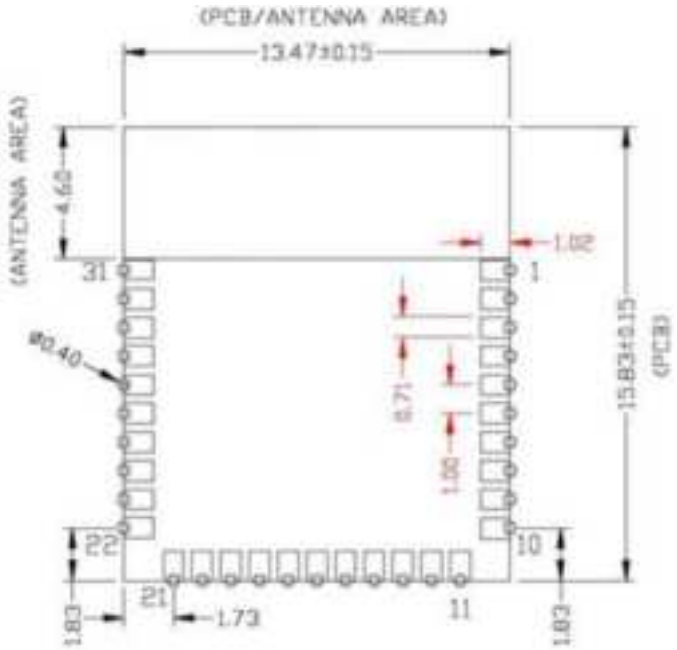



**Figure 3 Solder pad dimensions (seen from bottom)**

To maximize RF performance, the host layout should follow these recommendations:

1. Antenna area keepout: The host board directly below the antenna area of the module (see **Figure 2**) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module placement: The ideal placement of the Bluetooth® module is in a corner of the host board with the trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 3 below. Refer to **AN96841** for module placement best practices.
3. Optional keepout: To maximize RF performance, the area immediately around the Bluetooth® module trace antenna may contain an additional keep out area, where there are no grounding or signal traces. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in **Figure 4** (dimensions are in mm).

Pad connection interface

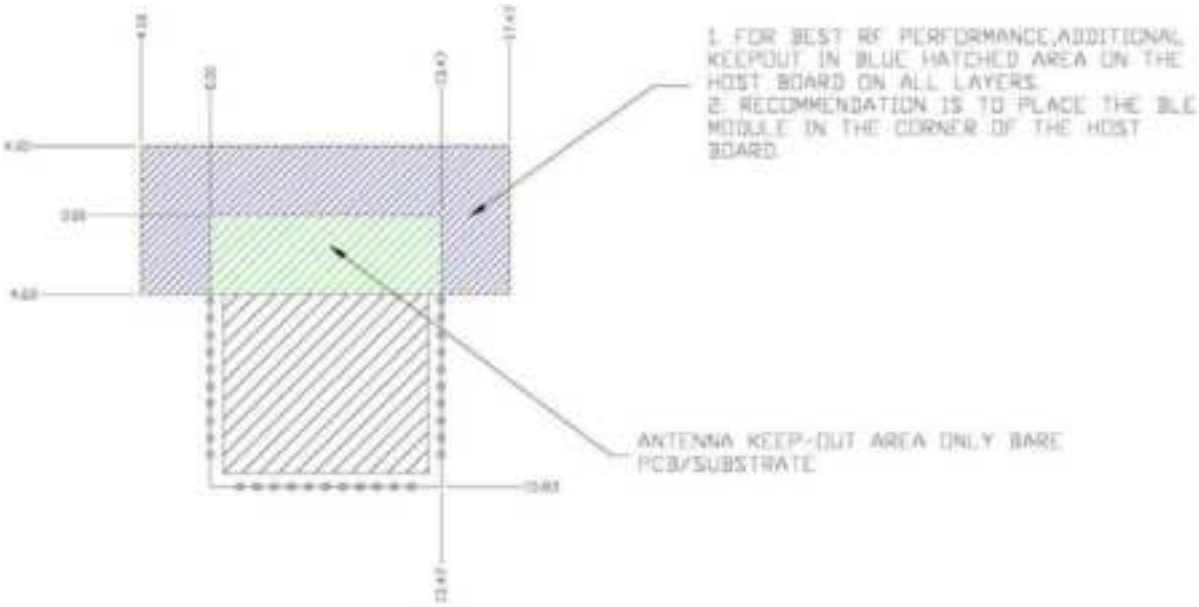



**Figure 4 Optional additional host PCB keep out area around the CYW30739B2-P5TAI051 trace antenna**

# 5 Recommended host PCB layout

**Figure 5**, **Figure 6**, provide details that can be used for the recommended host PCB layout pattern for the CYW30739B2-P5TAI051. Dimensions are in millimeters unless otherwise noted. Pad length of 1.02 mm (0.51 mm from center of the pad on either side) is the minimum recommended host pad length. The host PCB layout pattern can be completed using either **Figure5**, **Figure 6**. It is not necessary to use all figures to complete the host PCB layout pattern.

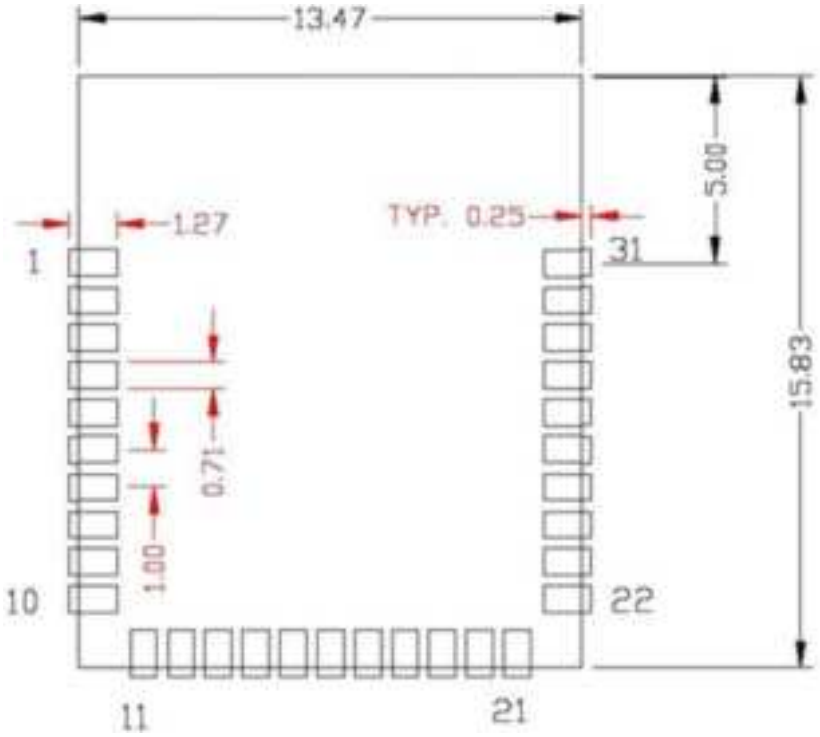



**Figure 5 CYW30739B2-P5TAI051 host layout (dimensioned)**

Recommended host PCB layout

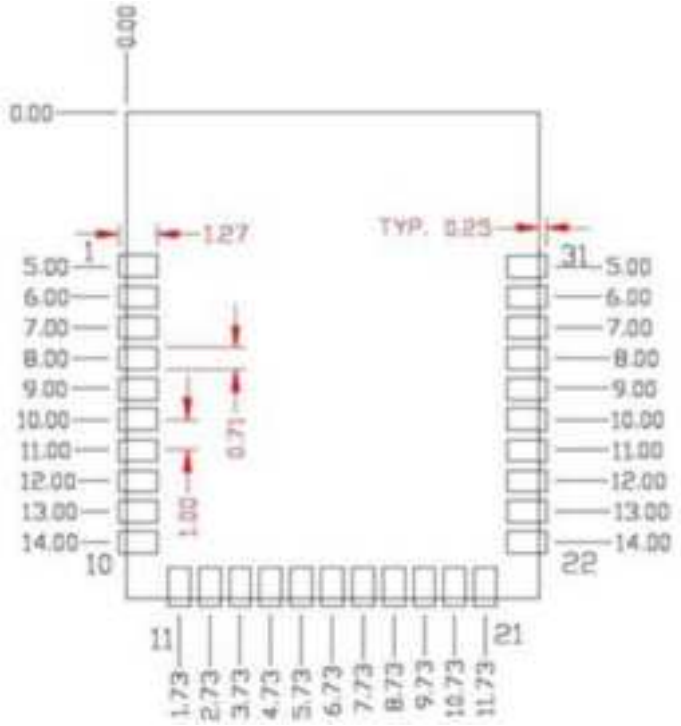



**Figure 6 CYW30739B2-P5TAI051 host layout (relative to origin)**

# 6 Module connections

**Table 3** details the solder pad connection definitions and available functions for each connection pad. The GPIO connections available on the CYW30739B2-P5TAI051 can be configured to any of the input or output functions listed in **Table 4**. **Table 3** specifies any function that is required to be used on a specific solder pad, and also identifies GPIOs that can be configured using the SuperMux.

**Table 3 CYW30739B2-P5TAI051 solder pad connection definitions**

| Pad | Pad name | Silicon pin name | XTAL I/O | ADC | GPIO | SuperMux capable[4] |
|---|---|---|---|---|---|---|
| 1 | GND | GND | Ground | | | |
| 2 | GND | GND | Ground | | | |
| 3 | HOST_WAKE | BT_HOST_WAKE | A signal from the CYW30739B2-P5TAI051 module to the host indicating that the Bluetooth® device requires attention. | | | |
| 4 | GND | GND | Ground | | | |
| 5 | GND | GND | Ground | | | |
| 6 | GND | GND | Ground | | | |
| 7 | HCI_RXD | BT_UART_RXD | UART serial input. Serial data input for the HCI UART interface. | | | |
| 8 | HCI_TXD | BT_UART_TXD | UART serial output. Serial data output for the HCI UART interface | | | |
| 9 | HCI_RTS | BT_UART_RTS_N | Request to send (RTS) for HCI UART interface. Leave unconnected if not used | | | |
| 10 | HCI_CTS | BT_UART_CTS_N | Clear to send (CTS) for HCI UART interface. Leave unconnected if not used. | | | |
| 11 | GND | GND | Ground | | | |
| 12 | XTALO_32K | XTALO_32K | Low-power oscillator output. | | | |
| 13 | XTALI_32K | XTALI_32K/P15 | Low-power oscillator input. | IN20 | V(P15) | Vsee **Table 4** |
| 14 | GND | GND | Ground | | | |
| 15 | P2 | P2 | | | V(P2) | Vsee **Table 4** |
| 16 | BTN | P4 | | | V(P4) | Vsee **Table 4** |
| 17 | DEBUG_TXD | P6 | | | V(P6) | Vsee **Table 4** |
| 18 | P_TXD | P7 | | | V(P7) | Vsee **Table 4** |
| 19 | P_RXD | P17 | | IN18 | V(P17) | Vsee **Table 4** |
| 20 | P_CTS | P10 | | IN25 | V(P10) | Vsee **Table 4** |
| 21 | P_RTS_LED | P28 | | IN11 | V(P28) | Vsee **Table 4** |
| 22 | P16 | P16 | | IN19 | V(P16) | Vsee **Table 4** |
| 23 | GND | GND | Ground | | | |
| 24 | DRDY_INT | P29 | | IN10 | V(P29) | Vsee **Table 4** |
| 25 | SCL | P26 | | | V(P26) | Vsee **Table 4** |
| 26 | SDA | P25 | | | V(P25) | Vsee **Table 4** |
| 27 | P33 | P33 | | IN6 | V(P33) | Vsee **Table 4** |
| 28 | XRST_N | RST_N | Active-low system reset with internal pull-up resistor. | | | |
| 29 | GND | GND | Ground | | | |
| 30 | VDD | SR_VDDBAT3V/ BT_VDDO/ VDDO | Power(1.76V~3.63V) | | | |
| 31 | GND | GND | Ground | | | |

**Notes**
1. The CYW30739B2-P5TAI051 can configure GPIO connections to any input/output function described in **Table 4**.
2. P15 should not be driven high externally while the part is held in reset (it can be floating or driven low). Failure to do so may cause some current to flow through P15 until the device comes out of reset.

**Table 4** details the available Input and output functions configurable to any solder pad in **Table 3** that are marked as SuperMux capable.

**Table 4 GPIO SuperMux input and output functions**

| Function | Input/output | Function type | GPIOs required | Function connection description |
|---|---|---|---|---|
| SPI | Input/output | Serial communication (Master or Slave) | 4 ~ 8 | SPI clock |
| | | | | SPI chip select |
| | | | | SPI MOSI |
| | | | | SPI MISO |
| | | | | SPI I/O 2 (Quad SPI) |
| | | | | SPI I/O 3 (Quad SPI) |
| | | | | SPI interrupt |
| | Output | | | SPI DCX (DBI-C DCX 8-bit mode) |
| PUART | Input | Serial communication input | 4 | Peripheral UART RX |
| | | | | Peripheral UART CTS |
| | Output | Serial communication output | | Peripheral UART TX |
| | | | | Peripheral UART RTS |
| $I^2C$ | Input/Output | Serial communication (Master or Slave) | 2 | I2C clock |
| | | | | I2C data |
| PCM In | Input | Audio input communication | 3 | PCM input |
| | | | | PCM clock |
| | | | | PCM sync |
| PCM Out | Output | Audio output communication | 3 | PCM output |
| | | | | PCM clock |
| | | | | PCM sync |
| $I^2S$ In | Input | Audio input communication | 3 | I2S DI, data input |
| | | | | I2S WS, word select |
| | | | | I2S clock |
| $I^2S$ Out | Output | Audio output communication | 3 | I2S DO, data output |
| | | | | I2S WS, word select |
| | | | | I2S clock |
| PDM | Input | Microphone | 1 ~ 2 | PDM input channel 1 |
| | | | | PDM input channel 2 |

## 6.1 Connections and optional external components

## 6.2 Power connections ($V_{DD}$)

The CYW30739B2-P5TAI051 contains one power supply connections, $V_{DD}$.

$V_{DD}$ is the power supply connection for the CYW30739 silicon device. $V_{DD}$ accepts a supply input of 1.76 V to 3.63 V. **Table 11** provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in **Table 11**.

### 6.2.1 Considerations and optional components for brownout (BO) conditions

Power supply design must be completed to ensure that the CYW30739B2-P5TAI051 module does not encounter a brownout condition, which can lead to unexpected functionality, or module lock up. A brownout condition may be met if power supply provided to the module during power up or reset is in the range shown below: $V_{IL} \leq VDD \leq VIH$.

Refer to **Table 17** for the $V_{IL}$ and $V_{IH}$ specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (i.e. battery installation, high value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the brownout voltage range from occurring during power removal.

**Figure 7** shows the recommended circuit design when using an external voltage detection IC.

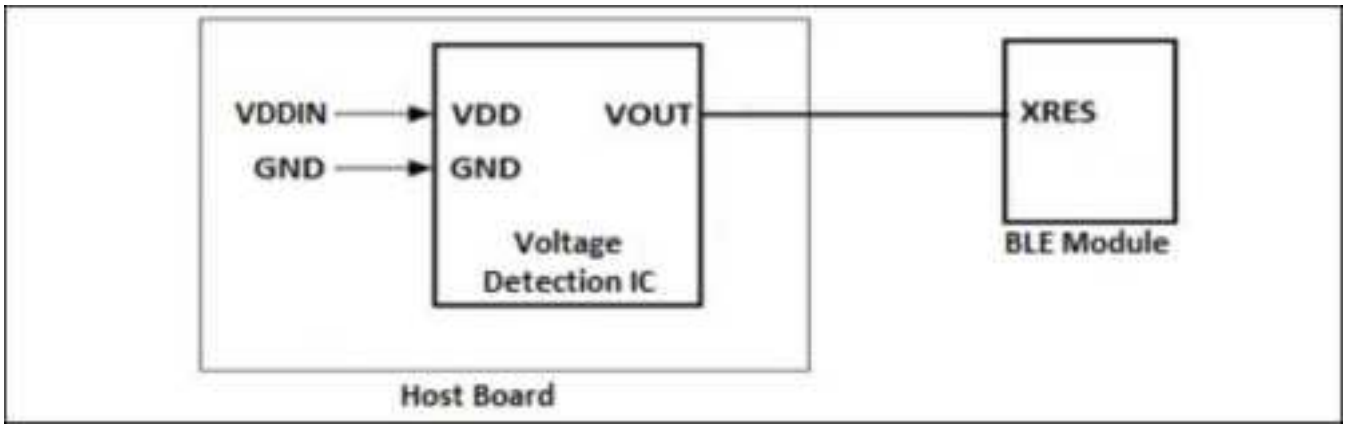



**Figure 7 Reference circuit block diagram for external voltage detection IC**

In the event that the module does encounter a brownout condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brownout conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a brownout condition.

## 6.3 External reset (XRES)

The CYW30739B2-P5TAI051 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be invoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYW30739B2-P5TAI051 module (solder pad 28). The CYW30739B2-P5TAI051 module does not require an external pull-up resistor on the XRES input.

During power on operation, the XRES connection to the CYW30739B2-P5TAI051 is required to be held low 50 ms after the $V_{DD}$ power supply input to the module is stable. This can be accomplished in the following ways:

- The host device can connect a GPIO to the XRES of CYW30739B2-P5TAI051 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after $V_{DD}$ is stable.
- If the XRES connection of the CYW30739B2-P5TAI051 module is not used in the application, a 0.33 µF capacitor may be connected to the XRES solder pad of the CYW30739B2-P5TAI051 in order to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the $V_{DD}$ power supply ramp time of the system. The capacitor value should result in an XRES release timing of at least 50 ms after $V_{DD}$ stability.
- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after $V_{DD}$ is stable.

Refer to **Figure 10** for XRES operating and timing requirements during power-on events.

## 6.4 HCI UART connections

The recommendations in this section apply to the HCI UART (Solder pads 7, 8, 9, and 10). For full UART functionality, all UART signals must be connected to the Host device (CTS must be pulled high when power-on/reset). If full UART functionality is not being used, and only UART RXD and TXD are desired or capable, then the following connection considerations should be followed for UART RTS and CTS:

- ·UART RTS: Must be left floating.
- ·UART CTS: Must be pulled high when power-on/reset and be pulled low after application startup to bypass flow control and ensure that continuous data transfers are made from the host to the module.

## 6.5 External component recommendation

### 6.5.1 Power supply input options and circuitry

It is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pad connection.

The recommended ferrite bead value is 330Ω, 100 MHz (Murata BLM21PG331SN1D).

Module connections

**Figure 8** illustrates the CYW30739B2-P5TAI051 schematic.

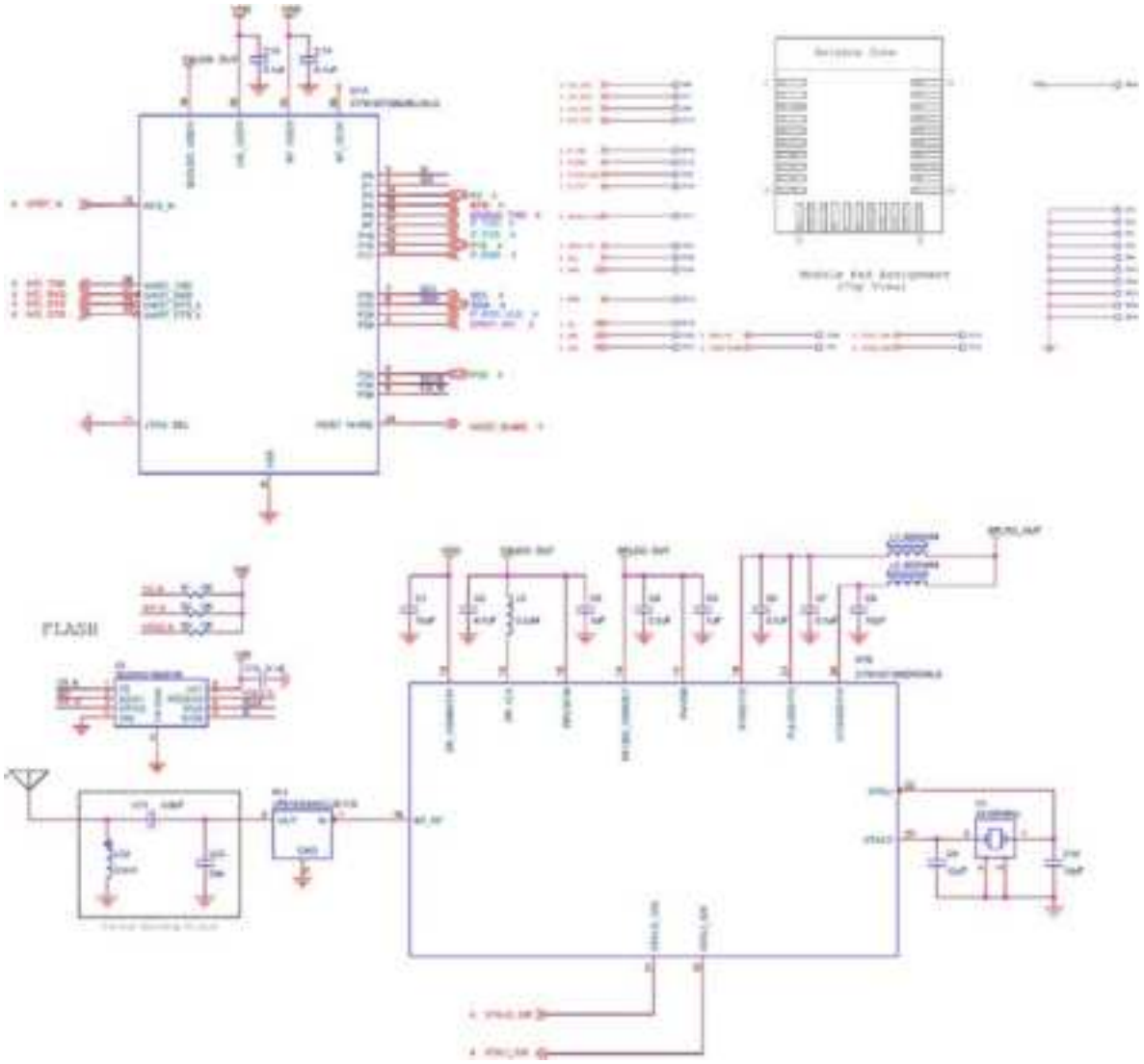


**Figure 8 CYW30739B2-P5TAI051 schematic diagram**

## 6.6 Critical components list

Table 5 details the critical components used in the CYW30739B2-P5TAI051 module.

**Table 5. Critical component list**

| Component | Reference designator | Description |
|---|---|---|
| Silicon | U1 | 40-pin QFN Bluetooth® silicon device – CYW30739 |
| Crystal | Y1 | 24 MHz, 12 pF |

## 6.7 Antenna design

Table 6 details the trace antenna used in the CYW30739B2-P5TAI051 module.

**Table 6. Trace antenna specifications**

| Item | Description |
|---|---|
| Frequency range | 2400 – 2500 MHz |
| Peak gain | –0.9 dBi typical |
| Return loss | –10.0 dB typical |

# 7 Bluetooth® Baseband Core

The Bluetooth® Baseband Core (BBC) implements all time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening.

**Table 7 Bluetooth® features**

| **Bluetooth® 1.0** | **Bluetooth® 1.2** | **Bluetooth® 2.0** |
|---|---|---|
| Basic rate | Interlaced scans | EDR 2 Mbps and 3 Mbps |
| SCO | Adaptive frequency hopping | – |
| Paging and inquiry | eSCO | – |
| Page and inquiry scan | – | – |
| Sniff | – | – |
| **Bluetooth® 2.1** | **Bluetooth® 3.0** | **Bluetooth® 4.0** |
| Secure simple pairing | Unicast connectionless data | Bluetooth® Low Energy |
| Enhanced inquiry response | Enhanced power control | – |
| Sniff subrating | eSCO | – |
| **Bluetooth® 4.1** | **Bluetooth® 4.2** | **Bluetooth® 5.0** |
| Low duty cycle advertising | Data packet length extension | LE 2 Mbps |
| Dual mode | LE secure connection | Slot availability mask |
| LE link layer topology | Link layer privacy | High duty cycle advertising |

## 7.1 BQB and regulatory testing support

CYW30739B2-P5TAI051 fully supports Bluetooth® Test mode as described in Part I:1 of the specification of the Bluetooth® system version 3.0. This includes the transmitter tests, normal and delayed loop back tests, and reduced hopping sequence.

In addition to the standard Bluetooth® Test mode, CYW30739B2-P5TAI051 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

# 8 Power management unit

Figure 9 shows the CYW30739 power management unit (PMU) block diagram. The CYW30739 includes an integrated buck regulator, a bypass LDO, a capless LDO for digital circuits and a separate LDO for RF. The bypass LDO automatically takes over from the buck once $V_{BAT}$ supply falls below 2.1 V.

The voltage levels shown in this figure are the default settings; the firmware may change voltage levels based on operating conditions.

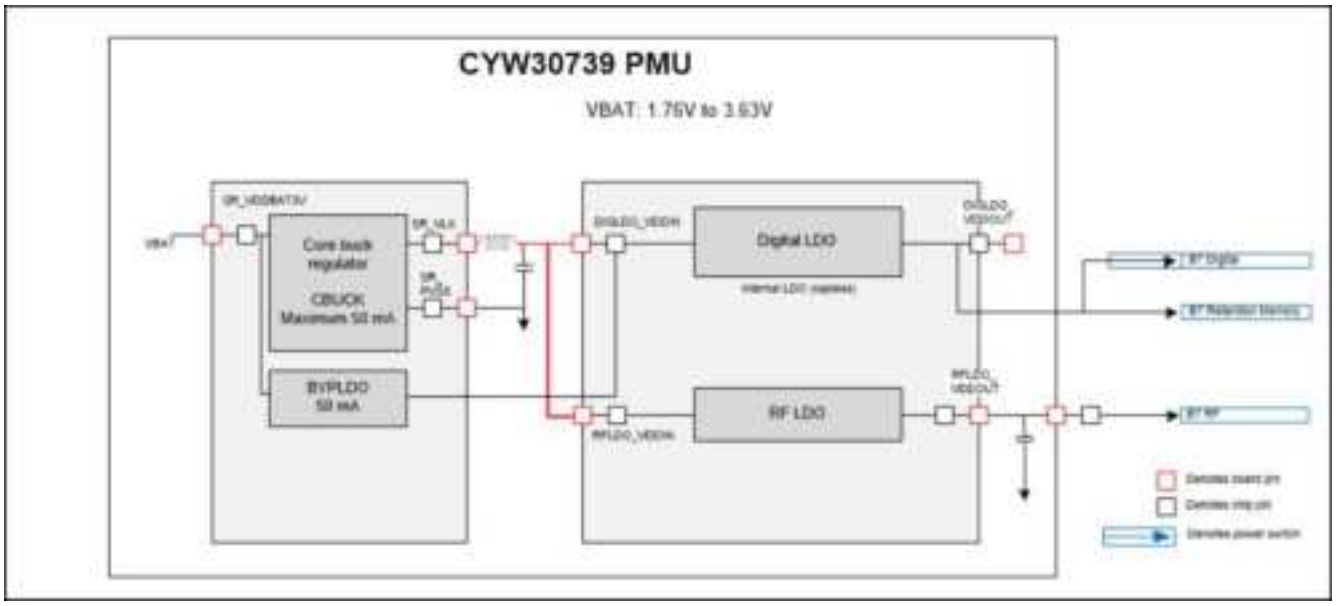



**Figure 9 Default usage mode**

# 9 Integrated radio transceiver

The CYW30739B2-P5TAI051 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth® Radio specification 3.0 and meets or exceeds the requirements to provide the highest communication link quality of service.

## 9.1 Transmitter path

CYW30739B2-P5TAI051 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

### 9.1.1 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

## 9.2 Receiver path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYW30739B2-P5TAI051 to be used in most applications without off-chip filtering.

### 9.2.1 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

### 9.2.2 Receiver signal strength indicator

The radio portion of the CYW30739B2-P5TAI051 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

## 9.3 Local oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The CYW30739B2-P5TAI051 uses an internal loop filter.

# 10 Microcontroller unit

The CYW30739B2-P5TAI051 includes a Arm® Cortex®-M4 processor with 2 MB of ROM, 448 KB of data RAM, 64 KB of patch RAM, and 1 MB of on-chip flash. The CM4 has a maximum speed of 96 MHz. CYW30739B2-P5TAI051 supports execution from on-chip flash (OCF).

The CM4 also includes a single precision IEEE 754 compliant floating point unit (FPU).

The CM4 runs all the BT layers as well as application code. The ROM includes LM, HCI, L2CAP, GATT, as well as other stack layers freeing up the flash for application usage. A standard serial wire debug (SWD) interface provides debugging support.

## 10.1 External reset

An external active-low reset signal, XRES, can be used to put the CYW30739B2-P5TAI051 in the reset state. An external voltage detector reset IC with 50 ms delay is recommended on the XRES connection. The XRES must only be released after the $V_{DDO}$ supply voltage level has been stabilized for 50 ms.

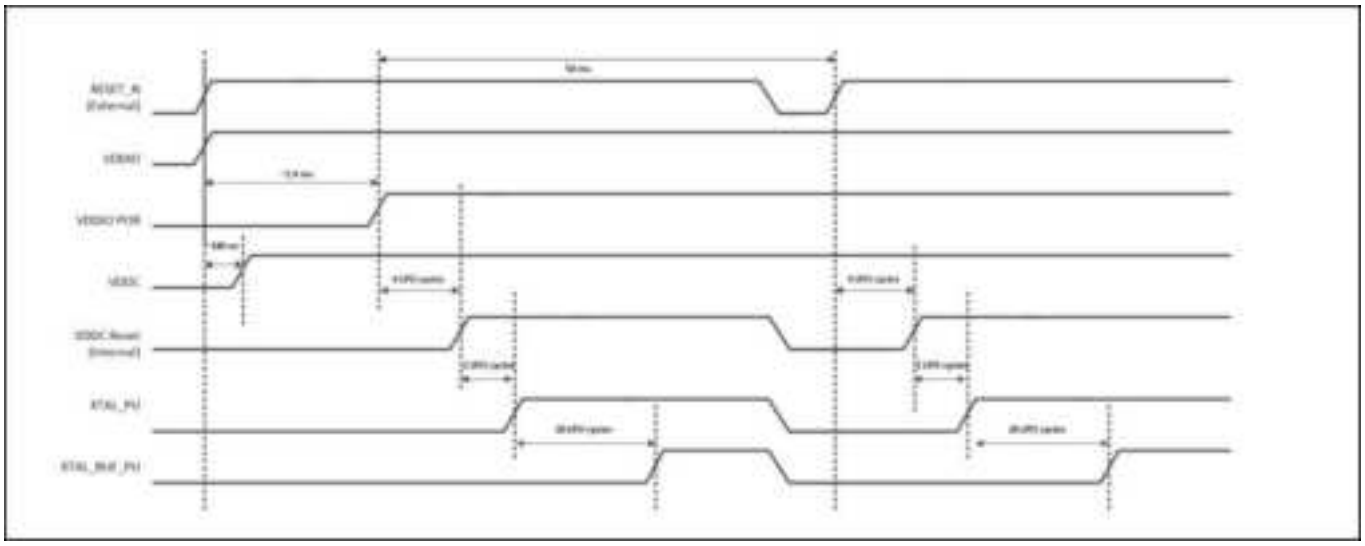


**Figure 10 Reset timing**

# 11 Peripheral and communication interfaces

## 11.1 I²C

The CYW30739B2-P5TAI051 provides a 2-pin I²C compatible master interface to communicate with I²C compatible peripherals. The following transfer clock rates are supported are:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I²C-compatible speed)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed)

SCL and SDA lines can be routed to any of the P0-P39 GPIOs allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. I²C block does not support multi master capability by either master or slave devices.

I²C is master only.

## 11.2 HCI UART interface

The CYW30739B2-P5TAI051 includes a UART interface for factory programming as well as when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 1.5 Mbps. Typical rates are 115200, 921600, 1500000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYW30739B2-P5TAI051 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%. The UART interface has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The CYW30739B2-P5TAI051 can wake up the host as needed or allow the host to sleep via the HOST_WAKE signal (solder pad 2). The signal allows the CYW30739B2-P5TAI051 to optimize system power consumption by allowing a host device to remain in low power modes as long as possible. The HOST_WAKE signal can be enabled via a vendor-specific command.

## 11.3 Peripheral UART interface

The CYW30739B2-P5TAI051 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYW30739B2-P5TAI051 can map the peripheral UART to any GPIO. The Peripheral UART functionality is the same as the HCI UART, but with a 256-byte transmit and receive FIFO.

## 11.4 Serial peripheral interface

The CYW30739B2-P5TAI051 has two independent SPI interfaces. Both interfaces support Single, Dual, and Quad mode SPI operations as well as MIPI DBI-C Interface. Either of the interface can be a master or a slave. SPI2 can support only 1 slave. SPI1 has a 1024 byte transmit and receive buffers which is shared with the host UART interface. SPI2 has a dedicated 256-byte transmit and receive buffers. To support more flexibility for user applications, the CYW30739B2-P5TAI051 has optional I/O ports that can be configured individually and separately for each functional pin. SPI IO voltage depends on $V_{DDO}$.

### 11.4.1 MIPI interface

There are three options in DBI type-C corresponding to 9-bit, 16-bit, and 8-bit modes. The CYW30739B2-P5TAI051 plays the role of host, and only the 9-bit and 8-bit modes (option 1 and option 3 in DBI-C spec) are supported. In the 9-bit mode, the SCL, CS, MOSI, and MISO pins are used. In the 8-bit mode, an additional pin (DCX) is required. The DCX pin indicates if the current outgoing bit stream is a command or data byte.

## 11.5 32-kHz crystal oscillator

The CYW30739B2-P5TAI051 utilizes the built-in local oscillator (LO) on the CYW30739 silicon device for 32-kHz timing. The accuracy of the LO is +/- 500 ppm. The use of an external XTAL oscillator is optional. CYW30739B2-P5TAI051 includes external XTAL oscillator connections for applications requiring higher timing accuracy. **Figure 11** shows an external 32-kHz XTAL oscillator with external components and **Table 8** lists the recommended external oscillator's characteristics. This oscillator input can be operated with a 32-kHz or 32.768-kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΙ and C1 = C2 = ~6 pF. The values of C1 and C2 are used to fine-tune the oscillator.

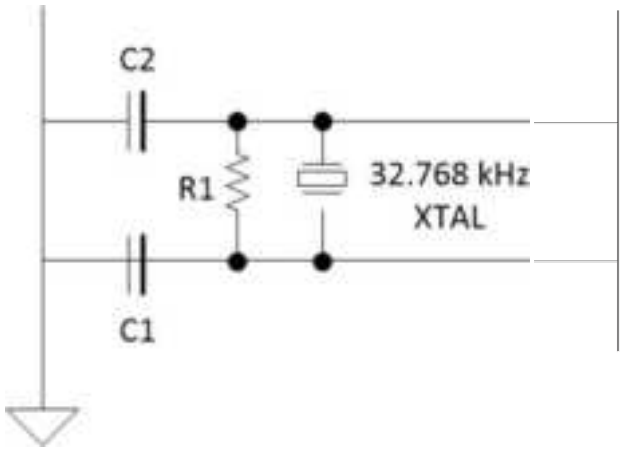



**Figure 11 32-kHz oscillator block diagram**

**Table 8 XTAL oscillator characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output frequency | $F_{oscout}$ | – | – | 32.76 | – | kHz |
| Frequency tolerance | – | Crystal-dependent | – | 100 | – | ppm |
| Start-up time | $T_{startup}$ | – | – | 500 | – | ms |
| XTAL drive level | $P_{drv}$ | For crystal selection | – | – | 0.5 | µW |
| XTAL series resistance | $R_{series}$ | For crystal selection | – | – | 70 | kΙ |
| XTAL shunt capacitance | $C_{shunt}$ | For crystal selection | – | – | 2.2 | pF |
| External AC input amplitude | $V_{IN}$ (AC) | $C_{couple}$ = 100 pF; $R_{bias}$ = 10 MΙ | 400 | – | – | mVpp |

## 11.6 ADC port

The ADC is a - ADC core designed for audio (13 bits) and DC (12 bits) measurement. It operates at 12 MHz and has 10 solder pad connections that can act as input channels. The internal bandgap reference has ±5% accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

The following CYW30739B2-P5TAI051 module solder pads can be used as ADC inputs:

- Pad 13: P15, ADC input channel 20

NoteP15 should not be driven high externally while the part is held in reset (it can be floating or driven low). Failure to do so may cause some current to flow through P15 until the device comes out of reset.

- Pad 19: P17, ADC input channel 18
- Pad 20: P10, ADC input channel 25
- Pad 21: P28, ADC input channel 11

- Pad 22: P16, ADC input channel 19
- Pad 24: P29, ADC input channel 10
- Pad 27: P33, ADC input channel 6

## 11.7 GPIO ports

The CYW30739B2-P5TAI051 has a maximum of 13 general-purpose I/Os (GPIOs). All GPIOs support the following:

- Programmable pull-up/down of approximately 45 kΩ.
- Input disable, allowing pins to be left floating or analog signals connected without risk of leakage.
- Source/sink 8 mA at 3.3 V and 4 mA at 1.8 V.
- P15 is Bonded to the same pin as XTALI_32K (Pad 13). If an external 32.768 kHz crystal is not used, then this pin can be used as GPIO P15.
- P26/P28/P29 can sink/source 16 mA at 3.3V and 8 mA at 1.8V.

Most peripheral functions can be assigned to any GPIO. For details, refer to **Table 4**. For more details on SuperMux configuration and control, refer to “Supermux Wizard for CYW30739” user guide.

The list below details the GPIOs that are available on the CYW30739B2-P5TAI051 module:

- P2, P4, P6, P7, P10, P16, P17, P25, P26, P28, P29, and P33
- P15/XTALI_32K (double bonded pin on the CYW30739B2-P5TAI051 module, only one of two is available)

For GPIOs highlighted as double bonded connections, only one of the connections can be used at a given time. When a certain GPIO is selected, the other GPIOs bonded to the same connection must be configured to input with output disable.

## 11.8 PWM

The CYW30739B2-P5TAI051 has six internal PWMs, labeled PWM0-5. The PWM module consists of the following:

- Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

The application can access the PWM module through the FW driver.

**Figure 12** shows the structure of one PWM channel.

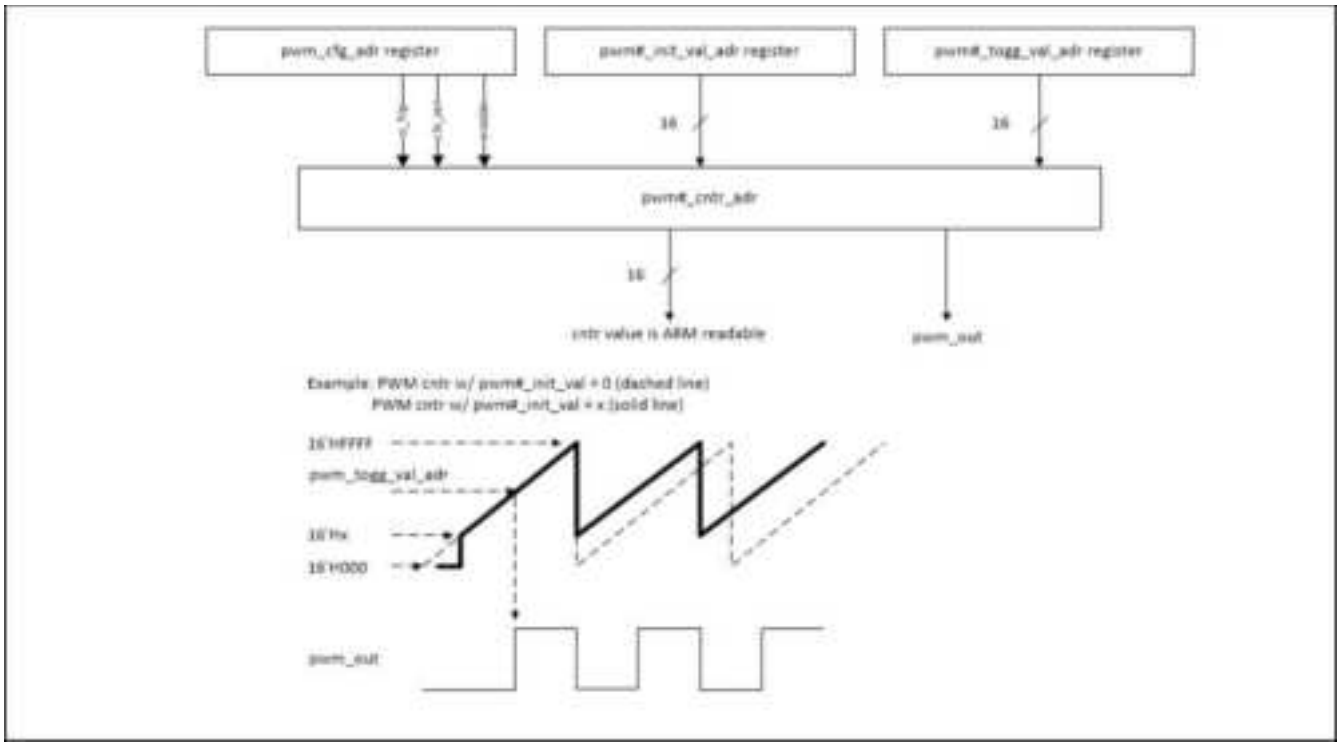



**Figure 12 PWM block diagram**

## 11.9 PDM microphone

The CYW30739B2-P5TAI051 accepts a L\-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM input shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4 MHz clock generated by the CYW30739B2-P5TAI051 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

**Note** Subject to the driver support in WICED Studio.

## 11.10 I²S interface

The CYW30739B2-P5TAI051 supports a single I²S digital audio port with both master and slave modes. The I²S signals are:

- I²S clock: I²S SCK
- I²S word select: I²S WS
- I²S data out: I²S DO
- I²S data in: I²S DI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S DO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSN of the left-channel data is aligned with the MSB of the I²S bus, per I²S Specifications. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW30739B2-P5TAI051 are synchronized with the falling edge of I²S SCK and should be sampled by the receiver on the rising edge of the I²S SCK.

**Note** The PCM interface shares HW with the I²S interface and only one can be used at a given time.

## 11.11 PCM interface

The CYW30739B2-P5TAI051 includes a PCM interface that can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW30739B2-P5TAI051 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW30739B2-P5TAI051.The configuration of the PCM interface may be adjusted by the host using vendor-specific HCI commands.

**Note** The PCM interface shares HW with the I²S interface and only one can be used at a given time.

### 11.11.1 Slot mapping

The CYW30739B2-P5TAI051 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM Interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

### 11.11.2 Frame synchronization

The CYW30739B2-P5TAI051 supports both short- and long-frame synchronization in both master and slave modes. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCGM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

### 11.11.3 Data formatting

The CYW30739B2-P5TAI051 may be configured to generate and accept several different data formats. For conventional narrow band speech mode, the CYW30739B2-P5TAI051 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

### 11.11.4 Burst PCM mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

## 11.12 Security engine

The CYW30739B2-P5TAI051 includes a hardware security accelerator which greatly decreases the time required to perform typical security operations. Access to the hardware block is provided via a firmware interface.

This security engine includes:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)

**Note** Security engine is used only by the Bluetooth® stack to reduce CPU overhead. It is not available for application use.

### 11.12.1 Random number generator

This hardware block is used for key generation for Bluetooth®.

**Note** Availability for use by the application is subject to the support in WICED Studio.

**Note** The random number generator block must be warmed up prior to use. A delay of 500 ms from cold boot is necessary prior to using the random number generator.

# 12 Power modes

The CYW30739B2-P5TAI051 support the following HW power modes are supported:

- **Active mode** - Normal operating mode in which all peripherals are available and the CPU is active.
- **Idle mode** - In this mode, the CPU is in “Wait for Interrupt” (WFI) and the HCLK, which is the high frequency clock derived from the main crystal oscillator is running at a lower clock speed. Other clocks are active and the state of the entire chip is retained.
- **Sleep mode** - In this mode, CPU is in WFI and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. State of the entire chip is retained, the internal LDOs run at a lower voltage (voltage is managed by the PMU), and SRAM is retained.
- **PDS mode** - This mode is an extension of the PMU Sleep wherein most of the peripherals such as UART and SPI are turned off. The entire memory is retained, and on wakeup the execution resumes from where it paused.
- **Shut Down Sleep (SDS)** - Everything is turned off except the IO power domain, RTC, and LPO. The device can come out of this mode either due to BT activity or by an external interrupt. Before going into this mode, the application can store some bytes of data into “Always On RAM” (AON). When the device comes out of this mode, the data from AON is restored. After waking from SDS, the application will start from the beginning (warmboot) and has to restore its state based on information stored in AON. In the SDS mode, a single BT task with no data activity, such as an ACL connection, Bluetooth® LE connection, or Bluetooth® LE advertisement can be performed.
- **HIDOFF (Timed-Wake) mode** - The device can enter this mode asynchronously, that is, the application can force the device into this mode at any time. IO power domain, RTC, and LPO are the only active blocks. A timer that runs off the LPO is used to wake the device up after a predetermined fixed time.
- **HIDOFF (External Interrupt-Waked) mode** - This mode is similar to Timed-Wake, but in HID-off mode even the LPO and RTC are turned off. So, the only wakeup source is an external interrupt.

Transition between power modes is handled by the on-chip firmware with host/application involvement. Refer to the **Firmware** section for details.

# 13 Firmware

The CYW30739B2-P5TAI051 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the BT/LE baseband, LM, HCI, GATT, ATT, L2CAP and SDP layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes.

# 14 Electrical characteristics

The absolute maximum ratings in the following table indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 9 Silicon absolute maximum ratings**

| Requirement parameter | Specification | | | Unit |
|---|---|---|---|---|
| | Min | Nom | Max | |
| Maximum junction temperature | – | – | 125 | °C |
| $V_{DDIO}$ | –0.5 | – | 3.795 | V |
| $V_{DDRF}$ | –0.5 | – | 1.38 | V |
| $V_{DDBAT3V}$ | –0.5 | – | 3.795 | V |
| DIGLDO_VDDIN1P5 | –0.5 | – | 1.65 | V |
| RFLDO_VDDIN1P5 | –0.5 | – | 1.65 | V |
| PALDO_VDDIN_5V | –0.5 | – | 3.795 | V |
| MIC_AVDD | –0.5 | – | 3.795 | V |

**Table 10 ESD/latchup**

| Requirement parameter | Specification | | | Unit |
|---|---|---|---|---|
| | Min | Nom | Max | |
| ESD tolerance HBM (Silicon) | –2000 | – | 2000 | V |
| ESD tolerance CDM (Silicon) | –500 | – | 500 | V |
| Latchup | – | 200 | – | mA |

**Table 11 Power supply specifications**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ input | Module chipset input | 1.76 | 3.0 | 3.63 | V |
| $V_{DDPA}$ input | Module PA/LNA input | 2.0 | 3.0 | 3.60 | V |
| $V_{DD}$ ripple | Module input ripple ($V_{DDPA}$, $V_{DD}$) | – | – | 100 | mV |
| $V_{BAT}$ input | Internal to module (not accessible) | 1.90 | 3.0 | 3.6 | V |
| PMU turn-on time | $V_{BAT}$ is ready | – | – | 300 | µs |

The CYW30739B2-P5TAI051 uses an onboard low voltage detector to shut down the part when supply voltage ($V_{DD}$) drops below operating range.

**Table 12 Power supply shut down specifications**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $V_{SHUT}$ | 1.625 | 1.7 | 1.76 | V |

**Table 13 Bluetooth®, Bluetooth® LE, BR and EDR current consumption**

| Parameter | Description | Silicon or module parameter | Typ | Unit |
|---|---|---|---|---|
| HCI | 48 MHz with pause | Silicon | 1.1 | mA |
| HCI | 48 MHz without pause | Silicon | 2.2 | mA |
| RX | Continuous RX | Silicon | 5.9 | mA |
| TX | Continuous TX - 0 dBm | Silicon | 5.6 | mA |
| PDS | – | Silicon | 6.1 | pA |
| HID-Off (SDS) | 32 kHz XTAL and 16 KB retention RAM on | Silicon | 1.6 | pA |
| Advertising | Unconnectable - 1 second | Silicon | 14 | pA |
| Advertising | Connectable undirected - 1 second | Silicon | 17 | pA |
| Page Scan - PDS | Interlaced - R1 | Silicon | 122 | pA |
| Sniff - PDS | 500 ms Sniff, 1 attempt, 0 timeout - Master | Silicon | 132 | pA |
| Sniff - PDS | 500 ms Sniff, 1 attempt, 0 timeout - Slave | Silicon | 138 | pA |
| Bidirectional data exchange | Continuous DM5 or DH5 packets - Master or slave | Silicon | 6.9 | mA |
| Bluetooth® Low Energy (20 dBm) | | | | |
| RX peak | Peak RX current | Module | 8.8 | mA |
| TX peak | Peak TX current | Module | 90 | mA |
| PDS | – | Module | 13.9 | pA |
| HID-Off (SDS) | – | Module | 14.9 | pA |
| Advertising - SDS | Connectable undirected - 1 second | Module | 48 | pA |
| LE connection - SDS | Slave - 1 second | Module | 35 | pA |
| Bluetooth® Classic (BR, EDR, 20 dBm) | | | | |
| IDLE | Module is idle, non-discoverable and non-connectable | Module | 8.3 | pA |
| Iscan | Inquiry scan (1.28 seconds) | Module | 160 | pA |
| Pscan | Page scan (1.28 seconds) | Module | 160 | pA |
| IScan + Pscan | Inquiry scan + page scan (1.28 seconds) | Module | 10.4 | pA |
| Connected | Connected with no data transfer | Module | 12.7 | mA |
| Connected + Pscan | Connected with no data transfer + page scan (1.28 seconds) | Module | 12.75 | mA |
| Connected + IScan + Pscan | Connected with no data transfer + inquiry scan (1.28 seconds) + page scan (1.28 seconds) | Module | 12.9 | mA |
| Connected + SNIFF | Connected with no data transfer + SNIFF (500 ms) | Module | 10 | mA |
| Connected + SNIFF + IScan + Pscan | Connected with no data transfer + SNIFF (500 ms) + inquiry scan and page scan 1.28 seconds | Module | 10.5 | mA |
| TX_BR | Data transfer @115200 baud rate | Module | 21.5 | mA |
| TX + SNIFF_BR | Data transfer @115200 baud rate + SNIFF (500 ms) | Module | 14.5 | mA |

**Table 14. Power amplifier/low noise amplifier current consumption specifications**

| Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX high power current | Pout = +20dBm | – | 100 | – | mA |
| TX quiescent current | No RF applied | – | 17 | – | mA |
| RX quiescent current | No RF applied | – | 8 | – | mA |

## 14.1 Core buck regulator

**Table 15 Silicon core buck regulator**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage DC, VBAT | DC voltage range inclusive of distur-bances | 1.90 | 3.0 | 3.63 | V |
| CBUCK output current | LPOM only | – | – | 65 | mA |
| Output voltage range | Programmable, 30 mV/step default = 1.2V (bits = 0000) | 1.2 | 1.26 | 1.5 | V |
| Output voltage DC accuracy | Includes load and line regulation | –4 | – | +4 | % |
| LPOM efficiency (high load) | – | – | 85 | – | % |
| LPOM efficiency (low load) | – | – | 80 | – | % |
| Input supply voltage ramp-up time | 0 to 3.3V | 40 | – | – | µs |

- Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.
- Maximum capacitor value refers to the total capacitance seen at a node where the capacitor is connected. This also includes any decoupling capacitors connected at the load side, if any.

## 14.2 Digital LDO

**Table 16 Digital LDO**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input supply voltage, Vin | Minimum Vin = Vo + 0.12V requirement must be met under maximum load. | 1.2 | 1.2 | 1.6 | V |
| Nominal output voltage, Vo | Internal default setting | – | 1.1 | – | V |
| Dropout voltage | At maximum load | – | – | 120 | mV |

## 14.3 Digital I/O characteristics

**Table 17 Digital I/O characteristics**

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input low voltage ($V_{DD}$ = 3 V) | $V_{IL}$ | – | – | 0.8 | V |
| Input high voltage ($V_{DD}$ = 3 V) | $V_{IH}$ | 2.4 | – | – | V |
| Input low voltage ($V_{DD}$ = 1.8 V) | $V_{IL}$ | – | – | 0.4 | V |
| Input high voltage ($V_{DD}$ = 1.8 V) | $V_{IH}$ | 1.4 | – | – | V |
| Output low voltage | $V_{OL}$ | – | – | 0.45 | V |
| Output high voltage | $V_{OH}$ | $V_{DDO}$ – 0.45V | – | – | V |
| Input low current | $I_{IL}$ | – | – | 1.0 | µA |
| Input high current | $I_{IH}$ | – | – | 1.0 | µA |
| Output low current ($V_{DD}$ = 3 V, $V_{OL}$ = 0.5 V) | $I_{OL}$ | – | – | 8.0 | mA |
| Output low current ($V_{DD}$ = 1.8 V, $V_{OL}$ = 0.5 V) | $I_{OL}$ | – | – | 4.0 | mA |
| Output high current ($V_{DD}$ = 3 V, $V_{OH}$ = 2.55 V) | $I_{OH}$ | – | – | 8.0 | mA |
| Output high current ($V_{DD}$ = 1.8 V, $V_{OH}$ = 1.35 V) | $I_{OH}$ | – | – | 4.0 | mA |
| Input capacitance | $C_{IN}$ | – | – | 0.4 | pF |

## 14.4 ADC electrical characteristics

**Table 18. Electrical characteristics**

| Parameter | Symbol | Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption | $I_{TOT}$ | – | – | 2 | 3 | mA |
| Power down current | – | At room temperature | – | 1 | – | µA |
| ADC core specification | | | | | | |
| ADC reference voltage | $V_{REF}$ | From BG with ±3% accuracy | – | 0.85 | – | V |
| ADC sampling clock | – | – | – | 12 | – | MHz |
| Absolute error | – | Includes gain error, offset and distortion. Without factory calibration. | – | – | 5 | % |
| | | Includes gain error, offset and distortion. After factory calibration. | – | – | 2 | % |
| ENOB | – | For audio application | 12 | 13 | – | Bit |
| | | For static measurement | 10 | – | – | |

**Table 18. Electrical characteristics** (continued)

| Parameter | Symbol | Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC input full scale | FS | For audio application | – | 1.6 | – | |
| | | For static measurement | 1.8 | – | 3.6 | |
| Conversion rate | – | For audio application | 8 | 16 | – | kHz |
| | | For static measurement | 50 | 100 | – | |
| Signal bandwidth | – | For audio application | 20 | – | 8K | Hz |
| | | For static measurement | – | DC | – | |
| Input impedance | RIN | For audio application | 10 | – | – | KW |
| | | For static measurement | 500 | – | – | |
| Startup time | – | For audio application | – | 10 | – | ms |
| | | For static measurement | – | 20 | – | µs |
| MIC PGA specifications | | | | | | |
| MIC PGA gain range | – | – | 0 | – | 42 | dB |
| MIC PGA gain step | – | – | – | 1 | – | dB |
| MIC PGA gain error | – | Includes part-to-part gain variation | –1 | – | 1 | dB |
| PGA input referred noise | – | At 42 dB PGA gain A-weighted | – | – | 4 | µV |
| Passband gain flatness | – | PGA and ADC, 100 Hz–4 kHz | –0.5 | – | 0.5 | dB |
| MIC bias specifications | | | | | | |
| MIC bias output voltage | – | At 2.5V supply | – | 2.1 | – | V |
| MIC bias loading current | – | – | – | – | 3 | mA |
| MIC bias noise | – | Refers to PGA input 20 Hz to 8 kHz, A-weighted | – | – | 3 | µV |
| MIC bias PSRR | – | at 1 kHz | 40 | – | – | dB |
| ADC SNR | – | A-weighted 0 dB PGA gain | 78 | – | – | dB |
| ADC THD + N | – | –3 dB FS input 0 dB PGA gain | 74 | – | – | dB |
| GPIO input voltage | | Always lower than VDDBAT | – | – | 3.6 | V |
| GPIO source impedance[4] | – | Resistance | – | – | 1 | k– |
| | | Capacitance | – | – | 10 | pF |

**Note**
4. Conditional requirement for the measurement time of 10 ms. Relaxed with longer measurement time for each GPIO input channel.

# 15 Chipset RF specifications

Table 19 and Table 20 apply to single-ended industrial temperatures. Unused inputs are left open.

**Table 19 Chipset receiver RF specifications**

| Parameter | Mode and conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frequency range | – | 2402 | – | 2480 | MHz |
| RX sensitivity[5] | GFSK, 0.1% BER, 1 Mbps | – | –92.0[5] | – | dBm |
| | 7t/4-DQPSK, 0.01% BER, 2 Mbps | – | –94.0[6] | – | dBm |
| | 8-DPSK, 0.01% BER, 3 Mbps | – | –88.0[6] | – | dBm |
| Maximum input | All data rates | – | – | –20 | dBm |
| **GFSK modulation** | | | | | |
| C/I cochannel | GFSK, 0.1% BER[5] | – | – | 11.0 | dB |
| C/I 1 MHz adjacent channel | GFSK, 0.1% BER[6] | – | – | 0 | dB |
| C/I 2 MHz adjacent channel | GFSK, 0.1% BER[7] | – | – | –30.0 | dB |
| C/I ≥ 3 MHz adjacent channel | GFSK, 0.1% BER[5] | – | – | –40.0 | dB |
| C/I image channel | GFSK, 0.1% BER[7] | – | – | –9.0 | dB |
| C/I 1 MHz adjacent to image channel | GFSK, 0.1% BER[7] | – | – | –20.0 | dB |
| **QPSK modulation** | | | | | |
| C/I cochannel | 7t/4-DQPSK, 0.1% BER[7] | – | – | 13.0 | dB |
| C/I 1 MHz adjacent channel | 7t/4-DQPSK, 0.1% BER[8] | – | – | 0 | dB |
| C/I 2 MHz adjacent channel | 7t/4-DQPSK, 0.1% BER[7] | – | – | –30.0 | dB |
| C/I ≥ 3 MHz adjacent channel | 7t/4-DQPSK, 0.1% BER[9] | – | – | –40.0 | dB |
| C/I image channel | 7t/4-DQPSK, 0.1% BER[7] | – | – | –9.0 | dB |
| C/I 1 MHz adjacent to image channel | 7t/4-DQPSK, 0.1% BER[7] | – | – | –20.0 | dB |
| **8PSK modulation** | | | | | |
| C/I cochannel | 8-DPSK, 0.1% BER[7] | – | – | 21.0 | dB |
| C/I 1 MHz adjacent channel | 8-DPSK, 0.1% BER[7] | – | – | 5.0 | dB |
| C/I 2 MHz adjacent channel | 8-DPSK, 0.1% BER[7] | – | – | –25.0 | dB |
| C/I ≥ 3 MHz adjacent channel | 8-DPSK, 0.1% BER[9] | – | – | –33.0 | dB |
| C/I image channel | 8-DPSK, 0.1% BER[7] | – | – | 0 | dB |
| C/I 1 MHz adjacent to image channel | 8-DPSK, 0.1% BER[7] | – | – | 13 | dB |
| Out-of-band blocking performance (CW)[8] | | | | | |
| 30 MHz to 2000 MHz | BDR GFSK 0.1% BER | – | –10.0 | – | dBm |
| 2000 MHz to 2399 MHz | BDR GFSK 0.1% BER | – | –27.0 | – | dBm |
| 2498 MHz to 3000 MHz | BDR GFSK 0.1% BER | – | –27.0 | – | dBm |
| 3000 MHz to 12.75 GHz | BDR GFSK 0.1% BER | – | –10.0 | – | dBm |
| **Inter-modulation performance[5]** | | | | | |
| BT, interferer signal level | BDR GFSK 0.1% BER | – | – | –39.0 | dBm |
| **Spurious emissions** | | | | | |
| 30 MHz to 1 GHz | – | – | – | –57.0 | dBm |
| 1 GHz to 12.75 GHz | – | – | – | –55.0 | dBm |

**Notes**
5. Dirty TX is Off.
6. Up to 1 dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
7. The receiver sensitivity is measured at BER of 0.1% on the device interface.
8. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
9. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).
10. Desired signal is -64 dBm Bluetooth®-modulated signal, interferer 1 is –39 dBm sine wave at frequency f1, interferer 2 is –39 dBm Bluetooth® modulated signal at frequency f2, f0 = 2 * f1 – f2, and |f2 – f1| = n * 1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.

**Table 20 Chipset transmitter RF specifications**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Transmitter section** | | | | |
| Frequency range | 2402 | – | 2480 | MHz |
| Class 2: GFSK TX power | – | 4.0 | – | dBm |
| Class 2: EDR TX Power | – | 0 | – | dBm |
| 20 dB bandwidth | – | 930 | 1000 | kHz |
| Adjacent channel power | | | | |
| \|M – N\| = 2 | – | – | –20 | dBm |
| \|M – N\| ≥ 3 | – | – | –40 | dBm |
| Out-of-band spurious emission | | | | |
| 30 MHz to 1 GHz | – | – | –36.0 | dBm |
| 1 GHz to 12.75 GHz | – | – | –30.0 | dBm |
| 1.8 GHz to 1.9 GHz | – | – | –47.0 | dBm |
| 5.15 GHz to 5.3 GHz | – | – | –47.0 | dBm |
| **LO performance** | | | | |
| Initial carrier frequency tolerance | –75 | – | +75 | kHz |
| Frequency drift | | | | |
| DH1 packet | –25 | – | +25 | kHz |
| DH3 packet | –40 | – | +40 | kHz |
| DH5 packet | –40 | – | +40 | kHz |
| Drift rate | –20 | | 20 | kHz/50 µs |
| **Frequency deviation** | | | | |
| Average deviation in payload (sequence used is 00001111) | 140 | – | 175 | kHz |
| Maximum deviation in payload (sequence used is 10101010) | 115 | – | – | kHz |
| Channel spacing | – | 1 | – | MHz |
| **Modulation accuracy** | | | | |
| /4-DQPSK frequency stability | –10 | – | 10 | kHz |
| /4-DQPSK RMS DEVM | – | – | 20 | % |
| /4-QPSK Peak DEVM | – | – | 35 | % |
| /4-DQPSK 99% DEVM | – | – | 30 | % |
| 8-DPSK frequency stability | –10 | – | 10 | kHz |
| 8-DPSK RMS DEVM | – | – | 13 | % |
| 8-DPSK Peak DEVM | – | – | 25 | % |
| 8-DPSK 99% DEVM | – | – | 20 | % |
| **In-band spurious emissions** | | | | |
| 1.0 MHz < \|M – N\| < 1.5 MHz | – | – | –26 | dBm |
| 1.5 MHz < \|M – N\| < 2.5 MHz | – | – | –20 | dBm |
| \|M – N\| > 2.5 MHz | – | – | –40 | dBm |

**Table 21 Bluetooth® LE RF specifications**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frequency range | N/A | 2402 | – | 2480 | MHz |
| RX sensitivity (QFN)[11] | LE GFSK, 0.1% BER, 1 Mbps | – | –95.0[12] | – | dBm |
| TX power | Bluetooth® LE silicon device CYW30739 Only | – | 4.0 | – | dBm |
| Mod Char: Delta F1 average | N/A | 225 | 255 | 275 | kHz |
| Mod Char: Delta F2 max[13] | N/A | 99.9 | – | – | % |
| Mod Char: Ratio | N/A | 0.8 | 0.95 | – | % |

**Table 22 CYW30739B2-P5TAI051 GPS and GLONASS band spurious emission**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1570-1580 MHz | GPS | – | –160 | – | dBm/Hz |
| 1592-1610 MHz | GLONASS | – | –159 | – | dBm/Hz |

**Notes**
11.Dirty TX is Off.
12.Up to 1 dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
13.At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz

# 16 Timing and AC characteristics

In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

## 16.1 UART timing

**Table 23 UART timing specifications**

| Reference | Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1 | Delay time, UART_CTS_N low to UART_TXD valid. | – | – | 1.50 | Bit periods |
| 2 | Setup time, UART_CTS_N high before midpoint of stop bit. | – | – | 0.67 | Bit periods |
| 3 | Delay time, midpoint of stop bit to UART_RTS_N high. | – | – | 1.33 | Bit periods |

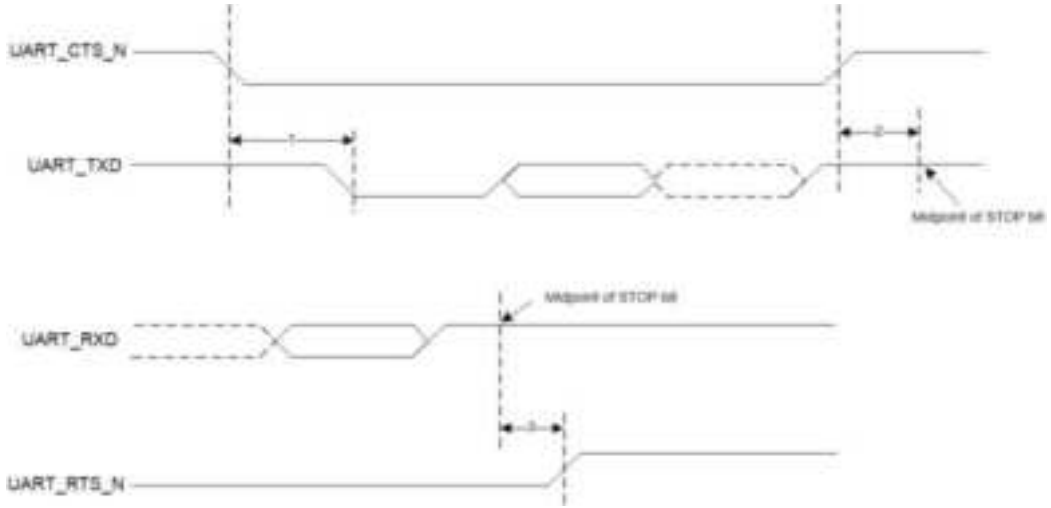



**Figure 13 UART timing**

## 16.2 SPI timing

The SPI interface can be clocked up to 24 MHz.

**Table 24** and **Figure 14** show the timing requirements when operating in SPI mode 0 and 2.

**Table 24 SPI mode 0 and 2**

| Reference | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 1 | Time from master assert SPI_CSN to first clock edge | 45 | – | ns |
| 2 | Hold time for MOSI data lines | 12 | ½SCK | ns |
| 3 | Time from last sample on MOSI/MISO to slave deassert SPI_INT | 0 | 100 | ns |
| 4 | Time from slave deassert SPI_INT to master deassert SPI_CSN | 0 | – | ns |
| 5 | Idle time between subsequent SPI transactions | 1 SCK | – | ns |

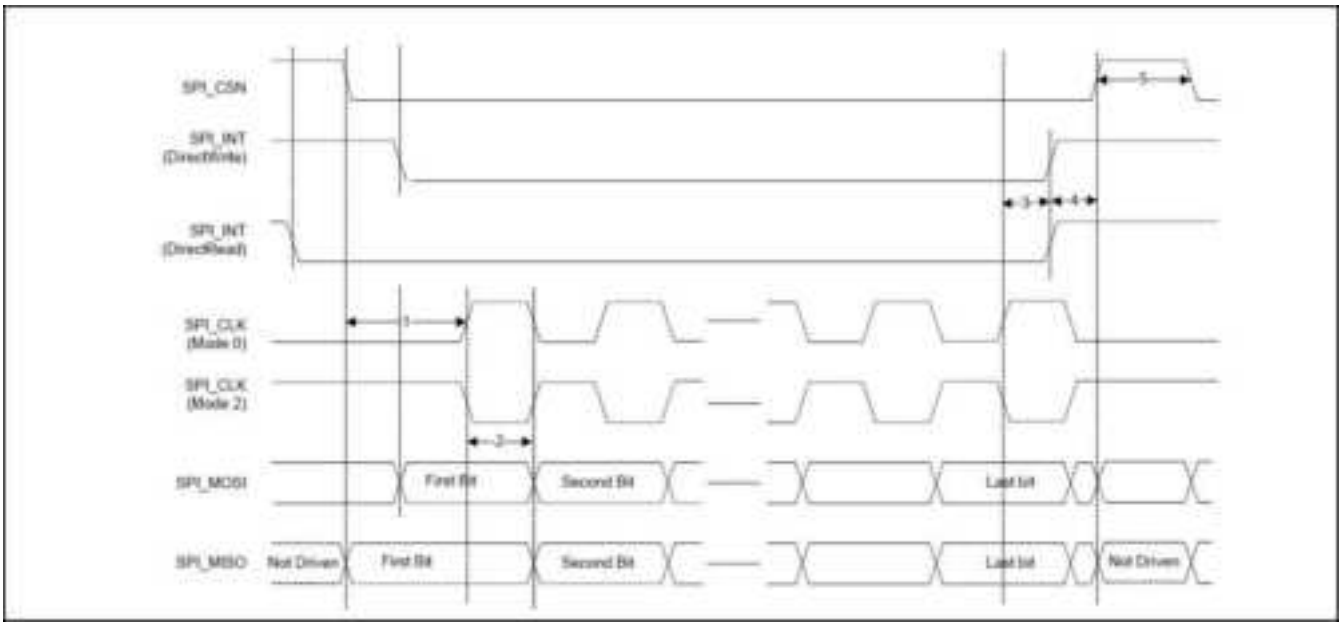



**Figure 14 SPI timing, Mode 0 and 2**

**Table 25** and **Figure 15** show the timing requirements when operating in SPI mode 1 and 3.

**Table 25 SPI mode 1 and 3**

| Reference | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 1 | Time from master assert SPI_CSN to first clock edge | 45 | – | ns |
| 2 | Hold time for MOSI data lines | 12 | 1/2 SCK | ns |
| 3 | Time from last sample on MOSI/MISO to slave deassert SPI_INT | 0 | 100 | ns |
| 4 | Time from slave deassert SPI_INT to master deassert SPI_CSN | 0 | – | ns |
| 5 | Idle time between subsequent SPI transactions | 1 SCK | – | ns |

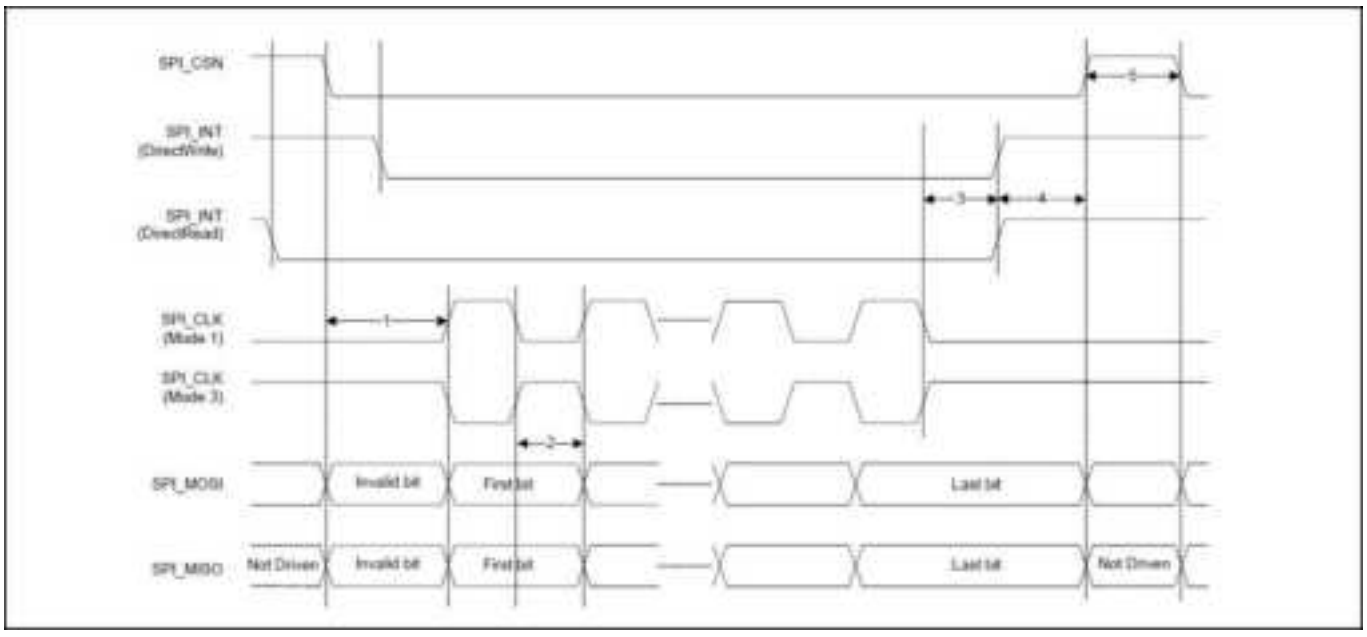



**Figure 15 SPI timing, Mode 1 and 3**

## 16.3 I²C compatible interface timing

The specifications in **Table 26** references **Figure 16**.

**Table 26 I²C compatible interface timing specifications (up to 1 MHz)**

| Reference | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 1 | Clock frequency | – | 100 | kHz |
| | | | 400 | |
| | | | 800 | |
| | | | 1000 | |
| 2 | START condition setup time | 650 | – | ns |
| 3 | START condition hold time | 280 | – | ns |
| 4 | Clock low time | 650 | – | ns |
| 5 | Clock high time | 280 | – | ns |
| 6 | Data input hold time[14] | 0 | – | ns |
| 7 | Data input setup time | 100 | – | ns |
| 8 | STOP condition setup time | 280 | – | ns |
| 9 | Output valid from clock | – | 400 | ns |
| 10 | Bus free time[15] | 650 | – | ns |

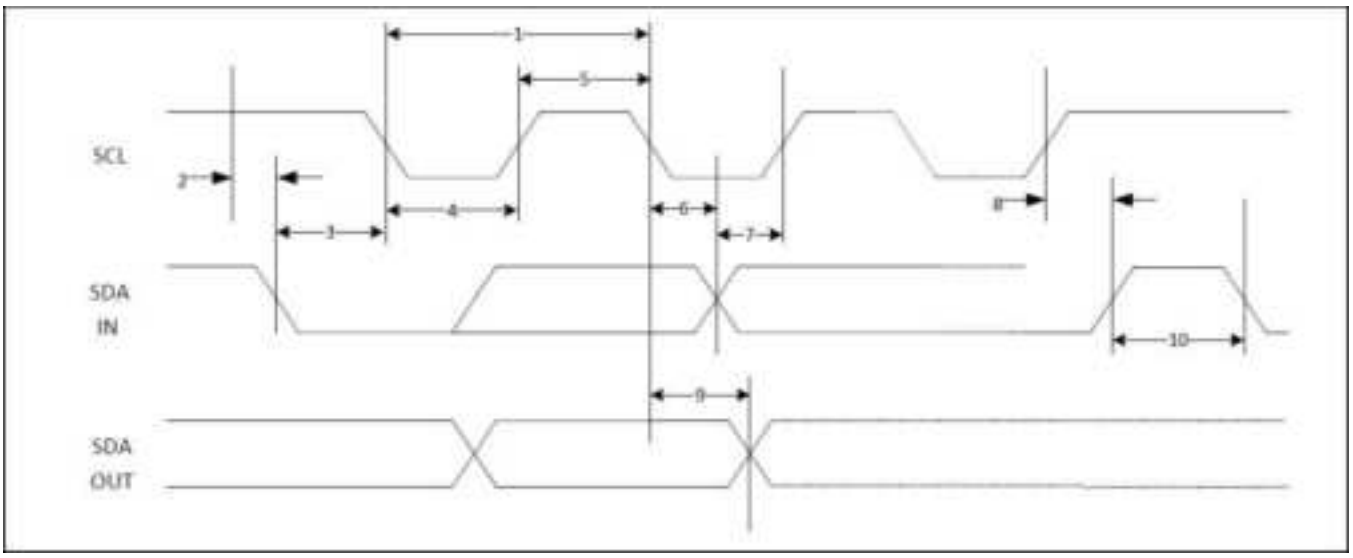



**Figure 16 I²C interface timing diagram**

**Notes**
14. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
15. Time that the CBUS must be free before a new transaction can start.

## 16.4 I²S interface timing

I²S timing is shown below in **Table 27**, **Figure 17**, and **Figure 18**.

**Table 27 Timing for I²S transmitters and receivers**

| Parameter | Transmitter | | | | Receiver | | | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | Lower limit | | Upper limit | | Lower limit | | Upper limit | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Clock period T | $T_{tr}$ | – | – | – | $T_r$ | – | – | – | Note 16 |
| **Master mode: Clock generated by transmitter or receiver** | | | | | | | | | |
| HIGH $t_{HC}$ | $0.35T_{tr}$ | – | – | – | $0.35T_{tr}$ | – | – | – | Note 17 |
| LOW $t_{LC}$ | $0.35T_{tr}$ | – | – | – | $0.35T_{tr}$ | – | – | – | Note 17 |
| **Slave mode: Clock accepted by transmitter or receiver** | | | | | | | | | |
| HIGH $t_{HC}$ | – | $0.35T_{tr}$ | – | – | – | $0.35T_{tr}$ | – | – | Note 18 |
| LOW $t_{LC}$ | – | $0.35T_{tr}$ | – | – | – | $0.35T_{tr}$ | – | – | Note 18 |
| Rise time $t_{RC}$ | – | – | $0.15T_{tr}$ | – | – | – | | – | Note 19 |
| Transmitter | | | | | | | | | |
| Delay $t_{dtr}$ | – | – | – | 0.8T | – | – | – | – | Note 20 |
| Hold time $t_{htr}$ | 0 | – | – | – | – | – | – | – | Note 19 |
| **Receiver** | | | | | | | | | |
| Setup time $t_{sr}$ | – | – | – | – | $0.2T_{tr}$ | – | – | – | Note 21 |
| Hold time $t_{hr}$ | – | – | – | – | $0.2T_{tr}$ | – | – | – | Note 21 |

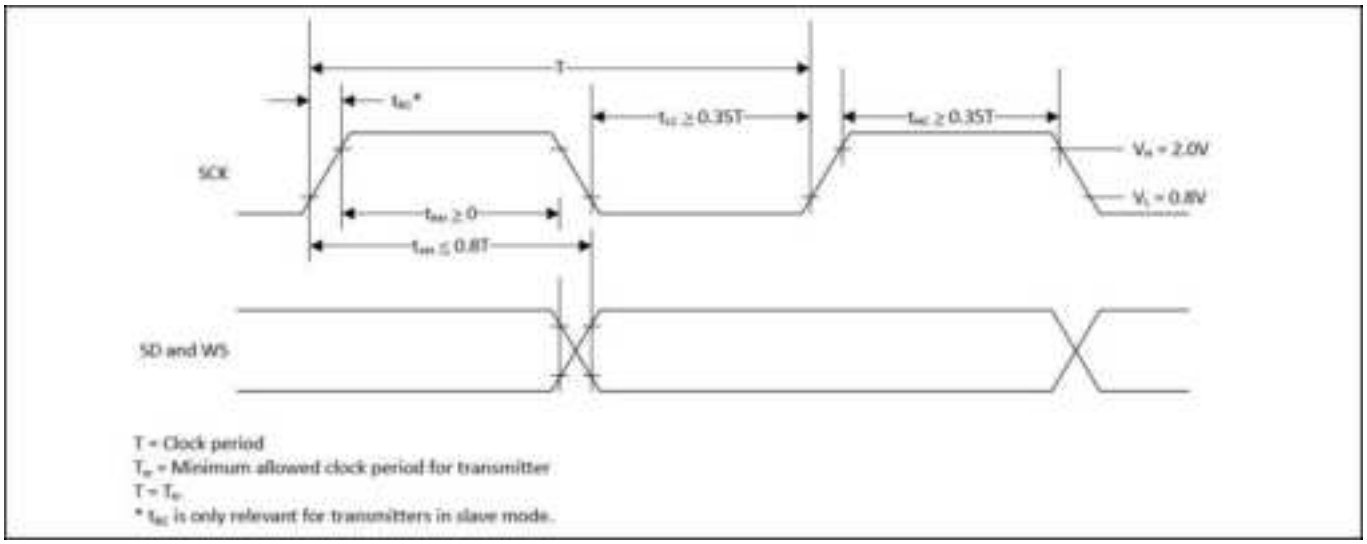
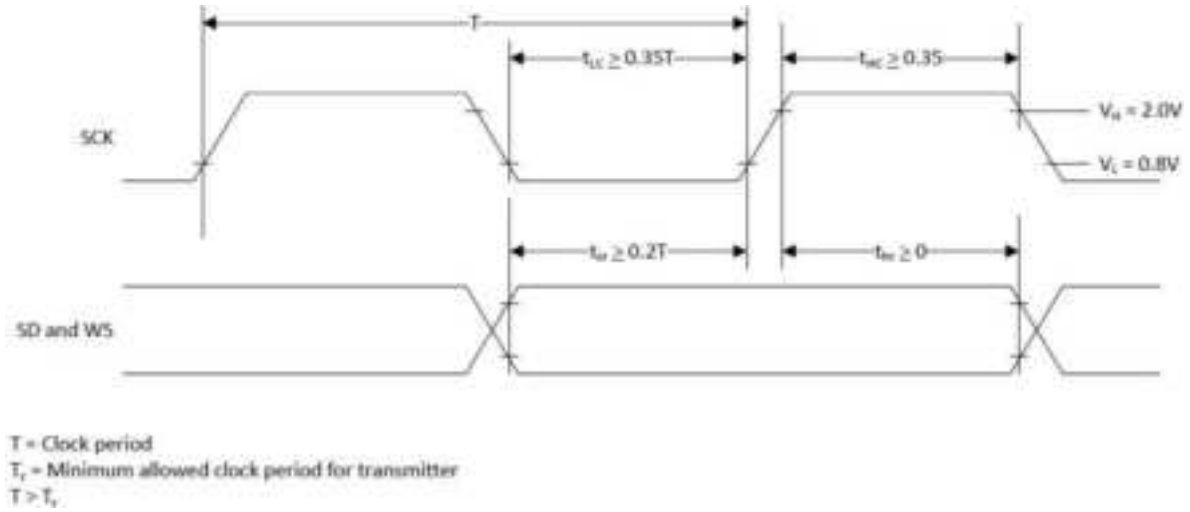



**Figure 17 I²S transmitter timing**

**Notes**

16. The system clock period T must be greater than $T_{tr}$ and $T_r$ because both the transmitter and receiver have to be able to handle the data transfer rate.
17. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, $t_{HC}$ and $t_{LC}$ are specified with respect to T.
18. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
19. Because the delay $(t_{dtr})$ and the maximum transmitter speed (defined by $T_{tr}$) are related, a fast transmitter driven by a slow clock edge can result in $t_{dtr}$ not exceeding $t_{RC}$ which means $t_{htr}$ becomes zero or negative. Therefore, the transmitter has to guarantee that $t_{htr}$ is greater than or equal to zero, so long as the clock rise-time $t_{RC}$ is not more than $t_{RCmax}$, where $t_{RCmax}$ is not less than $0.15T_{tr}$.
20. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
21. The data setup and hold time must not be less than the specified receiver setup and hold time.

Timing and AC characteristics




T = Clock period
$T_x$ = Minimum allowed clock period for transmitter
$T > T_x$

**Figure 18 I²S receiver timing**

# 17 Environmental specifications

## 17.1 Environmental compliance

This Bluetooth® LE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The module and components used to produce this module are RoHS and HF compliant.

## 17.2 RF certification

The CYW30739B2-P5TAI051 module is certified under the following RF certification standards:

- FCC: WAP739I05
- IC: 7922A-739I05
- MIC:
- CE

## 17.3 Safety certification

The CYW30739B2-P5TAI051 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

## 17.4 Environmental conditions

Table 28 describes the operating and storage conditions for the Bluetooth® LE module.

**Table 28. Environmental conditions for CYW30739B2-P5TAI051**

| Description | Minimum specification | Maximum specification |
|---|---|---|
| Operating temperature | -30 °C | 85 °C |
| Operating humidity (relative, non-condensation) | 5% | 85% |
| Thermal ramp rate | – | 10 °C/minute |
| Storage temperature | –40 °C | 85 °C |
| Storage temperature and humidity | – | 85 °C at 85% |
| ESD: Module integrated into system components[22] | – | 15 kV air<br>2.0 kV contact |

## 17.5 ESD and EMI protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device Handling**: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

**Note**
22.This does not apply to the RF pins (ANT).

# 18 Regulatory information

## 18.1 FCC

FCC notice:

The device CYW30739B2-P5TAI051 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

Caution:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Infineon may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

Labeling requirements:

The original equipment manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon FCC identifier for this product as well as the FCC notice above. The FCC identifier is FCC ID: WAP739I05.

In any case the end product must be labeled exterior with “Contains FCC ID: WAP739I05”.

Antenna warning:

This device is tested with a standard SMA connector and with the antenna listed in **Table 6**. When integrated in the OEMs product, this fixed antenna requires installation preventing end-users from replacing them with non-approved antennas. Any antenna not in **Table 6** must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF exposure:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in **Table 6**, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYW30739B2-P5TAI051 with the integrated trace antenna (FCC ID: WAP739I05) is far below the FCC radio frequency exposure limits. Nevertheless, use CYW30739B2-P5TAI051 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 8 mm between the radiator and your body.

## 18.2 ISED

**Innovation, Science and Economic Development (ISED) Canada Certification**

CYW30739B2-P5TAI051 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada.

License: IC: 7922A-739I05

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from **www.ic.gc.ca**.

This device has been designed to operate with the antennas listed in **Table 6**, having a maximum gain of -0.5 dBi. Antennas not included in **Table 6** or having a gain greater than -0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 Ω. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED notice:

The device CYW30739B2-P5TAI051 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYW30739B2-P5TAI051, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

ISED interference statement for Canada

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

ISED radiation exposure statement for Canada

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé.

Labeling requirements:

The original equipment manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-739I05. In any case, the end product must be labeled in its exterior with “Contains IC: 7922A-739I05”.

Le fabricant d'équipement d'origine (OEM) doit s'assurer que les exigences d'étiquetage ISED sont respectées. Cela comprend une étiquette clairement visible à l'extérieur de l'enceinte OEM spécifiant l'identifiant Infineon IC approprié pour ce produit ainsi que l'avis ISED ci-dessus. L'identificateur IC est 7922A-739I05. En tout cas, le produit final doit être étiqueté dans son extérieur avec “Contient IC: 7922A-739I05”.

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 10 mm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé. Cet équipement doit être installé et utilisé avec un minimum de 10 mm de distance entre la source de rayonnement et votre corps.

## 18.3 European Declaration of Conformity

Hereby, Infineon declares that the Bluetooth® module CYW30739B2-P5TAI051 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

All versions of the CYW30739B2-P5TAI051 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

# 19 Packaging

**Table 29 Solder reflow peak temperature**

| Module part number | Package | Maximum peak temperature | Maximum time at peak temperature | No. of cycles |
|---|---|---|---|---|
| CYW30739B2-P5TAI051 | 31-pad SMT | 260 °C | 30 seconds | 2 |

**Table 30 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

| Module part number | Package | MSL |
|---|---|---|
| CYW30739B2-P5TAI051 | 34-pad SMT | MSL 3 |

The CYW30739B2-P5TAI051 is offered in tape and reel packaging. **Figure 19** details the tape dimensions used for the CYW30739B2-P5TAI051.

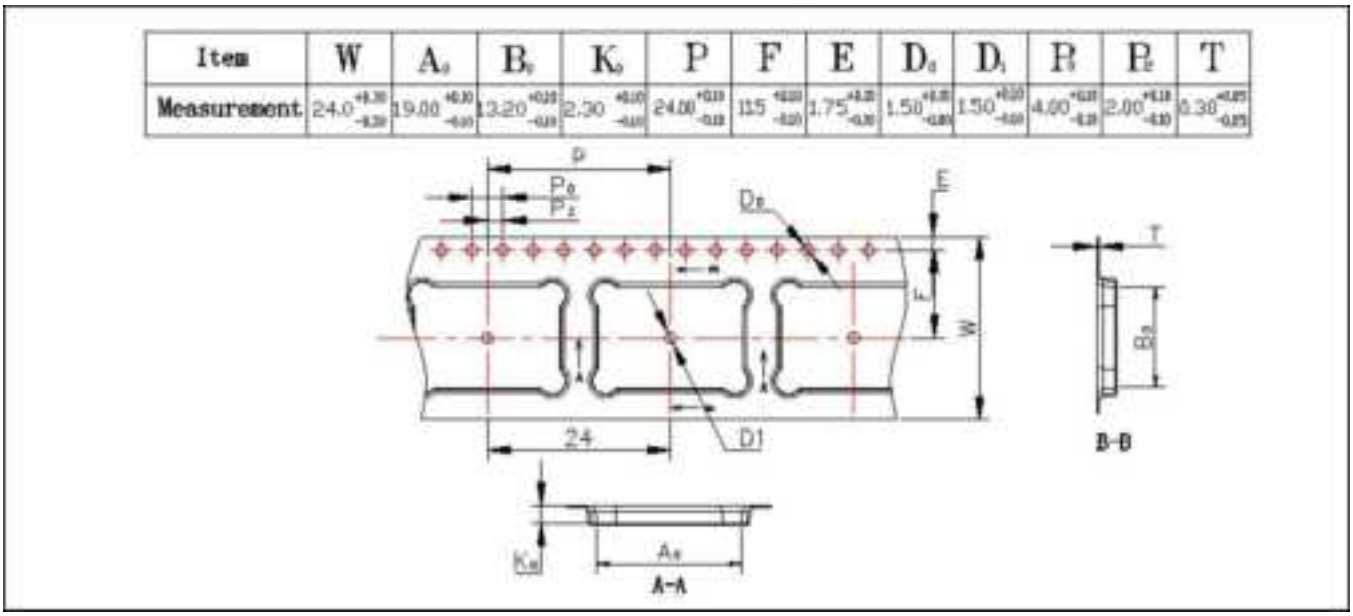



**Figure 19 CYW30739B2-P5TAI051 tape dimensions**

**Figure 20** details the orientation of the CYW30739B2-P5TAI051 in the tape as well as the direction for unreeling.

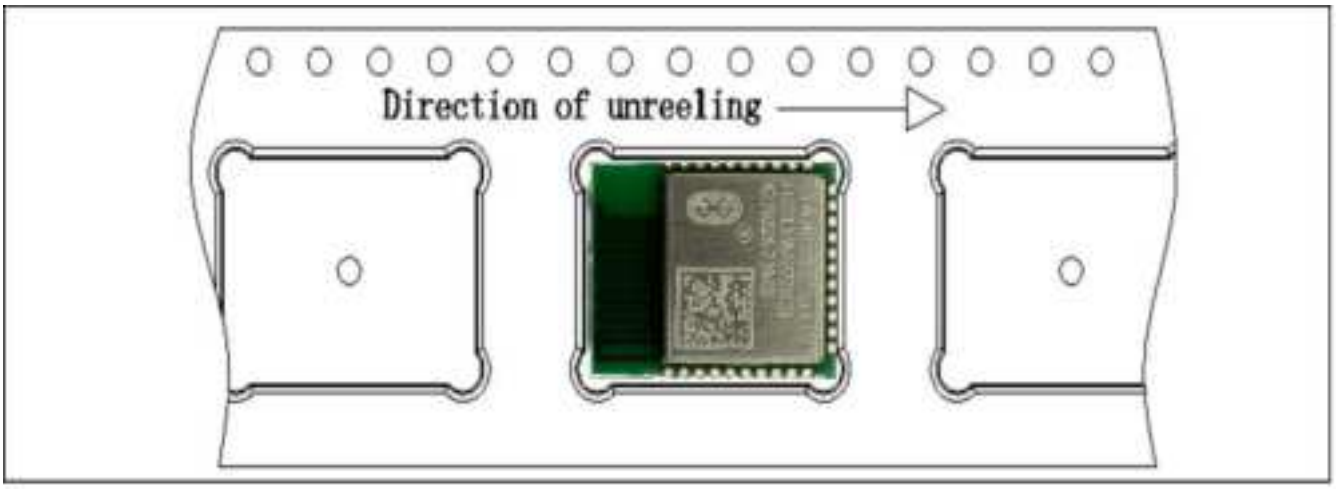
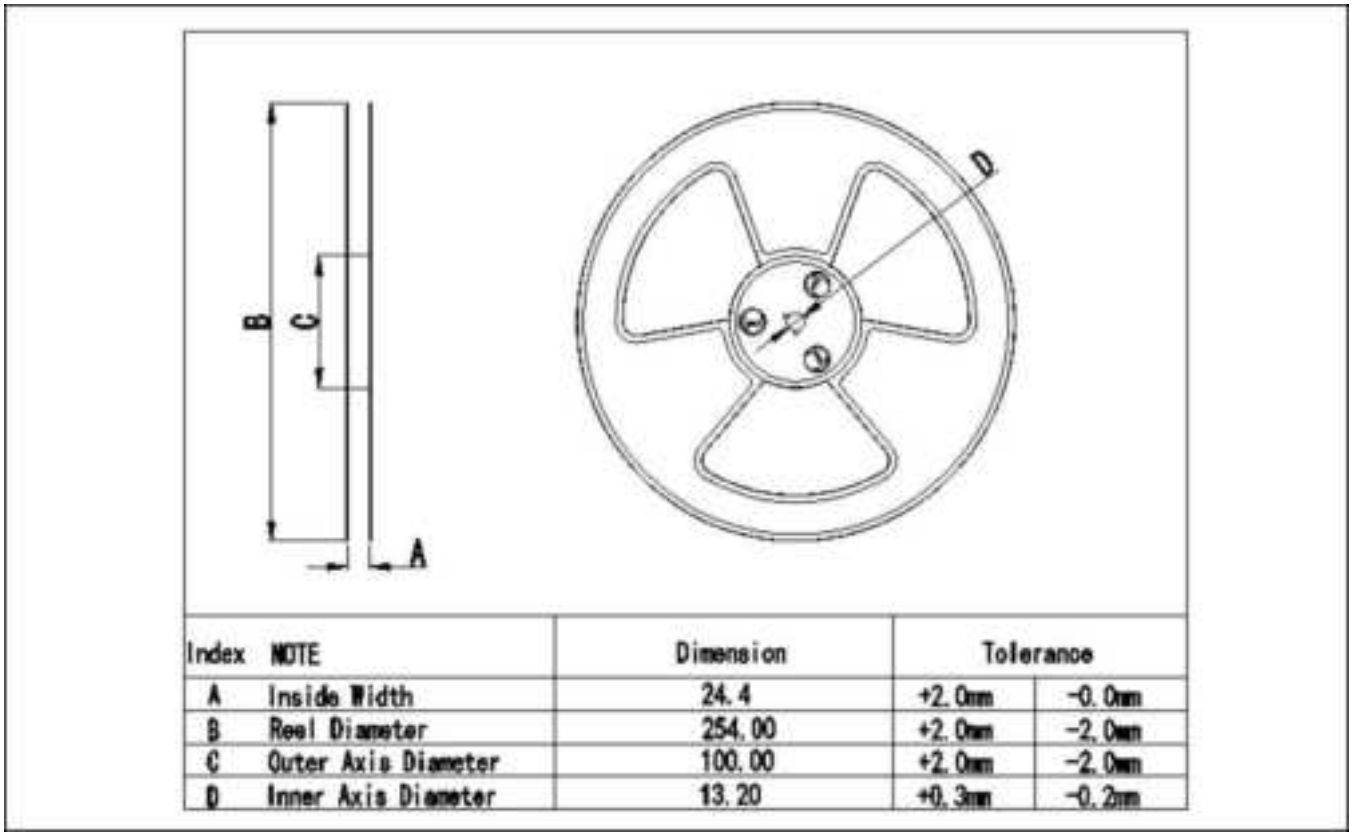



**Figure 20 Component orientation in tape and unreeling direction**

**Figure 21** details reel dimensions used for the CYW30739B2-P5TAI051.




| Index | NOTE | Dimension | Tolerance | |
|---|---|---|---|---|
| A | Inside Width | 24.4 | +2.0mm | -0.0mm |
| B | Reel Diameter | 254.00 | +2.0mm | -2.0mm |
| C | Outer Axis Diameter | 100.00 | +2.0mm | -2.0mm |
| D | Inner Axis Diameter | 13.20 | +0.3mm | -0.2mm |

**Figure 21 Reel dimensions**

# 20 Ordering information

**Table 31** lists the CYW30739B2-P5TAI051 part number and features. **Table 31** also lists the target program for the respective module ordering codes. **Table 32** lists the reel shipment quantities for the CYW30739B2-P5TAI051.

**Table 31** **Ordering information**

| Ordering part number | Max CPU speed (MHz) | Flash size (KB) | RAM size (KB) | UART | I²C | SPI | I²S | PCM | PWM | ADC inputs | GPIOs | Package | Packaging |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CYW30739B2-P5TAI051 | 96 | 1024 | 512 | Yes | Yes | Yes | Yes | Yes | 6 | 7 | 13 | 31-SMT | Tape and reel |

**Table 32** **Tape and reel package quantity and minimum order amount**

| Description | Minimum reel quantity | Maximum reel quantity | Comments |
|---|---|---|---|
| Reel quantity | 500 | 500 | Ships in 500 unit reel quantities. |
| Minimum order quantity (MOQ) | 500 | – | – |
| Order increment (OI) | 500 | – | – |

The CYW30739B2-P5TAI051 is offered in tape and reel packaging. The CYW30739B2-P5TAI051 ships in a reel size of 500 units.

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# 21 Acronyms

**Table 33 Acronyms used in this document**

| Acronym | Description |
|---|---|
| Bluetooth® LE | Bluetooth® Low Energy |
| Bluetooth® SIG | Bluetooth® Special Interest Group |
| CE | European Conformity |
| CSA | Canadian Standards Association |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FCC | Federal Communications Commission |
| GPIO | general-purpose input/output |
| ISED | Innovation, Science and Economic Development (Canada) |
| IDE | integrated design environment |
| KC | Korea Certification |
| MIC | Ministry of Internal Affairs and Communications (Japan) |
| OTA | Over-the-Air |
| PCB | printed circuit board |
| RX | receive |
| QDID | qualification design ID |
| SMT | surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs |
| TCPWM | timer, counter, pulse width modulator (PWM) |
| TUV | Germany: Technischer Überwachungs-Verein (Technical Inspection Association) |
| TX | transmit |

# 22 Document conventions

## 22.1 Units of measure

**Table 34 Units of measure**

| Symbol | Unit of measure |
|---|---|
| °C | degree Celsius |
| kV | kilovolt |
| mA | milliamperes |
| mm | millimeters |
| mV | millivolt |
| µA | microamperes |
| µm | micrometers |
| MHz | megahertz |
| GHz | gigahertz |
| V | volt |

Document conventions

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| ** | 2024-06-21 | Initial release |

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