7. THEORY OF OPERATION

Circuit Compositions and Operation Theory

The basic explanation for the circuit composition the two board controlling the analog circuit parts and the digital circuit parts for the other control.

Receiver

Transmission parts is composed in the double conversion system, which has the 1st IF Frequency of 21.7 MHz and 2nd IF Frequency of 450 kHz. With the sawfilter which has an excellent band characteristic and skite characteristic, the 2 pole MCF used in the 1st IF, and the sensitivity repression are reduced for the more stable reception.

RF Frontend

The signal received by the antenna will be transmitted to the band pass filter through the antenna switching circuit consisted of L26, L28, CT15, CT16 and CT18. The front RF amplifier transistor QR1 consists of the sawfilter and input/output band pass filter.
Sawfilter has the bandwidth of approximately 4 MHz, primarily diminishes the other signal rather then the 1st IF image and other signal within the reception band and amplifies only the necessary signal within the RF.

1st Mixer

The receiver signal which has been amplified in the RF fronted is provided to the base of the 1st mixer QR2. The 1st L/O signal provide from the VCO is supplied to the emitter of Q202 and converted to the 1st IF 21.7 MHz.

1st IF Filter and 1st IF Amplifier

The signal covered by QR2 to 21.7 MHz, the 1st frequency, change its impedance through CR13, LR5 and then is infused to the fundamental MCF which has the center frequency of 21.7 MHz and the width of +/-3.75 kHz.
Here, the signal reduces the image and other unwanted signal for the 2nd IF, and changes its impedance again through the RR14 and CR15. Then the signal is infused to the QR3, the 1st IF amplifier. The signal infused to the QR3 is amplified approximately by 20 dB in other to acquire the required reception sensitivity, and infused to the IC2 which functions as the 2nd mixer, the 2nd IF amplifier, and the FM detector.

2nd Mixer, and IF, FM Detector (IC2)

The receiver IF signal of 21.7 MHz, which has been infused to IC2 is mixed with the 2nd L/O signal of 21,250MHz, and converted to 450 kHz, the 2nd IF frequency. The receiver signal converted to the 2nd IF frequency passed through the CF2, the ceramic filter of 450 kHz again. After the limiting inside the IC2 and the FM demodulating by the quadrature detector inside the IC2, the signal offers the output through the 9th pin of IC2.
The squelch circuit is composed to detect the noised from the received signal demodulate in the 9th pin of the IC2. For this purpose, the noise filter is using the OP amplifier inside the IC2.

De-Emphasis and 300 Hz HPF (IC8)

The audio signal which has been FM demodulate in the IC2 is supplies to the IC8E which function as the De-emphasis and 300 Hz HPF.
Since the IC8D has the 300 Hz HPF with the 1st characteristics and the De-emphasis characteristic with the corner frequency of approximately 200 Hz, and IC8A, the IC8B, and the IC8C has the 300 Hz HPF with the 6th characteristics, they function as a normal De-emphasis and also reduce the signal such as CTCSS to unwanted noised from the speaker.
Audio Power Amplifier (IC3)
The received audio signal which has been adjusted to the appropriate volume in the VR101 are supplied to the 2nd pin of the IC3 amplified approximately by 20 dB. Then, it turns up the speaker with the maximum output of 0.3 Watts.
The 7th pin of the IC3 is the audio mute terminal. If a voltage supply to the 6th pin of the IC3 is supplied to this terminal, the IC3 stops functioning as the audio power amplifier regardless of the signal supplied to the 2nd pin of the IC3, and there is no sound emitter from the speaker.

Transmitter

The transmission parts of the 21-1822 is designed to amplify the RF signal oscillated and modulated by the synthesizer to approximately 500 mW by the power transistor of QT3.

Pre-emphasis and 300 Hz HPF. Limiter (IC9C, 9D)

The voice signal input from the microphone is pre-emphasized at the IC9D, and at the same time, the components below 300 Hz are reduce to minimize the influence to the CTCSS tone.
The signal which comes out of the IC9D is limited to a certain amplitude at the IC9C for the voice signal not to exceed the allowable band width assigned for transmission.

3 kHz LPF (IC9B, IC9A)

After passing the IC7 limiter, the signal is combined with the CTCSS tone at the digitalcircuits, passes the RV101, and is supplied to the 3 kHz LPF has the 4th characteristics and adjusts the assigned frequency band width not to exceed the allowable range.

TX Power (QT2)

The transmitted signal of approximately 7 mW, combined at the driver TR is supplied to the base of the QT2 amplifier, the transmitted signal amplified to 0.47 W here passes the TX LPF of the 2nd characteristic of the L24 and the L25, and RX/TX switching takes place by the DT1. After this, the signal is provided to the antenna the TX LPF of the 1st characteristics, consisted of the L26.

CPU and MEMORY

Most of the control functions of the 21-1822 are controlled by the IC10 CPU.
The IC10 CPU has the internal ROM in the capacity of 8 K byte, and the program for the operation of the IC10.
When the power of turned on, the IC10 reads the data necessity for the operation from the IC6 EEPROM, and decide the operation channel, frequency, etc.
If the user alters any parameter of the radio, the IC10 updates the altered parameter to the IC6.

Frequency Synthesizer

Voltage Control Oscillator (VCO)

The VCO of oscillates 462.5625 MHz to 467.7125 MHz under the transmission condition and 440.8625 MHz to 446.0125 Mhz under the reception condition. The VCO consists of the clip oscillator of the Q32, and contains the oscillator frequency of approximately 21.7 MHz during the transmission/reception conversion. That is since the VCO should oscillate relatively low frequency during reception compared t transmission, the D202 is directly biased by the Q31.

Therefore as a result, the C205 is added in parallel to the resonance circuit of the VCO to oscillate a low frequency. During transmission, a relatively high frequency should be oscillate compared to reception. Therefore, the D202 is adversely biased by the QR2, and as a result, the C205 which is added unparallel to the circuit of the VCO is removed to oscillate the desired transmission frequency.

The VCO is controlled by controlled by the IC4 PLL IC in order to oscillate the accurate frequency. The VCO is controlled by the IC4 PLL IC in order to oscillate accurate frequency. The output frequency of the VCO is supplied to the IC4 PLL IC immediately. At the IC2, TCXO(21.250 MHz) by the TCXO-1 is compared to the output frequency of the VCO.

The VCO is controlled the loop filter consisted of the RL21, RL22, and the CL21, CL22, C203 in order to oscillate the stable frequency wanted for the radio.

The VCO controlled voltage which ahs passed the loop filter is supplies to the D201 varactor diode, and the VCO an oscillate the PLL programmed frequency by the capacity variation in the D201. In addition, the L203 on the VCO circuit function as frequency for the VCO to be properly controlled by the IC4 PLL IC.

RX/TX Buffer Amplifier (Q33, QL1)

The RF signal oscillate at the VCO is provide to the QR2 RX 1st mixer through the QL1 during the reception, and is provide to the QT1 power driver amplifier through the QT2 during the transmission.

PLL Frequency Synthesizer (IC4)

The PLL synthesizer of the signal loop PLL circuit with the reference of 6.25 kHz. The IC4 PLL IC includes all the function such as the reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider.

At the reference oscillator, the 21.250 MHz TCXO of the TCXO-1 is connected to the pin 2,3 of the IC4 to oscillate the frequency of 21.250 MHz. The TCXO (21.250 MHz) is the temperature compensation circuit to maintain the frequency withen the allowable error range even under a low temperature of -30℃.

The phase detector send out the output power to the loop filter through 10 pin of the IC4. IF the oscillation frequency of the VCO is low compared to the referenced frequency, the phase detector sends out the output power in positive pulse. If the oscillation frequency of the VCO is high, phase detector send out can maintain the frequency set.

The programmable dicoder divider maintains the desired frequency with control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below:

N = VCO oscillation frequency / reference frequency

If the desired frequency is 462.5625 MHz

N = 462.5625 MHz / 0.00625 MHz = 74010

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