Fibocom
PERFECT WIRELESS EXPERIENCE

# L716-LA

# Hardware Guide

V1.5

## Contact Information

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## Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

# Contents



# Applicable Models

| No. | Applicable Model | Description |
| --- | --- | --- |
| 1 | L716-LA | CAT4, 128Mb FLASH, 256Mb DDR, LA band, MAIN+DIV ANT, 2/3/4G, Standard model |

# Change History

| | |
|---|---|
| V1.5 (2023-8-1) | Add module type and update template |
| V1.4 (2023-4-11) | Add module type and IO reset value |
| V1.3 (2022-9-26) | Add module type and USB description |
| V1.2 (2022-7-21) | Add module type and modify WAKEUP_IN default voltage state |
| V1.1 (2022-5-19) | Add module type and power consumption |
| V1.0 (2022-3-15) | Initial version |

# 1 Foreword

## 1.1 Declaration

This document defines in detail the hardware interfaces of the module. By reading this document, you can quickly understand the interface specification, electrical characteristics, mechanical size and other special requirements of the module. Combined with the reference documents provided by Fibocom, customers can quickly design and debug the wireless part of the circuit.

## 1.2 Reference standard

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0：Mobile Station（MS）conformance specification; Part 1：Conformance specification
- 3GPP TS 34.121-1 V10.8.0：User Equipment （UE）conformance specification; Radio transmission and reception（FDD）;Part 1：Conformance specification
- 3GPP TS 36.521-1 V15.0.0：User Equipment （UE） conformance specification; Radio transmission and reception; Part 1：Conformance testing
- 3GPP TS 36.124V10.3.0：Electro Magnetic Compatibility（EMC）requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0：USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0：Specification of the Subscriber Identity Module -Mobile Equipment （SIM-ME） interface
- 3GPP TS 31.102 V10.11.0：Characteristics of the Universal Subscriber Identity Module （USIM） application
- 3GPP TS 31.11 V10.16.0：Universal Subscriber Identity Module（USIM）Application Toolkit （USAT）
- 3GPP TS 27.007 V10.0.8：AT command set for User Equipment（UE）

- 3GPPTS27.005 V10.0.1：Use of Data Terminal Equipment -Data Circuit terminating Equipment （DTE - DCE）interface for Short Message Service（SMS）and Cell Broadcast Service （CBS）
- Universal Serial Bus Specification 2.0

# 2 Product Overview

## 2.1 Product Introduction

The L716-LA series product support LTE/WCDMA/GSM network systems. It is a highly integrated wireless communication module and can be widely used in security monitoring, power, industrial routing, CPE and MIFI scenarios.

The product RF band provides the following characteristics.

Table 1. RF band

| Type | ANT NO | Mode | RF Band |
|---|---|---|---|
| L716-LA | MAIN+DIV ANT | GSM | GSM850/900/1800/1900 |
| | | WCDMA | B1/2/3/4/5/8 |
| | | LTE-FDD | B1/2/3/4/5/7/8/28/66 |
| | | LTE-TDD | B38/40 |

## 2.2 Product Characteristics

The product hardware provides the following characteristics.

Table 2. Baseband characteristics

| Category | Description |
|---|---|
| Power supply | DC voltage: 3.3～4.4V，typical: 3.8V |
| Processor | ARM CORTEX-A53 |
| Operating system | Linux/Android/Windows |
| Network protocol | Support IPV4/IPV6 |
| SMS | Available |

| | |
|---|---|
| Storage space | The platform built-in 256 Mb or 512 Mb DDR, external 128Mb NOR or 1Gb NAND FLASH |
| Functional interface | USB x 1: Compliant with USB 2.0 specification (slave only), Used for AT command communication, software debugging and firmware upgrade<br>I2C x 1: Support standard mode 100KHz、fast mode 400KHz 和 high speed mode 3.4MHz, pull up inside<br>SPI x 1: Provides two working modes of Master and Slave<br>ADC x 2: Support 9-bit ADC interfaces, voltage range is from 0V to 5V<br>UART x 2: Main UART: Used for AT command communication and data transmission. Baud rates reach up to 921600bps, 115200bps by default. Support RTS and CTS hardware flow control<br>Debug UART: Used for log output 115200bps baud rate<br>RMII x 1<br>SDIO x 2: SD1 support only 2.8V SD card, SD0 support SD 3.0 protocol<br>SIM x 1: supports 1.8V and 3V SIM cards<br>PCM x 1: Used for audio function with external codec |
| Antenna interface | Main antenna x 1<br>Diversity antenna x 1 |
| LTE mode | Uplink: QPSK/16QAM/Downlink: QPSK/16QAM/64QAM |
| | LTE FDD: 150Mbps DL/50Mbps UL (Cat 4) |
| | LTE TDD: 130Mbps DL/30.5Mbps UL (Cat 4) |
| WCDMA mode | Uplink: BPSK/Downlink: QPSK |
| | HSDPA+: 21Mbps DL (Cat 14)/HSUPA: 5.76Mbps UL (Cat 6) |
| GSM mode | GSM&GPRS: GMSK, EDGE: 8-PSK |
| | GPRS: 85.6kbps DL/85.6kbps UL (multi-slot class 12) |
| | EDGE(E-GPRS): 236.8kbps DL/236.8kbps UL (multi-slot class 12) |

| | |
|---|---|
| Physical feature | Appearance size: 32mm × 29mm × 2.4mm<br>Package: 144pin LCC+LGA<br>Weight: 4g ± 0.5g |
| Temperature feature | Operating temperature: －30℃ to +75℃ The module works normally within this temperature range, and the related performance meets the requirements of 3GPP standards.<br>Extended temperature: －40℃ to +85℃ The module works normally within this temperature range, and the baseband and RF functions are normal. However, some RF indicators may exceed the range of 3GPP standards. When the temperature returns to the normal operating range of the module, all the indicators of the module meet the requirements of 3GPP standards.<br>Storage temperature: －40℃ to +90℃ The module application terminal store in certain temperature conditions. Modules may not operate properly or may be damaged beyond this range. |

## 2.3 Hardware Architecture

The hardware of the L716-LA product includes:

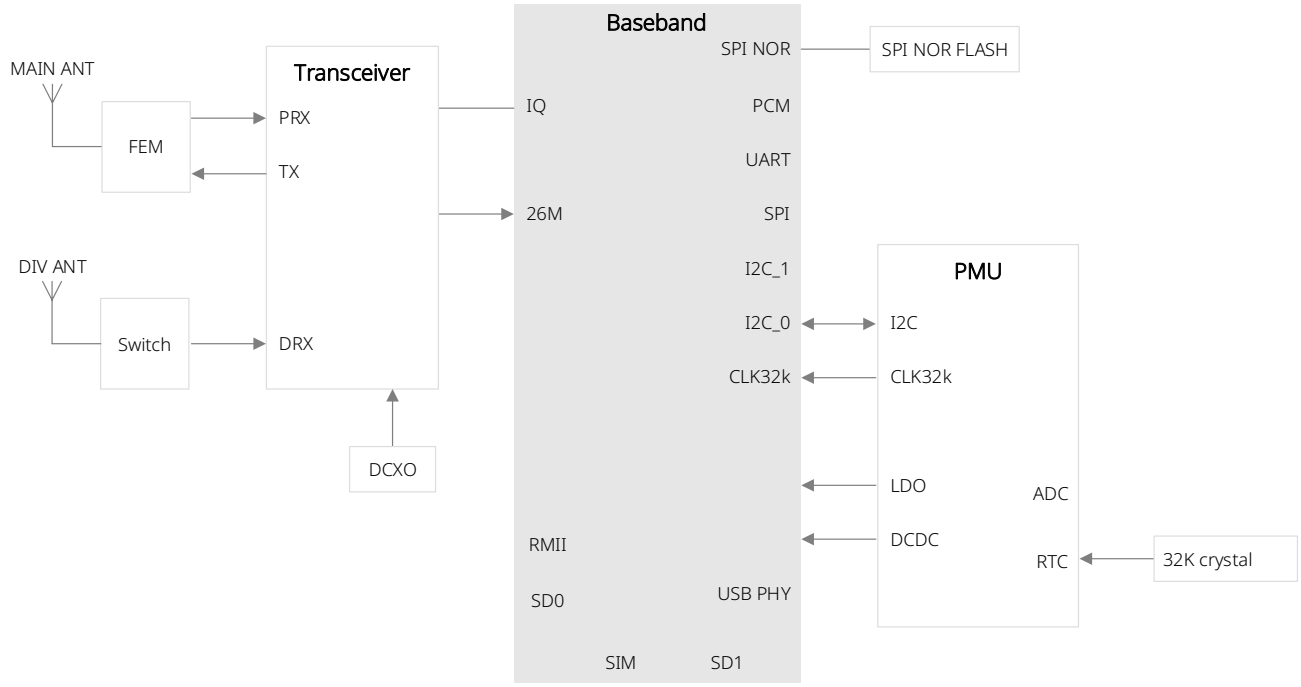



Figure 1. Hardware diagram

The main hardware features of the module includes the baseband and RF features.

- CPU
- PMU
- FLASH：NOR or NAND
- RF Transceiver
- RF Switch
- Antenna

## 2.4 ADP & EVB Description

In order to help customers develop applications with L716-LA module, Fibocom supplies an evaluation board to control or test the module. For more details, please refer to *Fibocom_L716_Series_Evaluation Board User Guide* and *Fibocom_EVB-LGA-F01_User Guide.*

# 3 Pin Definition

## 3.1 Pin Distribution

The L716-LA module adopts LCC+LGA packaging with a total of 144 pins, including 80 LCC pins and 64 LGA pins. The pin distribution is shown in the following figure.

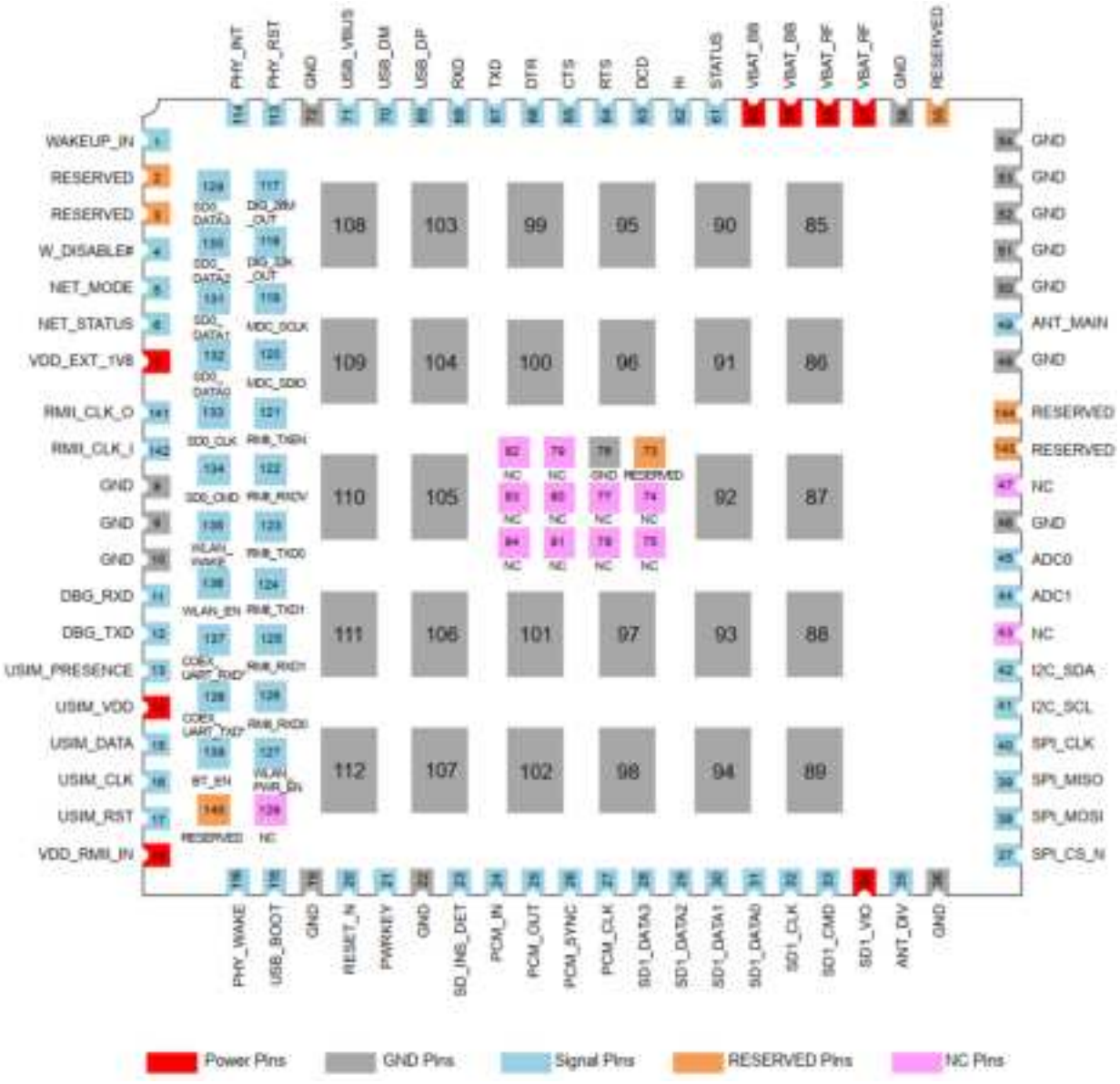



Figure 2. Pin distribution

## 3.2 Pin Details

Table 3. Pin attributes

| Attribute | Description |
|---|---|
| Number | Pin number |
| Name | Pin name |
| I/O | Indicates the direction of the pin signal.<br>PI: Power input<br>PO: Power output<br>DI: Digital input<br>DO: Digital output<br>DIO: Digital input/output<br>AI: Analog input<br>AO: Analog output<br>AIO: Analog input/output<br>OD: Open drain<br>G: Grounded<br>PU: Pull up<br>PD: Pull down |
| Voltage | Indicates the power domain the port is in. |
| Description | The detailed meaning of the pin and the handling when not in use. |

"*" indicates that the function is in development.

Table 4. Power interface

| Pin No. | Pin Name | I/O | Power Domain | Description |
|---|---|---|---|---|
| 7 | VDD_EXT_1V8 | PO | 1.8V | Module digital level 1.8V output, 80mA |
| 14 | USIM_VDD | PO | 1.8V/3V | (U)SIM power supply, the module automatically identifies 1.8 V or 3.0 V (U)SIM card |
| 18 | VDD_RMII_IN | PI | 3.3V | RMII IO power input |
| 34 | SD1_VIO | PO | 2.8V | SD card IO port power supply, non-SD card power supply, power supply capacity 100mA |
| 57 | VBAT_RF | PI | 3.3V~4.4V | Module power input, typical 3.8V, power supply capacity 2A |
| 58 | VBAT_RF | PI | 3.3V~4.4V | |
| 59 | VBAT_BB | PI | 3.3V~4.4V | |
| 60 | VBAT_BB | PI | 3.3V~4.4V | |
| 8~10, 19, 22, 36, 46, 48, 50~54, 56, 72, 76, 85~112 | GND | G | - - | GND |

Table 5. Control interface

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| 1 | WAKEUP_IN | DI | PD | 1.8V | External device wakeup module, active low by default, configurable by software |
| 4 | W_DISABLE# | DI | PD | 1.8V | Module flight mode control, pulled up by default, low level enables the module |

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| | | | | | to enter flight mode |
| 5 | NET_MODE | DO | PD | 1.8V | Module network state indicator (default) |
| 6 | NET_STATUS | DO | PD | 1.8V | Module network state indicator |
| 13 | USIM_PRESENCE | DI | PD | 1.8V | (U)SIM card hot plug detection, active high by default |
| 20 | RESET_N | DI | - - | 1.8V | Module reset signal, active low, pull up inside, without pulling up externally |
| 21 | PWRKEY | DI | - - | 3V | Module power-on/off signal, active low, pull up inside, without pulling up externally |
| 23 | SD_INS_DET | DI | PD | 1.8V | SIM card insertion detection signal, active low by default |
| 61 | STATUS | DO | PD | 1.8V | Module network state indicator |
| 115 | USB_BOOT | DI | PD | 1.8V | Reserve force download function, active high |

Table 6. BB interface

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| 11 | DBG_RXD | DI | PU | 1.8V | Debug serial port receiving |
| 12 | DBG_TXD | DO | PU | 1.8V | Debug serial port transmitting |
| 15 | USIM_DATA | IO | PD | 1.8 V/3V | (U)SIM data signal line, external pull-up is required |
| 16 | USIM_CLK | O | PD | 1.8 V/3V | (U)SIM clock signal line |

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| 17 | USIM_RST | O | PD | 1.8 V/3V | (U)SIM reset signal line |
| 24 | PCM_IN | DI | PD | 1.8V | PCM data input |
| 25 | PCM_OUT | DO | PD | 1.8V | PCM data output |
| 26 | PCM_SYNC | DIO | PD | 1.8V | PCM synchronization signal |
| 27 | PCM_CLK | DIO | PD | 1.8V | PCM clock signal |
| 28 | SD1_DATA3 | DIO | PU | 2.8 V | SD card data signal 3 |
| 29 | SD1_DATA2 | DIO | PU | 2.8 V | SD card data signal 2 |
| 30 | SD1_DATA1 | DIO | PU | 2.8 V | SD card data signal 1 |
| 31 | SD1_DATA0 | DIO | PU | 2.8 V | SD card data signal 0 |
| 32 | SD1_CLK | DO | PD | 2.8 V | SD card clock signal |
| 33 | SD1_CMD | DIO | PU | 2.8 V | SD card control signal |
| 37 | SPI_CS_N | DO | PU | 1.8V | SPI chip selection signal |
| 38 | SPI_MOSI | DO | PD | 1.8V | SPI master device data output, slave device data input |
| 39 | SPI_MISO | DI | PD | 1.8V | SPI master device data input, slave device data output |
| 40 | SPI_CLK | DO | PD | 1.8V | SPI clock signal |
| 41 | I2C_SCL | DO | PU | 1.8V | $I^2C$ clock signal (pulled up inside the module) |
| 42 | I2C_SDA | DIO | PU | 1.8V | $I^2C$ data signal (pulled up inside the module) |
| 44 | ADC1 | AI | - - | 0V–5V | Analog-to-digital conversion 1 (1k resistor in series is recommended to |

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| | | | | | prevent static) |
| 45 | ADC0 | AI | - - | 0V–5V | Analog-to-digital conversion 0 (1k resistor in series is recommended to prevent static) |
| 62 | RI | DO | PD | 1.8V | Ringing prompt; the module wakes up the upper computer; default high level; when there is a phone call, SMS, data to the module, output 1 second low pulse |
| 63 | DCD | DO | PD | 1.8V | Carrier detection |
| 64 | RTS | DO | PU | 1.8V | Main serial port requests to send |
| 65 | CTS | DI | PU | 1.8V | Main serial port clears to send |
| 66 | DTR | DI | PD | 1.8V | Ready |
| 67 | TXD | DO | PU | 1.8V | Main serial port transmits data |
| 68 | RXD | DI | PU | 1.8V | Main serial port receives data |
| 69 | USB_DP | DIO | - - | - - | USB differential data signal+ |
| 70 | USB_DM | DIO | - - | - - | USB differential data signal- |
| 71 | USB_VBUS | DI | PD | 3.3~5.25V | USB plugin detection, typical 5V |
| 113 | PHY_RST | DO | PD | 3.3V | PHY restart |
| 114 | PHY_INT | DO | PD | 3.3V | PHY interrupt |
| 116 | PHY_WAKE | DO | PD | 3.3V | PHY wakeup |
| 117 | DIG_26M_OUT | DO | PD | 1.8V | 26M clock output |

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| 118 | DIG_32K_OUT | DO | PD | 1.8V | 32.768K clock output |
| 119 | MDC_SCLK | DO | PD | 3.3V | Manage data clock |
| 120 | MDC_SDIO | DIO | PD | 3.3V | Manage data input/output |
| 121 | RMII_TXEN | DO | PD | 3.3V | RMII transmit enable |
| 122 | RMII_RXDV | DI | PD | 3.3V | RMII received data valid |
| 123 | RMII_TXD0 | DO | PD | 3.3V | RMII transmits data 0 |
| 124 | RMII_TXD1 | DO | PD | 3.3V | RMII transmits data 1 |
| 125 | RMII_RXD1 | DI | PD | 3.3V | RMII receives data 1 |
| 126 | RMII_RXD0 | DI | PD | 3.3V | RMII receives data 0 |
| 127 | WLAN_PWR_EN | DO | PD | 1.8V | WLAN power enable |
| 129 | SD0_DATA3 | DIO | PU | 1.8V | SDIO data line 3 |
| 130 | SD0_DATA2 | DIO | PU | 1.8V | SDIO data line 2 |
| 131 | SD0_DATA1 | DIO | PU | 1.8V | SDIO data line 1 |
| 132 | SD0_DATA0 | DIO | PU | 1.8V | SDIO data line 0 |
| 133 | SD0_CLK | DO | PD | 1.8V | SDIO clock line |
| 134 | SD0_CMD | DO | PU | 1.8V | SDIO control line |
| 135 | WLAN_WAKE | DO | PD | 1.8V | WLAN wakeup |
| 136 | WLAN_EN | DO | PD | 1.8V | WLAN enable |
| 137 | COEX_UART_RXD | DI | PD | 1.8V | Coexisting serial port receiving |
| 138 | COEX_UART_T | DO | PD | 1.8V | Coexisting serial port transmitting |

| Pin No. | Pin Name | I/O | Reset Value | Power Domain | Description |
|---|---|---|---|---|---|
| | XD | | | | |
| 139 | BT_EN | DO | PD | 1.8V | BT enable |
| 141 | RMII_CLK_O | DO | PD | 3.3V | 25M/50M clock output to PHY or MAC |
| 142 | RMII_CLK_I | DI | PD | 3.3V | 50M clock input is MAC |

Table 7. RF interface

| Pin No. | Pin Name | I/O | Power Domain | Description |
|---|---|---|---|---|
| 35 | ANT_DIV | AI | - - | Diversity antenna |
| 49 | ANT_MAIN | AIO | - - | Main antenna |

Table 8. Reserved interface

| Pin No. | Pin Name | I/O | Power Domain | Description |
|---|---|---|---|---|
| 2、3、55、73、140、143、144 | RESERVED | - - | - - | Reserved |
| 43、47、74、75、77~81、83、84、128 | RESERVED (L716-CN-70/80/85 and L716-LA-00)<br>NC (other type) | - - | - - | Reserved |
| 82 | NC | - - | - - | - - |

# 4 Application Interfaces

## 4.1 Power supply

### 4.1.1 Electrical Specifications

Table 9. Electrical indicator

| Indicator | | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| Power supply voltage | VBAT power supply | 3.3 | 3.8 | 4.4 | V |
| | RMII IO power supply | - - | 3.3 | - - | V |

Table 10. Absolute Maximum Ratings

| Indicator | | Minimum Value | Maximum Value | Unit |
|---|---|---|---|---|
| Power supply voltage | VBAT power supply | -0.3 | 6.3 | V |
| | RMII IO power supply | 3.15 | 3.465 | V |
| Analog voltage | ADC input | -0.3 | 6.3 | V |

### 4.1.2 Power Input

#### Background information

The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. If the power supply capacity is insufficient, the power supply voltage drops instantly, which may cause the module power-off or restart.

The following figure shows the power supply limit.

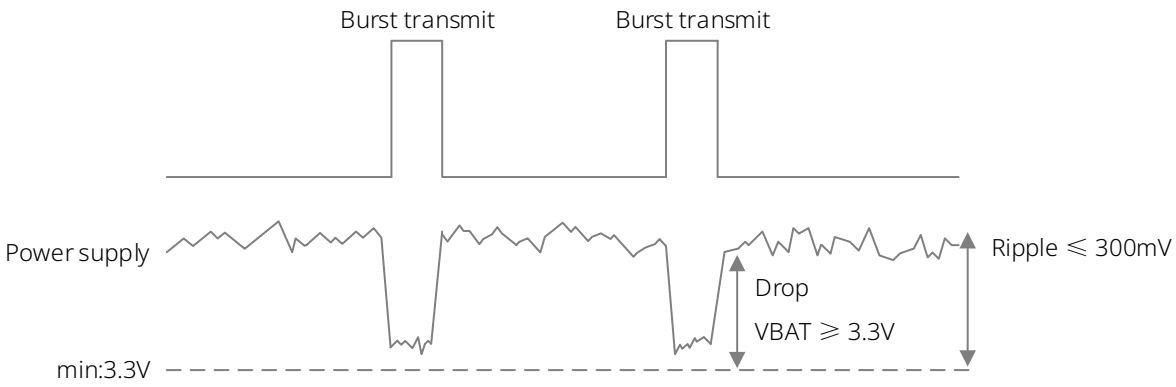



Figure 3. Power supply limit

The ripple of the power supply is less than 300mV, and the line ESR (equivalent series resistance) is less than 150mΩ. When the module is working, ensure that the DC power supply voltage is not lower than the minimum voltage.

### Schematic diagram design

Assuming that VBAT is the power pin of the module, and the reference design is shown in the following figure.

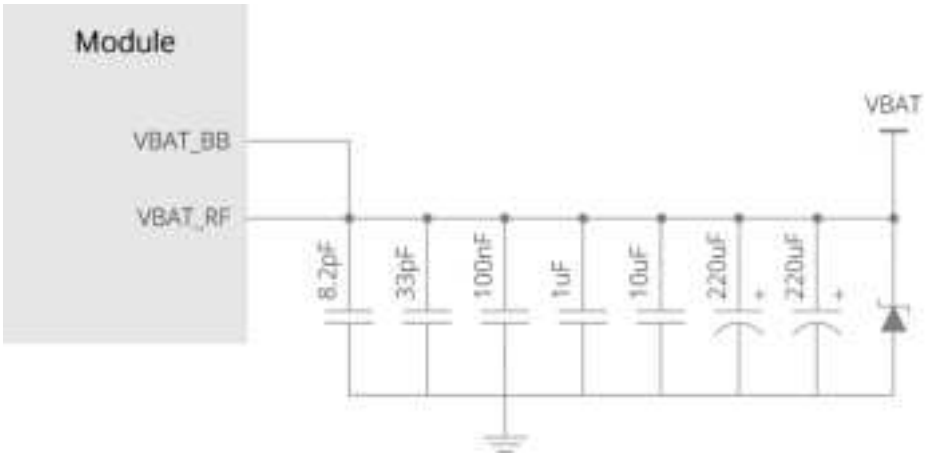



Figure 4. Power supply circuit reference design

Design description:

Table 11. Design description

| Design Consideration | Mode | Recommended Parameter |
|---|---|---|

| | | |
|---|---|---|
| Reduce power fluctuations during module operation | Voltage stabilizing capacitor | Low ESR capacitors are used, 220uF x 2<br>LDO or DC power supply requires no less than 440uF capacitor<br>Battery power supply requires 100 uF to 220 uF capacitor |
| Filter out interference from clock and digital signals | Filter capacitor | 10uF , 1uF and 100nF |
| Filter out RF interference at , high, low and intermediate bands | Decoupling capacitor | 33pF and 8.2pF |

It is recommended to reserve the position of TVS tube for VBAT power supply. The recommended model is EGA10402V05AH.

PCB design

In order to reduce the equivalent impedance of VBAT traces, the traces from external power supply to VBAT should be as short and wide as possible (at least 2 mm/2A in width to ensure sufficient power supply capacity), small capacitors should be placed close to the module, and the ground plane of the power supply should be as complete as possible.

## 4.1.3 Power Output

The power output interfaces of the module are described in the following table.

Table 12. Module power interfaces

| Pin No. | Pin Name | I/O | Description | DC Parameter | | |
|---|---|---|---|---|---|---|
| | | | | Minimum Value (V) | Typical Value (V) | Maximum Value (V) |
| 7 | VDD_EXT_1V8 | PO | Digital 1.8V level, | 1.62 | 1.8 | 1.98 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | 80mA | | | |
| 14 | USIM_VDD | PO | SIM card power supply, 50mA | 1.71/2.85 | 1.8/3 | 1.89/3.15 |
| 34 | VDD_SDIO | PO | SIM card IO power supply, 100mA | 2.7 | 2.85 | 3 |

## 4.2 Power-on/off

### Schematic diagram design

Power-on sequence of the module is shown in the following figure.

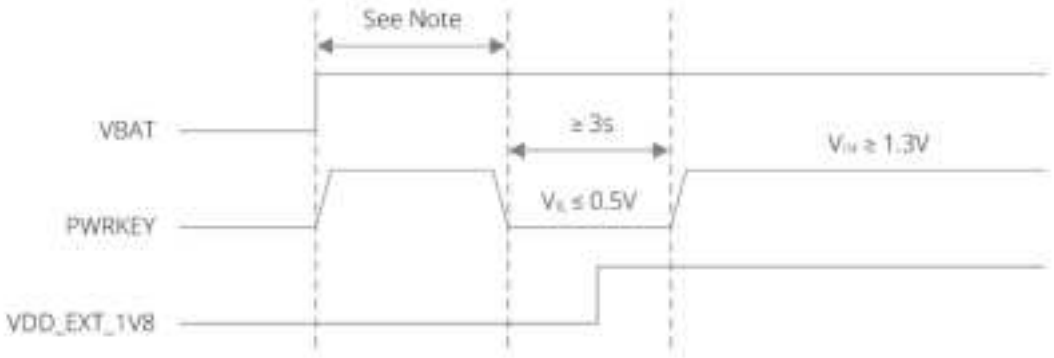



Figure 5. Power-on sequence

It is necessary to ensure that the power supply voltage VBAT is stable before pulling down the PWRKEY pin. It is recommended that the interval between powering on the VBAT and pulling down the PWRKEY pin be at least 30ms, and that the PWRKEY pin be pulled down for at least 3s.

One way is to use OC/OD driver circuit to control the PWRKEY pin. The reference circuit is shown in the following figure.

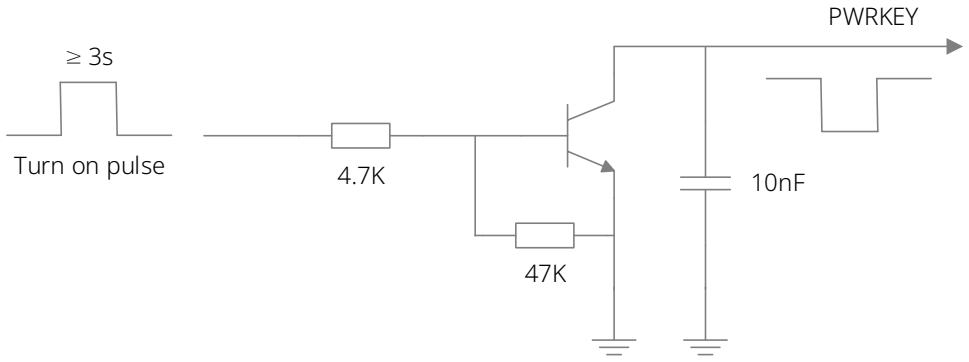



Figure 6. Reference circuit of OC/OD driver

The other way is to use a button switch. A TVS (ESD9X5VL-2/TR is recommended) should be located close to the button to implement ESD protection. The reference circuit is shown in the following figure.

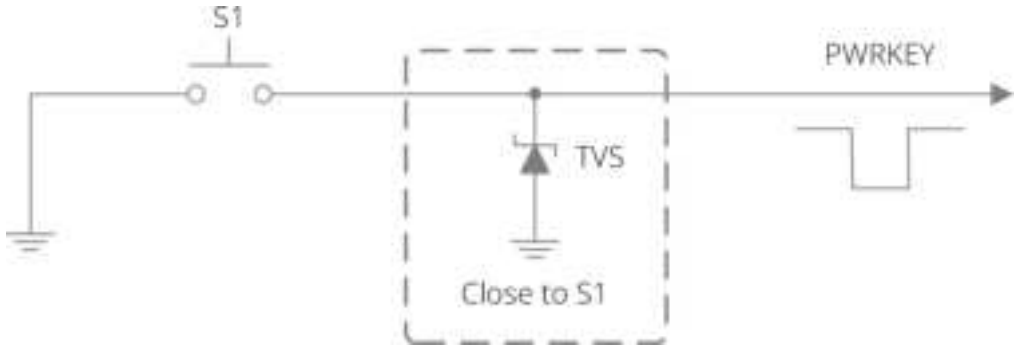



Figure 7. Button control reference circuit

To implement auto power-on, connect the PWRKEY pin in series with 0R resistor to ground.

The AT command does not apply to auto power-on.

Power-off modes:

Hardware power-off: Pull down the PWRKEY pin for 2.5s to power off the module.

Software power-off: Power off the module through the AT+CPWROFF command, only applicable to non-master control module.

When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal Flash and causing data loss. It is strongly recommended to power off the module normally before cutting off the power supply.

When using the software to power off the module, do not pull down the PWRKEY pin after the power off command is executed, otherwise the module will automatically boot again.

The hardware power-off sequence is shown in the following figure.

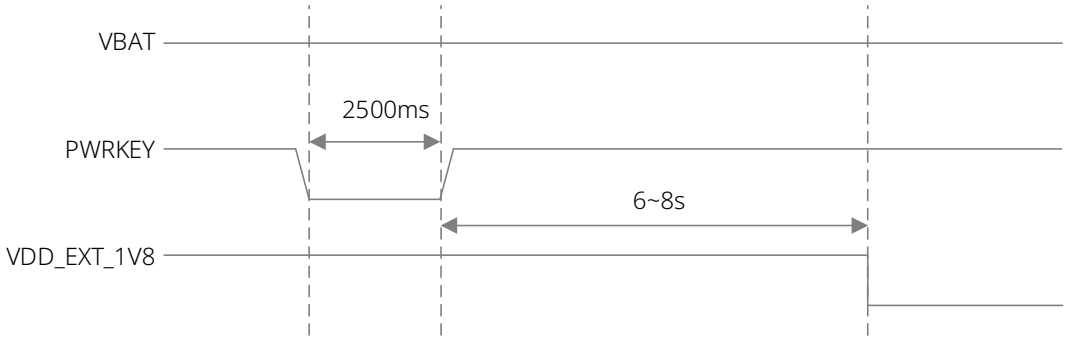



Figure 8. Hardware power-off sequence

After the PWRKEY signal is released, the next power-on trigger can be performed at least 8 seconds later. This interval is reserved for the module to perform the shutdown process and release the power of the peripheral circuit connecting with module interface.

## 4.3 Reset

### Background information

The module can be reset to the initial state.

The module can be reset by hardware and software.

- Hardware reset

Hardware reset control sequence is shown in the following figure.

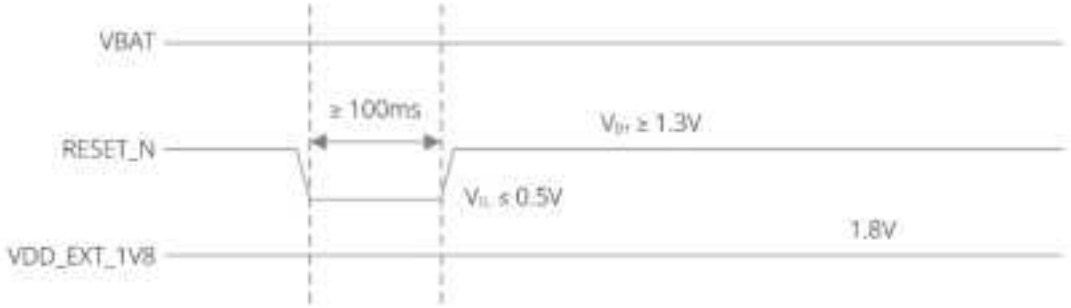



Figure 9. Hardware reset control sequence

Set RESET_N low for at least 100ms and then release. Similar to the power on/off control circuit, the reset reference circuit is shown in the following figures, and the RESET_N pin can be controlled using the OC/OD driver circuit or a button.

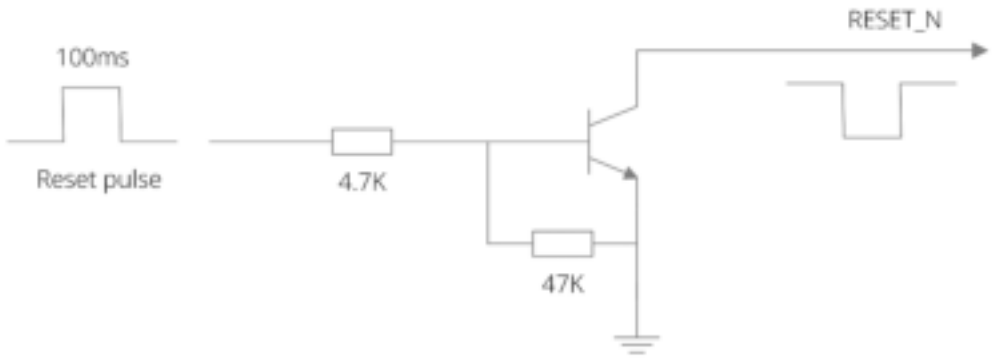



Figure 10. Reference circuit of OC/OD driver reset

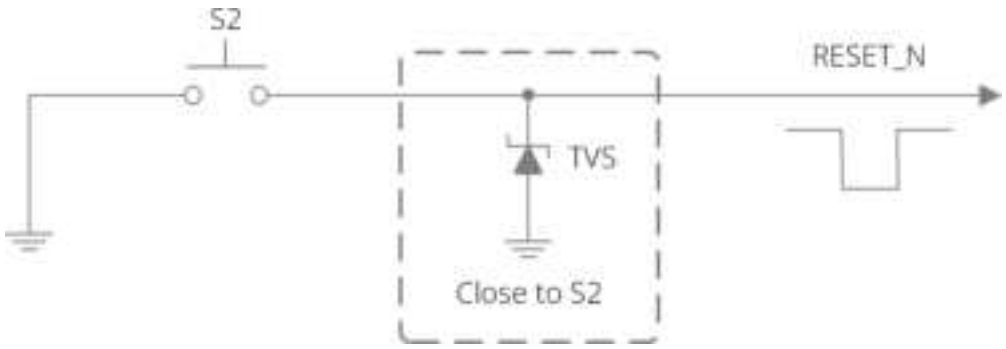



Figure 11. Reference circuit of button control reset

- Software reset

AT+CFUN=15

### PCB design

RESET_N is a sensitive signal. During PCB layout, keep it far away from radio frequency interference.

PCB traces must be protected using GND and kept away from edges of PCBs to avoid module reset due to ESD problems.

For the GPIO multiplexing function of Open models such as L716-CN-60 and L716-EU-60, please refer to *Fibocom_L716_GPIO Function Multiplex. Open version proprietary* interface include SDIO RMII SPI UART Keypad EXT_INT and GPIO etc.

## 4.4 USB

### Background information

USB (Universal Serial Bus) is an external bus standard used to standardize the connection and communication between computer and external equipment, and is an interface technology applied in the field of PC. USB is generally used for debugging or software upgrade.

### Schematic diagram design

Connect two 0R resistors in series between the module and MCU/connector, reserve the position of common mode choke, and make co-pad design, so as to facilitate debugging in case of EMI. In order to meet that signal integrity requirement of the USB data line, a common mode choke and a 0R resistor are placed close to the module, and the TVS is prevent the module from being damaged by static electricity, the interface circuit design is as follows.

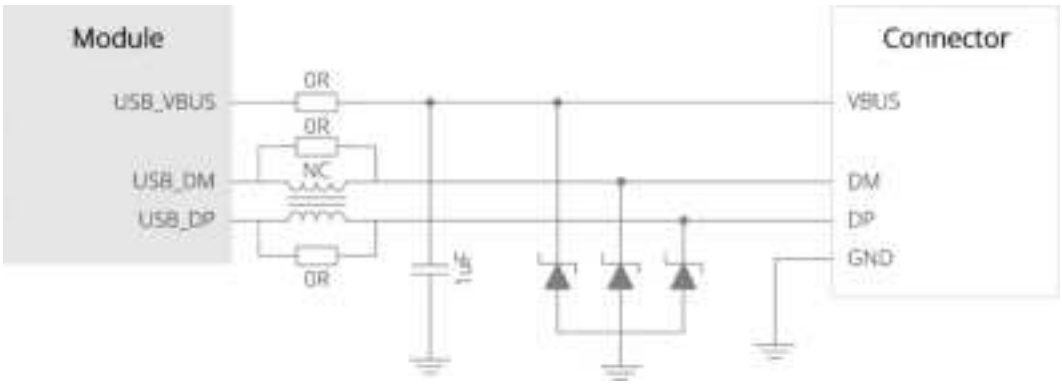



Figure 12. Interface circuit design

### PCB design

SB_DP and USB_DM are high-speed differential signal lines, which are required to be equal in length and parallel to avoid right-angle routing. The length difference of traces is controlled to be less than or equal to 2 mm, and the differential impedance is controlled at 90Ω±15%.

The USB data line cannot be routed under the crystal, oscillator, magnetic device, or RF signal. It is recommended to take an inner differential line that is wrapped with copper connected to the ground at all directions.

The ESD protector for the USB data line must be placed close to the USB interface. The parasitic capacitance of the ESD protector selected for the USB data line must not exceed 1 pF. TVS with a capacity of 0.5pF is recommended.

USB 2.0 differential signal line is laid on the signal layer nearest to the ground.

If the USB function is not used, suggest reserve test points for easy log capture.

Need to ensure that the VBUS signal connected to 5V power supply, if VBUS signal floating, USB port can't normal operation.

## 4.5 UART

### Background information

UART (Universal Asynchronous Receiver/Transmitter) converts a parallel input signal into a serial output signal. UARTs are typically used to communicate with PCs, including monitor debuggers and other devices, such as EEPROMs. For modules with high communication rate, USB 3.0 data interface is preferred for data transmission or AT communication with PC or other devices, and peripheral UART is only used as peripheral driver interface.

### Schematic diagram design

The module has three groups of serial ports: main serial port, debugging serial port and coexistence serial port *. The baud rate of the main serial port ranges from 300bps to 921600bps, and the default baud rate is 115200bps. The main serial port is used for data transmission or AT command transmission. The debugging serial port is used for debugging, suggest reserve test point, and the supported baud rate is 115200bps. In addition, the module reserves a group of coexistence serial ports.

The serial port level of the module is 1.8V. If the level of the client host system is 3.3V or any other value, you need to add a level translator to the serial port connecting the module and the host. The following figures show the reference circuit design of the serial port level conversion circuit.

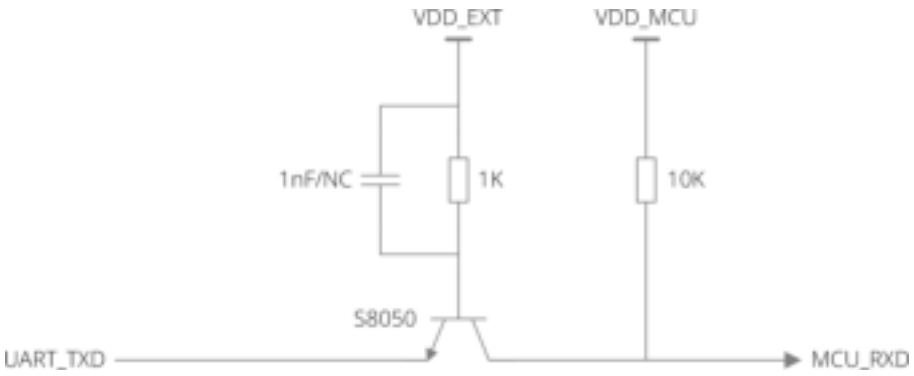



Figure 13. UART_TXD level conversion reference circuit

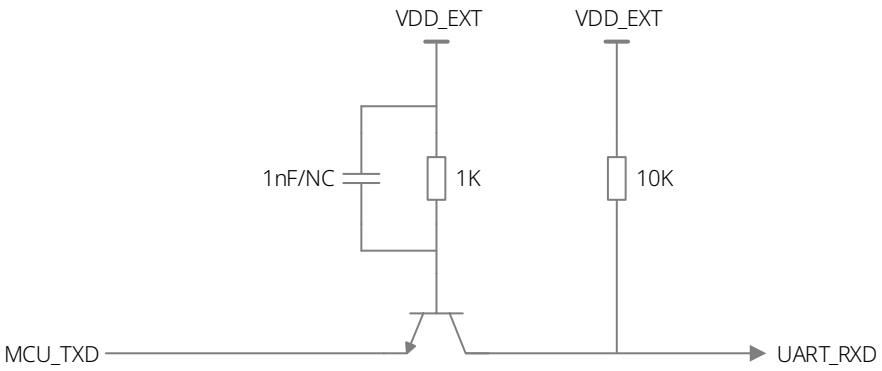



Figure 14. UART_RXD level conversion reference circuit

The level conversion circuits of UART_CTS and UART_RTS are the same as UART_RXD and UART_TXD.

The level conversion circuit is not recommended for applications with baud rates higher than 460Kbps.

The following figure shows the circuit design of the level conversion chip.

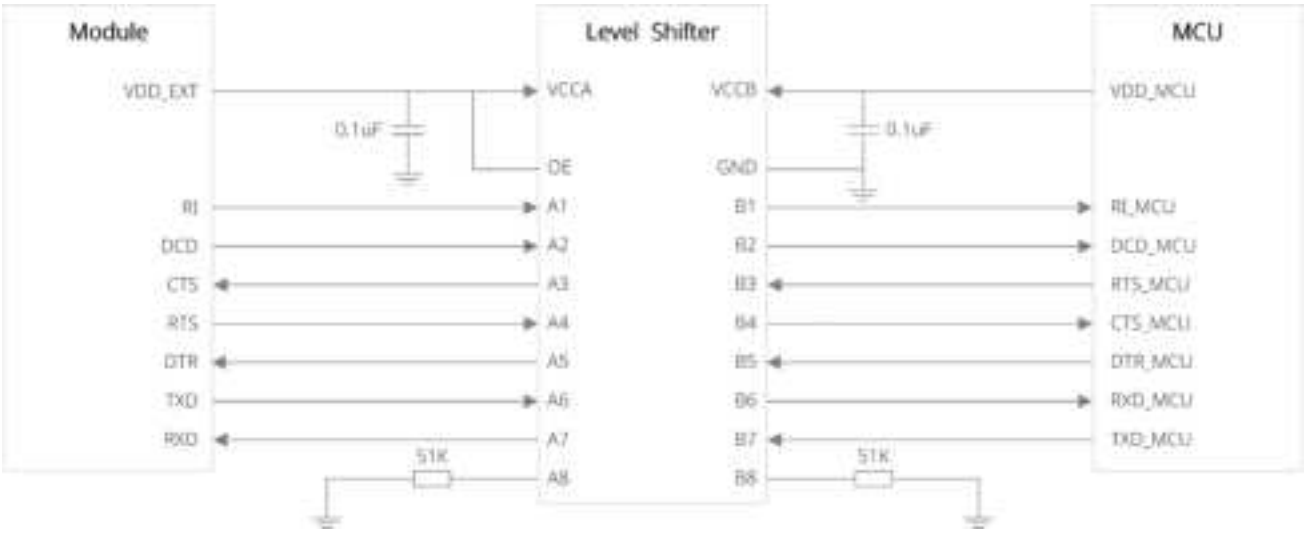



Figure 15. Reference circuit of level conversion chip

## 4.6 SPI

The module provides a set of general SPI interfaces to communicate with devices that

support the SSP standard. The module realizes the conversion between APB parallel data and SSP serial data, provides two working modes of Master and Slave, and supports three data formats: Motorola SPI, TI TISSP, and Silicion Labs ISI-SPI. The characteristics are as follows:

- APB slave devices conforming to the AMBA specification.
- ISI-SPI supports Master only.
- Interrupt mode is supported.
- The master mode supports a maximum of 52MHz clock rate, and the slave mode supports a maximum of 26MHz clock rate.

## 4.7 I2C

### Background information

The I2C bus is a simple, bi-directional, two-wire synchronous serial bus. It requires only one data line and one clock line to transfer information between devices connected to the bus. Mainly used for communication between multiple integrated circuits (ICs) within a system.

### Schematic diagram design

A pull-up resistor is connected to the I2C interface inside the module to the 1.8V power domain. External pull-up is not required. When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address. Support standard rate of 100Kbps, fast mode of 400Kbps, and high-speed mode of 3.4Mbps communication rate.

## 4.8 SDIO

### Background information

The module provides two groups of SDIO interfaces and supports SDIO 3.0 protocol. 2.8V SD card is recommended for SD1, and 1.8V SD card is not supported. SD0 supports master mode only and is often used to connect peripheral WIFI devices.

## Schematic diagram design

SD1 reference circuit design is shown in the following figure.

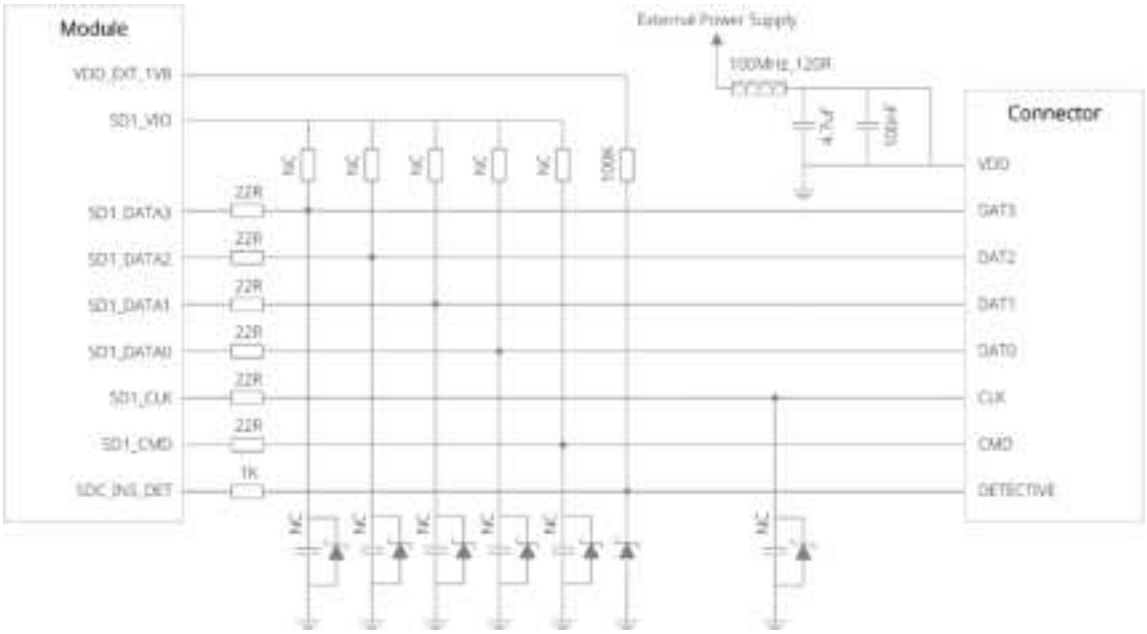



Figure 16. SD1 reference circuit design

SD0 reference circuit design is shown in the following figure.

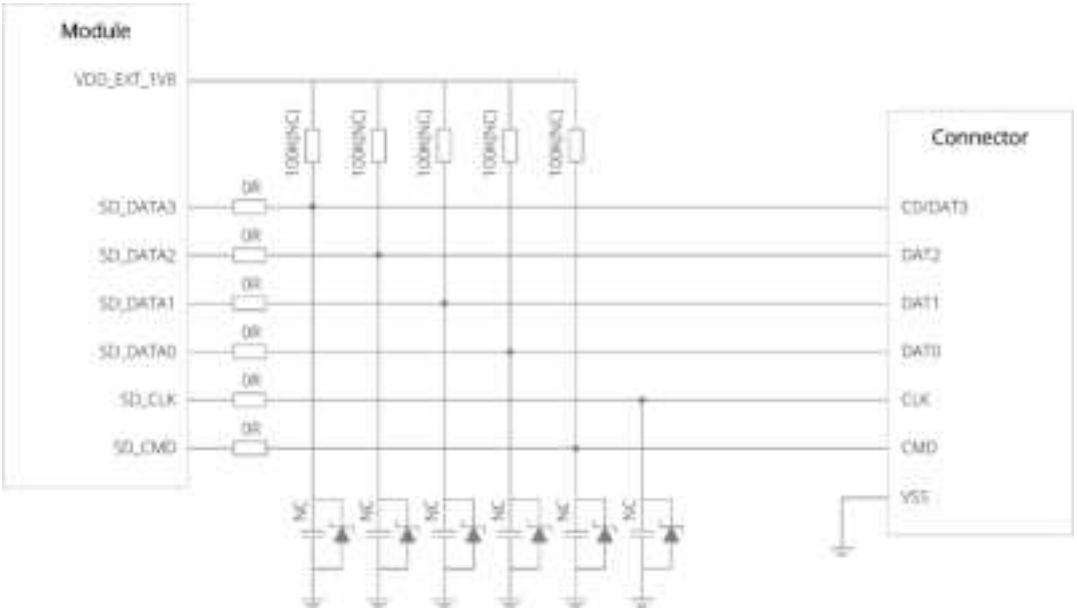



Figure 17. SD0 reference circuit design

## PCB design

SD card circuit design must meet EMC standards and ESD requirements, and at the same time, EMS capability must be improved to ensure that the SD card can work stably. The following principles must be strictly followed in the design:

- If the routing length of signal lines is equal to or less than 50 mm, it is recommended to place the SD card connector as close to the SD signal pin of the module as possible because the internal cabling length of the module is 40 mm. If the routing length is equal to or less than 10 mm, the routing length difference of the clock signal line and data signal line should be controlled equal to or less than 1 mm.
- The SD signal line must be grounded all around and kept away from RF antenna, DCDC power supply, clock signal line and other strong interference sources.
- Reference ground must be installed for the SD signal line, and data line impedance must be controlled with 50 Ω (±10%).
- It is recommended to install resistors between the module and SD card connector in serial mode, and reserve bypass capacitors. In case of interference or ESD issue, you can adjust the capacitors and resistors to improve signal quality.
- The total load capacitance on the SD signal lime must be less than 40 pF.

## 4.9 RMII

The module provides RMII interface to realize the function of full-duplex communication of common 100M network card. 100M Ethernet uses the technical specifications specified by Ethernet, such as CSMA/CD protocol, Ethernet frame, full duplex, flow control and management objects defined in IEEE802.3 standards. The characteristics are as follows:

- Supports IEEE 802.3 and adapts to 10Mbps/100Mbps RMII interface, and uses RMII interface Ethernet PHY for communication.
- Supports full-duplex/half-duplex operation mode.
- Supports transmission channel flow control operation.
- Supports optional MDIO Master interface to realize the configuration and management

of PHY equipment.

### Power-on sequence

The power-on sequence requires VDD_EXT_1V8 (7pin) to be powered on first, and VDD_RMII_IN (18pin) to be powered on after 20us. Or power on at the same time, but keep VDD_RMII_IN – VDD_EXT_1V8 < 1.8V during power-on.

### PCB design

It is recommended that RMII_TXD0/TXD1/TXEN/CLK_O are routed in the same group and equal in length, and the length difference should be controlled within ±2 mm; RMII_RXD0/RXD1/RXDV/CLK_I are routed in the same group and equal in length, and the length difference should be controlled within ±2 mm; MDC_SCLK/SDIO are routed in the same group and equal in length, and the length difference should be controlled within ±2 mm.

## 4.10 PCM

### Background information

The module provides a set of digital audio interface PCM, which uses I2S sequence to transmit voice/audio data to realize voice/audio data acquisition and playback. PCM adopts the mainstream European E1 standard in China and the coding of 16-bit/32-bit linear format. PCM_SYNC works at 8 KHz (488 ns). Module serves as master, supporting PCM as slave.

### Schematic diagram design

The reference circuit is shown in the following figure.

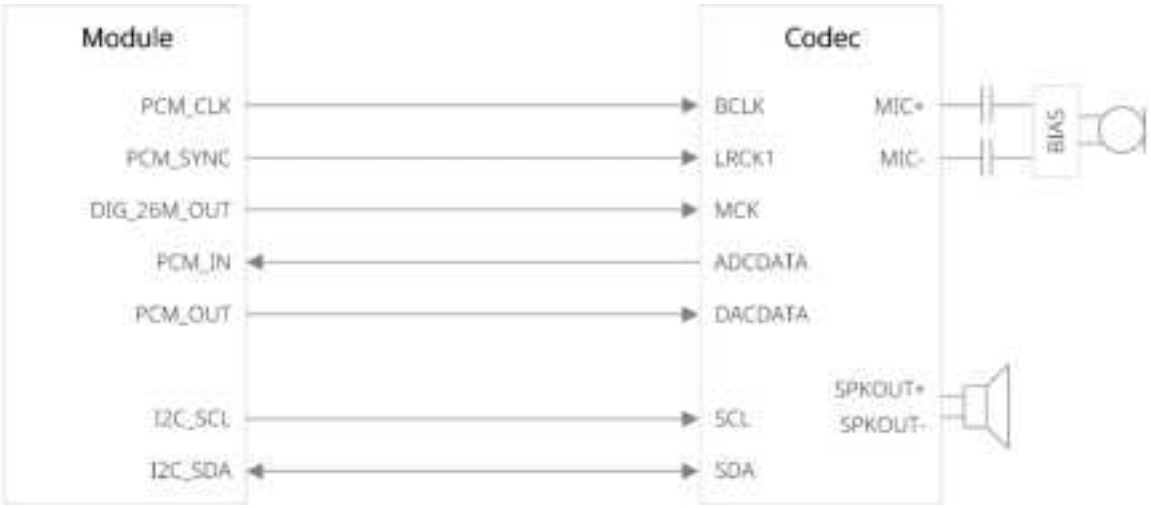



Figure 18. I2S reference circuit

## 4.11 SIM

### Background information

The module can only be used in the network after the SIM card is inserted. 1.8V and 3V SIM cards are supported. The USIM_DATA needs to be pulled up externally.

### Schematic diagram design

The schematic diagram design is divided into the following scenarios:

With detection signal: it supports the detection of SIM card insertion and pull-out, which is divided into normally open card slot and normally closed card slot. Generally used in conjunction with the hot plug function. It is recommended to use (U)SIM card slot with hot plug detection function. Without detection signal: it does not support the detection of SIM card insertion and pull-out.

Refer to the following design for normally closed SIM card slot.

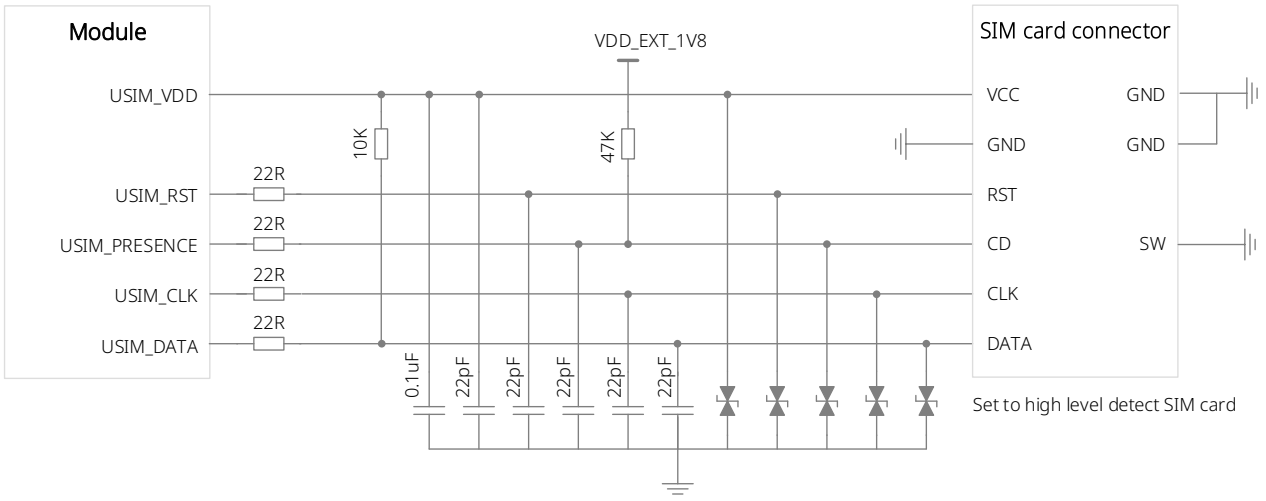



Figure 19. Normally closed SIM card slot

The principles of the normally closed SIM card slot are described as follows:

When SIM card is pulled out, CD and SW are shorted, and USIM_PRESENCE pin is at a low level. When SIM card is inserted, CD and SW are opened, and USIM_PRESENCE pin is at a high level.

Refer to the following design for normally opened SIM card slot.

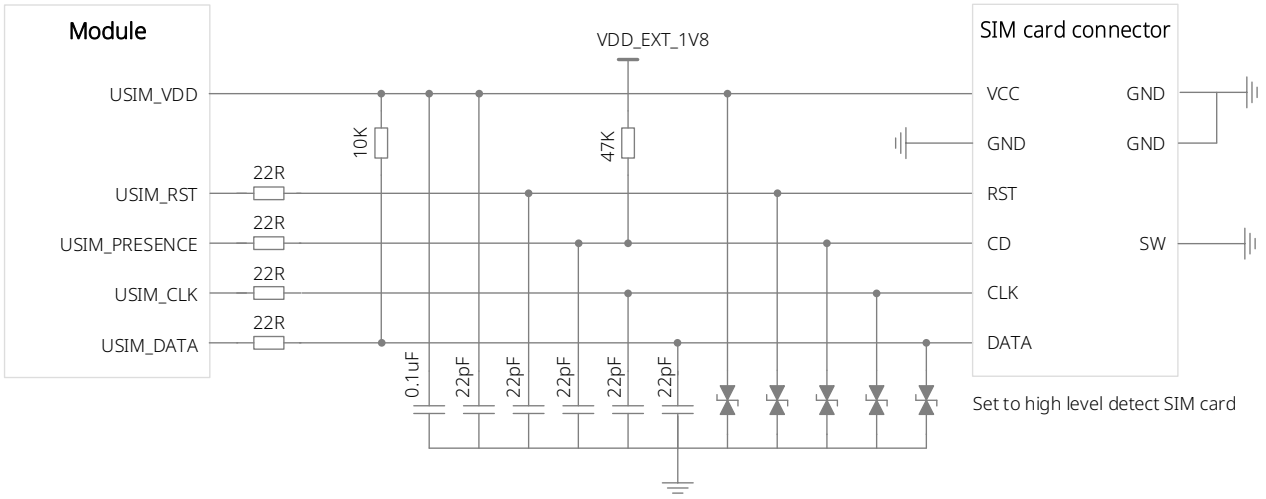



Figure 20. Normally opened SIM card slot

The principles of the normally opened SIM card slot are described as follows:

When SIM card is pulled out, CD and SW are opened, and USIM_PRESENCE pin is at a high level. When SIM card is inserted, CD and SW are shorted, and USIM_PRESENCE pin is at a

low level.

Refer to the following design for SIM card slot without detection signal.

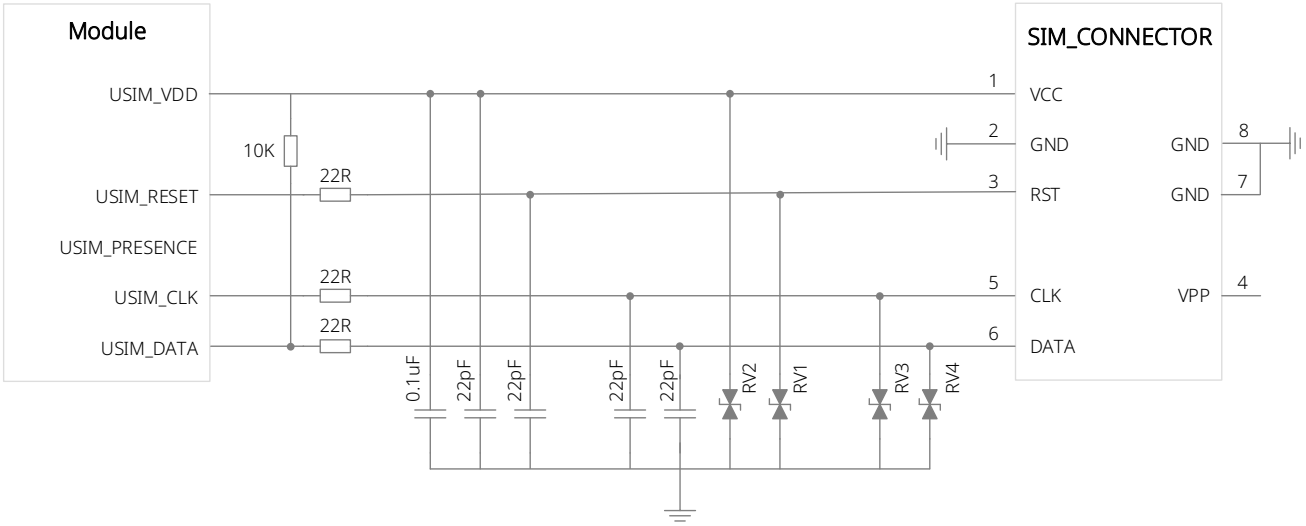



Figure 21. SIM card slot without detection signal

The USIM_PRESENCE pin of the module is disconnected, and the hot plug function is disabled through the AT command.

### PCB design

Layout key points:

- Please reserve capacitor filter for SIM signal line to prevent interference from GSM high frequency signal.
- SIM card and routing should be away from EMI interference source, such as power circuit, RF circuit, antenna, and high-speed digital signal circuit.
- ESD components of SIM card should be close to SIM card slot interface during PCB layout.
- When routing antenna feeder line, keep the line away from power device, and avoid the line paralleling to antenna copper foil, which causes the SIM card to drop abnormally.
- The filter capacitor and ESD device of SIM signal cable are placed close to the SIM card slot. Less than 11pF capacitor is recommended for ESD device.

Routing key points:

To reduce EMC problem, keep SIM signal line away from RF cable, power line, clock line and high-speed data line.

- Do not route the adjacent layers with the SIM signal line; otherwise, the routing poses an EMI risk. Design the other traces and SIM signal line to be perpendicular with each other to reduce risk.
- Ensure the ground connectivity and integrity of PCB environment and the connectivity and integrity of SIM_GND. The nearest path connects to a clean system ground. To avoid mutual interference, please separately ground SIM_CLK and SIM_DATA. If conditions do not permit, at least the SIM signal must be grounded as a set.
- The SIM signal line should be routed along the inner layer.
- A SIM card slot with a metal shielding case must be used to improve the anti-interference ability.
- To ensure the integrity of signal, the routing length from the module to SIM card should not exceed 100 mm. Longer routing will reduce signal quality.

### Hot plug

The module support SIM card status detection function. The module determines whether the SIM card is inserted or removed by detecting the pin status of USIM_ PRESENCE. Note: When the module is working normally, if you unplug the SIM card without enabling SIM card hot plug function, it may cause damage to the SIM card and module.

SIM card hot plug function is enabled by default, if the function is not used, it is recommended to choose one of the following operation

1. Disabled by running the AT+MSMPD=0 command
2. Disable hot plug function by default on software
3. Pull-up USIM_PRESENCE by 47KΩ resistor to VDD_EXT_1V8

- If USIM_PRESENCE is at a high level, the module detects that a SIM card is inserted and initializes the card. After reading the SIM card information, the module will register with the network.
- When the USIM_PRESENCE is at a low level, the module determines that the SIM card is removed and does not read it.

The USIM_PRESENCE is active at high level by default, and can be switched to be active at low level by the AT+GTSET command.

### Solutions for RF interference

In practice, radio frequency interference is quite normal. Here are some solutions:

- Antenna coupling interference:

  Reasons:

  - When antenna transmits with high power, it causes direct interference to the SIM signal.
  - When antenna transmits with high power, it is coupled to the ground, reducing the stability of the whole system and causing indirect interference to the SIM signal.

  Solutions:

  - Adjust the filter capacitance value of the SIM signal.
  - Use a longer antenna, and keep it far away from SIM card part.
  - Shield the interference signal to protect SIM card.
  - Pay attention to the design of the ground, especially the connectivity of SIM card, module and the system ground.
  - Fully ground each layer of PCB and increase holes to enhance the EMC performance of the system.

- RF coupling will cause interference to GND. Adjust the capacitance values of capacitor and ESD components or even remove the capacitor (if it is necessary) to avoid the interference.

- PCB crosstalk:

Reasons:

- Other signal line on the main board has crosstalk with the SIM signal through the PCB trace.
- Antenna interrupted signal has crosstalk with the SIM signal through the PCB routing.
- Fluctuations of power has crosstalk with the SIM signal through the PCB routing.

Solutions:

- Adjust the filter capacitance value of the SIM signal.
- Find out the interference source, and change the board specifically.

# 4.12 ADC

### Background information

ADC (Analog-digital Converter) converts analog signals to digital values for use in processing and control systems. It can be used for voltage detection and other peripheral circuits.

### Schematic diagram design

The module provides two 12bit ADC interfaces. Send AT+MMAD query command to read voltage on each channel, the ADC voltage range is from 0V to 5V, sampling rate is 5KHz, sampling accuracy is 5/4096(V). When using the ADC function, a 1KΩ resistor in series is recommended to enhance ESD protection.

Use the AT+CBC command to query the current VBAT voltage value.

### PCB design

It is recommended to ground ADC signal lines to improve ADC voltage measurement accuracy.

## 4.13 Status Indicator

### Background information

Network status indicator interface drives the network status indicator to describe the network status of the module.

Table 13. Working status of the network status indicators

| Mode | Level Status of the Module Network Indication Pin | Description |
|---|---|---|
| 1 | Quick flash (600 ms high level/600 ms low level) | SIM card is not inserted<br>Registering with the network (T < 15s)<br>Failed to register with the network |
| 2 | Slow flash (3000 ms high level/75 ms low level) | Standby |
| 3 | Speed flash (75 ms high level/75 ms low level) | Established a data connection |
| 4 | Low level | Voice call |
| 5 | High | Sleep |

### Schematic diagram design

The reference circuit of network status indicators is shown in the following figure.

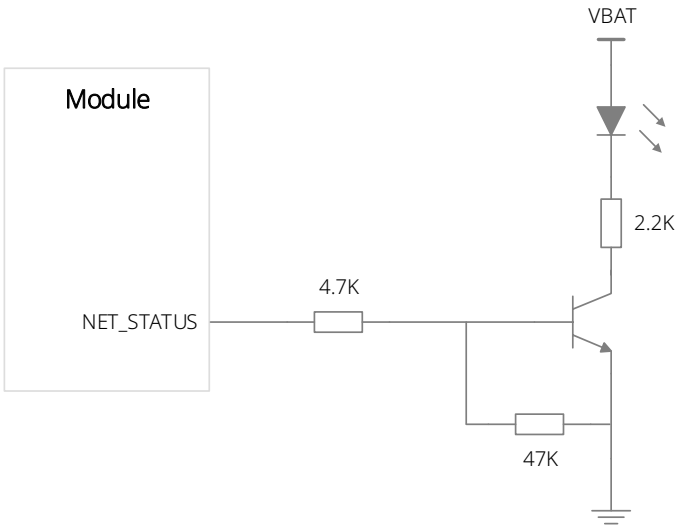



Figure 22. Reference circuit of network status indicators

Reserve 4.7K and 47K positions for voltage division to ensure that the VBE voltage of the triode is less than the turn-on voltage of the triode under the scenarios of booting, resetting, and waking to avoid the power consumption increase caused by the operation of the LED. The voltage of the VBE is greater than the turn-on voltage of the triode when the LED is working.

## 4.14 Flight Mode

### Background information

Flight mode can be enabled when it is necessary to turn off the transmission and reception of wireless signals to avoid interference with the surroundings. After entering flight mode, the RF function is disabled.

### Entering mode

- Hardware control:

Send AT+GTFMODE=1 to open the flight mode control function.

The module is in normal mode when the W_DISABLE# pin is pulled up or disconnected (pull-up by default), and the module enters flight mode when the pin is pulled down.

- Software control:

Run the AT+CFUN=4 command to enter flight mode.

### Exiting mode

- Hardware control:

The module is in normal mode when the pin is pulled up.

- Software control:

Run the AT+CFUN=1 command to exit flight mode.

## 4.15 Sleep Mode

### Background information

The sleep mode is also called the low-power mode. To minimize battery loss, the module can be set to enter the sleep mode when it is idle to save power. The module in the sleep mode can be waked up to the normal operation mode.

### Entering mode

AT commands and WAKEUP_IN signal are used to set the module into sleep mode and wake-up mode.

- Hardware control:

Send AT+GTLPMMODE=1,x to set the effective level of the WAKEUP_IN signal that sets the module into sleep mode and wake-up mode. Command is effective after restarting module.

  - X=0: Level wake-up. The module enters wakeup mode when pulling down the WAKEUP_IN pin and enters sleep mode at high level.
  - X=1: Level wake-up. The module enters wakeup mode when pulling up the WAKEUP_IN pin and enters sleep mode at low level.

WAKEUP_IN pin is pulled down by default.

- Software control:

Use the ATS24 command to make the module sleep, and the wake-up duration depends on the <value> in the ats24 = [<value>] command. Send AT command ats24= 2, the module will enter sleep mode after 2s, and the setting will not be saved after power failure of the module.

The system supports automatic sleep. The time from standby to sleep can be configured through software.

The module can be waked up by sending an AT command through the main serial port.

# 5 Antenna Interfaces

## 5.1 Antenna Interface

The antenna interface configuration of L716 series product is the same. During laboratory test, please select the correct antenna according to the tested frequency band for connection. For other support, please contact FAE of Fibocom.

## 5.2 RF Band

Table 14. RF band and frequency range

| Mode | Band | Transmit (MHz) | Receive (MHz) |
|---|---|---|---|
| GSM | DCS 1800 | 1710~1785 | 1805~1880 |
| | DCS 1900 | 1850~1910 | 1930~1990 |
| | GSM 850 | 824~849 | 869~894 |
| | GSM 900 | 880~915 | 925~960 |
| WCDMA | Band 1 | 1920~1980 | 2110~2170 |
| | Band 2 | 1852~1908 | 1932~1988 |
| | Band 4 | 1712~1753 | 2112~2153 |
| | Band 5 | 824~849 | 869~894 |
| | Band 8 | 880~915 | 925~960 |
| LTE FDD/LTE TDD | Band 1 | 1920~1980 | 2110~2170 |
| | Band 2 | 1850~1910 | 1930~1990 |
| | Band 3 | 1710~1785 | 1805~1880 |
| | Band 4 | 1710~1755 | 2110~2155 |
| | Band 5 | 824~849 | 869~894 |

| Mode | Band | Transmit (MHz) | Receive (MHz) |
|---|---|---|---|
| | Band 7 | 2500~2570 | 2620~2690 |
| | Band 8 | 880~915 | 925~960 |
| | Band 28 | 703~748 | 758~803 |
| | Band 66 | 1710~1780 | 2110~2180 |
| | Band 38 | 2570~2620 | 2570~2620 |
| | Band 40 | 2300~2400 | 2300~2400 |

# 5.3 RF Antenna

## 5.3.1 Antenna Introduction

### Antenna interface

The module only has RF antenna pad. The RF cable can be connected to the antenna after PCB design of the RF signal line.

### Antenna classification

According to the transceiver function, it mainly includes:

- Main antenna: transmits and receives RF signals, which is divided into internal and external antennas.
- Diversity antenna: generally, it only receives signals and does not send them to obtain diversity gain.

The antenna is a sensitive device and is easily affected by the external environment. For example, the position of the antenna, the space it occupies, and the surrounding ground all may affect antenna performance. In addition, the RF cable connecting the antenna, and the position of the fixed antenna also may affect antenna performance.

Add a shield cover on the DCDC device or keep DCDC device away from the module antenna,

Avoid RF signal interference of DCDC components, resulting in the output of the DCDC beyond specifications ripple.

## 5.3.2 Antenna Reference Design

Add a π-type circuit (two parallel-component- grounded pins are connected directly to the main GND) between the module and antenna connector (or feeding point) for antenna debugging. Two parallel components are directly connected across the RF trace, and the branch must not be pulled out.

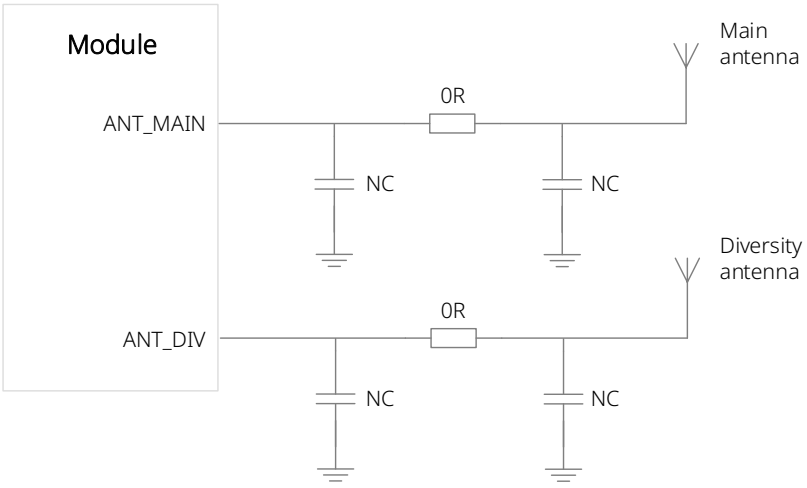



Figure 23. Antenna interface peripheral circuit

## 5.3.3 Impedance Design Principle

For modules that do not have a RF connector, customers need to route a RF trace to connect to the antenna feeding point or connector. It is recommended to use a microstrip line. The shorter the better. The insertion loss should be controlled less than 0.2dB; and impedance should be controlled within 50Ω.

In general, the impedance of the RF signal line is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB is usually in two ways: microstrip line and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip route and coplanar waveguide

when the impedance line is at 50Ω.

- Complete structure of microstrip line

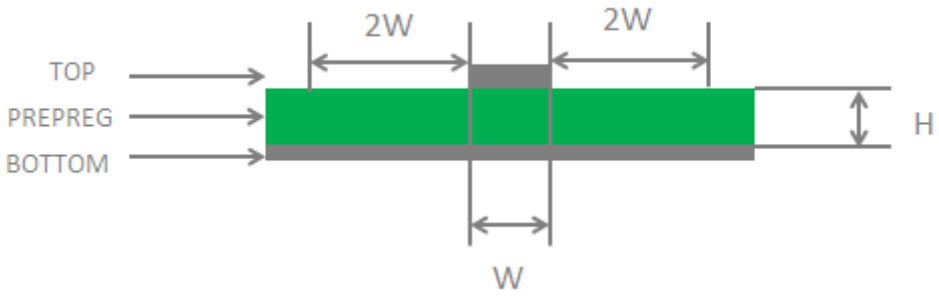



Figure 24. Two-layer PCB microstrip line structure

- Complete structure of coplanar waveguide

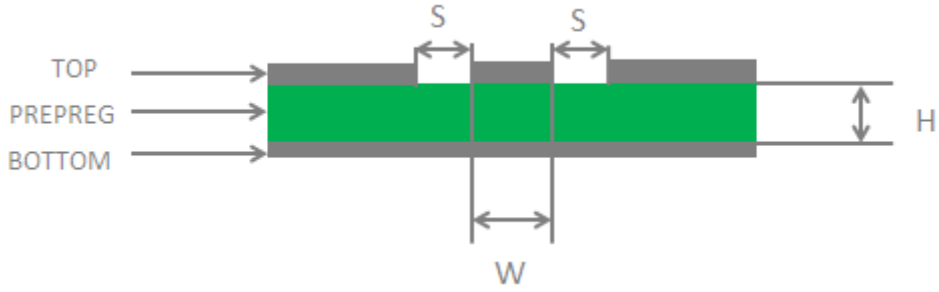



Figure 25. Two-layer PCB coplanar waveguide structure

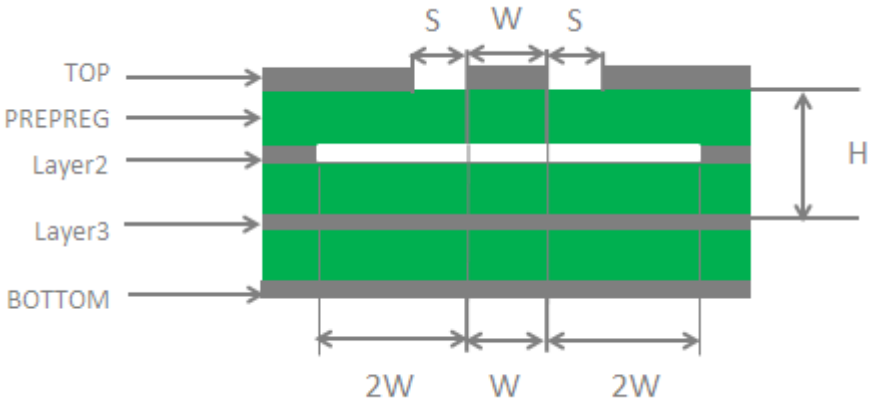



Figure 26. Four-layer PCB coplanar waveguide structure (refer to ground layer 3)

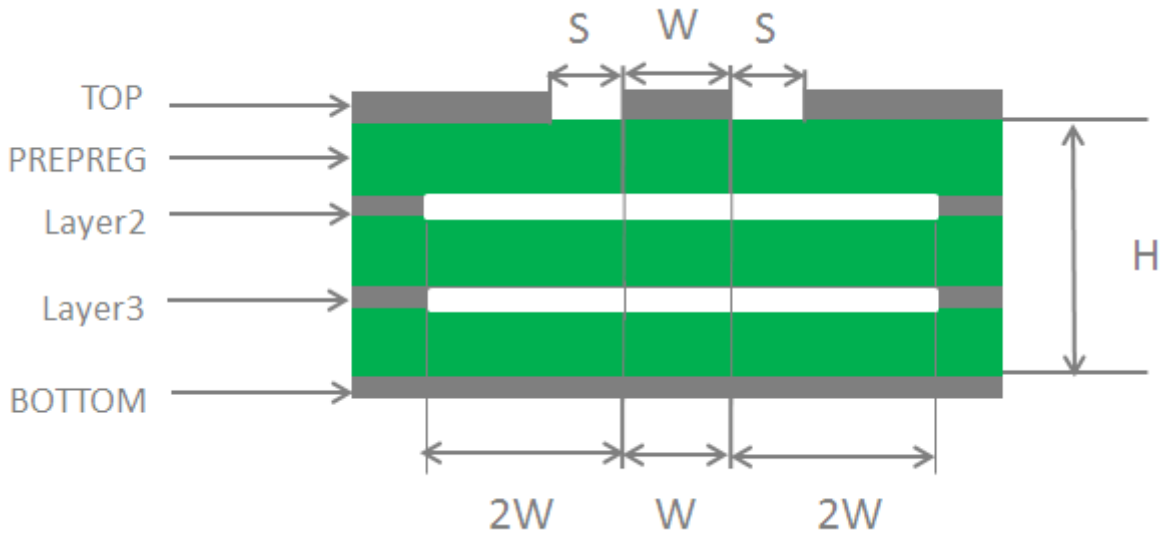



Figure 27. Four-layer PCB coplanar waveguide structure (refer to ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid right-angle routing. The recommended routing angle is 135 degrees.
- Attention should be paid to the establishment of the connection component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal line should be kept intact; adding a certain amount of ground holes around the signal and the reference ground can improve the RF performance; the distance between the ground hole and the signal line should be at least 2 times the line width (2 x W).
- The equivalent capacitance of TVS shall be less than 0.5pF.

### 5.3.4 Factors Affecting Antenna Performance

1. What affects transmitting performance?

- Shell: As the internal antenna is sensitive to the nearby medium, so the design of shell is closely related to antenna performance.
- Poor speaker layout will affect antenna performance.
- Poor battery layout will affect antenna performance.

2. What affects receiving performance?

- If both the conductive performance of module and the radiated power of antenna meet requirement, then low RX sensitivity may be caused by main board design issue.
- Poor coupling sensitivity is caused by poor circuit design of LCD, LDO, and DC/DC.
- Device receiving performance is affected by VCXO or TXVCO harmonic of 19.2MHZ, 26MHZ, and 38.4MHZ systems.
- Poor coupling sensitivity is caused by SIM card clock.
- Poor FPC layout affects the receiving performance of the device.

3. What affects EMC performance?

- Poor FPC layout affect EMC performance of the device.
- The metal element may absorb the antenna radiated power and produce a certain amount of secondary radiation, and coupling frequency is associated with the size of metal parts. Therefore, this kind of component should have a good grounding to eliminate or reduce secondary radiation.

### 5.3.5 Antenna Design Requirements

The design requirements of antenna are shown in the following table:

Table 15. Antenna design requirements

| Antenna type | Design requirement |
|---|---|
| GSM/UMTS/LTE | VSWR ≤ 2 |
| | Efficiency > 30% |
| | Gain: 1dBi |
| | Maximum input power: 50W |
| | Input impedance: 50 Ω |
| | Polarization: Vertical |
| | Line loss (insertion loss):<br>< 1Db: LB（< 1GHz）<br>< 1.5Db: MB（1~2.3GHz）<br>< 2Db: HB（> 2.3GHz） |

# 6 Electrical Characteristics

## 6.1 Logic Level

Table 16. Electrical indicator

| Indicator | | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| Logic level | Digital input high level | 1.17 | - - | 1.89 | V |
| | Digital input low level | –0.3 | - - | 0.63 | V |
| | Digital output high level | 1.35 | - - | - - | V |
| | Digital output low level | - - | - - | 0.45 | V |

## 6.2 Power consumption

The power consumption measurement is closely related to the working state of the module. The test conditions are 25 ℃ ambient temperature, 3.8V supply voltage, and the module USB default is Device mode

Table 17. Power consumption

| Parameter | Standard | Test Condition (VBAT=3.8V) | Power Consumption (mA) |
|---|---|---|---|
| $I_{off}$ | Shutdown leakage current | Power on without turn module on<br>PWRKEY control module shutdown<br>AT control module shutdown | 0.011 |
| $I_{sleep}$ | Flight and sleep mode | AT+CFUN=4<br>ATS24=3 | 1.2 |

| Parameter | Standard | Test Condition (VBAT=3.8V) | Power Consumption (mA) |
|---|---|---|---|
| $I_{IDLE}$ | GSM | MFRMS 2 (USB Sleep) | 4.8 |
| | | MFRMS 5 (USB Sleep) | 3.4 |
| | | MFRMS 9 (USB Sleep) | 2.8 |
| | WCDMA | DRX=6 (USB Sleep) | 2.8 |
| | | DRX=7 (USB Sleep) | 2 |
| | | DRX=8 (USB Sleep) | 1.4 |
| | | DRX=9 (USB Sleep) | 1.2 |
| | LTE FDD | Paging cycle #64 frames (USB Sleep) | 3.7 |
| | | Paging cycle #128 frames (USB Sleep) | 2.7 |
| | | Paging cycle #256 frames (USB Sleep) | 2.7 |
| | LTE TDD | Paging cycle #64 frames (USB Sleep) | 4 |
| | | Paging cycle #128 frames (USB Sleep) | 2.7 |
| | | Paging cycle #256 frames (USB Sleep) | 2.7 |
| | GSM | MFRMS=5 (USB sleep) | 48 |
| | | MFRMS=5 (USB wakeup) | 58 |
| | WCDMA | DRX=8 (USB sleep) | 47 |
| | | DRX=8 (USB wakeup) | 58 |
| | LTE FDD | Paging cycle #256 frames (USB sleep) | 47 |
| | | Paging cycle #256 frames (USB wakeup) | 57 |
| | LTE TDD | Paging cycle #256 frames (USB sleep) | 47 |
| | | Paging cycle #256 frames (USB wakeup) | 58 |

| Parameter | Standard | Test Condition (VBAT=3.8V) | Power Consumption (mA) |
|---|---|---|---|
| $I_{GSM-RMS}$ | GSM | EGSM900 PCL5 | 260 |
| | | DCS1800 PCL0 | 200 |
| | | DCS1900 PCL0 | TBD |
| | | GSM850 PCL5 | 260 |
| $I_{GPRS-RMS}$ CS4 | GPRS | GPRS Data transfer GSM900; PCL=5; 1Rx/4Tx | 600 |
| | | GPRS Data transfer GSM850; PCL=5; 1Rx/4Tx | 600 |
| | | GPRS Data transfer DCS1800; PCL=0; 1Rx/4Tx | 400 |
| | | GPRS Data transfer DCS1900; PCL=0; 1Rx/4Tx | TBD |
| $I_{EGPRS-RMS}$ MCS9 | EDGE | EDGE Data transfer GSM900; PCL=8; 1Rx/4Tx | 600 |
| | | EDGE Data transfer GSM850; PCL=8; 1Rx/4Tx | 500 |
| | | EDGE Data transfer DCS1800; PCL=2; 1Rx/4Tx | 500 |
| | | EDGE Data transfer DCS1900; PCL=2; 1Rx/4Tx | TBD |
| $I_{WCDMA-RMS}$ | WCDMA | WCDMA Data transfer Band 1 @+23.5dBm | 680 |
| | | WCDMA Data transfer Band 2 @+23.5dBm | TBD |
| | | WCDMA Data transfer Band 3 @+23.5dBm | TBD |

| Parameter | Standard | Test Condition (VBAT=3.8V) | Power Consumption (mA) |
|---|---|---|---|
| | | WCDMA Data transfer Band 4 @+23.5dBm | TBD |
| | | WCDMA Data transfer Band 5 @+23.5dBm | 650 |
| | | WCDMA Data transfer Band 8 @+23.5dBm | 650 |
| $I_{LTE-RMS}$ | LTE FDD<br>LTE TDD | LTE FDD Data transfer Band 1 @+23dBm | 750 |
| | | LTE FDD Data transfer Band 2 @+23dBm | TBD |
| | | LTE FDD Data transfer Band 3 @+23dBm | 750 |
| | | LTE FDD Data transfer Band 4 @+23dBm | TBD |
| | | LTE FDD Data transfer Band 5 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 7 @+23dBm | 780 |
| | | LTE FDD Data transfer Band 8 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 28 @+23dBm | 700 |
| | | LTE FDD Data transfer Band 66 @+23dBm | TBD |
| | | LTE TDD Data transfer Band 38 @+23dBm | 430 |
| | | LTE TDD Data transfer Band 40 @+23dBm | 430 |

The above power consumption data are measured average values, and the floating range within 10% is normal.

## 6.3 Transmitting power

The maximum transmit power refers to the power at the antenna pin at the ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when

designing, so as to avoid excessive insertion loss affecting the TRP index. The maximum transmission power of L716 series module is as follows.

Table 18. Transmitting power of each band

| Mode | Band | Transmitting Power (dBm) | Description |
|---|---|---|---|
| GSM | DCS 1800 | 29.5±1.5 | - - |
| | DCS 1900 | 29.5±1.5 | - - |
| | GSM 850 | 29.5±1.5 | - - |
| | GSM 900 | 29.5±1.5 | - - |
| WCDMA | Band 1 | 23.5±2 | - - |
| | Band 2 | 23.5±2 | - - |
| | Band 3 | 23.5±2 | - - |
| | Band 4 | 23.5±2 | - - |
| | Band 5 | 23.5±2 | - - |
| | Band 8 | 23.5±2 | - - |
| LTE FDD | Band 1 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 2 | 23.5±2 | 10MHz Bandwidth，1 RB |
| | Band 3 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 4 | 23.5±2 | 10MHz Bandwidth，1 RB |
| | Band 5 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 7 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 8 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 28 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 66 | 23.5±2 | 10MHz Bandwidth，1 RB |

| Mode | Band | Transmitting Power (dBm) | Description |
|---|---|---|---|
| LTE TDD | Band 38 | 23.5±2 | 10 MHz Bandwidth, 1 RB |
| | Band 40 | 23.5±2 | 10 MHz Bandwidth, 1 RB |

## 6.4 Receiving sensitivity

The receiving sensitivity refers to the sensitivity of the antenna pin at the ambient temperature of 25℃. The user should fully consider the insertion loss on the RF path when designing, so as to avoid the excessive insertion loss affecting the TIS index.

Table 19. Receiving sensitivity of each band

| Mode | Band | Sensitivity (dBm) | Description | 3GPP protocol |
|---|---|---|---|---|
| GSM | GSM 850 | –108 | BER < 2.43% | -102 |
| | GSM 900 | –108 | BER < 2.43% | -102 |
| | DCS 1800 | –105 | BER < 2.43% | -102 |
| | DCS 1900 | TBD | BER < 2.43% | -102 |
| WCDMA | Band 1 | –109 | BER < 0.1% | -106 |
| | Band 2 | TBD | BER < 0.1% | -104 |
| | Band 3 | TBD | BER < 0.1% | -103 |
| | Band 4 | TBD | BER < 0.1% | -106 |
| | Band 5 | –109 | BER < 0.1% | -104 |
| | Band 8 | –109.5 | BER < 0.1% | -103 |
| LTE FDD | Band 1 | –100.5 | 10 MHz Bandwidth | -96.3 |
| | Band 2 | TBD | 10MHz Bandwidth | -94.3 |

| Mode | Band | Sensitivity (dBm) | Description | 3GPP protocol |
|---|---|---|---|---|
| | Band 3 | –100.5 | 10 MHz Bandwidth | -93.3 |
| | Band 4 | TBD | 10MHz Bandwidth | -96.3 |
| | Band 5 | –99.5 | 10 MHz Bandwidth | -94.3 |
| | Band 7 | –100 | 10 MHz Bandwidth | -94.3 |
| | Band 8 | –101 | 10 MHz Bandwidth | -93.3 |
| | Band 28 | –100 | 10 MHz Bandwidth | -94.8 |
| | Band 66 | TBD | 10MHz Bandwidth | -95.8 |
| | Band 38 | –99 | 10 MHz Bandwidth | -96.3 |
| | Band 40 | –99.5 | 10 MHz Bandwidth | -96.3 |

The sensitivity in the above table is the result of the test using the main and diversity dual antenna. If only the main antenna is used (without diversity), the sensitivity of each LTE frequency band will be reduced by about 3dB accordingly.

## 6.5 ESD

The module is ESD sensitive component with weak ability to resist static electricity. So ESD precautions that apply to ESD sensitive components should be strictly followed. Proper ESD procedures must be applied throughout the processing, delivery, assembly and operation.

The allowable ESD discharge range of the module is as follows (temperature: 25 °C, relative humidity: 40%):

Table 20. ESD indicator

| Test Point | Air Discharge (kV) | Contact Discharge (kV) |
|---|---|---|

| | | |
|---|---|---|
| Antenna ground | ±15 | ±8 |
| Antenna core | - - | ±8 |

1. The data is based on the test of ADP-L716-CN-10 evaluation board.
2. ESD performance is strongly related to PCB design, and special attention should be paid to the protection of control signals.
3. During the design of the whole machine, the GND of the module and the main GND of the customer backplane maintain sufficient connectivity to ensure that ESD is discharged in the shortest path.

## 6.6 Reliability

The reliability test shall be conducted according to the industrial reliability test, and the following are the standard test items and test conditions.

Table 21. Industrial reliability test

| Test Project | Test Condition |
|---|---|
| High temperature aging | 85℃, 168H/504H/1008H |
| High temperature and humidity | 85℃, 85%RH, 168H/504H/1008H |
| Corner test | High and low temperature, high and low humidity, high and low voltage, six groups of combinations, each combination running test for 24 hours. |
| Temperature shock | 90/-45℃, 200C |
| Random vibration | Frequency range: (200～2000)Hz, PSD = 0.04$g^2$/Hz, 1 hour for each X/Y/Z axis. |

| Test Project | Test Condition |
| --- | --- |
| Monomer Drop | 1m, Six sides and two wheels. |
| Mechanical collision | Peak acceleration: 180m/s$^2$;<br>Pulse duration: 6ms;<br>Number of collisions: 1000 |
| Low temperature starting | -40℃; 30 minutes Off/ 5 minutes Idle; 3 days |
| Condensation Test | 3 days (3 cycles):<br>• First and second cycle with cold cycle;<br>• Third cycle without cold cycle |
| Temperature cycling | 85º C/ – 40º C; 10º C/min; 10min; 240cycles |
| Sinusoidal vibration | Amplitude: 3.0G peak to peak;<br>Frequency: 5 - 500Hz;<br>Sweep frequency: 0.5 Octave/min, linear;<br>2H per axis; |
| Salt spray test | Neutral salt spray, 48H |

## 6.7 Thermal Design

### 6.7.1 Main Board

Main board design suggestions:

Increase PCB size, and keep the module away from other heat source devices.

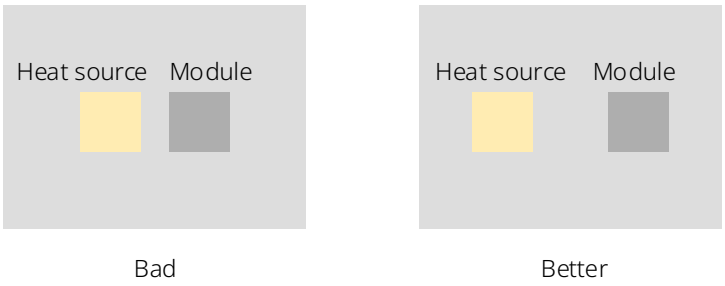



Figure 28. PCB layout

Increase PCB layers and the copper area at each layer.

Add adequate paths under and near the module. Plated holes boast better cooling effect than buried holes and blind holes. Vertically stacked paths boast better cooling effect than staggered paths.

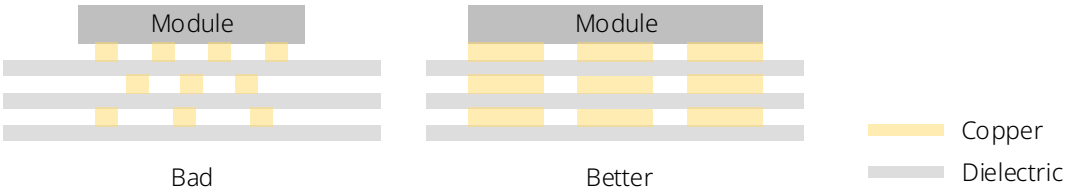



Figure 29. PCB stackup

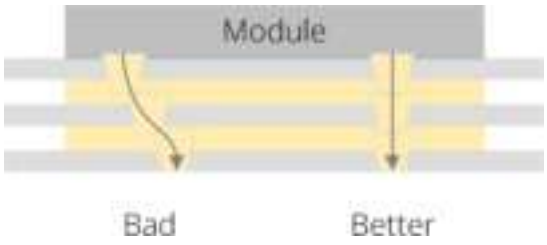



Figure 30. PCB drill hole

## 6.7.2 Product Structure

Recommendations for product structure:

Reduce the distance between module and heat sink and shell. Thermal conductive material thickness should not exceed 3 mm.

The thermal conduction path is shown in the following figure.

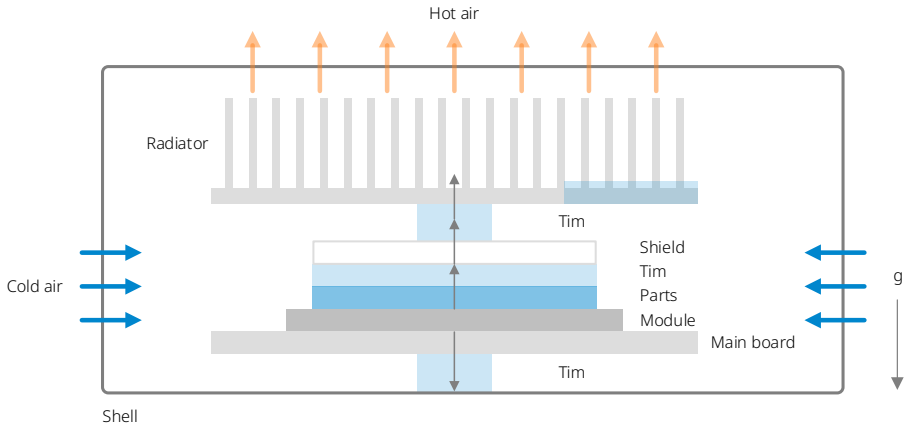



Figure 31. Heat conduction path

Use shell material with better thermal conductivity to facilitate cooling. Thermal conductivity sequence: Al > Fe > Plastic

Place the heat sink above the module.

Allow direct contact between the heat sink and thermal conductive material on the module if the heat sink can be exposed to the product surface.

Consider convection if the product has cooling holes.

# 7 Structural Specifications

## 7.1 Physical Appearance

The appearance of the L716-LA series module is shown in the following figures.


Figure 32. Top view

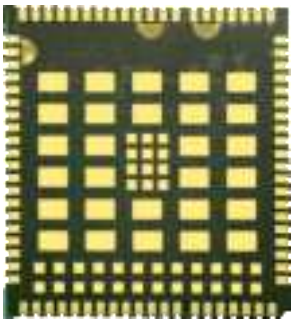


Figure 33 Bottom view

## 7.2 Physical Indicator

The structural size of the module is shown in the following figure.

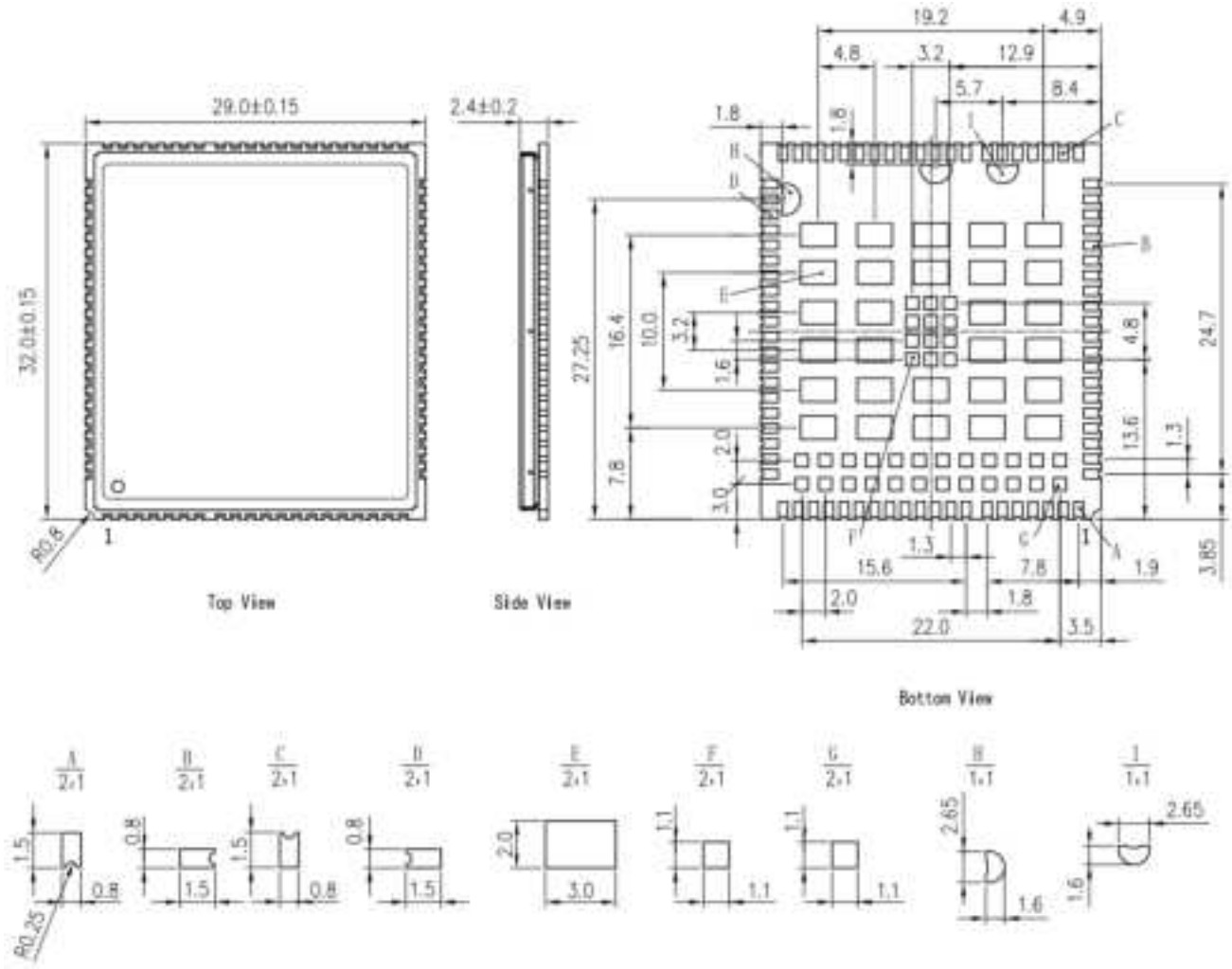



Figure 34. structure size (unit: mm)

## 7.3 PCB

The following figure shows the PCB package size of the module, and the user can design the PCB package. At the same time, Fibocom also provides users with the designed "Fibocom_L716_V3T_Package", which can be found in the document

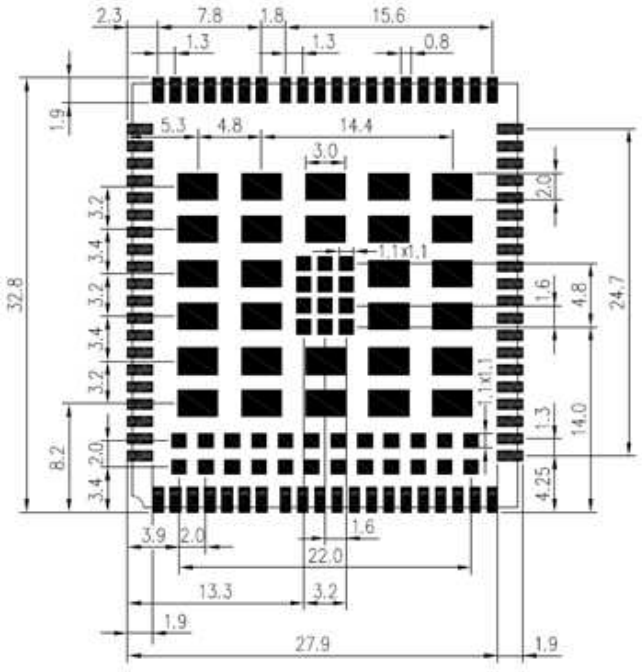



Figure 1. PCB Package（unit: mm）

# 8 Storage Manufacture Packaging

## 8.1 Storage

Modules are shipped in vacuum sealed bags. The module is humidity sensitive class 3 (MSL 3) and is stored under the following conditions:

1. Storage conditions (recommended): temperature 23℃±5℃, relative humidity RH 35%~70%;

2. Storage life (sealed vacuum package): 12 months under recommended storage conditions;

3. The module has a shop life of 168 hours after unpacking at shop conditions of 23±5°C and less than 60% relative humidity, where it can be directly used for reflow production or other high temperature operations. Otherwise, it is necessary to store the module in an environment with a relative humidity of less than 10%(e.g., a moisture-proof cabinet) to keep the module dry;

4. If the module is under the following conditions, it is necessary to pre-bake the module to prevent PCB blistering, cracking and delamination after the module is wetted and then soldered at high temperature:

- Storage temperature and humidity do not meet the recommended storage conditions;
- Failure to complete production or storage in accordance with clause 3 above after unpacking of the module;
- Air leakage in vacuum packaging and bulk materials;
- Before module repair.

5. Baking of modules:

- Baking at 120 ±5 °C for 8 hours;

- The module for the second baking shall be welded within 24 hours after baking, otherwise it shall be stored in the drying oven

## 8.2 SMT

Module steel mesh design, solder paste and furnace temperature control please refer to *FIBOCOM L716 SMT Application Design Notes*

## 8.3 Packaging

The module adopts tape packaging, so that the storage, transportation and the usage of the module can be protected to the greatest extent. Please read the packing instructions carefully to avoid damaging the product.

The product package is divided into three layers:

- Outer packaging

Hard card box

- Vacuum packaging

Anti-static sealed vacuum bag

- Inner packaging

Tape packaging

The module is a precise electronic product, and may be permanently damaged if you do not take correct ESD measures.

The module is moisture sensitive, please avoid moistening the product to prevent permanent damage.

Each roll is packed with 200 pcs, each box is packed with 1 rolls, and each hard carton box is packed with 4 boxes.

## Packaging process

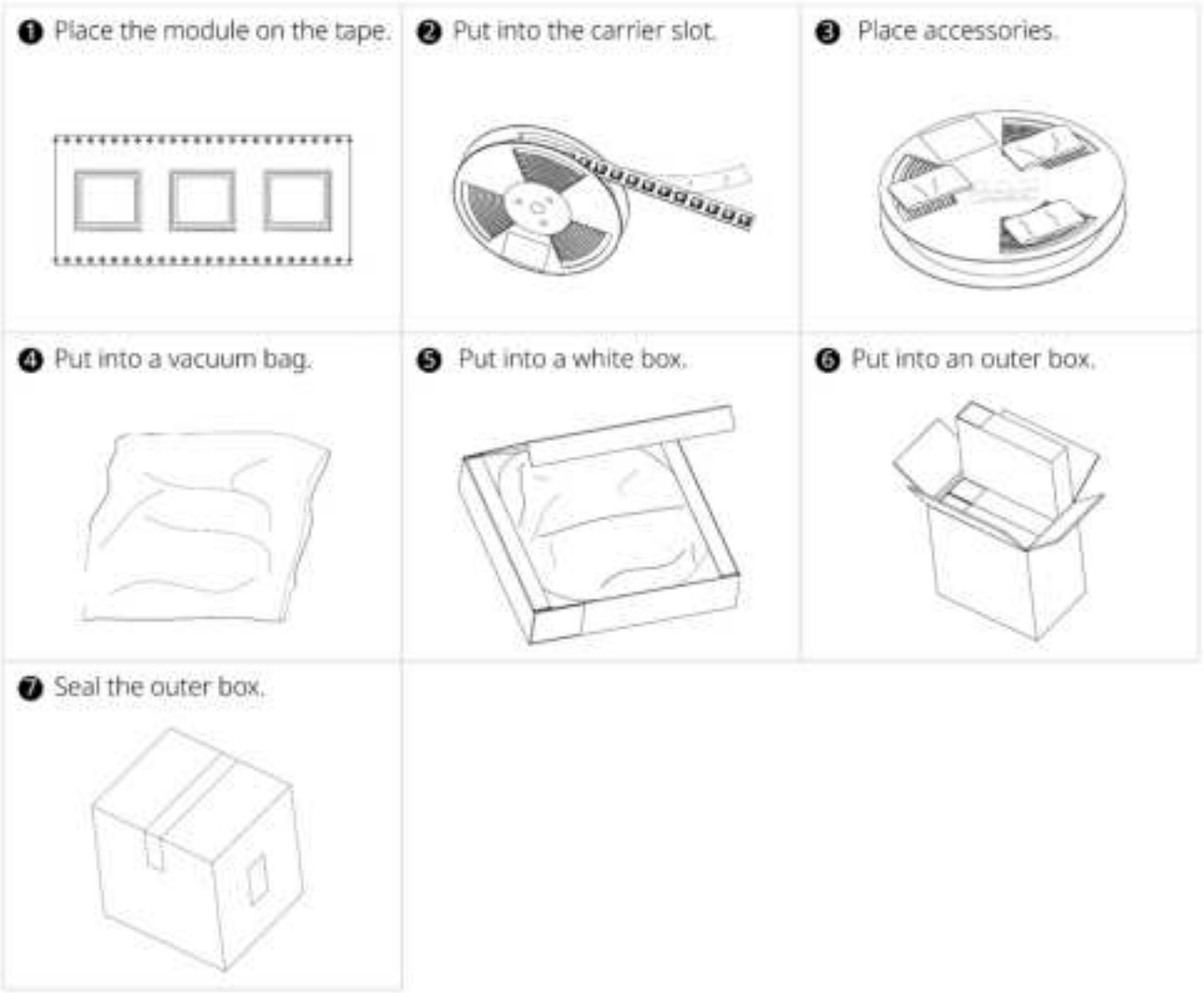



Figure 35. Tape packaging process

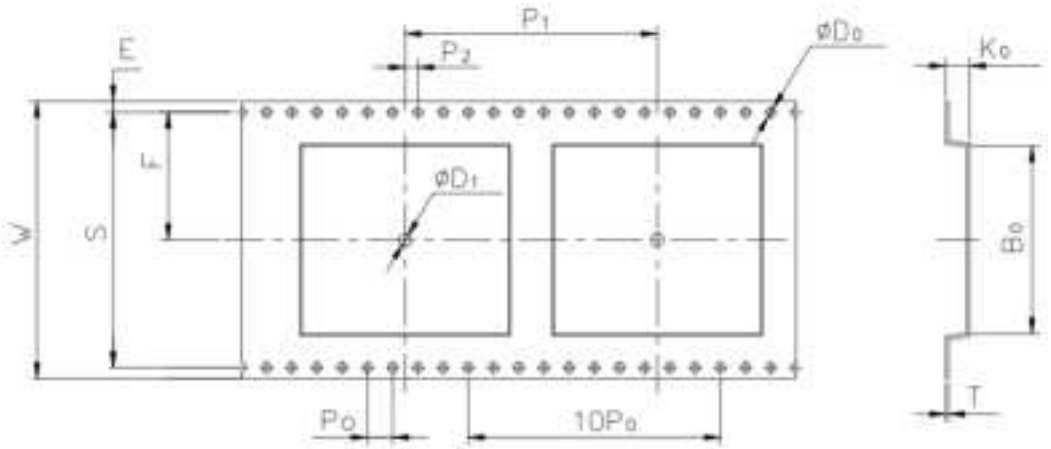
1. Place each module into the carrier slot frame in the same direction as specified, and sealing the heat-sealing film.
2. Place the specified number of module tapes as shown in the figure.
3. Before vacuumizing, place 3 bags of desiccant and a humidity card above the tape, and paste the label of the carrier tape.
4. Put the whole into a vacuum bag and vacuumizing.
5. Put the vacuum electrostatic bag into a white box, only one electrostatic

bag is put into a single white box. Buckle the white box and paste the label.

6. Seal the bottom of the outer box, and put the 4 PCS white boxes into the outer box as shown in the figure.
7. Seal the top of the outer box in an I-shape, paste an outer box label in the rectangular frame on the side, and paste a box sealing label on the top and bottom of the outer box respectively.

## Tape size

- Tape size:




| ITEM | Ao | Bo | Ko | Po | P1 | P2 | T |
|---|---|---|---|---|---|---|---|
| DIN | 32.8±0.1 | 29.8±0.1 | 5.8±0.1 | 4.0±0.1 | 40.0±0.1 | 2.0±0.15 | 0.5±0.05 |
| ITEM | E | F | Do | D1 | W | 10Po | S |
| DIN | 1.75±0.1 | 20.2±0.3 | 1.50 | 0.0 | 44.0 | 40.0±0.2 | 40.4±0.1 |

Figure 36. Carrier tape size

- Reel size:

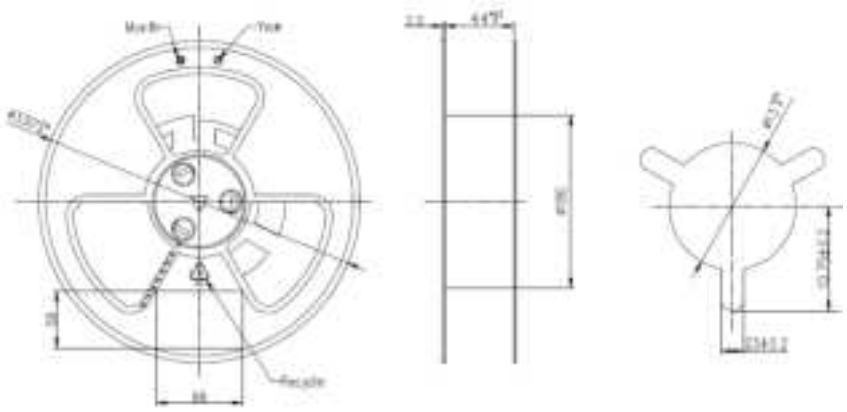


Figure 37. Reel size

# Appendix A: Reference Documents

The design of the product complies with the following documents:

| Type | Document |
|---|---|
| Software | *Fibocom_L716_Series_AT_Commands_User_Manual* |
| Hardware | *Fibocom_L716_V3T_Package* |
| | *Fibocom_L716_3D Module Diagram* |
| | *Fibocom_L716_V3T_Series_Reference_design* |
| | *Fibocom_L716_V3T_Customer SCH&PCB Design Checklist* |
| | *Fibocom_L716_ Compatibility Design Guide* |
| Development kit | *Fibocom_L716 Series Evaluation Board User Guide* |
| | *Fibocom_EVB-LGA-F01_User Guide* |
| Other | *Fibocom_L716_SMT Application Design Notes* |
| | *Fibocom_ Thermal Design Guide* |

# Appendix B: Acronyms and Abbreviations

| Abbreviation | Full Name |
|---|---|
| ADC | Analog to Digital Converter |
| ADP | Application Development Platform |
| BT | Bluetooth |
| CPE | Customer Premises Equipment |
| DCDC | Direct Current to Direct Current |
| DDR | Double Data Rate |
| EDGE | Enhanced Data rate for GSM Evolution |
| ESD | Electronic Static Discharge |
| FDD | Frequency Division Duplexing |
| FEM | Front End Module |
| GPRS | General Packet Radio Service |
| GSM | Global Standard for Mobile Communications |
| LDO | Low Dropout Regulator |
| LTE | Long Term Evolution |
| MIFI | Mobile WIFI |
| I2C | Inter Integrated Circuit |
| PCB | Printed Circuit Board |
| PCM | Pulse Code Modulation |
| PMU | Power Manager Unit |

| | |
|---|---|
| RF | Radio Frequency |
| RTC | Real Time Clock |
| RMII | Reduced Media Independent Interface |
| SDIO | Secure Digital Input and Output |
| SIM | Subscriber Identification Module |
| SPI | Serial Peripheral Interface |
| TDD | Time Division Duplexing |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |
| WCDMA | Wideband Code Division Multiple Access |
| WLAN | Wireless Local Area Network |

# Appendix C: Certification Statement

## Statements

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device. And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time averaging duty factor, antenna gain, and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3. A label with the following statements must be attached to the host end product: This device contains FCC ID: ZMOL716LA

4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

| Antenna Type | Band | FCC Max Antenna Gain（dBi) |
|---|---|---|
| Dipole | GSM850 | 1.32 |
| | GSM1900 | 1.92 |
| | WCDMA BII | 1.92 |
| | WCDMA BIV | 2.86 |
| | WCDMA BV | 1.32 |
| | LTE B2 | 1.92 |
| | LTE B4 | 2.86 |

| | | |
|---|---|---|
| | LTE B5 | 1.32 |
| | LTE B7 | 1.07 |
| | LTE B38 | 0.93 |
| | LTE B66 | 3.53 |

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For this device, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093.

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations. For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs: A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: ZMOL716LA" or "Contains FCC ID:

ZMOL716LA" must be used.

The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID. The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes, or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference,

(2) This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment. To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.