Functional Description of Wireless Headset

1.0 Introduction

The Wireless Headset consists of three functional entities which are described as the Base, Head-piece and Charger. The Base and the Head-piece are basically transceivers that provide a short-range wireless duplex audio link between a cellular phone and the Head-piece. The Head-piece basically contains a microphone and a speaker that replace the build-in microphone and speaker of the cellular phone in a wireless fashion. Detail operation instruction can be found in Appendix B.

2.0 Theory of operation

The Base and Head-piece communicate in frequency-division-duplex (FDD) fashion to establish a two-way voice link between the base and head-piece. The up-link and down-link frequency bands are chosen between 300Mhz to 450Mhz. The bands are chosen to be 40Mhz apart minimally and the channel band-width is minimum 200Khz. The RF circuits of the Base and Head-piece are identical and the following description of the receive and transmit circuits apply to both.

Refer to figure 1 which is the functional block diagram of the circuits. In the transmit circuit, a voltage control oscillator (VCO) and a phase lock loop is used to synthesize the transmit frequency. This synthesizer is programmed by the microprocessor and they both share a common 6MHz reference oscillator. The VCO is frequency modulated by the incoming audio source and also by the microprocessor. The synthesizer feeds its output to two stages of buffers and is low-pass filtered by a series of LC. The signal is then output to the transmit antenna. A helical antenna is used in the Base and a monopole antenna is used in the Head-piece. In the receive circuit, the same type of synthesizer as used in the transmit circuit is employed to create the local oscillator needed for ordinary super-heterodyne receiver. Signal comes from the receive antenna which is then fed to SAW band-pass filter. The filtered signal then goes through the RF amplifier and then to the mixer which down converts the RF signal to an intermediate frequency. The IF is 10.7Mhz and this IF signal is directly amplified and frequency-demodulated. The audio signal is then fed to an amplifier and then output to the audio destination.

3.0 Circuit schematic description

BASE circuit :

Refer to appendix A, circuit schematic with title ‘MIC BASE’. The microprocessor is IC3 and the RX and TX phase lock loops are contained in IC2. The 6Mhz reference oscillator is a crystal oscillator implemented with the internal circuitry of the microprocessor. The RX VCO contains Q5 and varactor diode D2. The TX VCO contains Q4 and varactor diode D1. The transmit buffers is composed of Q2 and Q3. Q7 is the RF amplifier and the MIXER, IF AMPLIFIER and FM-DEMODULATOR are all contained in IC4. The audio source and audio destination is the cellular phone’s 2.5mm socket which is the speaker output and microphone input. Q6 provides a voltage indicator which switches collector output to high whenever battery voltage drops below 3.0 volts with tolerance of -0.2 volt. At this level the microprocessor will switch off all circuitry. IC1 is a low-drop voltage regulator which outputs 2.5volt with 0.2volt threshold.

HEAD-PIECE circuit:

Refer to appendix A, circuit schematic with title ‘MIC HEADSET’. The microprocessor is IC3 and the RX and TX phase lock loops are contained in IC2. The 6Mhz reference oscillator is a crystal oscillator implemented with the internal circuitry of the microprocessor. The RX VCO contains Q5 and varactor diode D2. The TX VCO contains Q4 and varactor diode D1. The transmit buffers is composed of Q2 and Q3. Q7 is the RF amplifier and the MIXER, IF AMPLIFIER and FM-DEMODULATOR are all contained in IC5. The audio source is the amplified microphone signal, and the audio destination is the audio amplifier IC6 and speaker SP1. Q6 provides a voltage indicator which switches collector output to high whenever battery voltage drops below 3.0 volts with tolerance of -0.2

volt. At this level the microprocessor will switch off all circuitry. IC1 is a low-drop voltage regulator which outputs 2.5volt at 0.2volt threshold.

4.0 Specifications

Transmission:	BASE	HEAD-PIECE	UNIT
Frequency:	300<bf<450	bf+40	MHz
Frequency stability:	+/-50	+/-50	ppm
(at extreme temperature)			
Channels:	5	5	
Channel separation:	>200	>200	KHz
Terminal output power	-35	-35	dbm
Reception:			
Frequency:	hf-40	300<hf<450	MHz
Frequency stability:	+/-50	+/-50	ppm
(at extreme temperature)			
Channels:	5	5	
Channel separation:	>200	>200	KHz
Receiver type:	----- super-heterodyne ------		
Intermediate frequency:	10.7	10.7	MHz
General:			
Working voltage:	3.0-6.0	3.0-6.0	volt
Current consumption:	26	29	ma
Battery voltage:			
(fully charged)	4.2	4.2	volt
(stop-working)	3.0	3.0	volt

Software:
Version number is 3.0.

FREQUENCY TABLE (in MHz)

	BASE		HEAD-PIECE	
CHANNEL	TX	RX	TX	RX
1	397.6	447.2	447.2	397.6
2	397.9	447.5	447.5	397.9
3	398.2	447.8	447.8	398.2
4	398.5	448.1	448.1	398.5
5	398.8	448.4	448.4	398.8

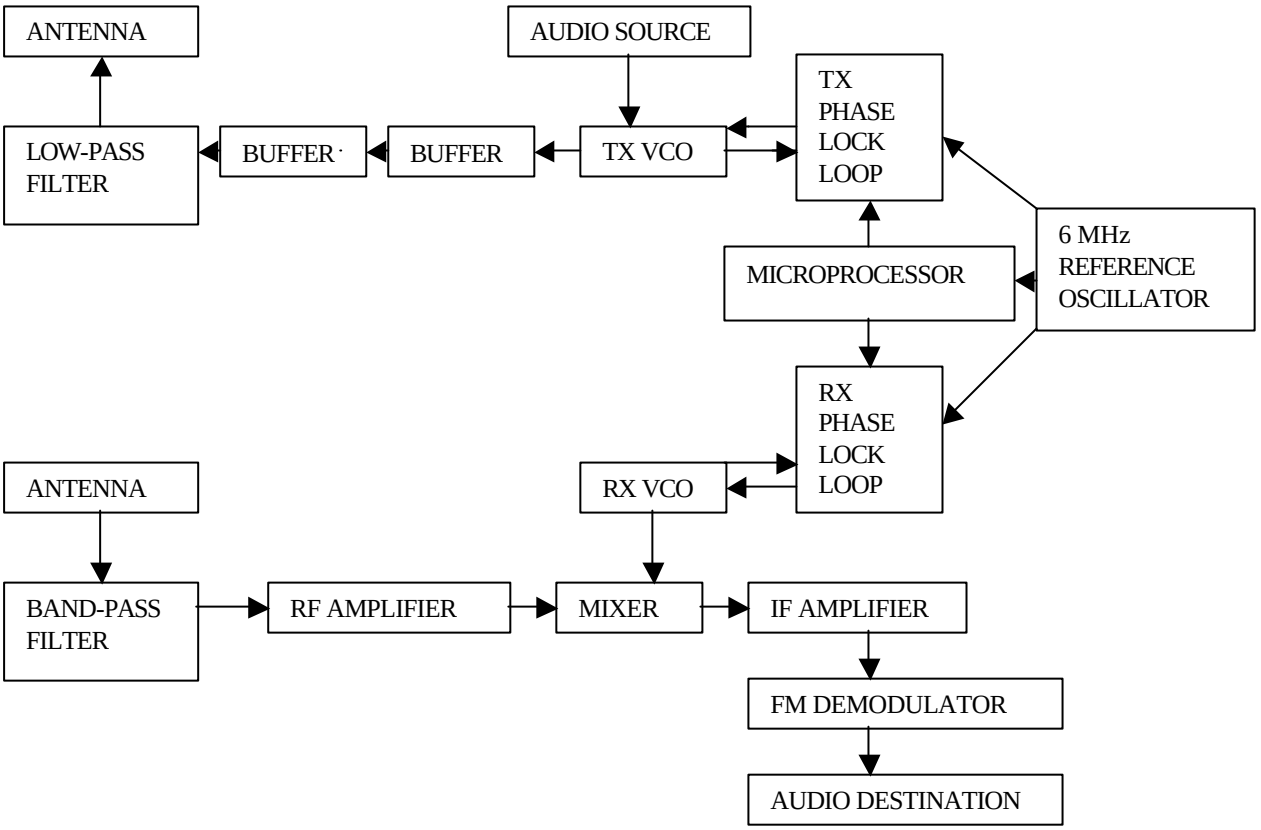
ANTENNA
AUDIO SOURCE
TX PHASE LOCK LOOP
LOW-PASS FILTER
BUFFER
BUFFER
TX VCO
6 MHz REFERENCE OSCILLATOR
MICROPROCESSOR
RX PHASE LOCK LOOP
ANTENNA
RX VCO
BAND-PASS FILTER
RF AMPLIFIER
MIXER
IF AMPLIFIER
FM DEMODULATOR
AUDIO DESTINATION

Figure 1