Operational Description

Of

connectBlue Design 0005-01

The

OEM Bluetooth module

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1 Definitions

JTAG	Standard interface for in circuit debug and emulation
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver Transmitter
LDO	Low Drop Out
HCI	Host Controller Interface
RS-232	A standard for signal levels and impedances for serial communication
Barney	Ericsson internal project name for one of their Bluetooth module

2 Objectives

With these two documents, it will be possible to implement a custom made design with the same functionality as connectBlue design cB-0005-01.

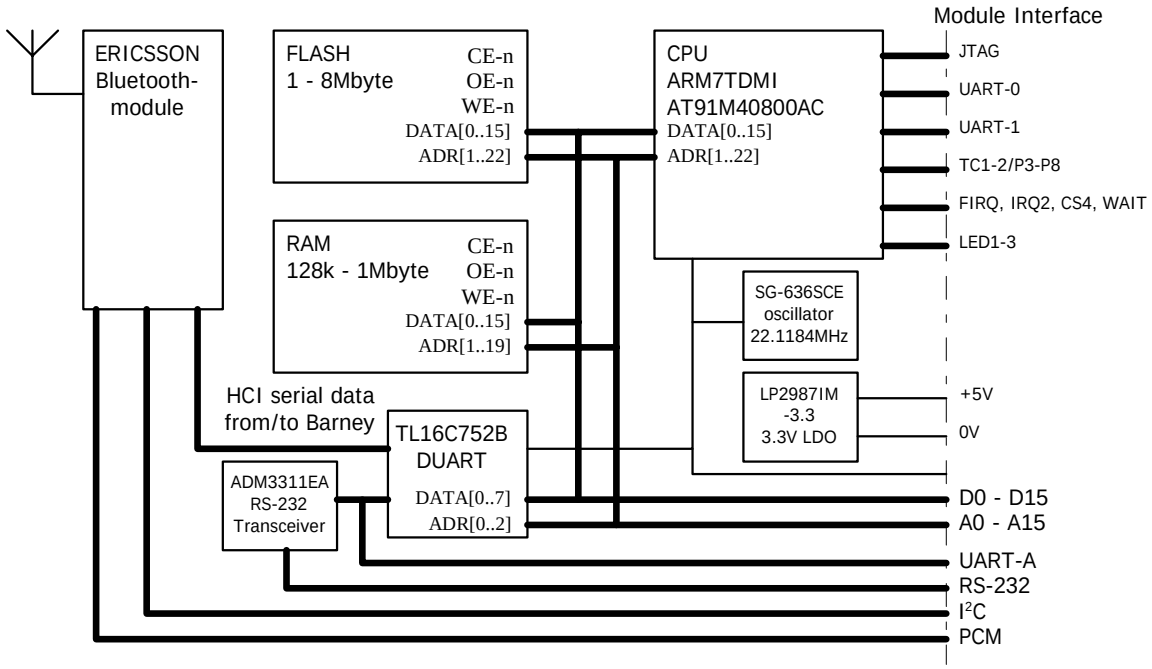

Figure 1 Block diagram of connectBlue design cB-0005-01

3 Components description

This section contains a short description and some hints about the components used in connectBlue design cB-0005-01.

3.1 CPU

The CPU is AT91M40800 from ATMEL with an ARM7TDMI core.

The CPU has build in chip select logic that supports up to 8 CS signals. CS0 – CS3 are active low and CS4 – CS7 are active high.
By holding the BMS signal (CPU pin 84) low during power-up with 10kΩ resistor R2, CS0 is set up for 16-bit wide external boot memory selection.

Table 1 - Chip select signals

Signal	Active Level	Selects	Wait States	Data Float Wait States
CS0	LOW	Flash (D2)	1	0
CS1	LOW	SRAM (D3)	1	0
CS2	LOW	UART B (D5)	3	1
CS3	LOW	UART A (D5)	3	1
CS4	HIGH	Reserved for external expansion	-	-

3.2 Flash memory

The amount of Flash memory with the same PCB-layout can vary from 1MB to 8MB. With an oscillator frequency of 22.1184MHz and 1 wait state 90ns access time is sufficient.

Table 2 - Suppliers of Flash memory

	1M byte	2M byte	4M byte	8M byte
SST	-	SST36VF1601	-	-
AMD	AM29DL800BT	AM29DL163DT	AM29DL322DT	AM29LV640DU
ATMEL	AT49LV8011T	AT49LV1614T	-	-

3.3 SRAM

The can have the size of 128 kB to 1 MB with the same PCB-layout.

Table 3 - Suppliers of SRAM

	128k byte	512k byte	1M byte
HYNIX	HY62UF16101C-DF70I	HY62UF16406D-DF70I	HY62UF16804A-DM70I
SAMSUNG	K6F1016V4B-FF70	K6F4016U6E-EF70	K6F8016U6M-FF70

3.4 Oscillator

The crystal oscillator is a SG-636SCE from EPSON because of two fundamentals, its low power consumption and the narrow tolerance of the duty cycle.

The selected crystal oscillator frequency of 22.1184MHz gives an exact match on the baud rate generator with integer division.

3.5 DUART

The Dual Universal Asynchronous Receiver Transmitter (DUART) used in the design is TL16752B from Texas Instruments.

There are a couple of things to keep in mind when using this circuit.

- The reset input is active high, and the DUART is held in reset by 10kΩ pull-up resistor. In order to take the circuit out of reset configure the GPIO “P0” (pin 49 on the CPU) to a logic low output.
- The interrupt outputs are active high and the registers in the CPU controlling IRQ0 and IRQ1 must be configured accordingly.
- The number of wait states required by the DUART is based on the number of clock cycles that the internal state machine needs when accessed by the CPU.

3.6 RS232 transceiver

The serial port transceiver is an ADM3311EARU from Analog. It accommodates the level shift from the internal 3.3V CMOS logic to the external RS-232 interface.

The transceiver is normally in shut down mode by 10kΩ pull-up resistor. To enable RS-232 level UART-communication configure the GPIO “P1” (pin 50 on the CPU) to a logic low output.

3.7 Bluetooth module

The Bluetooth module is ROK 101 007 from Ericsson.

The reset input of the Bluetooth module is controlled from two sources RESET-N and WDOVF-N. The two signals are or:ed together.

3.8 Voltage Regulator

The voltage regulator is a linear regulator (LM2987IM-3.3) converting the incoming power to 3.3V and generates the reset signal during power up. Input power should be between 3.6VDC to 6.5VDC. If the incoming supply voltage drops below 3.3V, the reset signal is activated.

4 Electrical module interface

4.1 PCM and I²C connection

These pins are directly connected to the on-board Bluetooth unit and are reserved for future use.

Pin Name	Type	Description
PCM_CLK	In/Out	100kΩ pull-up to 3.3V, connected to the Bluetooth module PCM interface
PCM_SYNC	In/Out	100kΩ pull-up to 3.3V, connected to the Bluetooth module PCM interface
PCM_OUT	Output	100kΩ pull-up to 3.3V, connected to the Bluetooth module PCM interface
PCM_IN	Input	100kΩ pull-up to 3.3V, connected to the Bluetooth module PCM interface
I^2C_CLK	Output	Connected to the Bluetooth module I^2C interface
I^2C_DATA	In/Out	Connected to the Bluetooth module I^2C interface

4.2 General Purpose I/O

All General Purpose Input and Output are logic level 0V – 3.3V.
Use VSS as low-level reference and VCC_3V3 as high-level reference.

Maximum load on all GPIO are 2mA.

Pin Name	Type	Description
Mode 1	GPIO	10kΩ pull-up to 3.3V
Mode 0	GPIO	10kΩ pull-up to 3.3V
Reset	Open collector	10kΩ pull-up to 3.3V. Pulled low by internal reset logic during power up. External logic can pull this pin low to reset module.
Firq	GPIO	10kΩ pull-up to 3.3V
P8	GPIO	
P7	GPIO	
P6	GPIO	
P5	GPIO	
P4	GPIO	
P3	GPIO	
RXD1	GPIO	
TXD1	GPIO	
SCK1	GPIO	
B-LED	GPIO	
R-LED	GPIO	
G-LED	GPIO	

4.3 UART-communication

It is possible to select if external UART-communication is made with RS232 levels or 3.3V CMOS logic level.

4.3.1 RS232 level UART-communication

Pin Name	Type	Description	Level
CTSA	Do NOT connect these pins. When UART-communication with RS232 signal levels is enabled this signals are used internally.		
RXA			
RTSA			
TXA			
RS232-DSR	Input	Data Set Ready	RS232
RS232-RX	Input	Receive data	RS232
RS232-CTS	Input	Clear To Send	RS232
RS232-RTS	Output	Request to Send	RS232
RS232-TX	Output	Transmit data	RS232
RS232-DTR	Output	Data Terminal Ready	RS232

4.3.2 Logic level UART-communication

Pin Name	Type	Description	Level
CTSA	Input	Clear To Send	0V/3,3V
RXA	Input	Receive data	0V/3,3V
RTSA	Output	Request to Send	0V/3,3V
TXA	Output	Transmit data	0V/3,3V
RS232-DSR	Input	Inputs accepts RS232 voltage levels but are internally disconnected from the UART when UART-communication with logic level is enabled	
RS232-RX	Input		
RS232-CTS	Input		
RS232-RTS	Output	Although output drivers are active specific output levels can not be guaranteed when UART-communication with logic level is enabled	
RS232-TX	Output		
RS232-DTR	Output		

4.4 Power connection

Pin Name	Type	Description
VSS	I/O-signal return path	Internal signal ground, separated from module power ground with filter. 5 pins are available for VSS.
VCC_3V3	Output	Internal regulated supply voltage, Max load 10mA.
+5V	Power	Module power supply voltage 3.6 – 6.5V
0V	Power	Module power ground.
CHGND	Power	Two 2.5mm plated mounting holes, connected to filter center tap for EMI suppression.

4.5 JTAG interface

The JTAG interface is connected to the ICE interface of the CPU for debugging purpose.

Pin Name	Type	Description
TMS	Input	Test Mode Select
TDI	Input	Test Data Input
TDO	Output	Test Data Output
TCK	Input	Test Clock

4.6 Address and data bus

Pin Name	Type	Description
D00-D15	Open collector	The Entire data bus
A00-A15	Output	The lowest 16 bits of the Address bus
CS4	Output	Chip select 4
WAIT	Input	