LCUH22-LD Hardware Design

LTE Standard Series

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Revision History

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-	2024-04-07	Creation of the document
1.0.0	2024-04-07	Preliminary

Contents

Table Index

Figure Index

1 Introduction

This document defines the LCUH22-LD and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. With application note and user guide, you can use the module to design and set up mobile applications easily.

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3. A label with the following statements must be attached to the host end product: This device contains FCC ID: 2BEY3LCUH22LDA

4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

Operating Band	Peak gain	Manufacturer	Impedance	Antenna type
WCDMA Band II	1.59 dBi	Shanghai Saintenna Electronic Technology Co., Ltd.	50 Ω	External Antenna
WCDMA Band IV	2.00 dBi			
WCDMA Band V	2.53 dBi			
LTE Band 2	1.59 dBi			
LTE Band 4	2.00 dBi			
LTE Band 5	2.53 dBi			
LTE Band 12	3.95 dBi			
LTE Band 13	4.45 dBi			
LTE Band 25	1.59 dBi			
LTE Band 26(814-824)	3.19 dBi			
LTE Band 26(824-849)	2.53 dBi			

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC

ID: 2BEY3LCUH22LDA" or "Contains FCC ID: 2BEY3LCUH22LDA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN
"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :
1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF
L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.
The host product shall be properly labeled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:
"Contains IC: 32052-LCUH22LDA" or "where: 32052-LCUH22LDA is the module's certification number".
Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.
L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:
"Contient IC: 32052-LCUH22LDA " ou "où: 32052-LCUH22LDA est le numéro de certification du module".

KDB 996369 D03 OEM Manual rule sections:

2.2 List of applicable FCC rules
This module has been tested for compliance to FCC Part 15.247

2.3 Summarize the specific operational use conditions
The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class 2 permissive change application or new certification.

2.4 Limited module procedures
Not applicable.

2.5 Trace antenna designs
Not applicable.

2.6 RF exposure considerations
This equipment complies with FCC mobile radiation exposure limits set forth for an controlled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas
Please refer to page 8 of the manual

2.8 Label and compliance information
The host system using this module, should have label in a visible area indicated the following texts: “Contains FCC ID: 2BEY3LCUH22LDA, Contains IC: 32052-LCUH22LDA”

2.9 Information on test modes and additional testing requirements5
Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.

2.10 Additional testing, Part 15 Subpart B disclaimer
The module without unintentional-radiator digital circuity, so the module does not require an evaluation by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.

2.11 Note EMI Considerations
Please follow the guidance provided for host manufacturers in KDB publications 996369 D02 and D04.

2.12 How to make changes
Only Grantees are permitted to make permissive changes.

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2 Product Overview

2.1. Frequency Bands and Functions

LCUH22-LD is an embedded LTE/WCDMA wireless communication module with receive diversity. It supports data connectivity on LTE-FDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA networks.

The following table shows the supported frequency bands and GNSS functions of the module.

Table 1: Frequency Bands and Functions

Module	LTE Band (with Rx-diversity)	WCDMA (with Rx-diversity)	GNSS (Optional)
LCUH22-LD	FDD: B2/B4/B5/B12/B13/ B25/B26	B2/B4/B5	GPS, GLONASS, BDS, Galileo, QZSS

LCUH22-LD is an SMD type module which can be embedded into applications through its 106 LGA pins. With a compact profile of 29.0 mm × 25.0 mm × 2.45 mm, it can meet almost all requirements for M2M applications.

The module is integrated with internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for you to use these internet service protocols easily.

2.2. Key Features

The following table describes the detailed features of the module.

Table 2: Key Features of the Module

Feature	Details
Power Supply	● Supply voltage range: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 3 (23 dBm ±2 dB) for WCDMA bands ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands
LTE Features	● Support up to non-CA Cat 1 FDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidths ● Modulations: – DL: QPSK, 16QAM and 64QAM – UL: QPSK and 16QAM ● LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL)
UMTS Features	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Support QPSK, 16QAM and 64QAM modulations ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL), Max. 384 kbps (UL)
Internet Protocol Features	● Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/ NITZ/MMS/SMTP/SSL/MQTT/FILE/CMUX/SMTPS protocols ● Support PAP and CHAP protocols for PPP connections

SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	● Support 1.8 V and 3.0 V (U)SIM cards ● Support Dual SIM Single Standby
Audio Features	● Support one digital audio interface: PCM interface ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB
PCM Interface	● Used for audio function with external codec ● Support 16-bit linear data format ● Support long frame synchronization and short frame synchronization ● Support master and slave mode, but must be the master in long frame synchronization
USB Interface	● Compliant with USB 2.0 specification (slave mode only); the data transmission rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade ● Support USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–6.7, Android 4.x–13.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rates reach up to 921600 bps, 115200 bps by default ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
SPI Interface	● Provides a duplex, synchronous and serial communication link with the peripheral devices. ● Dedicated to one-to-one connection, without chip selection. ● 1.8 V operation voltage with clock rates up to 50 MHz.
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features (Optional)	● Protocol: NMEA 0183 ● Data update rate: 1 Hz by default
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Enhanced AT commands
Network Indication	NETLIGHT pin for network activity status indication
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Size: (29.0 ±0.15) mm × (25.0 ±0.15) mm × (2.45 ±0.2) mm ● Package: LGA ● Weight: approx. 4.2 g
Temperature Ranges	● Operating temperature range: -35 °C to +75 °C [1] ● Extended temperature range: -40 °C to +85 °C [2] ● Storage temperature range: -40 °C to +90 °C

[1] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[2] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

Firmware Upgrade	● USB interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency
- Peripheral interfaces

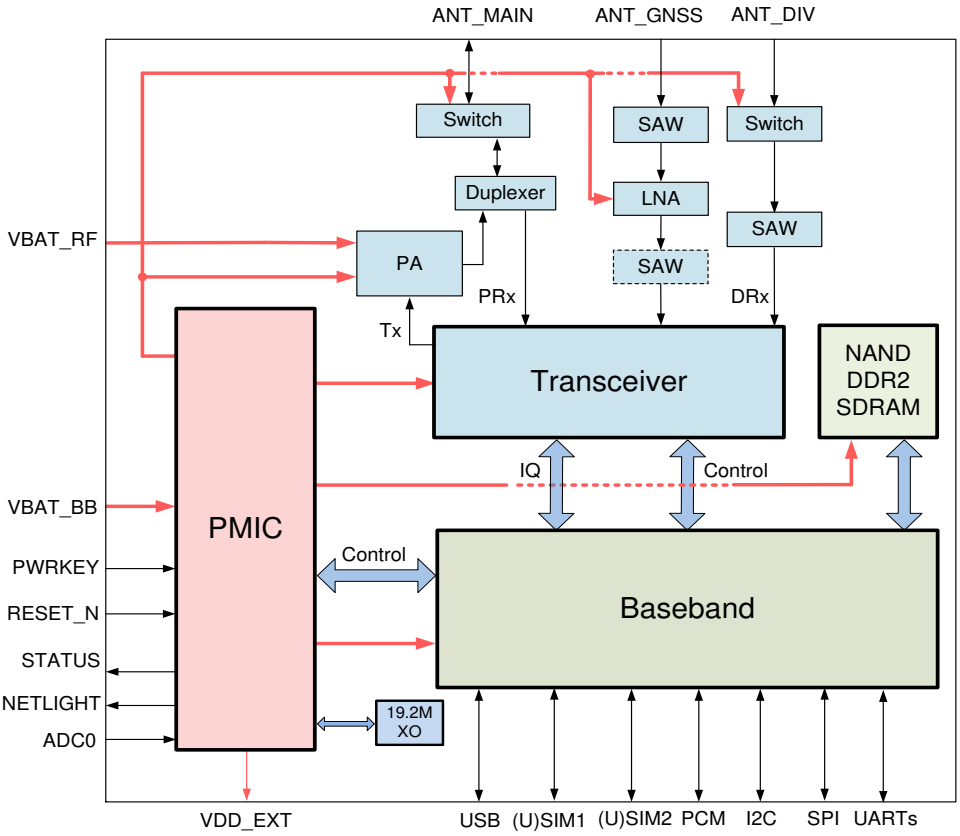


Figure 1: Functional Diagram

2.4. EVB Kit

NetPrisma supplies an evaluation board (UMTS&LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***

3 Application Interfaces

3.1. General Description

The module is equipped with 106 LGA pins that can be connected to your cellular application platforms. The subsequent chapters will provide detailed descriptions of the following interfaces/functions.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SPI interface
- Indication signals
- ADC interface
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

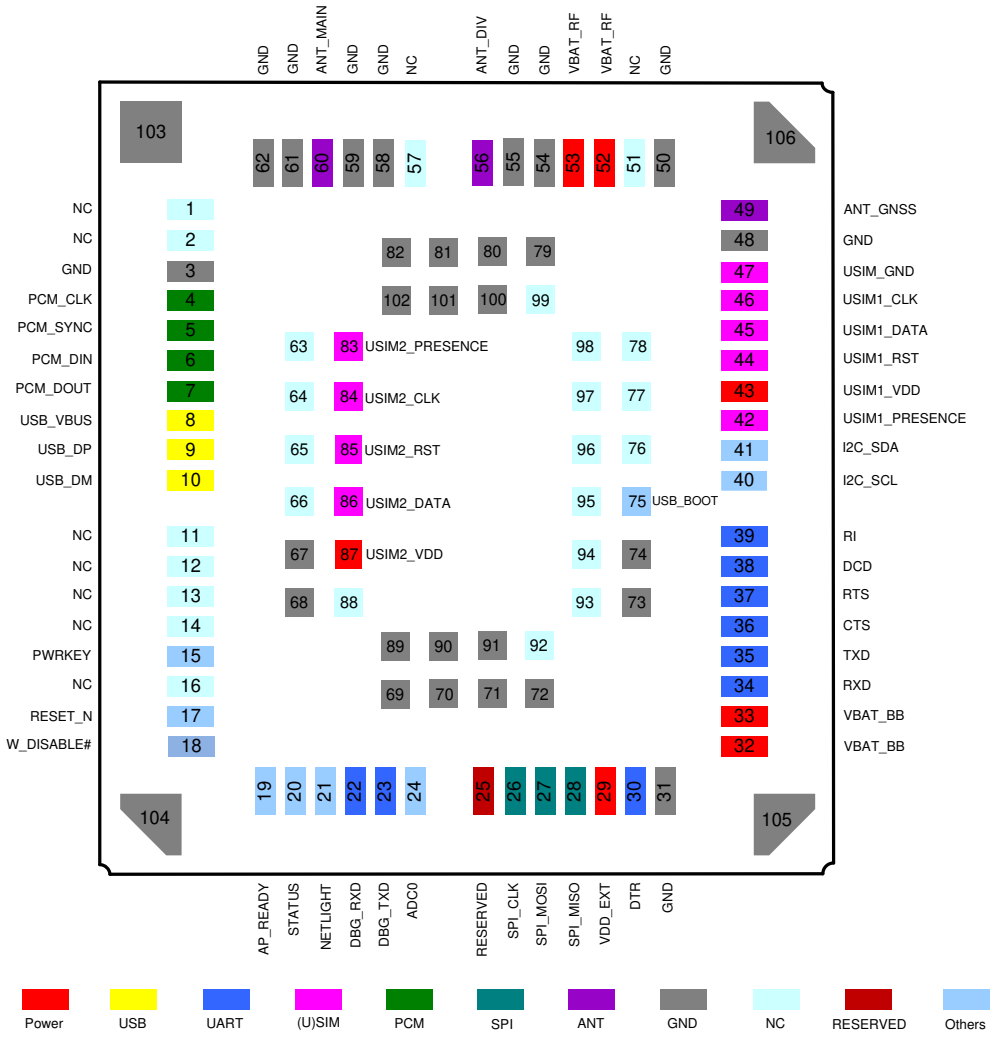


Figure 2: Pin Assignment (Top View)

NOTE

1. PWRKEY output voltage is 0.8 V because of the diode drop in the baseband chipset.
2. Keep all RESERVED pins and unused pins unconnected.
3. GND pins should be connected to ground in the design.
4. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact NetPrisma Technical Support.

3.3. Pin Description

The following tables show the pin definition and description of the module.

Table 3: Parameter Definition

Parameter	Description

AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 4: Pin Description

Power Supply

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	32, 33	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A. A test point is recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 1.8 A in a burst transmission. A test point is recommended to be reserved.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106				

Turn On/Off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.
RESET_N	17	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Require pull-up resistor to 1.8 V internally. Active LOW. If unused, keep it open.

Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	20	DO	Indicate the module's operating status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep them open.
NETLIGHT	21	DO	Indicate the module's network activity status		

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Typical value: 5.0 V If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	47	-	Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_PRESENCE	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:**	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.

				Vmax = 3.05 V Vmin = 2.7 V	
USIM2_DATA	86	DIO	(U)SIM2 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	If unused, keep them open.
USIM2_CLK	84	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	85	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_PRESENCE	83	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.

Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	39	DO	Ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DCD	38	DO	Data carrier detect		
CTS	36	DO	Clear to send signal from the module		Connect to the MCU's CTS. 1.8 V power domain. If unused, keep it open.
RTS	37	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep it open.
DTR	30	DI	Data terminal ready Sleep mode control		1.8 V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
TXD	35	DO	Transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
RXD	34	DI	Receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	

Debug UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment

DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	

PCM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	5	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM_CLK	4	DIO	PCM clock		

I2C Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	OD	I2C serial clock (for external codec)		Require an external pull-up to 1.8 V If unused, keep them open.
I2C_SDA	41	OD	I2C serial data (for external codec)		

ADC Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0.3 V to VBAT_BB	If unused, keep it open.

SPI Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
SPI_MOSI	27	DO	SPI master-out slave-in		
SPI_MISO	28	DI	SPI master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	

RF Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω impedance. If unused, keep them open.
ANT_DIV	56	AI	Diversity antenna interface		
ANT_MAIN	60	AIO	Main antenna Interface		50 Ω impedance.

Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. At low voltage level, module can enter airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor ready		1.8 V power domain. If unused, keep it open.
USB_BOOT	75	DI	Force the module to enter download mode		1.8 V power domain. Active HIGH. A test point is recommended to reserved.

NC and RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
NC	1, 2, 11–14, 16, 51, 57, 63–66, 76–78, 88, 92–99	Keep them unconnected.
RESERVED	25	

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. USB_BOOT pin and BOOT_CONFIG pins (SPI_CLK, PCM_CLK and PCM_SYNC) cannot be pulled up before startup.

3.4. Operating Modes

The table below briefly outlines the operating modes to be mentioned in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on network, and it is ready to send and receive data.
	Data	Network is connected. In this mode, the power consumption is decided by network setting and data transmission rate.
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid.	

Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Sleep Mode	In this mode, the power consumption of the module will be reduced to an ultra-low level. During this mode, the module can still receive paging message, SMS and TCP/UDP data from the network normally.
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

For details of the above AT command, see ***document [2]***.

3.5. Power Saving

3.5.1. Sleep Mode

The module is able to reduce its power consumption to an ultra-low level during the sleep mode. The following sub-chapters describe the power saving procedures of the module.

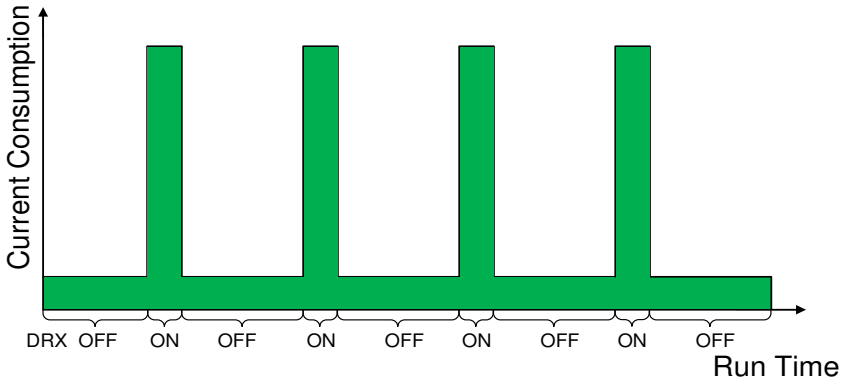


Figure 3: Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.5.1.1. UART Application Scenario

If the MCU communicates with the module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the MCU.

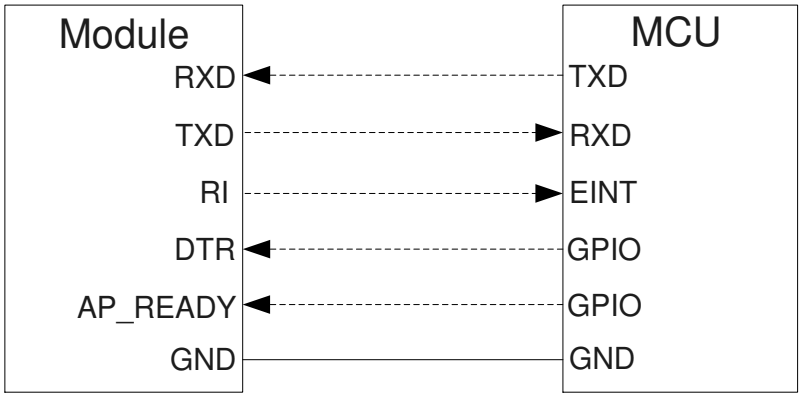


Figure 4: Sleep Mode Application via UART

- Driving the module's DTR to low level will wake up the module.
- When the module has a URC to report, RI signal will wake up the MCU. See ***Chapter 3.15.3*** for details about RI behaviors.
- AP_READY will detect the sleep state of the MCU (can be configured to high-level or low-level detection). See ***document [3]*** for details about **AT+QCFG="apready"**.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

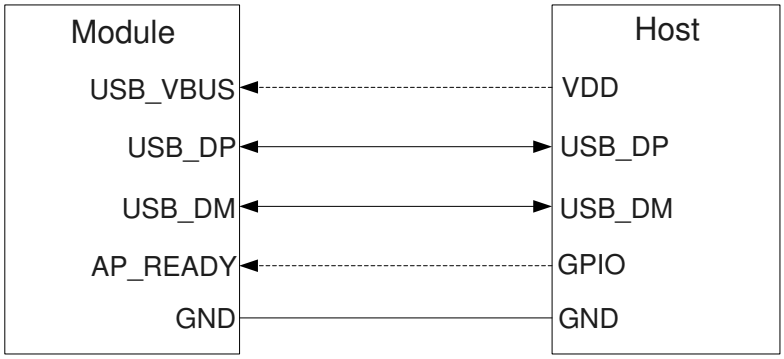


Figure 5: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, it will send remote wakeup signals via USB bus to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.

- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspended state.

The following figure shows the connection between the module and the host.

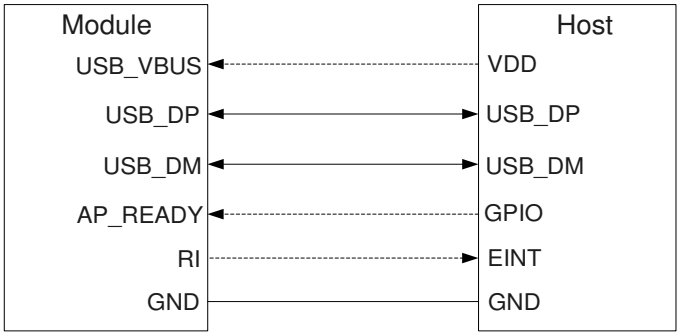


Figure 6: Sleep Mode Application with RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, USB_VBUS should be disconnected with an external control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

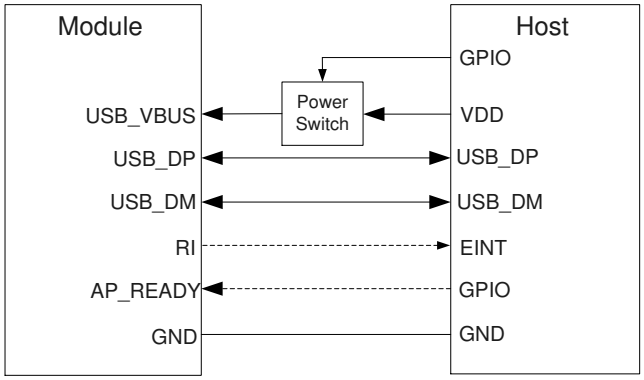


Figure 7: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level-matching shown in dotted line between the module and the host.
2. For more details about the module power management application, see ***document [4]***.
3. For details of **AT+QSCLK**, see ***document [2]***.
4. For details of **AT+QCFG**, see ***document [3]***.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** as 0, 1 or 4. See ***document [2]*** for more details.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode (RF function is disabled).

NOTE

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**. See ***document [3]*** for more details.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's BB part.

The following table shows the details of VBAT pins and ground pins.

Table 6: Pin Definition of VBAT and GND

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for the module's RF part.	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for the module's BB part.	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106					

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure that the input voltage will never drop below 3.3 V.

To decrease voltage drop, a filter capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used for VBAT_BB and VBAT_RF respectively, and a multi-layer ceramic chip (MLCC) capacitor array should

also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 100 pF for VBAT_BB and 100 nF, 33 pF, 10 pF for VBAT_RF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be not less than 1 mm, and the width of VBAT_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to avoid the damage caused by electric surge and ESD, it is suggested that a TVS diode with low reverse stand-off voltage V_{RWM} (4.5 V), low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

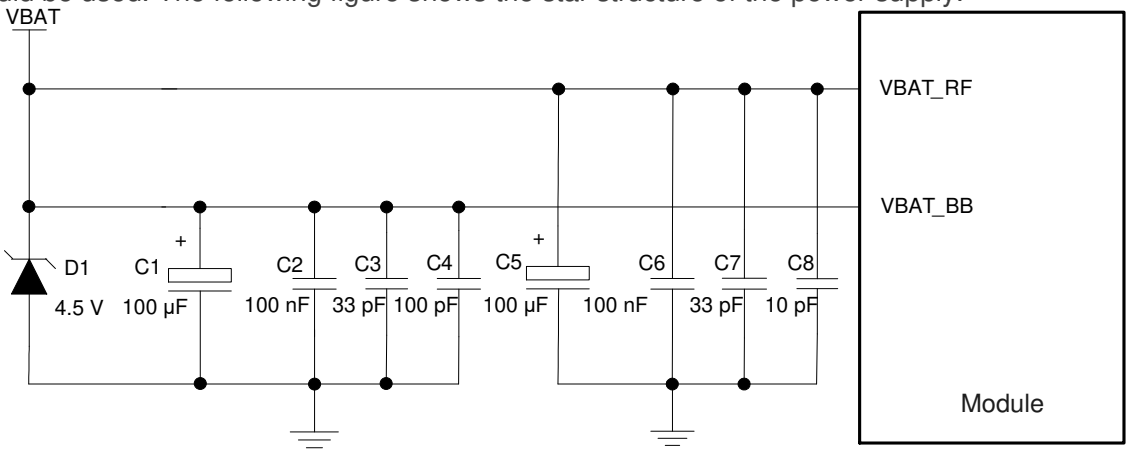


Figure 8: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 1.5 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3 A.

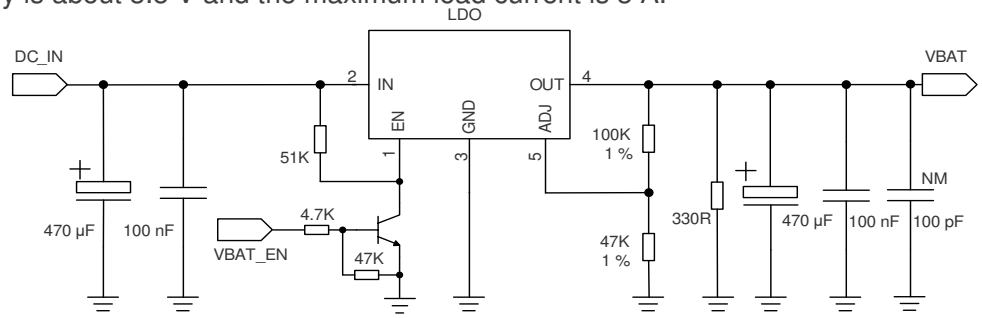


Figure 9: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

3.6.4. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.7. Turn On

3.7.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	Comment
PWRKEY	15	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the baseband chipset.

When the module is in power-down mode, it can be turned on to full functionality mode by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY, and release PERKEY after STATUS outputs a high level. The STATUS pin is used as an indicator to show that the module has been turned on normally.

A simple reference circuit is illustrated in the following figure.

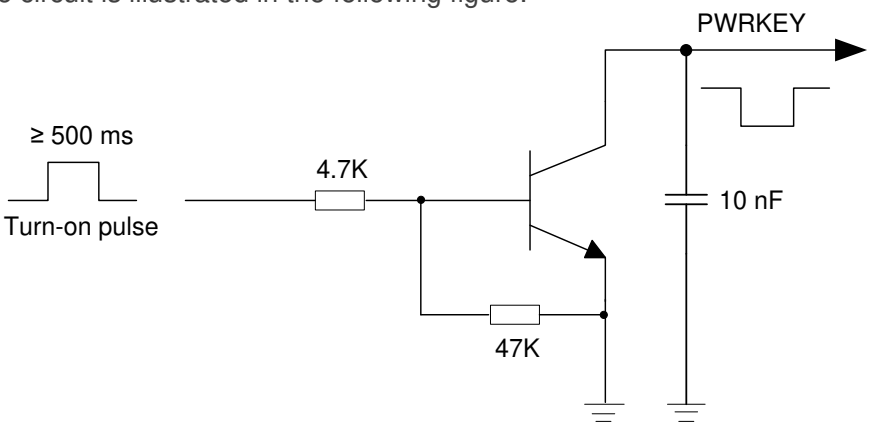


Figure 10: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may be generated from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

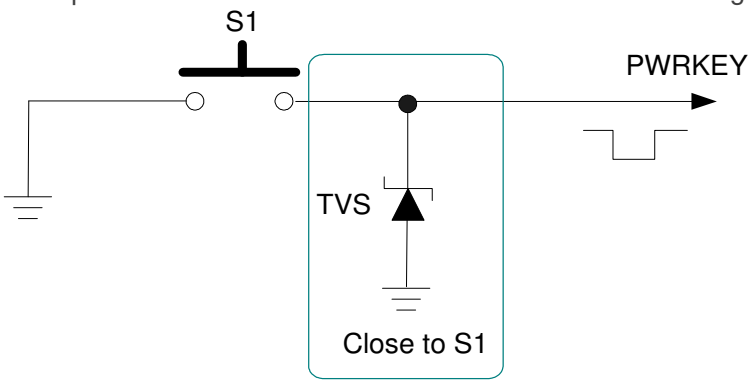


Figure 11: Turn On the Module Using a Button

The power-up timing is illustrated in the following figure.

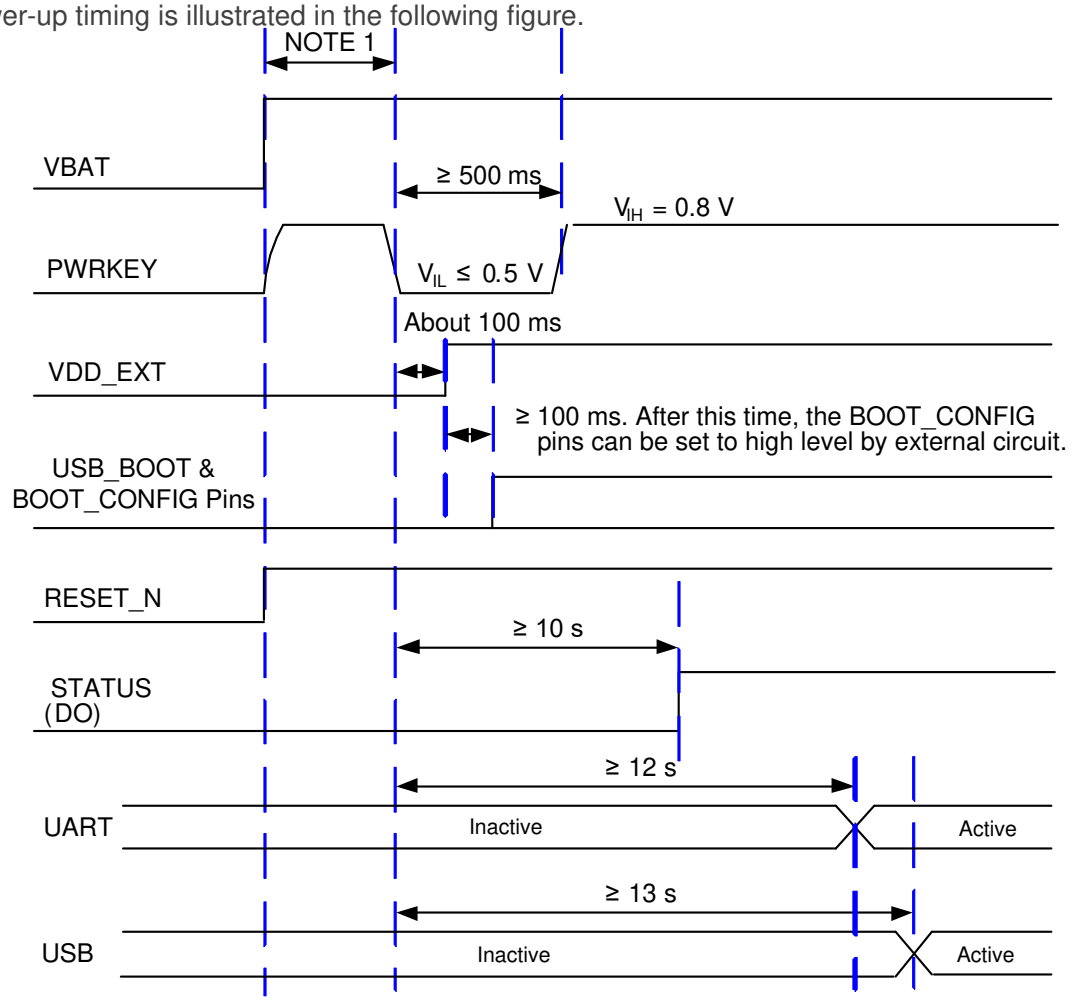


Figure 12: Turn-on Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.
3. USB_BOOT pin and BOOT_CONFIG pins (SPI_CLK, PCM_CLK and PCM_SYNC) cannot be pulled up before startup.

3.8. Turn Off

Either of the following methods can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD**

3.8.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 650 ms, the module will execute power-down procedure after the PWRKEY is released. The power-down timing is illustrated in the following figure.

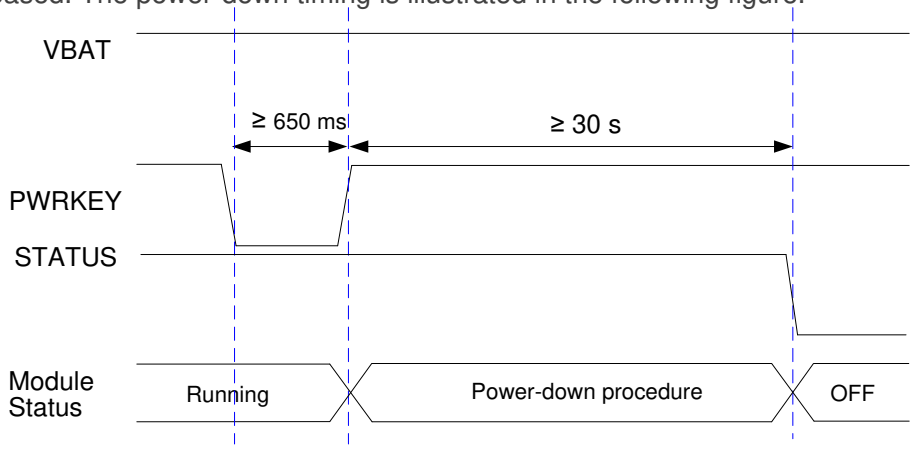


Figure 13: Turn-off Timing

3.8.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via PWRKEY pin.

See ***document [2]*** for details about the **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successfully turn-off.

3.9. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N low for 150–460 ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	Description	Comment
RESET_N	17	Reset the module	Require pull-up resistor to 1.8 V internally. Active low. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

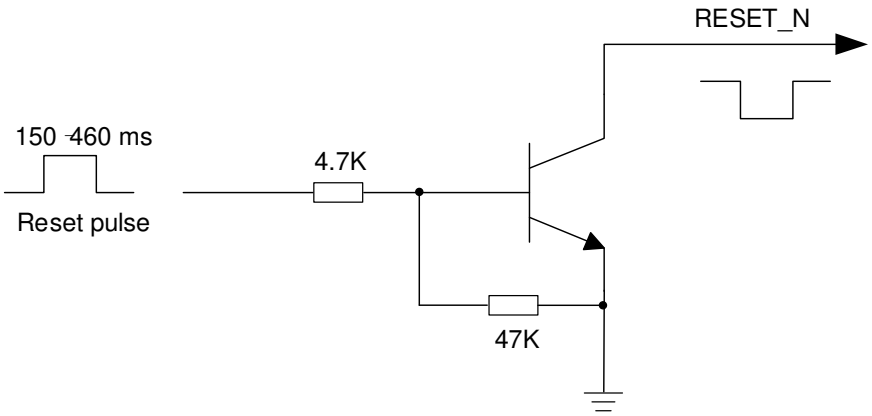


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

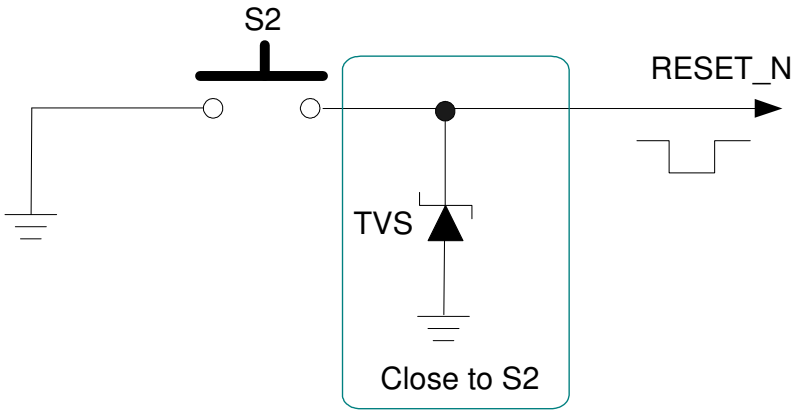


Figure 15: Reference Circuit of RESET_N by Using a Button

The reset timing is illustrated in the following figure.

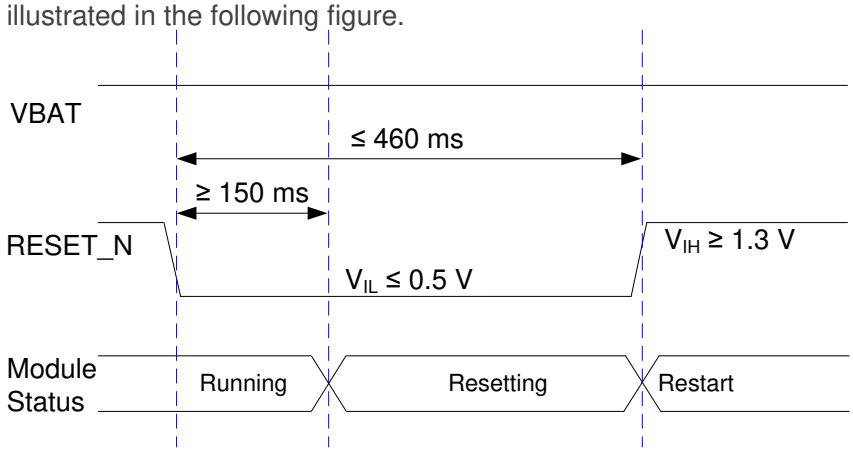


Figure 16: Reset Timing

NOTE

1. Use RESET_N only when turning off the module by **AT+QPOWD** and PWRKEY pin are failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.10. (U)SIM Interfaces

The module provides two (U)SIM interfaces, and only one (U)SIM card can work at a time. The (U)SIM1 and (U)SIM2 cards can be switched by **AT+QDSIM**. For more details, see ***document [5]***.

The (U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 9: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM_GND	47	-	Specified ground for (U)SIM card	Connect to ground of (U)SIM card connector.
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_PRESENCE	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
USIM2_DATA	86	DIO	(U)SIM2 card data	If unused, keep them open.
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_PRESENCE	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.

The module supports (U)SIM card hot-plug via USIM_PRESENCE pin, and both high-level and low-level detection are supported. The function is disabled by default, and see ***document [2]*** for more details about **AT+QSIMDET**.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

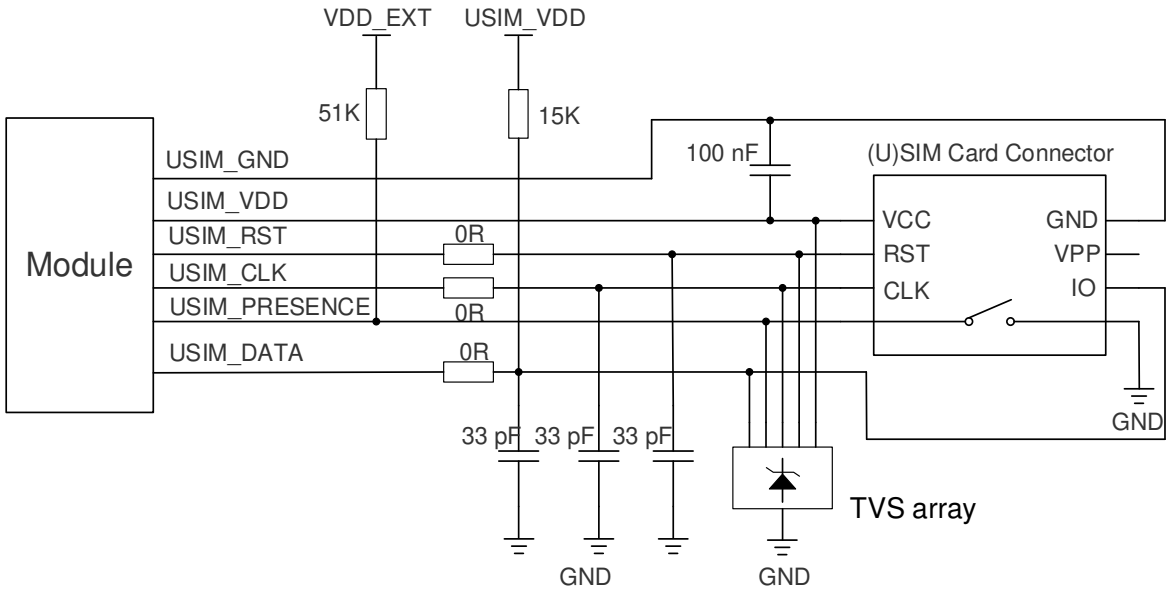


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

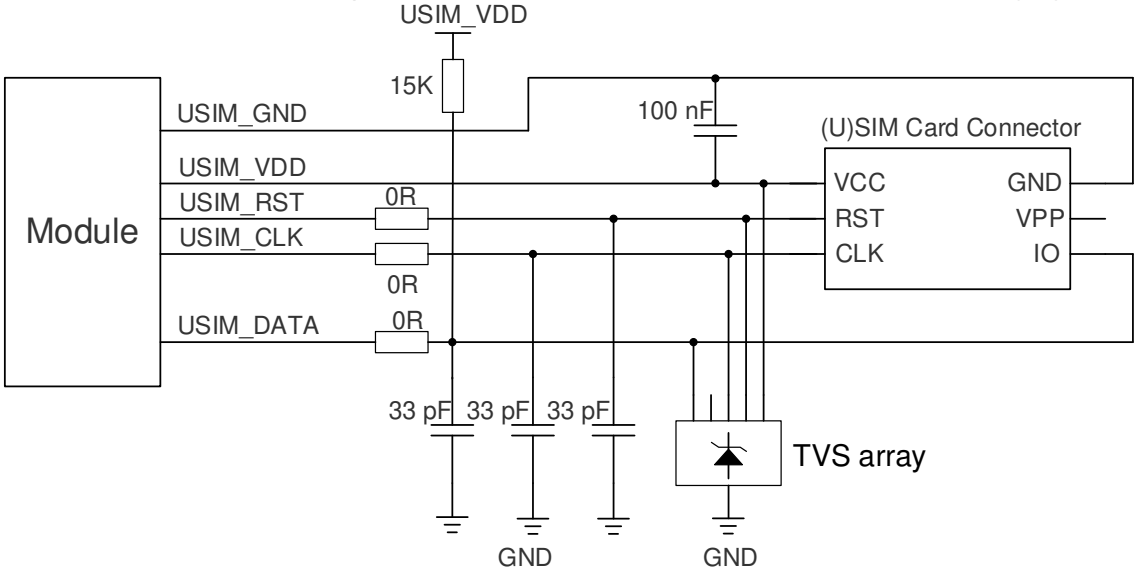


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM cards in your applications, follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, it is recommended to add a TVS array whose parasitic capacitance should be less than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA,

USIM_CLK and USIM_RST signal traces to filter out RF interference. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.

- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.11. USB Interface

The module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes.

The USB interface can only serve as a slave device and is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)	
USB_VBUS	8	AI	USB connection detect	Typical value: 5.0 V If unused, keep it open.
GND	3	-	Ground	

For more details about USB 2.0 specifications, visit http://www.usb.org/home.

The test points are recommended to be reserved for firmware upgrade and software debugging in your design. The following figure shows a reference circuit of USB interface.

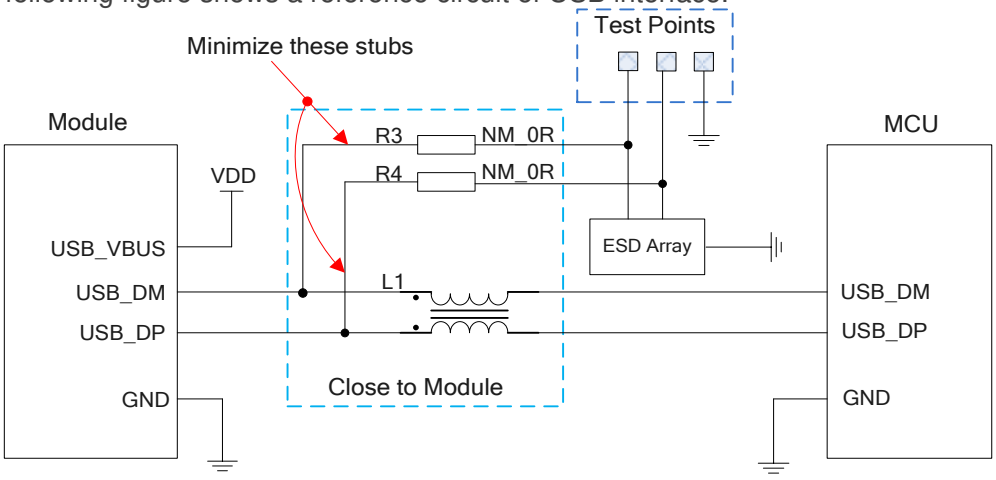


Figure 19: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R3 and R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, the following principles should be complied with when design the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so pay attention to the selection of the component. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components as close to the USB connector as possible.

3.12. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. It supports RTS and CTS hardware flow control, and is used for AT command communication and data transmission.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the two UART interfaces.

Table 11: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	39	DO	Ring indication	1.8 V power domain If unused, keep them open.
DCD	38	DO	Data carrier detect	
CTS	36	DO	Clear to send signal from the module	Connect to the MCU's CTS. 1.8 V power domain If unused, keep it open.
RTS	37	DI	Request to send signal to the module	Connect to the MCU's RTS. 1.8 V power domain If unused, keep it open.
DTR	30	DI	Data terminal ready Sleep mode control	1.8 V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
TXD	35	DO	Transmit	1.8 V power domain. If unused, keep them open.
RXD	34	DI	Receive	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Debug UART transmit	1.8 V power domain. If unused, keep them open.
DBG_RXD	22	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

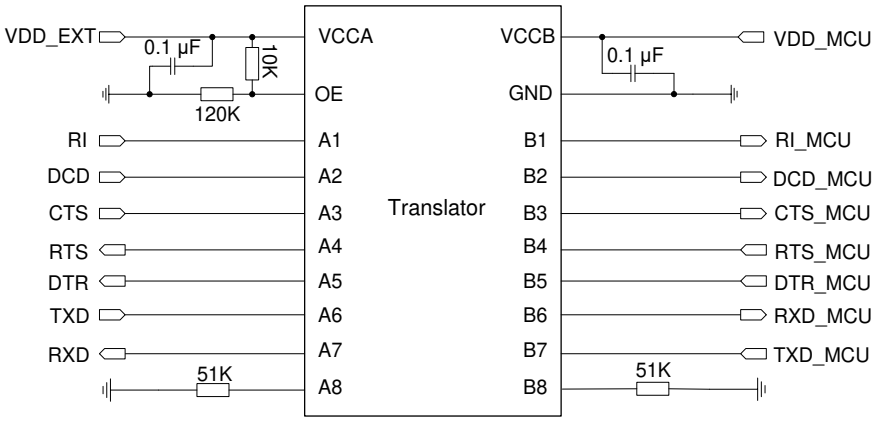


Figure 20: Reference Circuit with Translator Chip

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

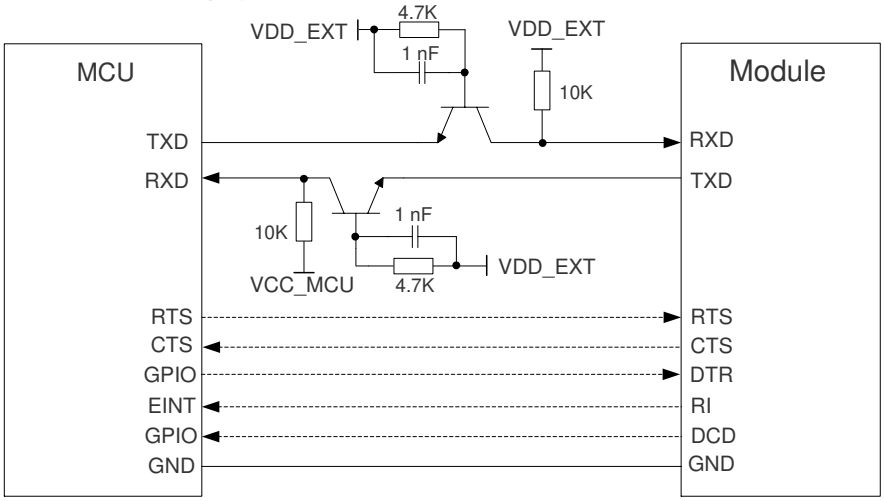


Figure 21: Reference Circuit with Transistor Circuit

NOTE

- Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
- Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
- To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

3.13. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design which supports the following modes, and provides one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC. The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

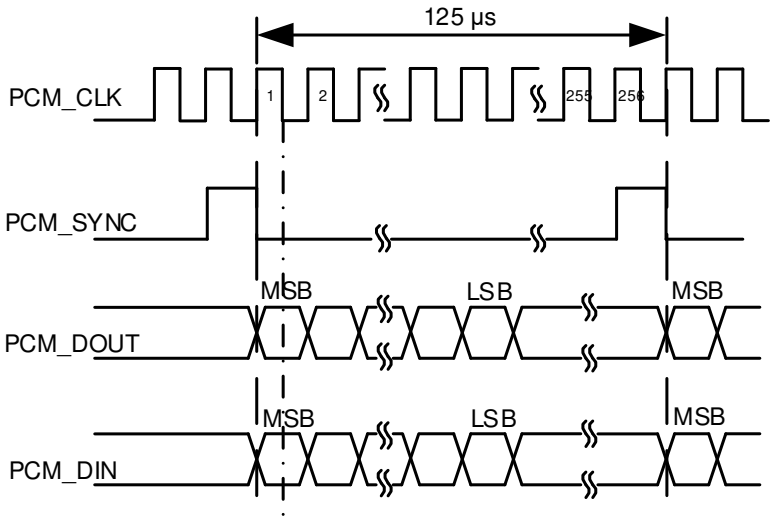


Figure 22: Primary Mode Timing

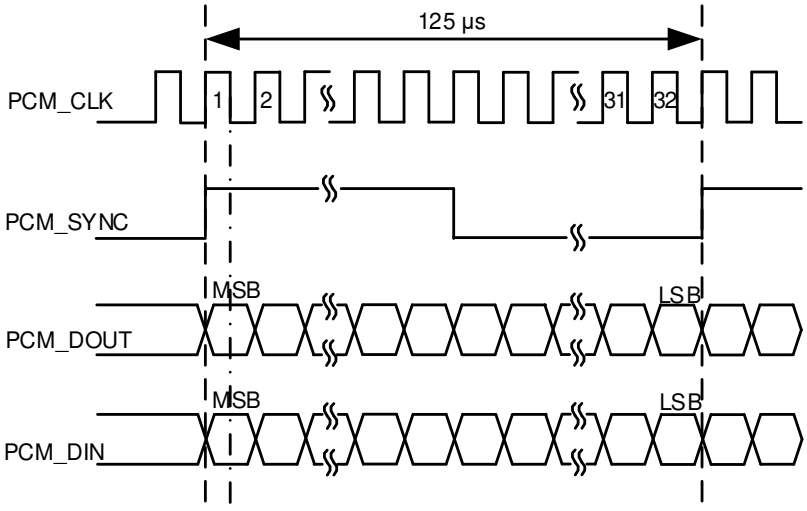


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 13: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DIO	PCM data frame sync	1.8 V power domain. In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM_CLK	4	DIO	PCM data clock	
I2C_SCL	40	OD	I2C serial clock (for external codec)	Require an external pull-up to 1.8 V If unused, keep them open.
I2C_SDA	41	OD	I2C serial data (for external codec)	

The clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** about **AT+QDAI** for details.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

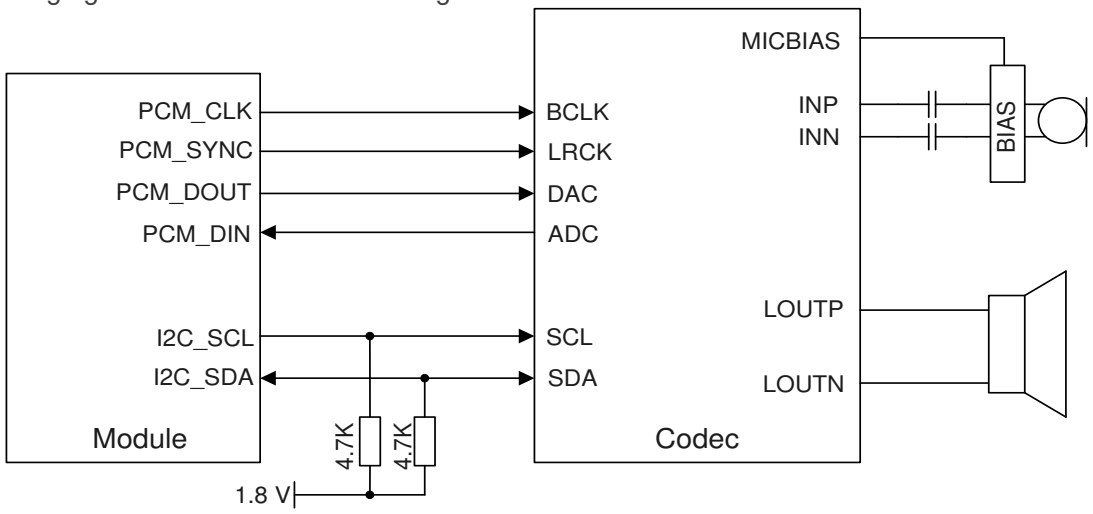


Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The module works as a master device pertaining to I2C interface.

3.14. SPI Interface

SPI interface only acts as master device. It provides a duplex, synchronous and serial communication link with the peripheral devices. It is dedicated to one-to-one connection without chip selection. Its operation voltage is 1.8 V with clock rates up to 50 MHz.

The following table shows the pin definition of SPI interface.

Table 14: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain. If unused, keep them open.
SPI_MOSI	27	DO	SPI master-out slave-in	
SPI_MISO	28	DI	SPI master-in slave-out	

The following figure shows a reference design of SPI interface with peripheral.

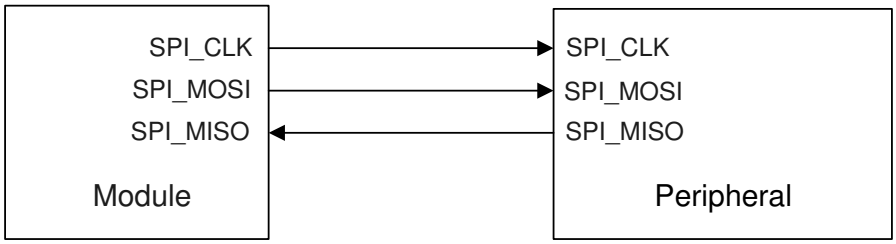


Figure 25: Reference Circuit of SPI Interface with Peripheral

NOTE

The module provides 1.8 V SPI interface. A voltage-level translator should be used between the module and the host if your application is equipped with a 3.3 V processor or device interface.

3.15. Indication Signals

3.15.1. Network Status Indication

The module provides one network indication pin: NETLIGHT. The pin is used to indicate LED status.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network status.

Table 15: Pin Definition of Network Status Indication

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep it open.

Table 16: Working State of Network Status Indication

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Blink slowly (200 ms High/1800 ms Low)	Network searching

	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing

A reference circuit is shown in the following figure.

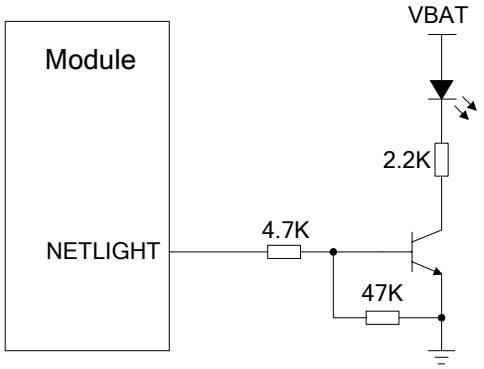


Figure 26: Reference Circuit of Network Status Indication

3.15.2. STATUS

The STATUS pin is set as the module's operation status indicator. It will output high level when the module is turned on normally. The following table describes the pin definition of STATUS.

Table 17: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operating status	1.8 V power domain. If unused, keep it open.

The following figure shows the reference circuit of STATUS.

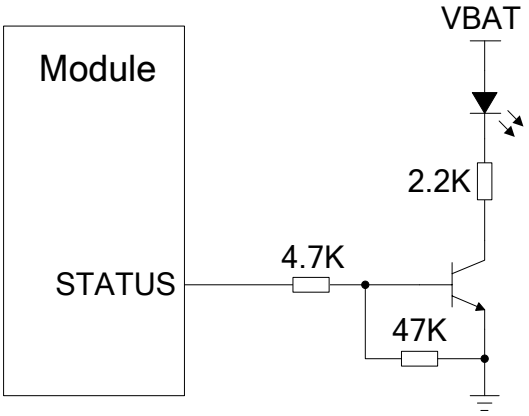


Figure 27: Reference Circuit of STATUS

3.15.3. RI

AT+QCFG="risignaltype","physical" can be used to configure RI behaviors. See ***document [3]*** for details.

No matter on which port (UART port, USB AT port or USB modem port) a URC is presented, the URC will trigger the behaviors of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG**. The default port is USB AT port. See ***document [2]*** for details.

The default behaviors of the RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document [3]*** for details.

Table 18: Default Behaviors of RI

State	Response
Idle	RI keeps at high level.
URC	RI outputs 120 ms low pulse when a new URC returns.

3.16. ADC Interface

The module provides one analog-to-digital converter (ADC) interface. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. For more details about the command, see ***document [2]***.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded by ground.

Table 19: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	If unused, keep it open.

The following table describes the characteristics of ADC interface.

Table 20: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	-	15	bits

NOTE

1. It is prohibited to supply any voltage to ADC pins when ADC pin is not powered by VBAT.
2. It is recommended to use resistor divider circuit for ADC application.

3.17. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before VDD_EXT is powered up, and the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 21: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter download mode	1.8 V power domain. Active high. A test point is recommended to be reserved.

The following figures show the reference circuit of the USB_BOOT interface and the timing sequence of entering forced download mode.

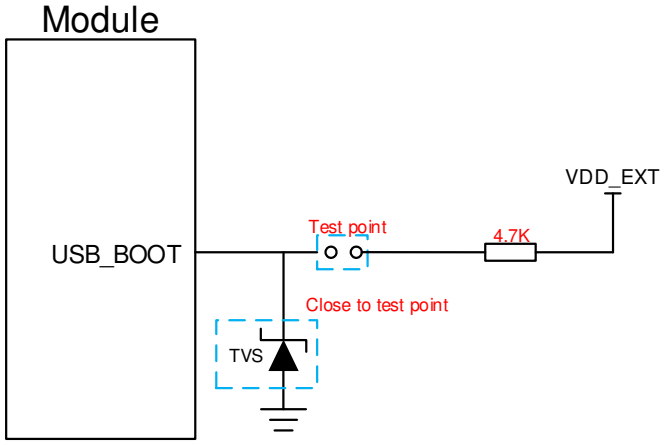


Figure 28: Reference Circuit of USB_BOOT Interface

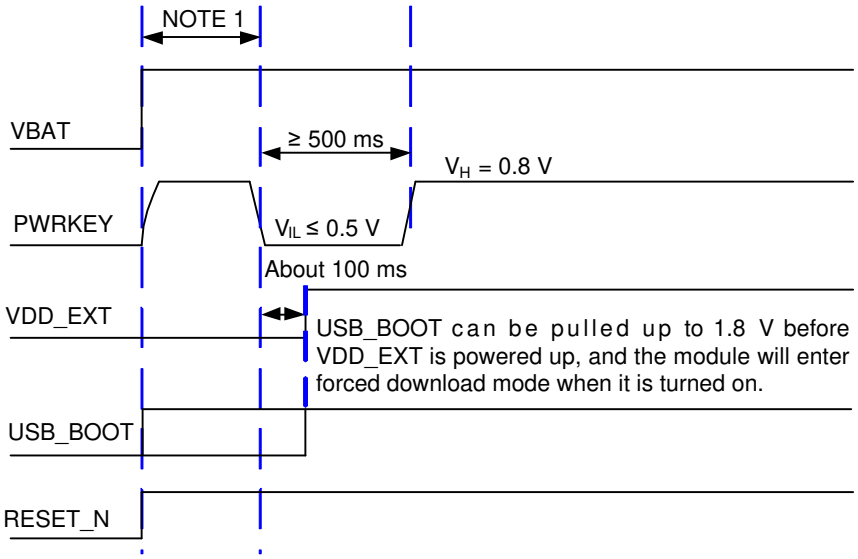


Figure 29: Timing of Entering Forced Download Mode

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. When using MCU to control the module to enter the forced download mode, follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Short the test points as shown in ***Figure 28*** can manually force the module to enter download mode.

4 RF Specifications

The impedance of the antenna port is 50 Ω. The antenna interfaces of the module are shown as follow:

- One main antenna interface
- One Rx-diversity antenna interface (which is used to resist the fall of signals caused by high-speed movement and multipath effect)
- One GNSS antenna interface

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

4.1. Celluar Network

4.1.1. Antenna Interfaces & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 22: Pin Definition of RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep them open.
ANT_DIV	56	AI	Diversity antenna interface	

Table 23: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
LTE FDD B2	1850–1910	1930–1990	MHz
LTE FDD B4	1710–1755	2110–2155	MHz
LTE FDD B5	824–849	869–894	MHz
LTE FDD B12	699–716	729–746	MHz
LTE FDD B13	777–787	746–756	MHz

LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz

4.1.2. Tx Power

The following table shows the Tx power of the module.

Table 24: Tx Power

Frequency Band	Max. Tx Power	Min. Tx Power
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE-FDD bands	23 dBm ±2 dB	< -39 dBm

4.1.3. Rx Sensitivity

The following tables show the conducted RF receiver sensitivity of the module.

Table 25: Conducted RF Receiver Sensitivity

Frequency Band	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.4 dBm	-100 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.6 dBm	-99 dBm	-102.2 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.1 dBm	-99.9 dBm	-102.7 dBm	-93.8 dBm

4.1.4. Reference Design

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default. Place the π-type matching components (R1/C1/C2, R2/C3/C4) as close to the antenna as possible.

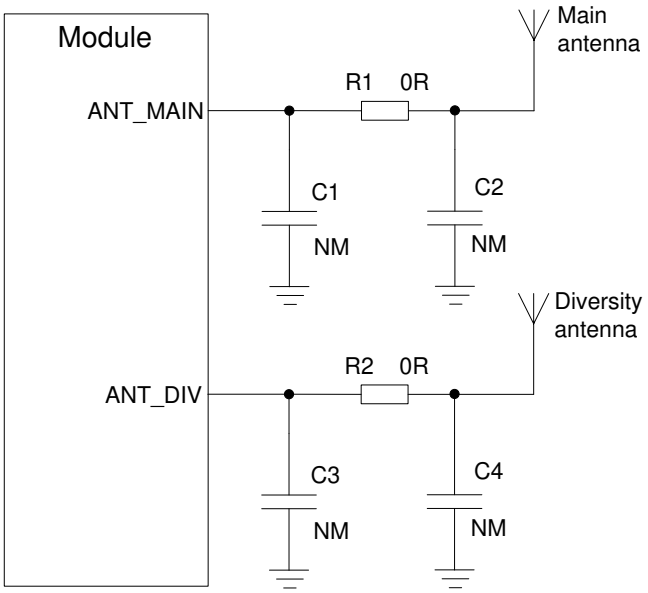


Figure 30: Reference Circuit of RF Antenna Interface

NOTE

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiver sensitivity.
2. For the operation of ANT_MAIN and ANT_DIV, see **AT+QCFG="divctl"** in ***document [3]*** for details.

4.2. GNSS (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.
It supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine of the module is turned off by default. It has to be turned on via AT command. For more details about GNSS engine technology and configurations, see ***document [6]***.

4.2.1. Antenna Interfaces & Frequency Bands

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 26: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 27: GNSS Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

4.2.2. GNSS Performance

The following table shows GNSS performance of the module.

Table 28: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF	Cold start @ open sky	Autonomous	34.6	s
		XTRA start	11.57	s
	Warm start @ open sky	Autonomous	26.09	s
		XTRA start	3.7	s
	Hot start @ open sky	Autonomous	1.8	s
		XTRA start	3.4	s
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.

3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.2.3. Reference Design

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design.

A reference design of GNSS antenna is shown as below.

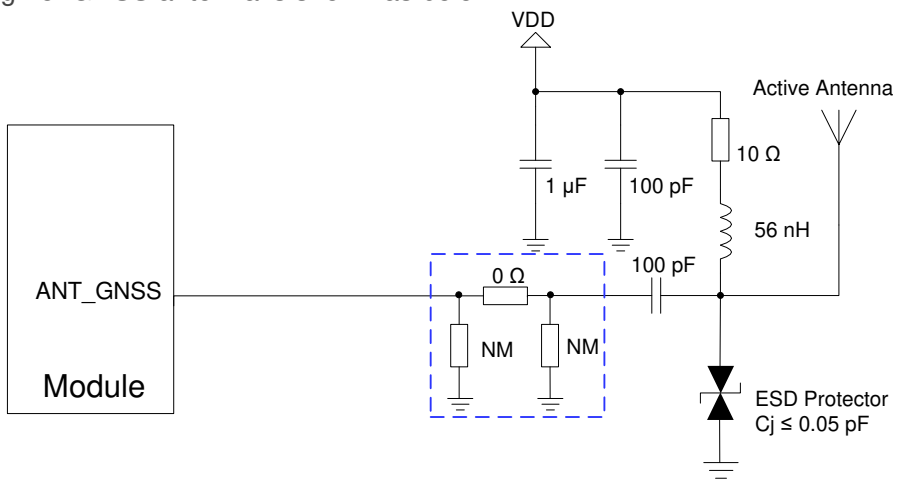


Figure 31: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, you will not need the VDD circuit.
3. It is recommended to use a passive antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

4.2.4. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50 Ω.

4.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and

grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

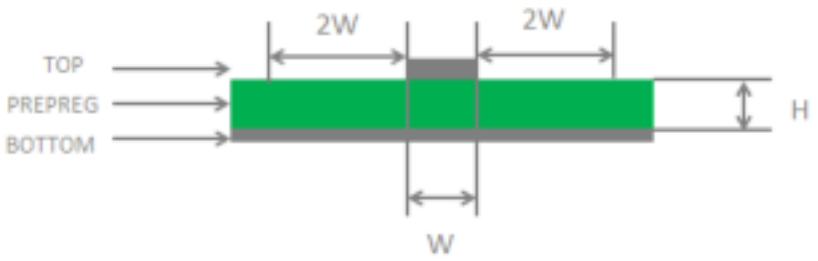


Figure 32: Microstrip Design on a 2-layer PCB

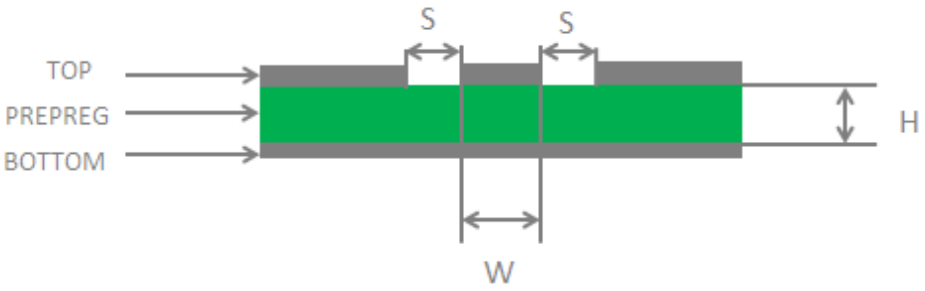


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

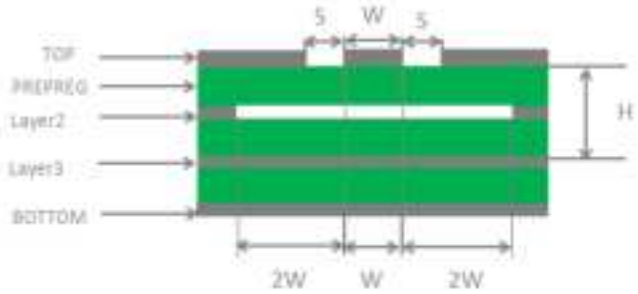


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

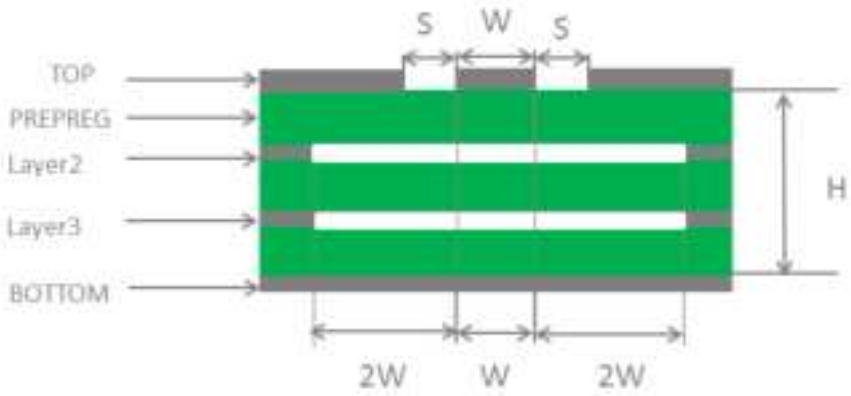


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, refer to ***document [7]***.

4.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 29: Antenna Requirements

Type	Requirements
GNSS (Optional)	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: ≤ 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna embedded LNA gain: < 17 dB
Cellular	VSWR: ≤ 2 Efficiency: > 30 % Gain: 1 dBi Max. input power: 50 W Input impedance: 50 Ω Vertical polarization Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

4.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

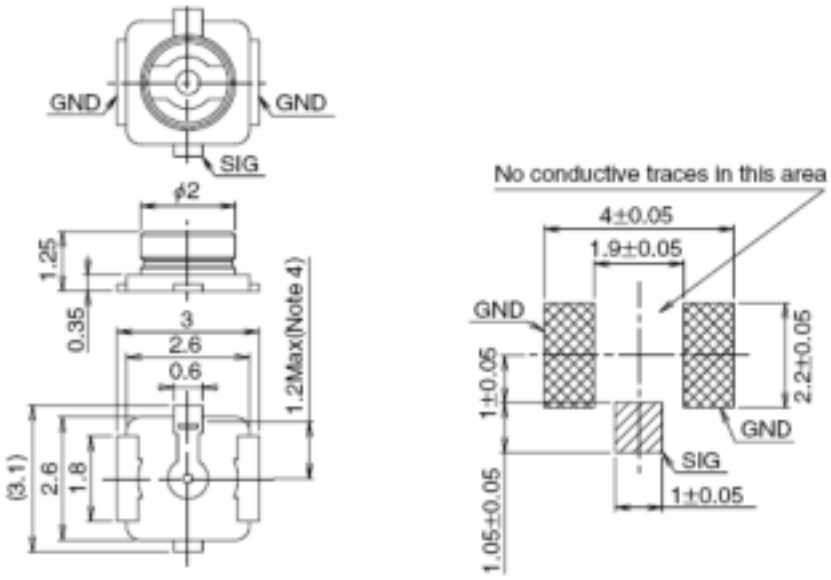


Figure 36: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

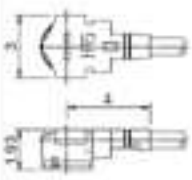
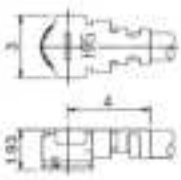
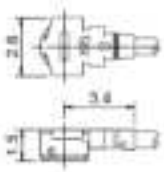
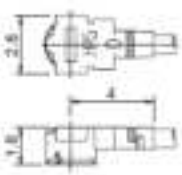
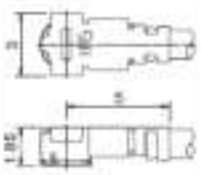
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

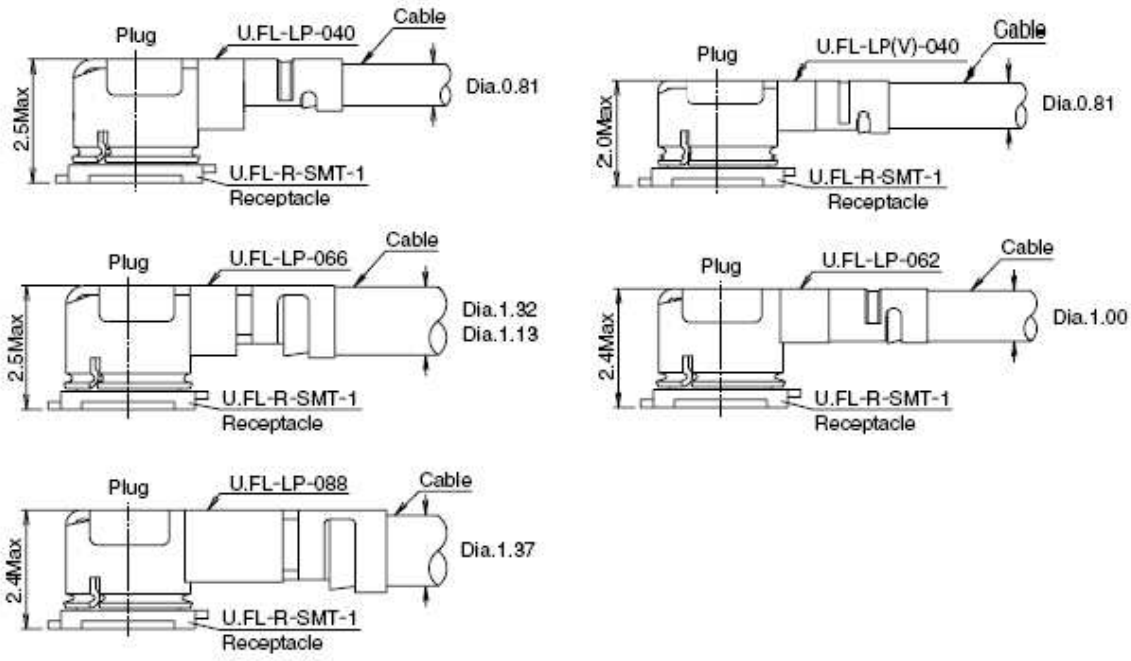


Figure 38: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 30: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.3	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 31: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak supply current	At maximum power control level	-	-	1.5	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 32: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [3]	-35	+25	+75	ºC
Extended Temperature Range [4]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

5.4. Power Consumption

Table 33: Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	9	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
	WCDMA PF = 64 (USB disconnected)	2.1	mA
	WCDMA PF = 64 (USB suspend)	2.2	mA
	WCDMA PF = 512 (USB disconnected)	1.6	mA
	LTE-FDD PF = 64 (USB disconnected)	2.6	mA
	LTE-FDD PF = 64 (USB suspend)	2.7	mA
	LTE-FDD PF = 256 (USB disconnected)	1.8	mA
Idle state	WCDMA PF = 64 (USB disconnected)	16.7	mA
	WCDMA PF = 64 (USB connected)	32.2	mA
	LTE-FDD PF = 64 (USB disconnected)	14.0	mA
	LTE-FDD PF = 64 (USB connected)	32.6	mA
WCDMA data transmission	WCDMA B2 HSDPA @ 21.74 dBm	528	mA
	WCDMA B2 HSUPA @ 21.47 dBm	536	mA

[3] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.
[4] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

	WCDMA B4 HSDPA @ 22.67 dBm	542	mA
	WCDMA B4 HSUPA @ 22.30 dBm	550	mA
	WCDMA B5 HSDPA @ 22.63 dBm	523	mA
	WCDMA B5 HSUPA @ 22.31 dBm	523	mA
LTE data transmission	LTE-FDD B2 @ 23.08 dBm	694	mA
	LTE-FDD B4 @ 23.31 dBm	691	mA
	LTE-FDD B5 @ 23.23 dBm	586	mA
	LTE-FDD B12 @ 23.03 dBm	613	mA
	LTE-FDD B13 @ 23.13 dBm	626	mA
	LTE-FDD B25 @ 22.96 dBm	689	mA
	LTE-FDD B26 @ 23.11 dBm	636	mA

5.5. GNSS Power Consumption

Table 34: GNSS Power Consumption

Description	Conditions	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Passive antenna	54	mA
	Hot start @ Passive antenna	54	mA
	Lost state @ Passive antenna	53	mA
Tracking (**AT+CFUN=0**)	Open sky @ Passive antenna	32	mA

5.6. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 35: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

5.7. Thermal Dissipation

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On your PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier and power supply.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to your application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and you can choose one or both of them according to their application structure.

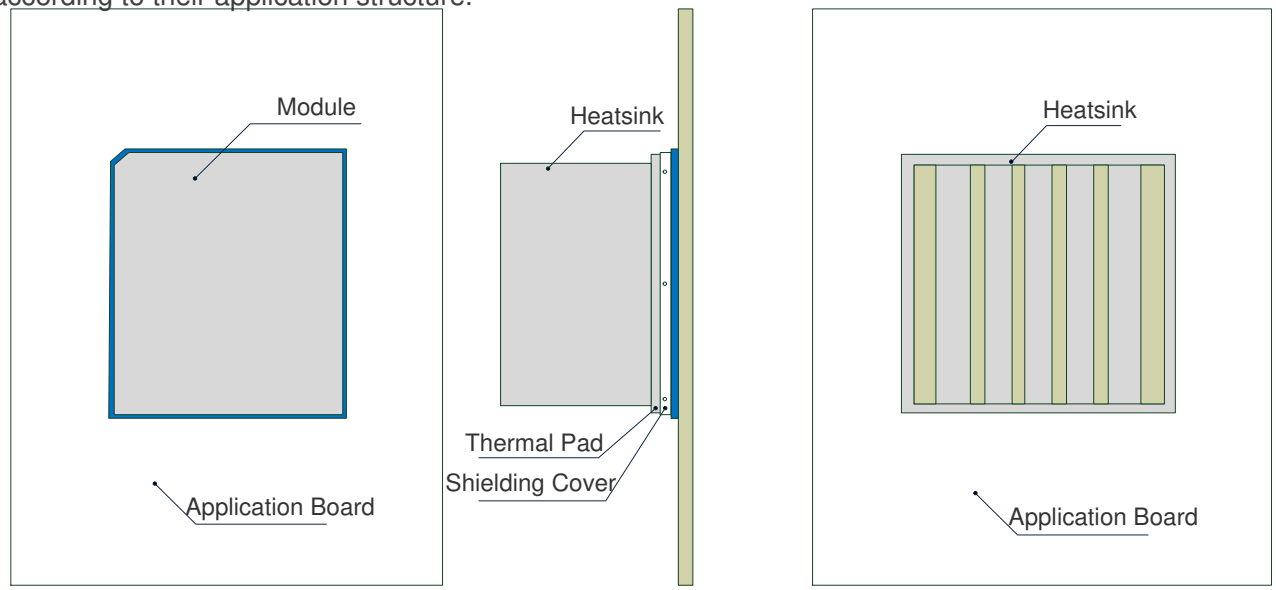


Figure 39: Referenced Heatsink Design (Heatsink at the Top of the Module)

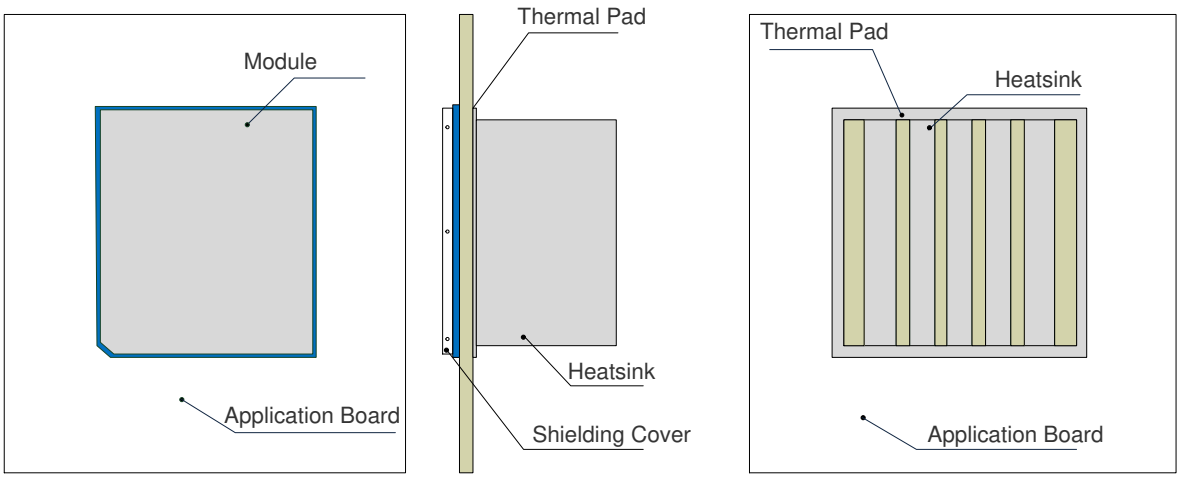


Figure 40: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTE

The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power and data rate). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. You can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value. For more details, see ***document [8]***.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

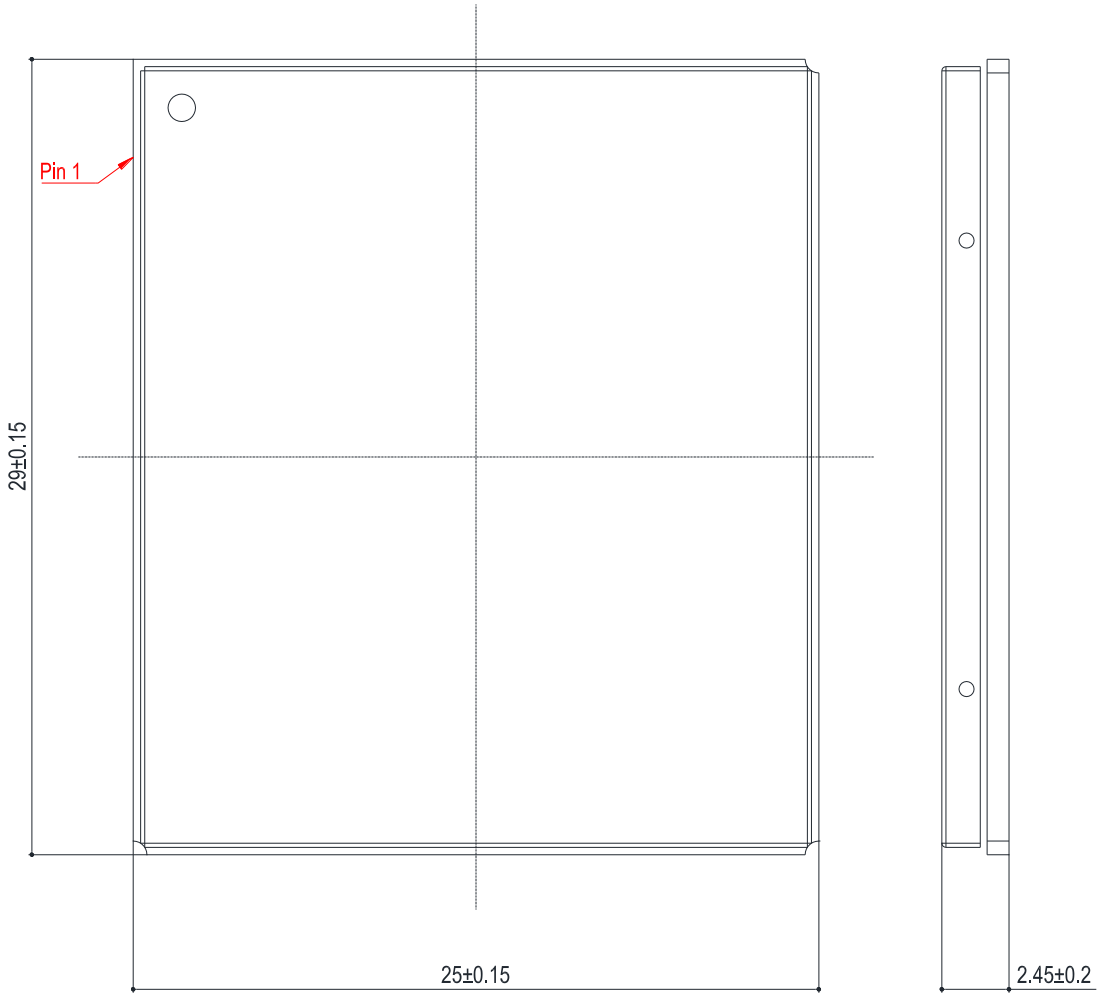


Figure 41: Top and Side Dimensions

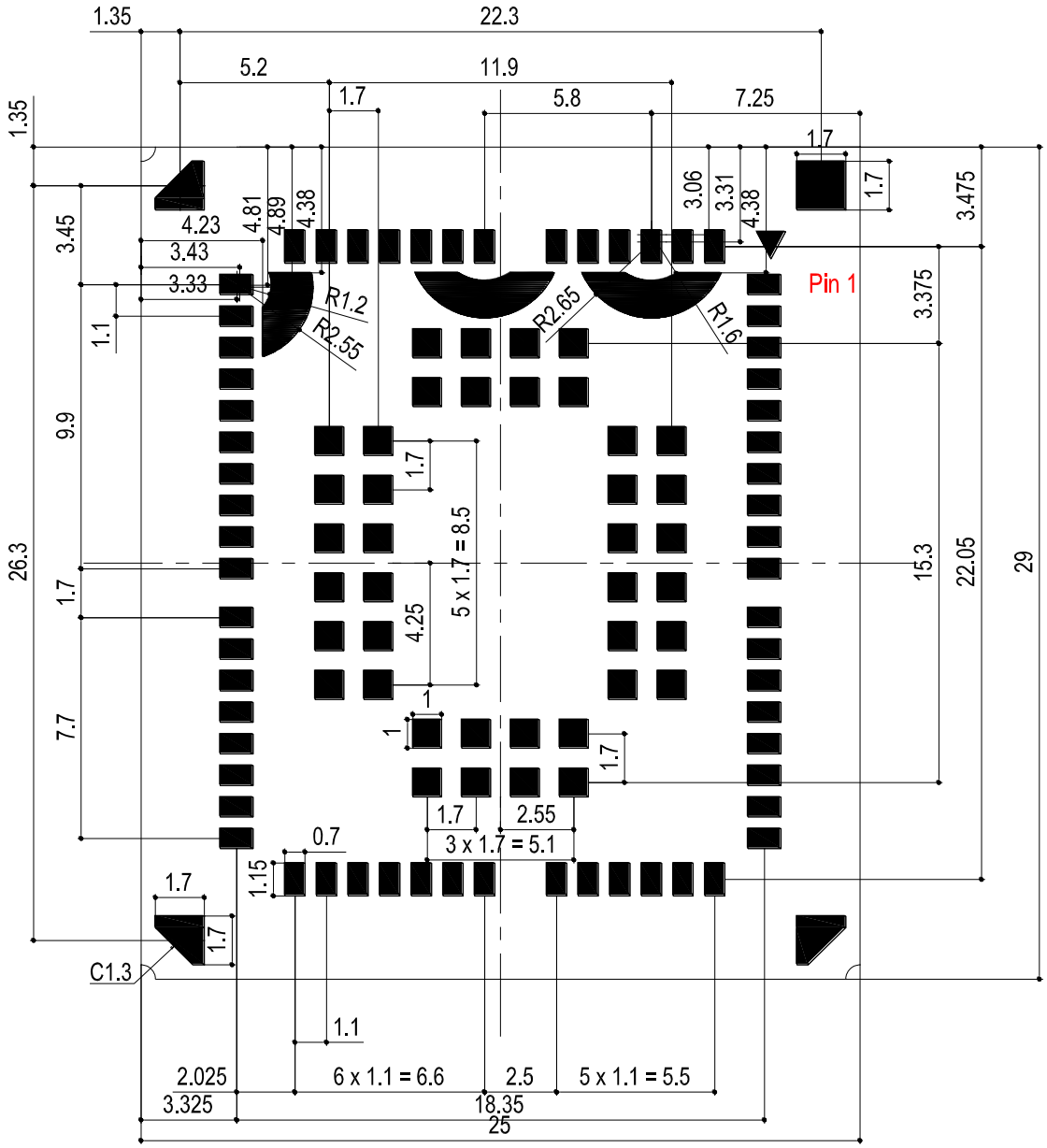


Figure 42: Bottom Dimensions (Top View)

NOTE

The package warpage level of the module refers to *JEITA ED-7306* standard.

6.2. Recommended Footprint

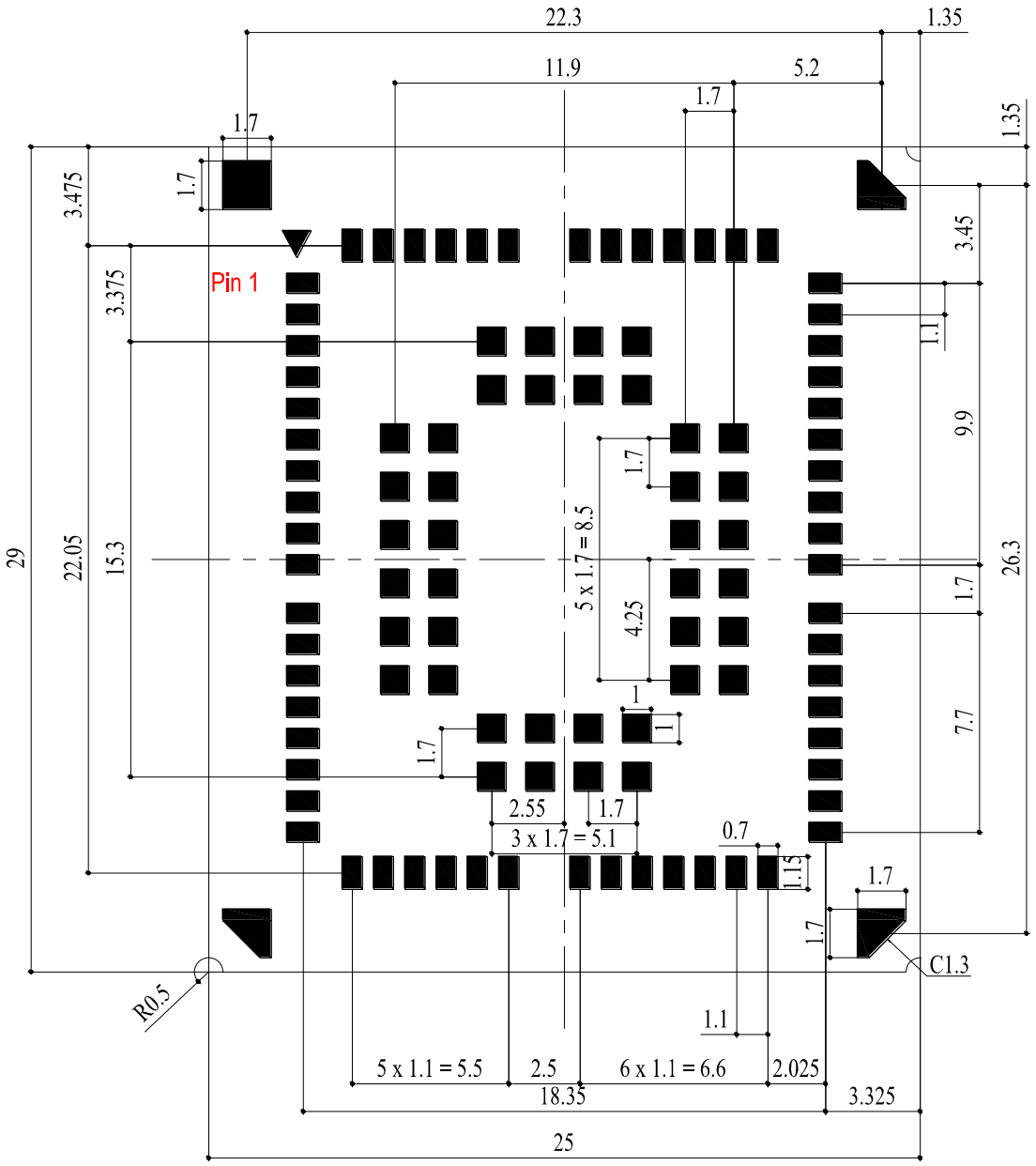


Figure 43: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

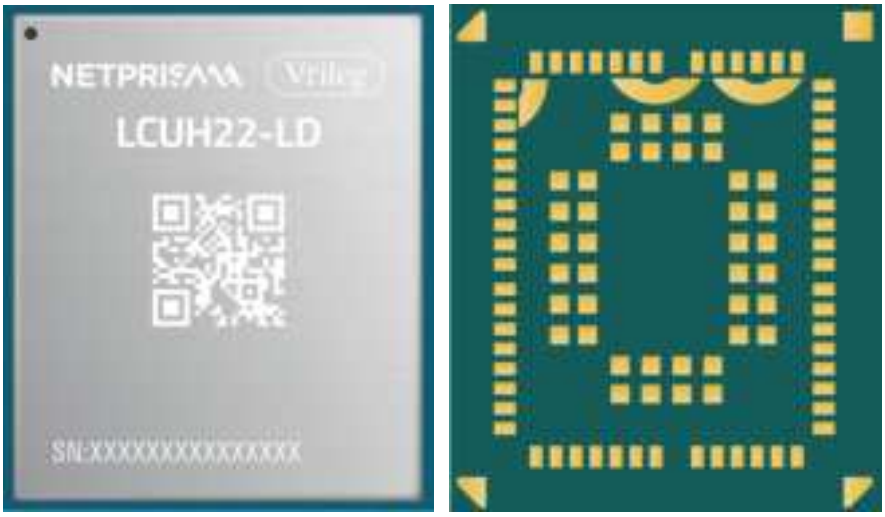


Figure 44: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours [5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.18 mm. For more details, see ***document [9]***.

[5] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

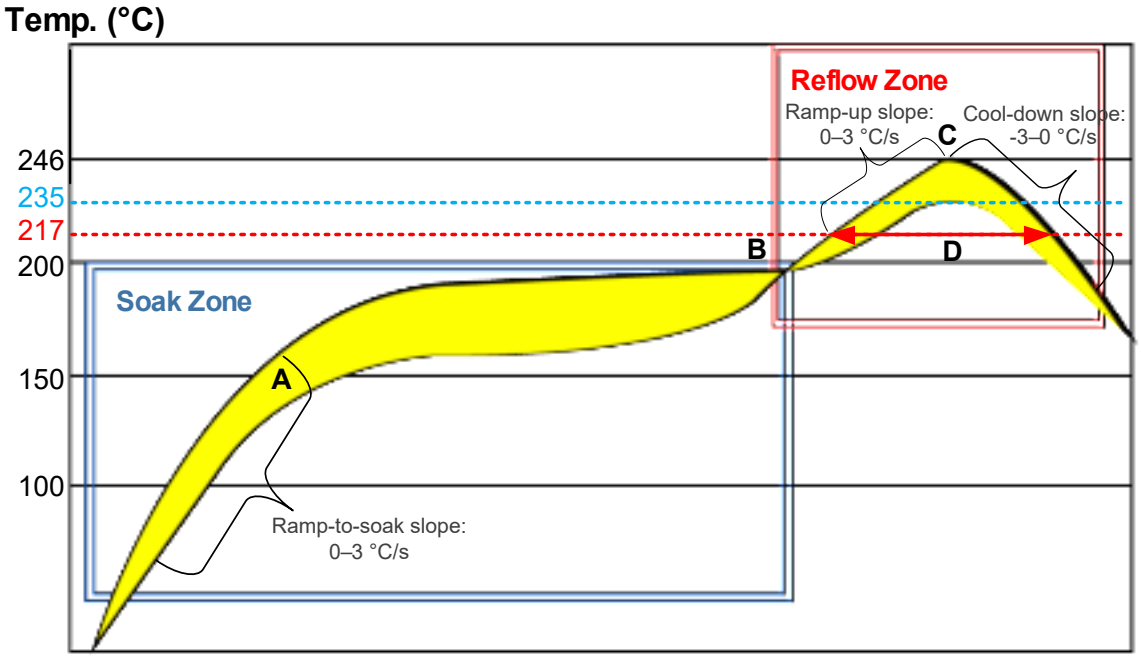


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 36: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [10]***.

7.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table.

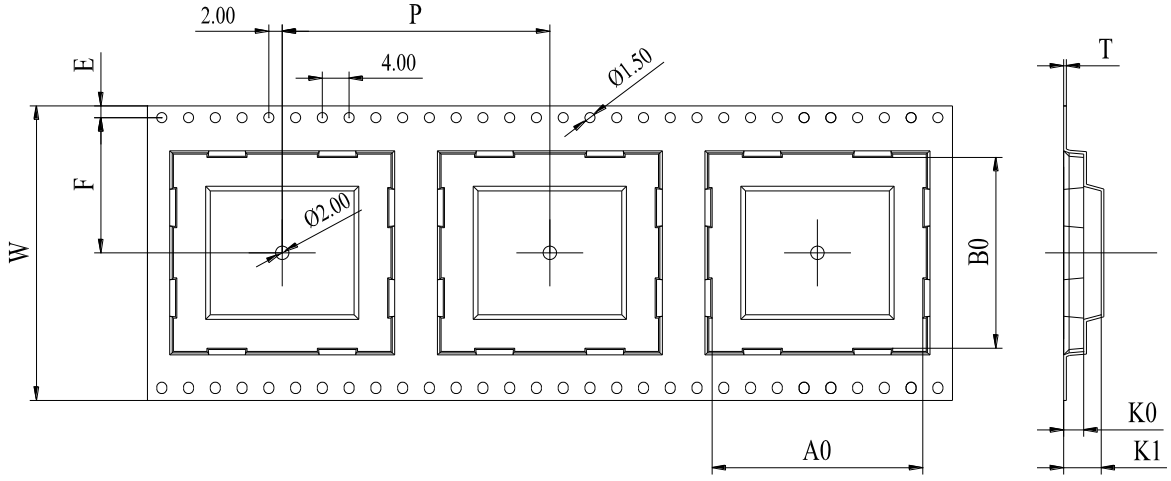


Figure 46: Carrier Tape Dimension Drawing (Unit: mm)

Table 37: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

NOTE

Actual pads in kind prevail when mounting.

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

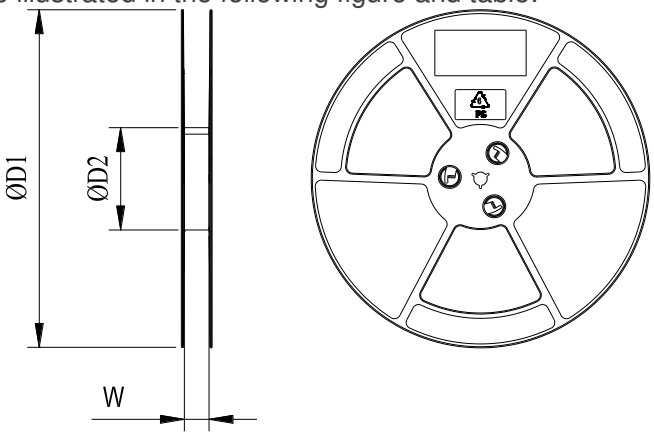


Figure 47: Plastic Reel Dimension Drawing

Table 38: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

7.3.3. Mounting Direction

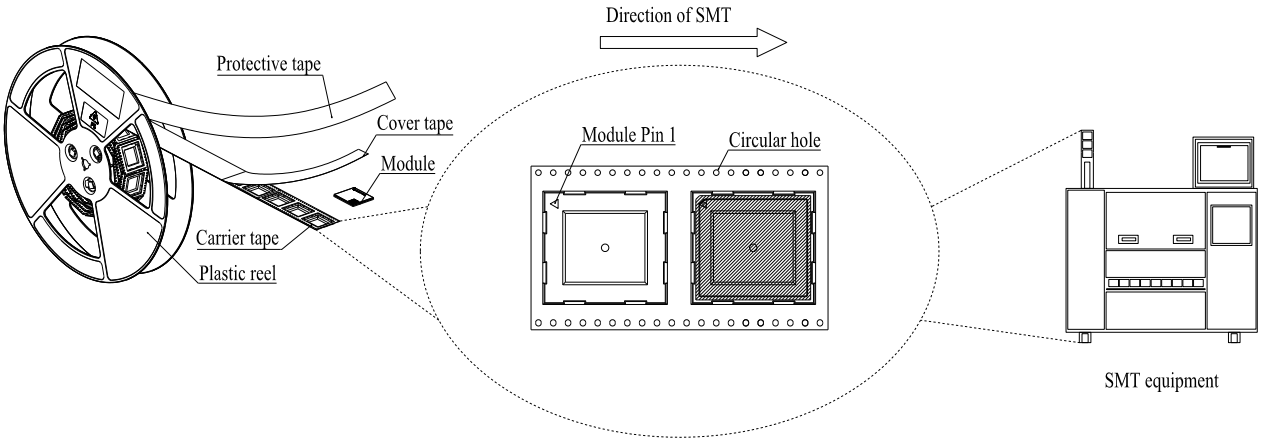
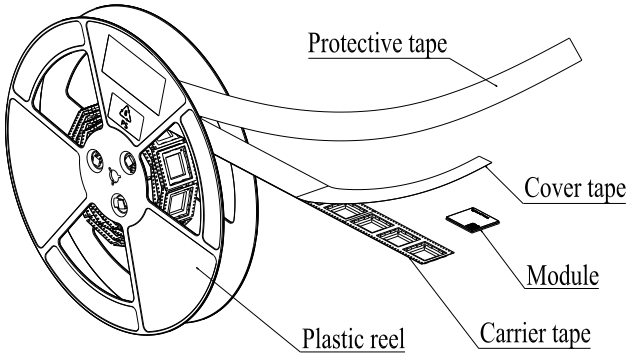


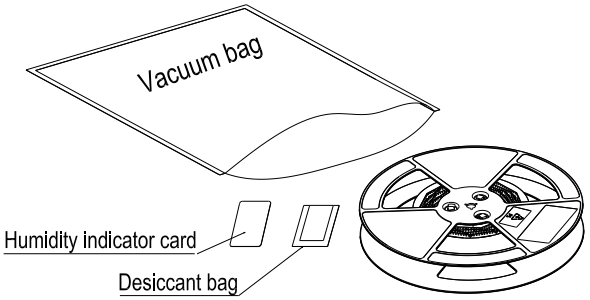
Figure 48: Mounting Direction

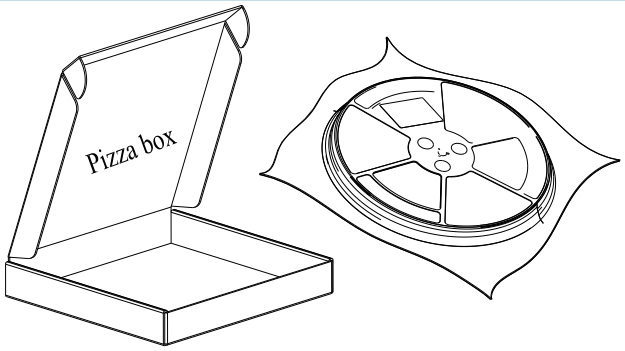
7.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

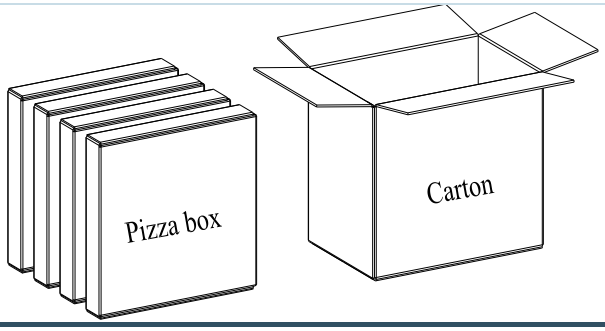


Figure 49: Packaging Process

8 Appendix References

Table 39: Related Documents

Document Name
[1] NetPrisma_UMTS&LTE_EVB_User_Guide
[2] NetPrisma_LCUH22-LD_AT_Commands_Manual
[3] NetPrisma_LCUH22-LD_QCFG_AT_Commands_Manual
[4] NetPrisma_LCUH22-LD_Low_Power_Mode_Application_Note
[5] NetPrisma_LCUH22-LD_AT+QDSIM_Command_Manual
[6] NetPrisma_LCUH22-LD_GNSS_Application_Note
[7] NetPrisma_RF_Layout_Application_Note
[8] NetPrisma_LCUH22-LD_Software_Thermal_Management_Guide
[9] NetPrisma_Module_Stencil_Design_Requirements
[10] NetPrisma_Module_SMT_Application_Note

Table 40: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
Cj	Junction Capacitance
CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear To Send

DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DC-HSPA+	Dual-carrier High Speed Packet Access
DCS	Data Coding Scheme
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output
Inom	Nominal Current
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier

LTE	Long Term Evolution
M2M	Machine to Machine
MCS	Modulation and Coding Scheme
MCU	Microcontroller Unit
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MS	Mobile Station (GSM engine)
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
NAND	Non-volatile Memory Device
NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency

RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTS	Request to Send
Rx	Receive
SAW	Surface Acoustic Wave
SMD	Surface Mount Device
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SMS	Short Message Service
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter.
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USB	Universal Serial Bus
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-evel Input Voltage
V_{IH}min	Minimum High-evel Input Voltage
V_{IL}max	Maximum I Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
$V_I$max	Absolute Maximum Input Voltage

$V_I$min	Absolute Minimum Input Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access