PARTS LIST AND TUNE UP PROCEDURES

(CONFIDENTIALITY REQUESTED)

This exhibit contains a list of the semiconductor devices used in the transceiver and the test equipment and tuning procedures for maintaining the transceiver.

EXHIBIT 10A Function of RF Semiconductors and Other Active Devices

EXHIBIT 10B List of Recommended Test Equipment for Servicing

EXHIBIT 10C Tune Up Information

Exhibit 10A - Function of RF Semiconductors & Other Active Devices

Pursuant to 47 CFR 2.10339(c)(10)

REF	PART	CIRCUIT	OPERATING	INDUSTRY
NO.	NUMBER	APPLICATION	FREQUENCY	EQUIVALENT
CR1	4813825A19	RF LIMITER	403 - 440 MHz	MMBD352
CR41	4802246J04	RX FIRST MIXER	44.85 - 440 MHz	HSMS2829
CR51	4813825A19	RF LIMITER	44.85 MHz	MMBD352
D51	4802245J97	RF SWITCH	455 kHz	DAN235ETL
D52	4802245J97	RF SWITCH	455 kHz	DAN235ETL
D120	4880973Z02	TX ANTENNA SERIES SWITCH	403 - 440 MHz	MA4PH261
D121	4809948D12	RX ANTENNA SHUNT SWITCH	403 - 440 MHz	MA4PH261
D201	4862824C03	REF OSC FREQ CONTROL	16.8 MHz	1SV232
D220	4802233J09	VOLTAGE MULTIPLIER VOLTAGE MULTIPLIER RX VCO FREQ CONTROL TX VCO FREQ CONTROL TX VCO MODULATOR	1.05 MHz	IMN10
D221	4802233J09		1.05 MHz	IMN10
D251	4862824C01		358.15 – 395.15 MHz	1SV229
D261	4862824C01		403 - 440 MHz	1SV229
D262	4862824C01		AUDIO - 440 MHz	1SV229
D301	4813833A19	REVERSE POLARITY PROTECT	DC	MBRM120ET3
D414	4805129M41	BOOT CONTROL	DC	MMBD501
D424	4809924D18	BATT CHEMISTRY DETECT	DC	RB520S-30
D440	4805729G49	RED/GRN LED INDICATOR	DC	BRPY1204W
D470	4809924D18	BATT CHARGER	DC	RB520S-30
D471	4809924D18	BOOT/RESET LOGIC	DC	RB520S-30
D491	4805129M41	AUDIO AGC CONTROL	AUDIO	MMBD501
Q21	4802247J01	RF AMPLIFIER CURRENT MIRROR FIRST I-F AMPLIFIER RX DETECTOR BUFFER TX PRE-DRIVER CURRENT-VOLTAGE CONVERTER	403 - 440 MHz	BFS505
Q22	4805723X02		DC	UMT1
Q51	4802197J95		44.85 MHz	PBR941
Q70	4880214G02		455 kHz	MMBT3904
Q100	4885593U03		403 - 440 MHz	BFG540W
Q150	4880214G02		DC	MMBT3904
Q170	4809939C34	TX DC SWITCH TX DC SWITCH RX VCO BUFFER AMP DC SWITCH DC SWITCH DC SWITCH	DC	EMB10
Q171	4880048M01		DC	DTC144EKA
Q280	4802245J95		358.15 – 395.15 MHz	BFS540
Q311	4809579E18		DC	TP0101T
Q312	4809579E18		DC	TP0101T
Q313	4802245J54		DC	UMG5
Q402	4880048M01	DC SWITCH DC SWITCH DATA SWITCH DC SWITCH DC SWITCH BOOT/RESET LOGIC	DC	DTC144EKA
Q403	4813824A17		DC	MMBT3906
Q410	4802245J54		≤ 19.2 kHz	UMG5
Q440	5180159R01		DC	IMX1
Q470	4805723X02		DC	UMT1
Q471	4802245J54		DC	UMG5

Exhibit 10A - Function of RF Semiconductors & Other Active Devices (cont'd)

Q472	4805723X02	BOOT/RESET LOGIC AUDIO SWITCH AUDIO SWITCH DC/AUDIO SWITCH DC SWITCH DC SWITCH DC SWITCH DC SWITCH	DC	UMT1
Q481	4813824A17		AUDIO	MMBT3906
Q482	4813824A10		AUDIO	MMBT3904
Q490	4802245J54		DC - AUDIO	UMG5
Q493	4809579E18		DC	TP0101T
Q494	4802245J54		DC	UMG5
Q520	5180159R01		DC	IMX1
U51	5186144B01	RECEIVER SYSTEM DC SWITCH TX RF POWER AMP MODULE TRANSMITTER POWER CONTROL	AUDIO - 44.85 MHz	SA616
U52	5109522E10		DC	TC7W04F
U110	0186438Z03		403 - 440 MHz	RA07M4047M
U150	5113818A01		DC	LM2904
U201	5185963A27	FREQUENCY SYNTHESIZER VCO/BUFFER IC VOLTAGE REGULATOR VOLTAGE REGULATOR VOLTAGE REGULATOR	1.05 - 440 MHz	63A27
U251	5105750U54		358.15 - 440 MHz	50U54
U310	5102478J01		DC	TK71750S
U320	5185963A55		DC	LP2986
U330	5102479J01		DC	TK71730S
U401	5102226J56	MICROPROCESSOR	7.4 MHz	MC68HC11FL0
U402	5102463J64	EEPROM	1 MHz	X25128-2.7
U404	5102480J01	FLASH ROM	1.85 MHz	AT49HLV001
U451	5185130C53	AUDIO FILTER	AUDIO - 16.8 MHz	30C53
U480	5113818A01	AUDIO AMPLIFIER	AUDIO	LM2904
U490	5108858K99	AUDIO POWER AMPLIFIER	AUDIO	TDA8541
U510	5113818A01	AUDIO AMPLIFIER	AUDIO	LM2904
VR110 VR301 VR302 VR471 VR472 VR473 VR474 VR475	4813830A86 4813830A33 4813830A33 4813830A18 4813830A09 4813830A33 4813830A33 4880140L20	ESD PROTECTION ESD PROTECTION ESD PROTECTION DC LEVEL DETECTOR DC LEVEL DETECTOR ESD PROTECTION ESD PROTECTION ESD PROTECTION	DC DC DC DC DC DC DC DC	MM3Z3V9T1 MMBZ5250B MMBZ5250B MMBZ5235B MMBZ5226B MMBZ5250B MMBZ5250B MMBZ5250B

Exhibit 10B - List of Recommended Test Equipment for Servicing

Instrument	Recommended Type	Application
RF Signal Generator *	HP 8656B or equivalent	Receiver Measurements
Modulation Analyzer *	HP 8901B or equivalent	Frequency and Deviation Measurements
Audio Analyzer *	HP 8903A or equivalent	Receiver Measurements
Power Meter *	HP 438A or equivalent	Transmitter Power Output
Power Sensor *	HP 8482A or equivalent	Transmitter Power Output
DC Power Supply	0-20 volts at 15 amps	
Attenuator Pad *	50 Ω , 75 Watts, 30 dB	Transmitter Measurements
DC Ammeter	30 mA to 20 A	Current Drain Measurements
Computer	IBM PC, PC/XT or PC/AT	Radio Alignment
Radio Interface Box	RLN4008E	Computer Interface to Radio
Cable	3080369B72	From RIB to Computer
Cable	AAPMKN4004	From RIB to Radio
Software	RVN4191	Radio Alignment

^{*} These items can be replaced by a Motorola 2000 Series Communications System Analyzer or equivalent piece of integrated communications test equipment.

Exhibit 10C - Tune Up Information

Pursuant to 47 CFR 2.10339(c)(9)

All transmitter adjustments are performed by electronic means. The transmitter contains no electromechanical components for the purpose of transmitter tuning or adjustment.

The tuning elements that are used for transmitter adjustment are:

Location	Type of Element	Function
U401	Microprocessor	Supplies data to Audio Filter IC, Fractional-N Synthesizer, Temperature Compensated Crystal Oscillator, and Power Control IC for Transmitter Modulation, Frequency and Power Adjustment
U201	Programmable Attenuator	Reference Modulation Balance
U451	Programmable Attenuator	Deviation Adjustment
U201	Digital to Analog Converter	Transmitter Frequency Adjustment
U451	Digital to Analog Converter	Transmitter Power Adjustment

The value of a particular tuning element is determined by data sent to that tuning element by microprocessor U401. This data is generated by the microprocessor based on tuning information that is stored in the EEPROM (Electrically Erasable Programmable Read Only Memory).

Tuning information is stored in the EEPROM during factory adjustment or by qualified field service facilities, using the attached procedure and recommended test equipment.

Tuning Procedure

1. Reference Oscillator Warping

- 7.1 FLASH THE RADIO WITH THE APPROPRIATE CODE FOR THE MODEL BEING TUNED.
- 7.2 DOWNLOAD DEFAULT CODEPLUG
- 7.3 SCAN THE 2D BARCODE OF THE REFERENCE XTAL (FOR REFERENCE ONLY)
 - 7.3.1 DECODE OF THE BARCODE
 - a) Decode the crystal code to get crystal inflection temperature (xtal_infl_temp) and crystal curve ppm(t) (crystal ppm at given temperature) and store them, xtal_infl_temp and xtal_curve_ppm(t). The following equations are used to calculate the above parameters

```
xtal_infl_temp = 22+A+B/10
a1 = (C+D/10+E/100)^*(-0.1)
a3 = (8.20+(C+D/10+E/10)(0.2)+(F+G/10+H/100)(.02)^*(.00001)
```

```
delta_temp=temps(t)-ref_temp
xtal curve ppm(t) =a1*delta temp+a3*delta temp^3
```

where

```
A = Digit 1, B = Digit 2, C = Digit 3, D = Digit 4, E = Digit 5, F = Digit 6, G = Digit 7, H = Digit 8 temps(t): Array of temperature in steps of 5 deg C from -35 deg C to 90 deg C
```

7.4 TEMPERATURE COMPENSATION TUNING (FOR REFERENCE ONLY)

7.4.1 OSCILLATOR SENSITIVITY MEASUREMENT

- a) Use SBEP command to program synthesizer to receive frequency F1 of table 8.2 and also set the INFLECTION, COLD, HOT AND LINEAR dacs to maximum to turn them off (INFLECTION dac=63, COLD dac=127, HOT dac=127, LINEAR dac=63)
- b) Use SBEP command to adjust warp dac to get frequency F1 within +/- 0.2 ppm. Store warp dac value in warp dac center
- c) Indicate the PASS/FAIL status of the warp dac value. If FAIL: "Failed set warp dac value" warp_dac_center must fall within range of 64 to 391
- d) Obtain warp_dac_high and warp_dac_low using the equations below:

```
warp_dac_high = INT(warp_dac_center+(64))
warp_dac_low = INT(warp_dac_center-(64))
```

where

```
warp_dac_step_v = 0.0065 v/step
approx_sens = 20 ppm/v
```

- e) Use SBEP command to program the radio to warp dac high
- f) Use DMM to get voltage reading. Store it in V_H
- g) Use frequency counter to get frequency reading. Store it in F_H
- h) Use SBEP command to program the radio to warp dac low
- i) Use DMM to get voltage reading. Store it in V_L
- j) Use frequency counter to get frequency reading. Store it in F_L
- k) Calculate the oscillator sensitivity using the equation below.

```
comp_range_v=V<sub>L</sub>-V<sub>H</sub>
ppm_range=[(F<sub>L</sub>-F<sub>H</sub>)/F<sub>H</sub>]*10^6
osc_sens=ABS(ppm_range/ comp_range_v)+osc_sens_offset
```

where

osc_sens=The sensitivity of the oscillator's frequency to the voltage applied to the varactor osc sens offset= 0

7.4.2 TRANSLATE CRYSTAL'S PPM CURVE INTO VOLTAGE CURVE

 a) Convert the crystal ppm curve vs. temperature to voltage vs. temperature curve as follows;

V(t)=[(xtal_curve-ppm(t)+osc_contrib(t)]/osc_sens

Where

V(t)=voltage at given temperature osc_contrib(t)=Currently equal to zero osc sens=determined in 7.4.1.k

b) Invert the voltage vs. temperature curve for compensation procedure as follows;

```
comp_curve_v(t)=comp_curve_vref+reg_contrib(t)-V(t)
```

where

comp_curve_v(t)=inverted voltage at given temperature comp_curve_vref=1/2 of VRO=2.500V req-contrib(t)=Currently equal to zero V(t)=voltage at given temperature calculated in 7.4.2a)

7.4.3 SEARCH THE IC'S T.C. TABLE FOR BEST COMPENSATION CURVE

 a) Compare the converted crystal curve to the table of compensation of voltage curves located in the file given to the factory to find the curve which gives the minimum error over the entire temperature range. The curve fitting would give cold, hot and linear dacs values

7.4.4 ALIGN THE CRYSTAL CURVE TO THE ICIS COMPENSATION CURVE

- a) Send SBEP command to program the LVFRACN with a warp value of warp_daccenter found in 7.4.1(a) with cold, hot and linear dacs off and inflection at mid point,
 63
- b) Measure the voltage on the IC's WARP pin . Store it in ic infl ref
- c) Send SBEP command to program the LVFRACN with inflection, cold, hot and linear dacs to settings in 7.4.3(a). If linear dac > 50, set it to 50 (for this step only).
- d) Use SBEP command to adjust inflection dac setting to get the WARP voltage as close to the ic_infl_ref in 7.4.4(b). Store it in ic_infl_set_amb
- e) Use thermo-hunter to get the temperature at the LVFRACN. Store it in ic_temp
- f) Calculation of inflection dac setting using the equation below;

where

infl_dac=inflection dac value
ic_infl_set_amb=inflection dac value in 7.4.4(d)
ic_temp=temperature measured in 7.4.4(e)
xtal_infl_temp=temperature read from 2D code in 7.3.1(a)
constants:
infl_dac_step=0.33 deg/step
infl_tmp_offset=0 deg

g) Use SBEP command to save inflection, cold, hot and linear dac settings in the codeplug

7.5 REFERENCE OSCILLATOR WARPING (FINAL WARP, DONE IN RX MODE)

a) Use SBEP command to adjust warp dac setting to obtain RX frequency F4 of table 8.2.

Frequency adjustment tolerance:

UHF radios: ± 0.2 ppm

b) Use SBEP command to save warp dac setting in codeplug

Note: The actual frequency measured in step (a) will be the frequency in Table 8.2 plus or minus the I-F frequency (depending weither high-side or low-side injection is used). The frequency is measured at the LO TEST point.

For UHF radios: F4 – 44.85 MHz

2. Transmitter Power Adjustment

There are 14 bins for power tuning, 7 for the high power setting, 7 for the low power setting on the radio. The center frequency of each tuning bin is given in table 8.2.

- a) Set the radio for the test frequency of the bin to be tuned and for CSQ mode. F1 should be tuned first and then proceed sequentially to F7.
- b) Set the PWR_SET DAC to a value of 255 (\$FF) (DAC $_{MAX}$).
- c) Key the radio and measure the power out of the antenna test port as P_{MAX}.
- d) Dekey the radio.
- e) Set the PWR_SET DAC to a value of 64 (\$40) (DAC_{MIN}).
- f) Key the radio and measure the power out of the antenna test port as P_{MIN}.
- g) Dekey the radio
- h) Interpolate the the PWR_SET DAC value required from:

$$DAC_{REQ} = \{(P_{REQ} - P_{MIN})(DAC_{MAX} - DAC_{MIN})/(P_{MAX} - P_{MIN})\} + DAC_{MIN}$$

- i) Set the PWR SET DAC to a value of DAC_{REQ}.
- j) Key the radio and measure the power out of the antenna test port. Verify that it is within the limits given in table 8.9.4. If it is not within the limits given, Increase or decrease DAC_{REQ} by 1 and repeat steps i) and j) until it is.
- k) Save the DAC_{REQ} value in the approipate codeplug location for the power level and test bin being set.
- Repeat steps a) thru k) until all test frequencies and power levels have been set.

NOTE: If it can be shown that the DAC values required for tuning across the band are linear, then test bins 1, 4, and 7 can be tuned and bins 2,3,5,and 6 can be interpolated. Do not implement this until Development Engineering has verified.

Radio	Power Level	Target Power	Lower Limit	Upper Limit
	High	4.30 W	4.20 W	4.40 W
UHF	Low	1.20 W	1.10 W	1.30 W

Table 8.9.4

3. Modulation Balance and Deviation Limiting Adjustment

- 1.2 BALANCING/LIMITING LOW AND HIGH PORT MODULATION OF THE SYNTHESIZER
 - a) Program the radio for low power using the settings obtained in procedure 8.9 above.
 - b) Program the ASFICCMP to mute the microphone. Set ASFICcmp for FLAT_TX_RTN mode (Flat audio

response) and default attenuator settings.

NOTE: The attenuator settings of the ASFICcmp are defaulted for minimum attenuation (MOD6 - MOD0 = \$3F) before start of balancing. The fractional-N modulation attenuator should be set to 6.4dB, i.e. \$20 (32 decimal).

- c) Program the synthesizer to the lowest transmit tune frequency (F1 from Table 8.2) and set the ADC bits 12-11= "10". These bits set the fractional-N low port sensitivity to a max of 5.0 kHz. Set the Mod Attenuator enable bit to "1" to enable the high port modulation.
- d) Key the radio.
 - e) Apply an 80 Hz tone, 100 mVrms at the external test box "Audio In" input.
 - f) Measure deviation (D1)
 - g) Change the input tone to 3 kHz, 100mVrms and measure deviation (D2)
 - h) Find the ratio in dB using 20log[D1/D2]
 - i) Remove the audio signal by disabling the external TX audio path
 - j) Program the Mod attenuator setting of the fractional-N using the equation below:

Modulation attenuator setting = (current setting at step i) + $-(5 \times (dB \times i))$

- k) Re-enable the External TX audio path .
- I) Repeat steps f) I) until the ratio in dB of step i) is $\leq \pm 0.20$ dB, store modulation attenuator setting to

the appropriate codeplug elements.

Modulation Limiting 25 kHz CHANNEL SPACING

- a) Set radio to the first tuning frequency.
- b) Disable the FLAT TX RTN mode. Select the Ext Mic and key the radio.
- c) Inject at the Ext Mix Input a 1 kHz tone, 80mVrms with the preemphasis enabled and adjust the Mod attenuator of the ASFICcmp to obtain the deviation shown in table 8.10.2 for 25 kHz channel spacing.
- d) Dekey the radio.
- e) Repeat the steps (b) to (e) for all other frequencies shown in Table 8.2.
- f) Store the attenuator settings in the appropriate codeplug elements.

Channel Spacing	Deviation	
25 kHz	4.40 - 4.60 kHz	
12.5 kHz	2.20 - 2.30 kHz	

Table 8.10.2

Modulation Limiting 12.5 kHz CHANNEL SPACING

a) Program the synthesizer ADC bits 12-11 to "11" (reduces deviation sensitivity of the synthesizer).

- b) Set the radio to the highest tuning frequency. F7 from Table 8.2.
- c) Verify that the deviation reduces to the range shown in table 8.10.2 for 12.5 kHz channel spacing.
- d) If tuning is required adjust only the Mod attenuator of the ASFICcmp to ensure the deviation is within the range shown in table 8.10.2 for 12.5 kHz channel spacing.
- e) Store the attenuator setting in the appropriate codeplug element.