ENGINEERING STATEMENT

For Type Certification of

MIDLAND CONSUMER RADIO

Model No: 77-104XL

FCC ID: MMA77104XL

I am an Electronics Engineer, a principal in the firm of Hyak Laboratories, Inc., Springfield, Virginia. My education and experience are a matter of record with the Federal Communications Commission.

Hyak Laboratories, Inc. has been authorized by Midland Consumer Radio to make type certification measurements on the 77-104XL transceiver. These tests were made by me or under my supervision in our Springfield laboratory.

Test data and documentation required by the FCC for type certification are included in this report. It is submitted that the above-mentioned transceiver meets all applicable FCC requirements.

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Rowland S. Johnson

Dated: April 12, 2000

A. INTRODUCTION

The following data are submitted in connection with this request for type certification of the 77-104XL transceiver in accordance with Part 2, Subpart J of the FCC Rules.

The 77-104XL is a double-sideband amplitude modulated transmitter/receiver combination intended for mobile operation in the citizens radio service. The transmitter has 40-channel capability in the 26.965 - 27.405 MHz band utilizing phase locked loop (PLL) technology.

B. GENERAL INFORMATION REQUIRED FOR TYPE ACCEPTANCE
(Paragraph 2.983 of the Rules)

1. Name of applicant: Midland Consumer Radio
2. Identification of equipment: FCC ID: MMA77104XL

a. The equipment identification label is submitted as a separate exhibit.
Photographs of the equipment are submitted as a separate exhibit.

3. Quantity production is planned.

4. Technical description:

a. 6k00A3E emission
b. Frequency range: 26.965 - 27.405 MHz
c. Operating power of transmitter is fixed at the factory at less than 4 watts, AM.
d. Maximum power rating under 95.635(c) of the Rules is 4 watts.
e. The dc voltage and dc currents at final amplifier:

Collector voltage: 13.7 V
Collector current: 611 mA @ 13.8 Vdc.

f. Function of each active semiconductor device:
See Appendix 1.
g. Complete circuit diagram is submitted as a separate exhibit.
A draft instruction book is submitted as a separate exhibit.
The transmitter tune-up procedure is submitted as a separate exhibit.
j. A description of circuits for stabilizing

frequency is included in Appendix 2.

k. A description of circuits and devices employed for suppression of spurious radiation and for limiting modulation is included in Appendix 3.

l. Not applicable.

B. GENERAL INFORMATION...(Continued)

5. Data for 2.985 through 2.997 follow this section.

6. RF_Power_Output (Paragraph 2.985(a),(b)(1) of the Rules)

RF power output in the AM mode was measured with a Bird 4421 RF power meter and a Narda 765-20 50 ohm dummy load. (The transmitter was tuned by the factory.) Power was measured with a supply voltage of 13.8 Vdc and indicated:

Channel	Power, watts
1	4.0
21	4.0
40	4.0

B. MODULATION CHARACTERISTICS

1. AF_Frequency_Response

A curve showing frequency response of the transmitter is shown in Figure 1. Reference level was taken as a 1 kHz tone with 50% modulation, as measured on a Datatech 209 modulation meter, using a Audio Precision TRMS voltmeter and tracking generator.

2. Modulation_Limiting

Curves of AM modulation limiting for both positive and negative peaks are shown in Figures 2a and 2b, respectively. Characteristics at 300, 830, and 2500 Hz are shown using a Datatech 209 modulation meter. Signal level was established with a Audio Precision TRMS voltmeter and tracking generator. The curves show compliance with Paragraph 95.633(d) of the Rules.

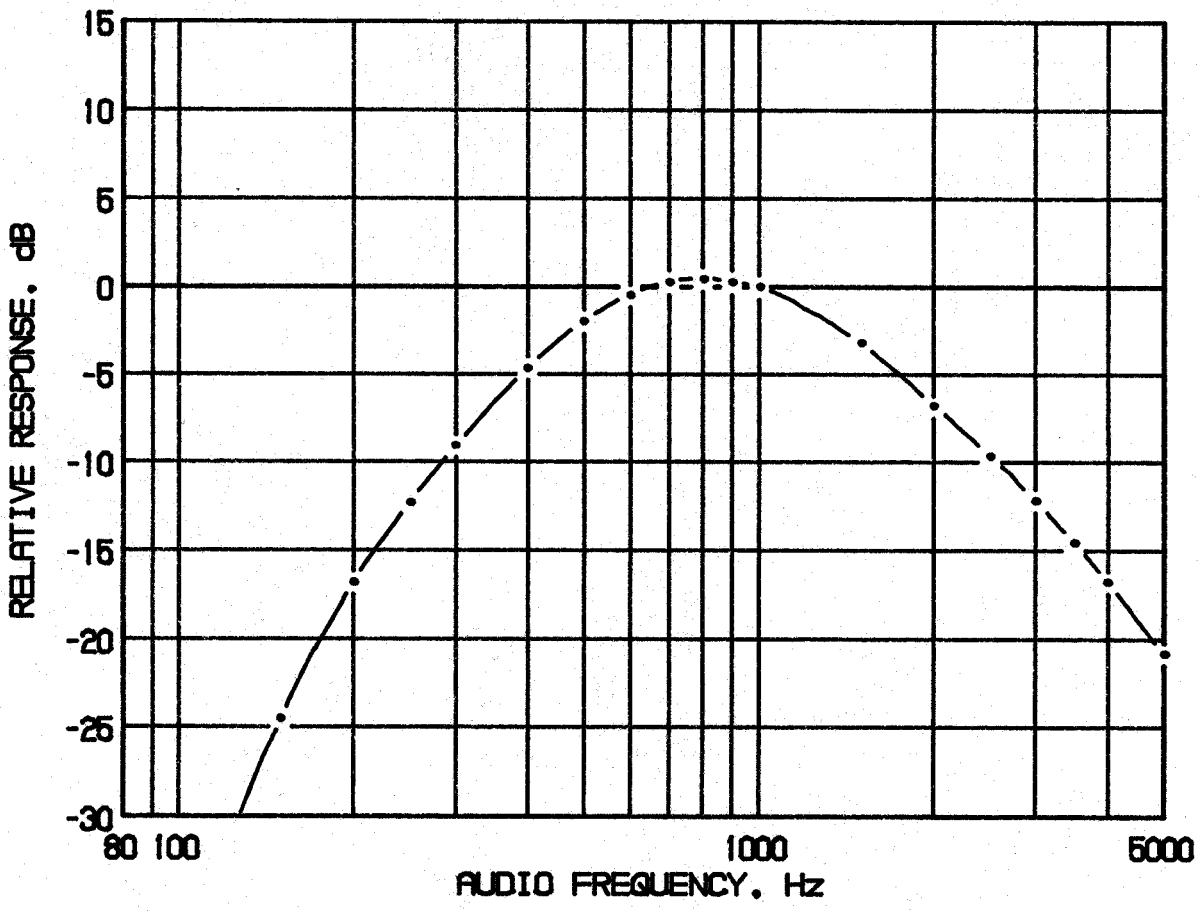
3. Modulation_Limiter_Attack_Time

Modulation limiter attack time was measured by applying to the microphone input terminals a pulsed tone at 2500

Hz, 16 dB above the level required for 50% modulation at the frequency of maximum response, 830 Hz. The spectrum analyzer was tuned to upper and lower fourth-order sidebands in the time domain. Sweep speed was 100 milliseconds per division. Plots are included as Figures 3a and 3b. Any transients observed in excess of 33 dB attenuation as referenced to the carrier were less than 20 ms in duration.

FIGURE 1

TRANSMITTER FREQUENCY RESPONSE

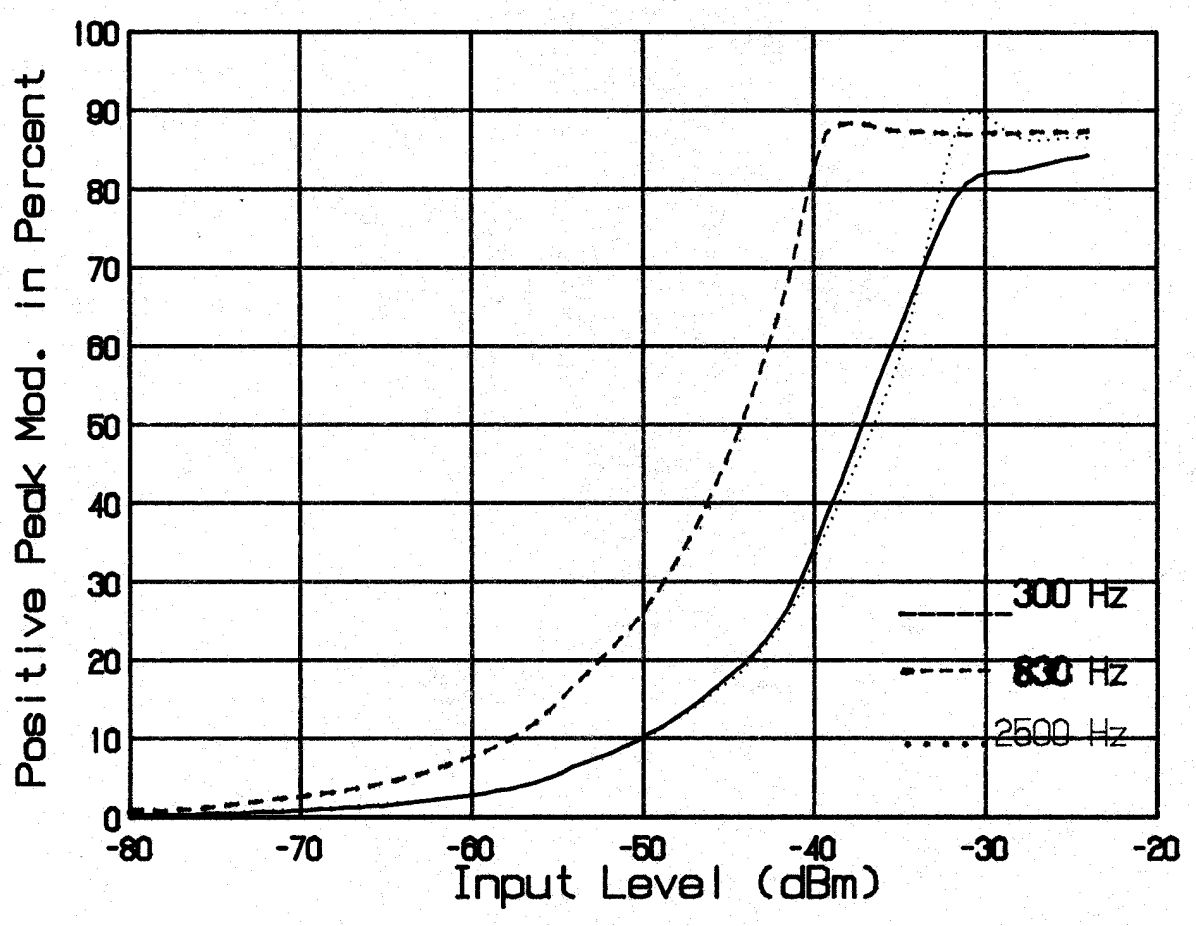


TRANSMITTER FREQUENCY RESPONSE
FCC ID: MMA77104XL

FIGURE 1

FIGURE 2a

AM MODULATION LIMITING - POSITIVE PEAKS



MODULATION LIMITING CHARACTERISTICS

Percent modulation as a function of input level at microphone jack in dBm for 300 Hz, 830 Hz, and 2500 Hz tones.

MODULATION LIMITING POSITIVE PEAKS
FCC ID: MMA77104XL

FIGURE 2a

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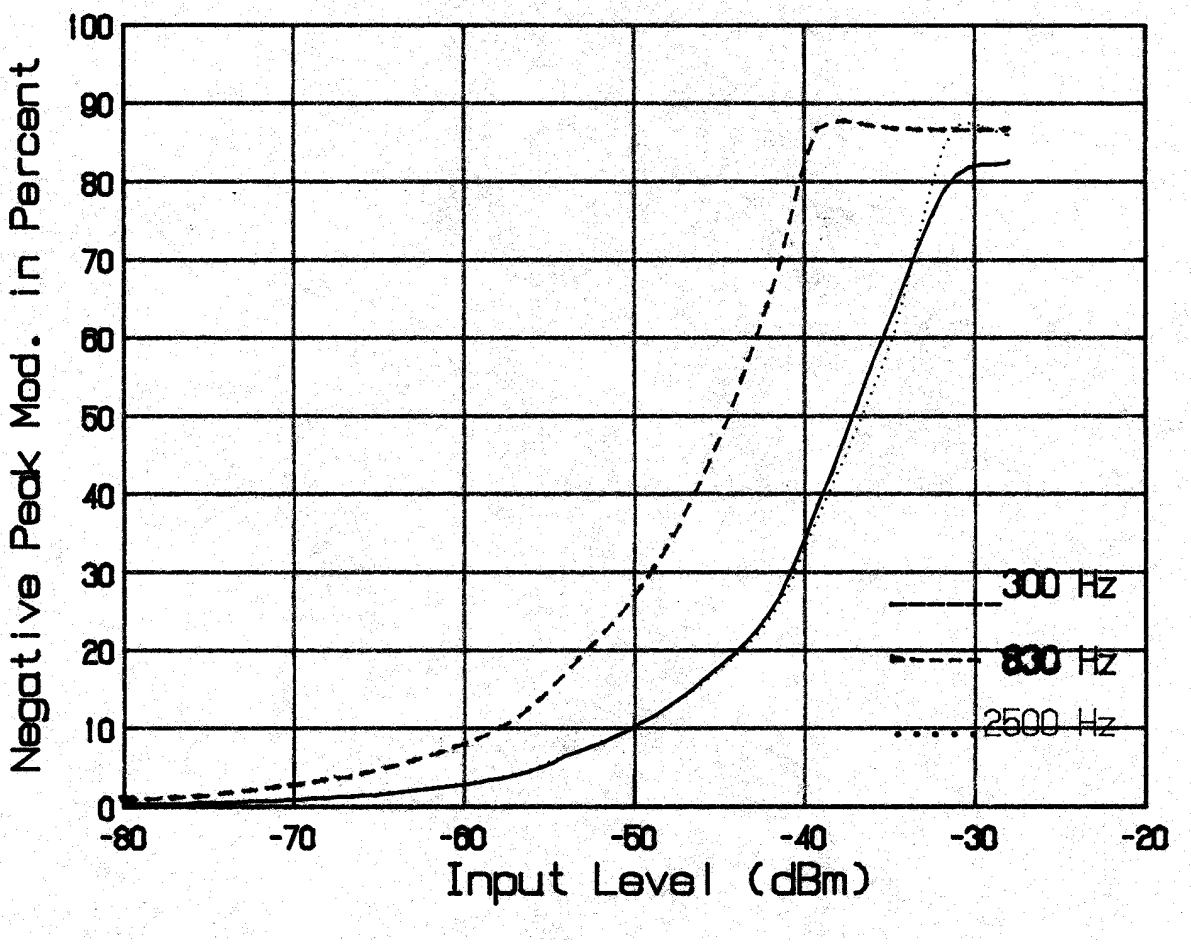
FIGURE 2b

AM MODULATION LIMITING - NEGATIVE PEAKS



MODULATION LIMITING CHARACTERISTICS

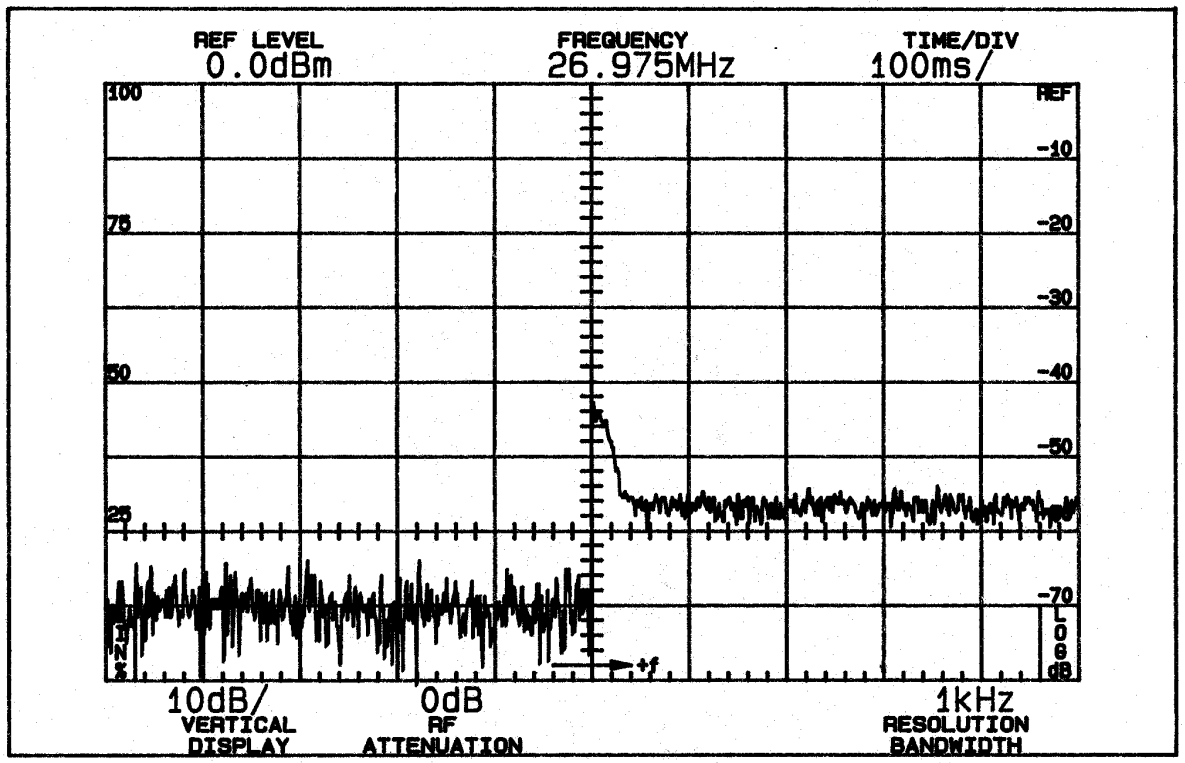
Percent modulation as a function of input level at microphone jack in dBm for 300 Hz, 830 Hz, and 2500 Hz tones.

MODULATION LIMITING NEGATIVE PEAKS
FCC ID: MMA77104XL

FIGURE 2b

FIGURE 3a

MODULATION LIMITER ATTACK TIME



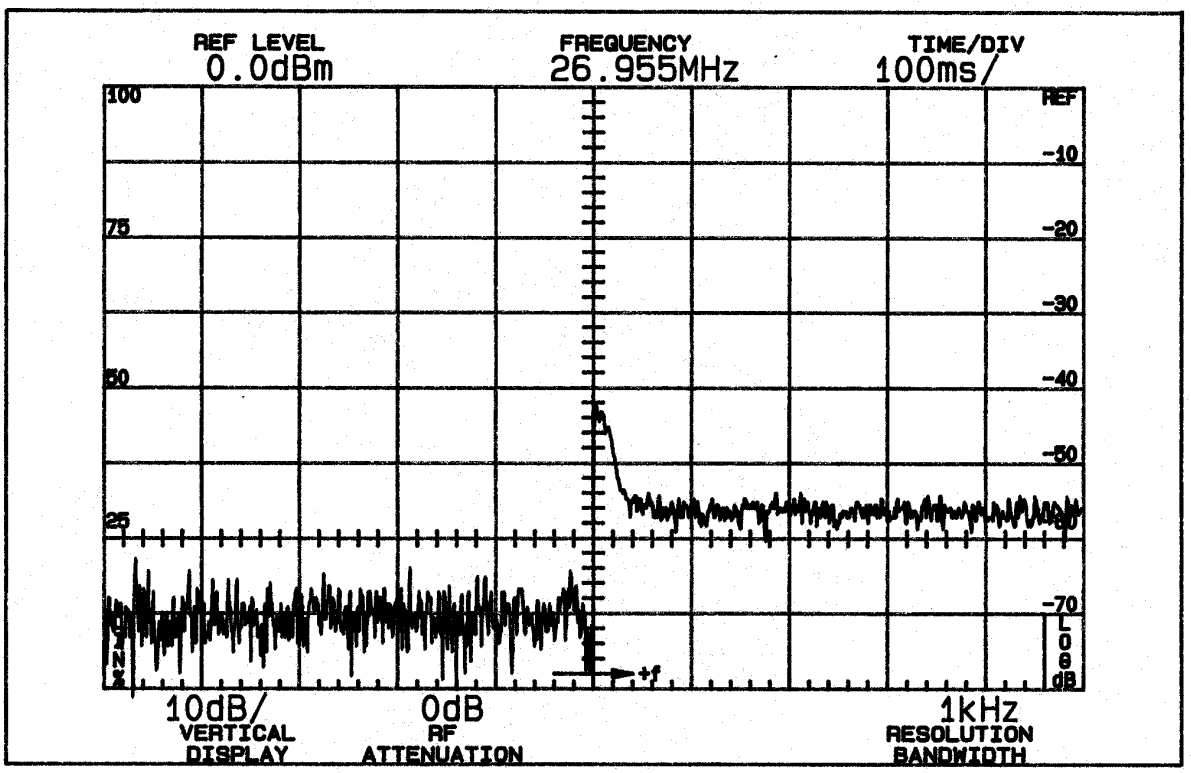
Measurement_Conditions: 16 dB over 50% modulation level at 830 Hz with 2500 Hz tone, upper fourth order sideband; horizontal scale 100 ms/div.

UPPER FOURTH-ORDER SIDEBAND
LIMITER ATTACK TIME
FCC ID: MMA77104XL

FIGURE 3a

FIGURE 3b

MODULATION LIMITER ATTACK TIME



Measurement_Conditions: 16 dB over 50% modulation level at 830 Hz with 2500 Hz tone, lower fourth order sideband; horizontal scale 100 ms/div.

LOWER FOURTH-ORDER SIDEBAND
LIMITER ATTACK TIME
FCC ID: MMA77104XL

FIGURE 3b

C. MODULATION CHARACTERISTICS (Continued)

4. Occupied_Bandwidth_-_AM

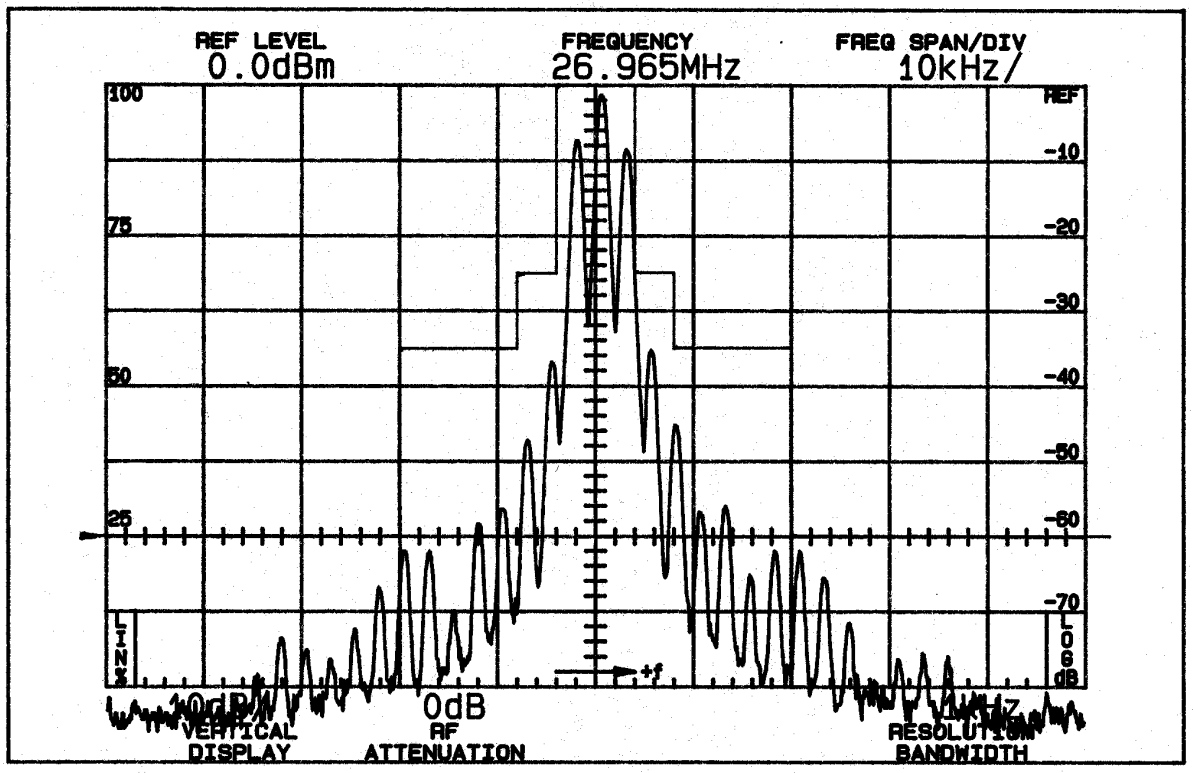
(Paragraph 2.989(c) of the Rules)
Figure 4 is a plot of the sideband envelope of the transmitter taken from a Tektronix 494P spectrum analyzer. Modulation corresponded to conditions of 2.989(a) and consisted of 2500 Hz tone at an input level 16 dB greater than that necessary to produce 50% modulation at 830 Hz, the frequency of maximum response. Measured modulation at 1150 Hz was 85% positive, 86% negative.

The plot is within the limits imposed by Paragraph 95.631(b)(1,3) for double sideband AM modulation. The horizontal scale, frequency, is 10 kHz per division and the vertical scale, amplitude, is a logarithmic presentation equal to 10 dB per division.

Reference carrier was set to 0 dB.

FIGURE 4

OCCUPIED BANDWIDTH - AM



ATTENUATION IN dB BELOW

	MEAN OUTPUT POWER Required
On any frequency more than 50% up to and including 100% of the authorized bandwidth, 8kHz (4-8kHz)	25
On any frequency more than 100%, up to and including 250% of the authorized bandwidth (8-20kHz)	35
On any frequency removed from the assigned frequency by more than 250% of the authorized bandwidth	60

OCCUPIED BANDWIDTH - AM
FCC ID: MMA77104XL

FIGURE 4

D. SPURIOUS EMISSIONS AT THE ANTENNA TERMINALS
(Paragraph 2.991 of the Rules)

The 77-104XL transmitter was tested for spurious emissions at the antenna terminals while the equipment was modulated with a 2500 Hz signal, 16 dB above minimum input signal for 50% modulation at 830 Hz, the frequency of highest sensitivity.

Measurements were made with Tektronix 494P spectrum analyzer coupled to the transmitter output terminal through Narda 765-20 50 ohm power attenuation.

In order to improve measurement system dynamic range, a series trap tuned to the carrier frequency was used on the Narda attenuator output. The trap, which had negligible shunt attenuation at the second harmonic and high frequencies, provided 26 dB attenuation of the fundamental. The trap was not used during close-in (within 10 MHz of the carrier) spurious measurements.

During the tests, the transmitter was terminated in the Narda 765-20 dummy load. Power was monitored on a Bird 43 Thru-Line wattmeter; supply was 13.8 Vdc throughout the tests.

Spurious emission was measured on Channels 1, 21, and 40 throughout the RF spectrum from 10 to 300 MHz. Any emissions that were between the 60 dB attenuation required and the noise floor of the spectrum analyzer were recorded. Data are shown in Table 1.

TABLE 1

TRANSMITTER CONDUCTED SPURIOUS

Channel	Spurious Frequency MHz	dB Below Unmod Carrier Ref.
1	53.930	68
1	80.895	90
1	107.860	89
1	134.825	106
1	161.790	90
1	188.755	105
1	215.720	104
1	242.685	95
1	269.650	101
21	54.430	70
21	81.645	90
21	108.860	89
21	136.075	100
21	163.290	90
21	190.505	108
21	217.720	99
21	244.935	92
21	272.150	96

40	54.810	71
40	82.215	92
40	109.620	90
40	137.025	107
40	164.430	93
40	191.835	108
40	219.240	103
40	246.645	94
40	274.405	104
	Required:	60

All other spurious were over 20 dB below required 60 dB suppression.

E. FIELD STRENGTH MEASUREMENTS OF SPURIOUS RADIATION
(Paragraph 2.993(a)(b,2) of the Rules)

Field intensity measurements of radiated spurious emissions from the 77-104XL transmitter were made with a Tektronix 494P spectrum analyzer and dummy load located in an open field 3 meters from the test antenna. Output power was 4.0 watts. The supply voltage was 13.8 Vdc. The transmitter and test antennae were arranged according to OCE 42 to maximize pickup. The unit has no accessory jacks. Both vertical and horizontal test antenna polarization were employed. Measurements were made from 10 MHz to 10 times the maximum operating frequency of 26.965 or 270 MHz.

Reference level for the spurious radiations was taken as an ideal dipole excited by 4.0 watts, the output power of the transmitter according to the following relationship:*

$$E = \frac{(49.2 \times P_t)^{1/2}}{R}$$

where E = electric-field intensity in volts/meter

P_t = transmitter power in watts

R = distance in meters

for this case $E = \frac{(49.2 \times 4.0)^{1/2}}{3} = 4.7$ V/m

Since the spectrum analyzer is calibrated in decibels above one milliwatt (dBm):

4.7 volts/meter = 4.7×10^6 uV/m

dBu/m = 20 $\text{Log}_{10}(4.7 \times 10^6)$

= 133 dBu/m

Since 1 uV/m = -107 dBm, the reference becomes

133 - 107 = 26 dBm

Representing a conversion for convenience, from dBu to dBm. The measurement system was capable of detecting signals 100 dB or more below the carrier reference level. Data, including antenna factor and line loss corrections, are shown in Table 2.

*Reference_Data_for_Radio_Engineers, International Telephone and Telegraph Corporation, Sixth Edition.

F. FIELD STRENGTH MEASUREMENTS (Continued)

TABLE 2

TRANSMITTER CABINET RADIATED SPURIOUS
Channel 1, 26.965 MHz; 4.0 watts; 13.8 Vdc

	dB Below Carrier Reference			
	With Accessories		Without Accessories	
Frequency, MHz	Vertical	Horizontal	Vertical	Horizontal
53.930	79	81	83	91
80.895	73	66	84	84
107.860	88	83	94	95
134.825	75	83	78	94
161.790	80	82	77	95
188.755	85	83	94	105
215.720	86	80	84	76
242.685	75	88	77	80
269.650	74	74	73	74

FCC Limit: 60 60 60 60

Unlisted spurious were more than 80 below carrier reference from 10 to 270 MHz.

F. FREQUENCY STABILITY
(Paragraph 2.995(a)(1) of the Rules)

Measurement of frequency stability versus temperature was made at temperatures from -30°C to +50°C in 10° increments. At each temperature, the unit was exposed to the test chamber ambient a minimum of 60 minutes after indicated chamber temperature ambient had stabilized to within ±2° of the desired test temperature. Following a 30 minute soak at each temperature, the unit was turned on, keyed and frequency measured within 2 minutes. Test temperature was sequenced in the order shown in Table 3, starting with -30°C.

A Thermotron S1.2 temperature chamber was used. The transmitter output stage was terminated in a dummy load. Primary supply was 13.8 Vdc. Frequency was measured with a HP 5385A digital frequency counter connected to the transmitter through a power attenuator. Measurements were made on Channel 9, 27.065 MHz. No transient keying effects were observed. Data are shown in Table 3.

G. FREQUENCY STABILITY (Continued)

TABLE 3

Temperature	Output_Frequency,_MHz
-29.2	27.065635
-19.8	27.065640
- 9.8	27.065597
0.0	27.065499
10.4	27.065344
19.9	27.065243
30.5	27.065044
40.4	27.064885
49.9	27.064749
Maximum frequency error:	27.065640
	27.065000
	- .000640 MHz

FCC Rule 95.625(b) specifies .005% or a maximum of ± .001353 MHz.

G. FREQUENCY STABILITY AS A FUNCTION OF SUPPLY VOLTAGE
(Paragraph 2.995(d)(2) of the Rules)

Oscillator frequency as a function of power supply voltage was measured with a HP 5385A digital frequency counter as supply voltage provided by Heath SP-5220 variable ac power supply was varied from ±15% above the nominal 13.8 Vdc. A Keithley 177 digital voltmeter was used to measure supply voltage at transmitter primary input terminals. Measurements were made at 20°C ambient. (See Table 4).

TABLE 4

Supply_Voltage	Output_Frequency,_MHz
15.87	27.065256
15.18	27.065252
14.49	27.065247
13.80	27.065243
13.11	27.065239
12.42	27.065236
11.73	27.065233
Maximum frequency error:	27.065256
	27.065000
	+ .000256 MHz

FCC Rule 95.625(b) specifies .005% or a maximum of ± .0001353 MHz.

No effects on frequency related to keying the unit were observed.

H. ADDITIONAL REQUIREMENTS FOR TYPE ACCEPTANCE
(Paragraph 95.669 of the Rules)

The 77-104XL meets the applicable provision of 95.669(a).
External controls are limited to the following per 95.669(a):

1. Primary power connection
2. Microphone jack
3. RF output power connection
4. External speaker jacks
5. On-off switch (combined with receiver volume control)
6. Not applicable, AM only
7. Not applicable
8. Transmitting frequency selector
9. Transmit-receive switch
10. Meter for monitoring transmitter performance
11. Meter/pilot lamp for RF output indication

Other front panel controls and functions follow on pages 17 and 18, and are representative of functions approved on other submissions.

The serial number of each unit will be implemented in accordance with 95.971.

A copy of Part 95, Subpart D, of the FCC rules for the Citizens Band Radio Service, current at the time of packing of the transmitter, must be furnished with each CB transmitter marketed per 95.673.

I. PLL RESTRICTIONS (Per Public Notice of April 27, 1978)
The 77-104XL meets the following conditions specified:

1. All frequency-determining elements, including crystals, PLL integrated circuits and channel selector switches are permanently wired and soldered in place.

2. The PLL integrated circuit division ratio selection is BCD coded. All the 40 channels are mask programmed into the CPU and can not be changed.

3. Channel selection is controlled by the masked program of the CPU and has only 40 positions for use in the US.

4. All the undedicated leads in the CPU and PLL integrated circuits are disabled and not serviceable by the user.

5. A copy of the PLL data sheet is shown in Appendix 4.

J. FINAL AMPLIFIER DATA

1. A copy of the final RF amplifier data sheet is included in Appendix 5.

APPENDIX 1

FUNCTION OF DEVICES

FUNCTION OF DEVICES FOLLOWS THIS SHEET

FUNCTION OF DEVICES
FCC ID: MMA77104XL

APPENDIX 1

1) IC

Ref. No.	Description	Function		Manufacturer
		RX	TX	
IC1	LC7185	PLL IC	PLL IC	SANYO
IC2	NJM4558D	Squelch	Audio Amp.	JRC
IC3	TDA2003	Audio Amp.	Audio Amp.	SGS

2) TR

Ref. No.	Description	Function		Manufacturer
		RX	TX	
Q1	KTA1267Y	AGC	-	K.E.C.
Q2	KTC3195Y	RF Amp.	-	K.E.C.
Q3	KTC3195Y	RX 1ST Mixer	-	K.E.C.
Q4	KTC3195Y	RX 2ND Mixer		K.E.C.
Q5	KTC3195Y	IF Amp.	-	K.E.C.
Q6	KTC3199Y	IF Amp.	-	K.E.C.
Q7	KTC3199Y	ANL Clipping	-	K.E.C.
Q8	KTC3199Y	-Audio switching		K.E.C.
Q9	KTC3199Y	-	Audio switching	K.E.C.
Q10	KTC3199Y	Squelch		K.E.C.
Q11	KTC3199Y	Squelch		K.E.C.
Q12	KTA1267Y		Mic amp	K.E.C.
Q13	KTC3199Y		ALC	K.E.C.
Q14	KTC3199Y		ALC	K.E.C.
Q15	KTC3198Y	Regulator	Regulator	K.E.C.
Q16	KTC3875S		TX B+ Switching	K.E.C.
Q17	KTC3198Y	RX B+ Switching	-	K.E.C.
Q20	KTC3195Y	VCO	VCO	K.E.C.
Q21	KTC3199Y	VXO amp	VXO amp	K.E.C.
Q22	KTC3199Y	Buffer	buffer	K.E.C.
Q23	KTC3199Y		Doubler amp	K.E.C.
Q24	KTC3198Y	-	PRE Amp.	K.E.C.
Q25	KTC1006	-	RF Driver Amp.	K.E.C.
Q26	KTC2075A	-	Power Amp.	K.E.C.
Q27	KTA1267Y	Display logic	Display logic	K.E.C.
Q28	KTA1267Y	Display logic	Display logic	
Q30	KTC3199Y	RX ind cont.		
Q32	KTC3198Y	6v. reg	6v. reg	K.E.C.
Q35	KTC3199Y	Active filter	Active filter	K.E.C.
Q36	KTC3199Y	Active filter	Active filter	K.E.C.

APPENDIX 2

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

All 40 channels of transmitting, and receiving, frequencies are provided by PLL (Phase Locked Loop)circuitry.

The purpose of the PLL is to provide a multiple number of frequencies from a VCO (Voltage Controlled Oscillator) with quartz crystal accuracy and stability locked to crystal oscillator reference frequency.

The reference crystal oscillator frequency is 10.240 MHz.

FCC ID: MMA77104XL

APPENDIX 2

APPENDIX 3

1. Circuits_For_Suppression_Of_Spurious_Radiation

The tuning circuit between frequency synthesizer and final AMP Q26 and 3-stage “PI” network, C110, C112, C113, C115 C116, L6, L7 and L8 in the Q26 output circuit serves to suppress spurious radiation. This network serves to impedance match Q26 to the antenna and to reduce spurious content to acceptable levels in the frequency synthesizer.

2. Circuits_For_Limiting_Modulation

The mic input is fed to the mic amp IC2 (1/2) and then to the audio power amp IC3 which feeds the signal to the modulation transformer T6. The audio output at the top of T6 is fed in series with the B+ voltage through diode D11 to the collector of Q25 and the final Q26 to collector modulate at both stages.

A portion of the modulation voltage is fed to Q13 and Q14 and turn on and at the same time, Q14 attenuates the mic, in put to the mic amp IC2 (1/2). The resulting feedback loop keeps the modulation from exceeding 100% for input approximately 40 dB greater than that required to produce 50% modulation. The attack time is about 18 ms and the release time is about 300 ms.

3. Circuits For Limiting Power

During factory alignment, the series base resistor Q26 (R127) is selected to limit the available power to slightly less than 4 watts. The tuning is adjusted so that the actual power is from 3.6 to 4.0 watts; there are no other controls for adjusting power.

DEVICES AND CIRCUITS TO SUPPRESS
SPURIOUS RADIATION; LIMIT
MODULATION AND POWER
FCC ID: MMA77104XL

APPENDIX 3

APPENDIX 4

PLL DATA SHEETS

TWELVE (12) PAGES FOR LC7185-8750 FOLLOW THIS SHEET

COPY OF PLL DATA SHEETS
FCC ID: MMA77104XL

APPENDIX 4

Ordering number: EN 3356A

CMOS IC

LC7185-8750

CB Transceiver PLL Frequency Synthesizer and Controller

Overview

This 27 MHz band, PLL frequency synthesizer LSI chip is designed specifically for CB transceivers.
The specifications are suited for use in U.S.A.(FCC).

Functions

The LC7185-8750 incorporates PLL circuitry and a controller for CB applications on a single CMOS chip. The controller handles the PLL circuitry, frequency data ROM, channel preset/recall RAM, and LED display driver. It also supports channel scan, channel preset/recall, and emergency channel call.

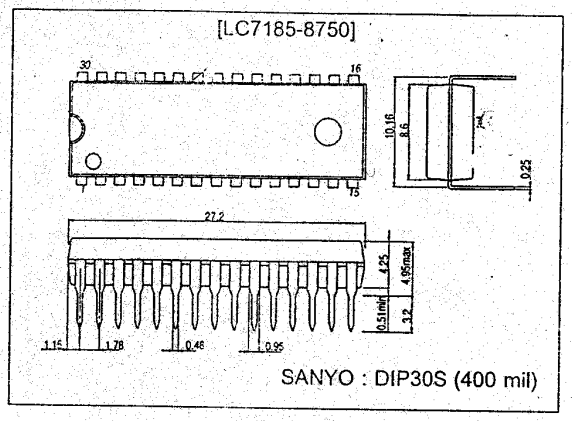
Features

1. A built-in programmable divider for the 16 MHz VCO
2. Transmission is inhibited when the PLL is unlocked (digital lock monitor).
3. Direct channel 9 or 19 selection (sliding switch)
4. A 7-segment, 2-character LED display
5. "PA" is displayed in public announcement mode.
6. Output beep-tone control circuitry
7. Up to 5 channel settings can be stored in memory.
8. 4 × 3 key matrix implementation

Package Dimensions

unit : mm

3061-DIP30S



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Pin V_{DD}	–0.3 to +9.0	V
Input voltage	V_{IN}1 max	Pins $\overline{HOLD}$, $\overline{TX}$	–0.3 to +15	V
	V_{IN}2 max	Input pins other than V_{IN}1 max	–0.3 to V_{DD} +0.3	V
Output voltage	V_O1 max	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	–0.3 to +15	V
	V_O2 max	Pins $\overline{UL}$, BEEP	–0.3 to +15	V
	V_O3 max	Pin PD	–0.3 to V_{DD} +0.3	V
	V_O4 max	Output pins other than mentioned above	–0.3 to V_{DD} +0.3	V
Output Current	I_O1 max	Pins SA, SB, SC, SD, SE, SF, SG	0 to +30	mA
	I_O2 max	Pins D1, D2	0 to +10	mA
	I_O3 max	Pins $\overline{UL}$	0 to +20	mA
	I_O4 max	Pin BEEP	0 to +10	mA
Allowable power dissipation	Pd max	(Ta ≦ 85°C)	350	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Conditions at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		5.0		8.0	V
Input high-level voltage	$V_{IH}1$	Pins $\overline{HOLD}$, $\overline{TX}$	$0.7V_{DD}$		12	V
	$V_{IH}2$	Pin $\overline{INIT}$	3.2		V_{DD}	V
	$V_{IH}3$	Pins KI1, KI2, KI3, KI4	$0.6V_{DD}$		V_{DD}	V
Input low-level voltage	$V_{IL}1$	Pins $\overline{HOLD}$, $\overline{TX}$	0		$0.3V_{DD}$	V
	$V_{IL}2$	Pin $\overline{INIT}$	0		1.3	V
	$V_{IL}3$	Pins KI1, KI2, KI3, KI4	0		$0.4V_{DD}$	V
Output voltage	$V_{OUT}1$	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	0		13	V
	$V_{OUT}2$	Pins $\overline{UL}$, BEEP	0		8	V
Input frequency	$f_{IN}1$	Pin XIN (sine wave, capacitor coupled)	1.0	10.24	15	MHz
	$f_{IN}2$	Pin PIN (sine wave, capacitor coupled)	10		30	MHz
Input amplitude	$V_{IN}1$	Pin XIN (sine wave, capacitor coupled)	0.5		1.5	Vrms
	$V_{IN}2$	Pin PIN (sine wave, capacitor coupled)	0.15		1.5	Vrms
Required oscillating frequency	X'tal	Pins XIN, XOUT (CI ≦ 50 Ω)	5.0	10.24	15	MHz

Electrical Characteristics at under allowable operating conditions

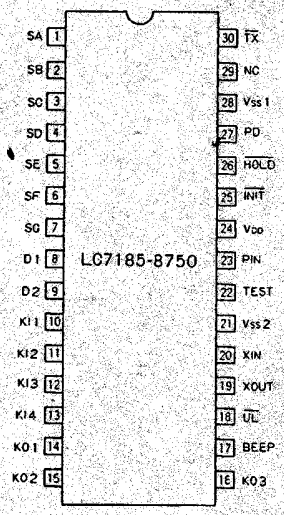
Parameter	Symbol	Conditions	min	typ	max	Unit
Internal feedback resistance	Rf1	Pin XIN		1.0		MΩ
	Rf2	Pin PIN		500		kΩ
Pull-down resistor	RpdN	Pins KI1, KI2, KI3, KI4, TEST	30	50	70	kΩ
Input high-level current	$I_{IH}1$	Pins $\overline{HOLD}$, $\overline{TX}$ V_I = 12 V			5.0	μA
	$I_{IH}2$	Pin $\overline{INIT}$ $V_I = V_{DD}$			5.0	μA
	$I_{IH}3$	Pin XIN $V_I = V_{DD}$			25	μA
	$I_{IH}4$	Pin PIN $V_I = V_{DD}$			50	μA
Input low-level current	$I_{IL}1$	Pins $\overline{HOLD}$, $\overline{TX}$ $V_I = V_{SS}$			5.0	μA
	$I_{IL}2$	Pin $\overline{INIT}$ $V_I = V_{SS}$			5.0	μA
	$I_{IL}3$	Pin XIN $V_I = V_{SS}$			25	μA
	$I_{IL}4$	Pin PIN $V_I = V_{SS}$			50	μA
Output high-level voltage	$V_{OH}1$	Pins KO1, KO2, KO3 I_O = 1 mA	V_{DD}–2.0	V_{DD}–1.0	V_{DD}–0.5	V
	$V_{OH}2$	Pin PD I_O = 0.5 mA	V_{DD}–1.0			V
Output low-level voltage	$V_{OL}1$	Pins KO1, KO2, KO3 I_O = 20 μA	0.6	1.0	1.4	V
	$V_{OL}2$	Pin PD I_O = 0.5 mA			1.0	V
	$V_{OL}3$	Pin BEEP I_O = 2 mA			1.0	V
	$V_{OL}4$	Pins SA, SB, SC, SD, SE, SF, SG I_O = 20 mA			1.0	V
	$V_{OL}5$	Pins D1, D2 I_O = 5 mA			1.0	V
	$V_{OL}6$	Pin $\overline{UL}$ I_O = 10 mA			1.0	V
Output leakage current	$I_{OFF}1$	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2 V_O = 13 V			5.0	μA
	$I_{OFF}2$	Pins $\overline{UL}$, BEEP V_O = 8 V			5.0	μA
High-level tristate leakage current	I_{OFFH}	Pin PD $V_O = V_{DD}$		0.01	10.0	nA
Low-level tristate leakage current	I_{OFFL}	Pin PD $V_O = V_{SS}$		0.01	10.0	nA
Supply current	$I_{DD}1$	Normal mode *1 (PLL operates)		5	10	mA
	$I_{DD}2$	Hold mode V_{DD} = 3.2 V *2 (memory backup)			5	μA
		V_{DD} = 8.0 V			15	μA

*1: $f_{IN}2$ = 20 MHz (PIN)
$V_{IN}2$ = 0.15 Vrms
X'tal = 10.240 MHz
$\overline{TX}$ = $\overline{HOLD}$ = $\overline{INIT}$ = V_{DD}
Other inputs = V_{SS}
Other outputs = open

*2: $\overline{HOLD}$ = V_{SS}
$\overline{TX}$ = $\overline{INIT}$ = V_{DD}
Other inputs = V_{SS}
Other outputs = open

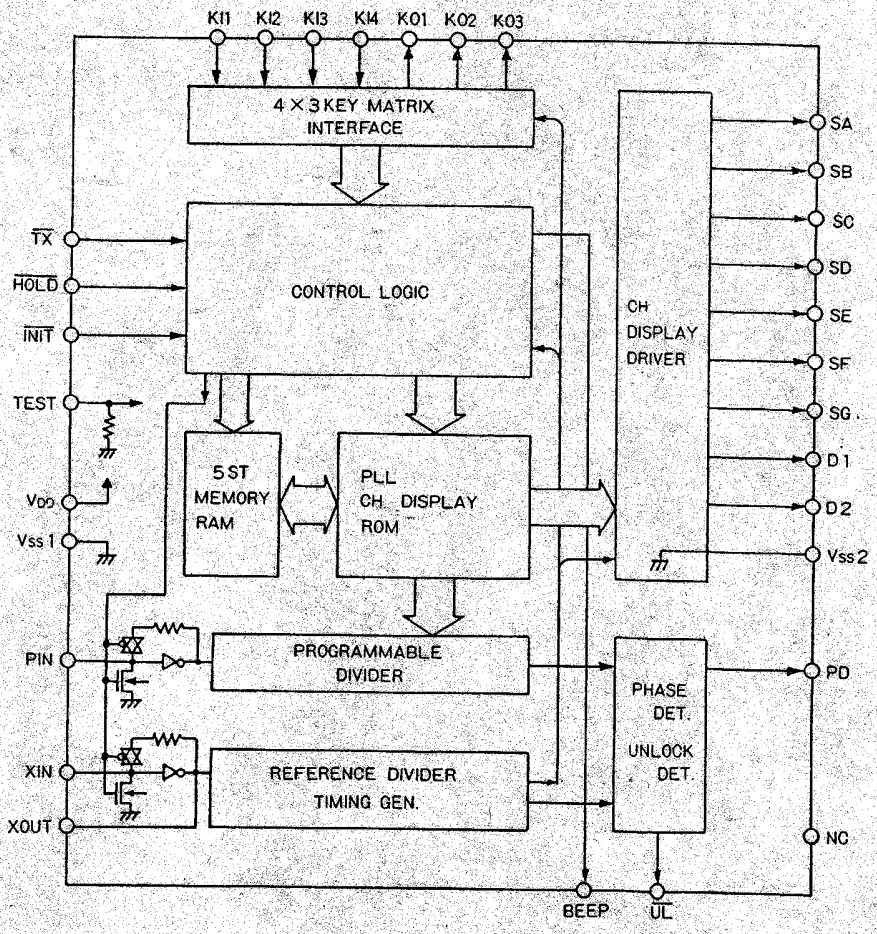
Note: Be careful that the dielectric strength of pins SA, SB, SC, SD, SE, SF, D1, D2, UL, BEEP are weak.

Pin Assignment



Top view

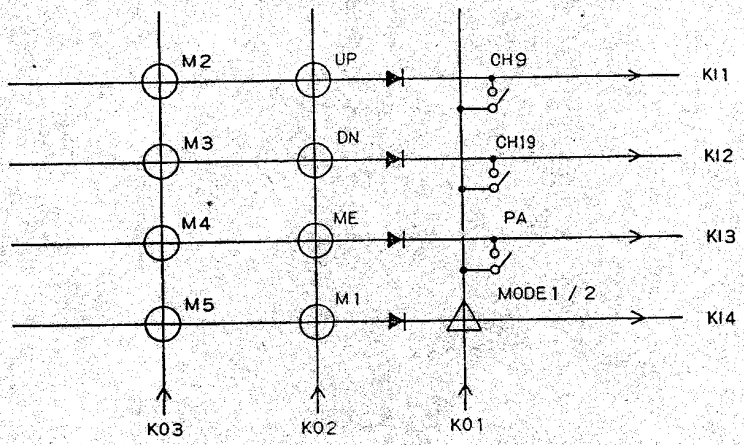
Block Diagram



Pin Descriptions

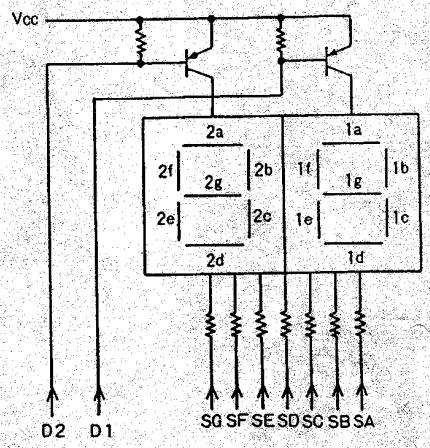
$\overline{TX}$	Transmit/receive select	PD	Charge pump output
$\overline{HOLD}$	Hold mode select	NC	NC pin
$\overline{INIT}$	Initial input	SA to SG	Segment driver (for display)
TEST	Test point (input)	D1, D2	Digit output (for display)
V_{DD}, $V_{SS}1$, $V_{SS}2$	Power supply	KI1 to KI4	Key inputs
PIN	Programmable divider input	KO1 to KO3	Key scan outputs
XIN, XOUT	Crystal oscillator input, output (10.240 MHz)	BEEP	Beep-tone control output
$\overline{UL}$	Unlock detection signal output		

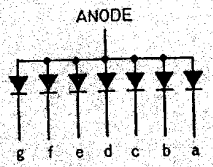
Key Matrix



CH9	Emergency CH9 recall	ME	Station Memory Enable
CH19	Emergency CH19 recall	M1 to M5	Station Memory recall
PA	Public announcement display	UP/DN/ME/M1 to 5	Momentary SW
MODE 1/2	Display Mode	CH9/CH19/PA	Slide SW
UP	CH up/scan	MODE 1/2	Diode
DN	CH down/scan		

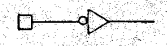
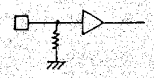
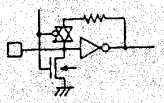
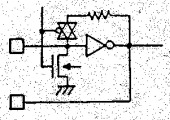
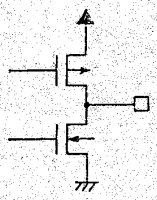
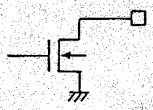
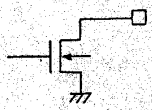
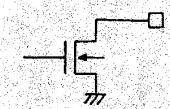
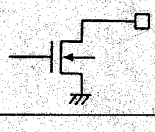
LED Display Configuration (Common anode/7 segment)





	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

Pin Description

Pin Name	Pin No.	Type	Description
$\overline{TX}$	30		• Transmit/receive select $\overline{TX}$ = "0"...Transmit, TX = "1"...Receive
$\overline{HOLD}$	26		• Hold mode select $\overline{HOLD}$ = "0"...Hold mode select " = "1"...Normal mode select
$\overline{INIT}$	25		• Reset line $\overline{INIT}$ = "0"...Reset
TEST	22		• Test point (input) Tie to ground or leave floating
V_{DD}	24		• Power supply (+) Normal mode: 5.0 to 8.0 V Hold mode: ≧ 3.2 V
$V_{SS}2$	21		• Channel display LED driver ground
PIN	23		• Programmable divider input 150 mVrms min Hold mode: Programmable divider is disabled.
XIN XOUT	20 19		• Crystal oscillator Frequency: 10.24 MHz Hold mode: Oscillator is disabled.
PD	27		• Charge pump output from the phase comparator. If the frequency of fV (the signal obtained by dividing the PIN input by N) is higher than that of fR (the reference signal), or if the phase of fV leads that of fR, positive pulses are output on this pin. If the frequency is lower or the phase lags, negative pulses are output on this pin. If they match, the pin goes to high impedance. • fV > fR OR leading: Positive Pulses • fV < fR OR leading: Negative Pulses • fV = fR and phase muched: High impedance Hold mode: High impedance
$V_{SS}1$	28		• PLL circuit and controller ground
NC	29		• No-connection
$\overline{UL}$	18		• Unlock detected output Fixed to low level when unlocked, when changing channels, in PA mode, or in hold mode. Open: Locked
BEEP	17 NC		• Beep-tone control output During station memory operation During I/O on emergency channel When changing channels During reset During hold mode recovery Fixed to low level in hold mode Transistor: Off (50 ms cycle) → Open
SA to SG	1 to 7		• Segment drivers for the display (Common anode/7 segments)
D1 D2	8 9		• Digit output (150 Hz) for the display (common anode/7 segments) Hold mode: Transistor goes off.

Continued on next page.

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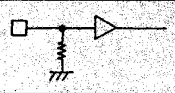
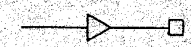
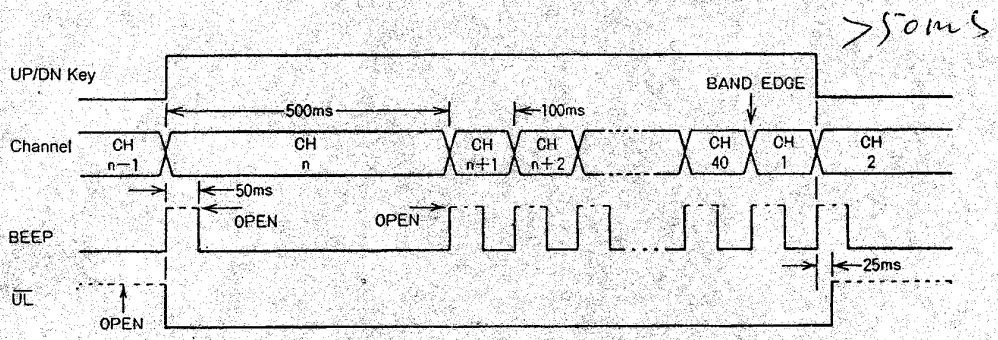
Pin Name	Pin No.	Type	Description
KI1 to KI4	10 to 13		• Key inputs Input from the key matrix
KO1 to KO3	14 to 16		• Key scan output (75 Hz) Output to the key matrix Hold mode: Low (scanning stops)

Operation

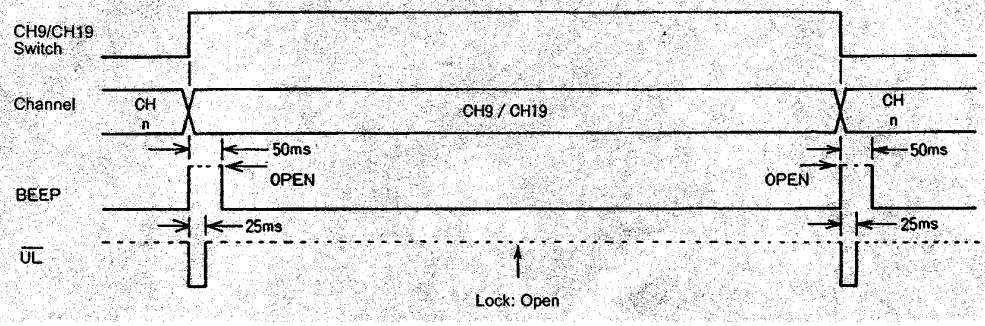
(1) Channel Selection (up/down)

1. Manual scanning (up/down)
   Pressing the UP key increments by one channel and pressing the DN key decrements by channel.
   When scanning reaches the end of the band, it automatically wraps around to the beginning.
2. Auto scanning (up/down)
   Holding the UP (or DN) key down for 500 ms or longer starts auto scanning. For both up and down scanning, each channel takes 100 ms to scan.
3. The unlock detected line ($\overline{UL}$) is asserted (low) when the UP (or DN) key is pressed and deactivated 25 ms after the key is released.
4. The beep-tone control line (BEEP) is asserted (open) for 50 ms after each new channel is selected.



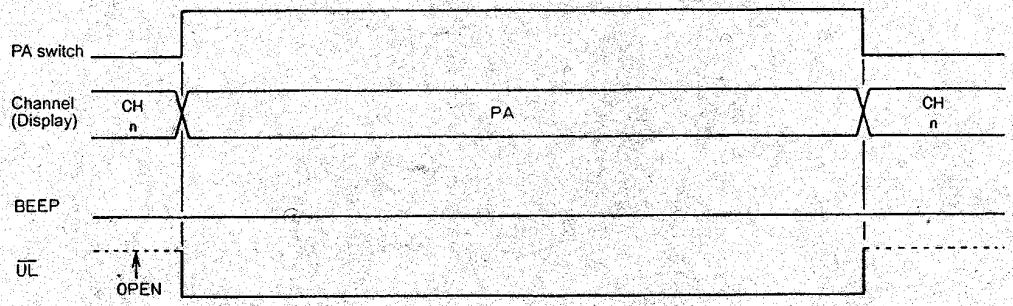
(2) Selecting an Emergency Channel (CH9/CH19)

1. If the CH9 or CH19 switch is turned on, the LC7185 stores the value of the previous channel and asserts the beep-tone control line for 50 ms.
2. While the CH9 or CH19 switch is turned on, the LC7185 disables all keys except $\overline{TX}$ and PA (UP/DN, ME, and M1 to M5 switches).
3. Even if the CH9 or CH19 switch is turned off while transmitting using the CH9 or CH19 switch, keep the emergency channel open until the LC7185 is in the receive mode.
4. After the CH9 or CH19 switch is turned back off, the beep-tone control line is asserted for 50 ms and the LC7185 reopens the previous channel.
5. Note the CH9 has a higher priority over CH19. As a result, if both switches are turned on, CH9 will be opened.
6. The $\overline{UL}$ line is asserted for 25 ms after the CH9 or CH19 switch is turned off or on.
7. Causes either "9" or "19" to blink on the display.



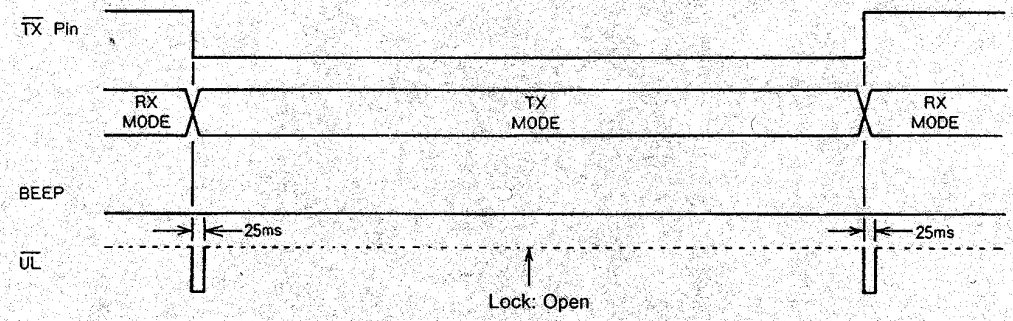
(3) Public Announcement (PA) Mode

1. When the PA switch is turned on, the LC7185 stores the value of the previous channel and enters the PA mode.
2. While the PA switch is turned on, the LC7185 disables all keys ($\overline{TX}$, CH9/CH19, UP/DN, ME, M1 to M5)
3. "PA" is displayed on the channel display.
4. When the PA switch is turned back off, the LC7185 enters the CB mode and reopens the previous channel.
5. The $\overline{UL}$ line is asserted while the PA switch is turned on.



(4) Transmit/Receive Selection

1. When the $\overline{TX}$ line is asserted, the LC7185 enters TX mode.
2. If the PA switch is turned on while the LC7185 is in TX mode, the device enters PA mode. However, if any other switch (other than the PA switch) or key (UP/DN, ME, M1 through M5, CH9, CH19) is pressed while the LC7185 is in TX mode, that switch or key has no effect.
3. The unlock detected signal is output each time the device switches between transmitting and receiving.



(5) Channel Preset/Recall Facility

1. The LC7185 allows up to 5 channels to be preset (assigned to M1 to M5).
   - After a reset (when the power is turned on, etc.), M1 to M5 are assigned to CH33.
2. Recalling preset channels
   - A preset channel is recalled by pressing one of the preset memory keys (M1 to M5) to which the channel was previously assigned.
   - There are two different display modes as shown below.

   Mode 1 (without diode)

   Each time a key is pressed (M1 to M5), the new channel is displayed.

   Example: Display 21 → 15

   key [M1]

   Mode 2 (with diode)

   Each time a key is pressed (M1 to M5), a key mnemonic ("P1" to "P5") is displayed for 400 ms, then the new channel is displayed.

   Example: Display 21 → P1 → 15

   400 ms

   Key [M1]

3. Presetting channels
   - First select the channel to be preset, then hold down the ME key and press the preset memory key (M1 to M5) to which you would like to assign the current channel.

   In the following cases, a channel will not be preset:
   - M1 to M5 is pressed and in the memory preset mode.
   - Emergency channels CH9 or CH19 are currently selected.
   - The $\overline{TX}$ line is asserted.
   - The PA switch is turned on (PA mode).
   - The $\overline{HOLD}$ line is asserted (hold mode).

   Even if the above key operations are not performed, the preset mode will be canceled automatically after 9 seconds.

   - There are two different display modes as shown below.

   Mode 1 (without diode)

   The current channel is displayed throughout the preset process.

   Example: Display 15 ⟶ 15
   Key [ME] [M1]

   Mode 2 (with diode)

   When the ME key is held down, "PE" is flashed on the display, indicating that presetting is possible. Once a preset memory key (M1 to M5) is pressed, the key mnemonic ("P1" to "P5") is displayed for 400 ms before the current channel is redisplayed.

   Example: Display 15 → PE → P1 → 15
   400 ms
   Key [ME] [M1]

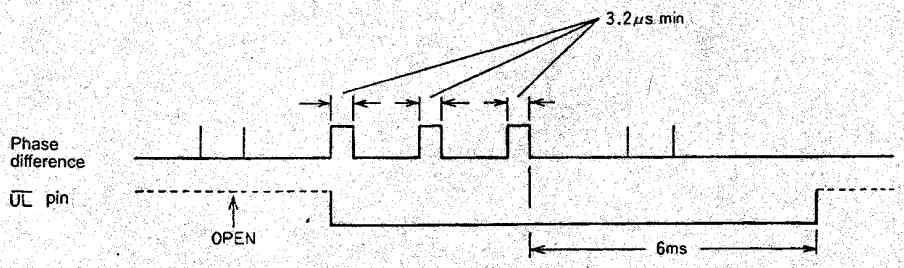
   - Note that if two or more keys are pressed at the same time, priority is assigned as follows:
     M1 > M2 > M3 > M4 > M5

(6) Beep-tone Control Output (BEEP pin)

After each of the following events, the BEEP line is asserted for 50 ms:
- A reset, such as a battery replacement ($\overline{INIT}$ = 0)
- Any key press associated with the channel memory
- Any emergency channel switch activation
- A new channel is selected
- Leaving hold mode

(7) Unlock Detected Output ($\overline{UL}$ pin)

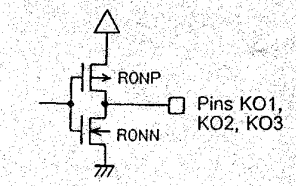
In the following cases, the $\overline{UL}$ line is asserted.
- When the phase difference between the programmable and reference divider outputs exceeds 3.2 µs, the $\overline{UL}$ line is held low for 6 ms after the last out-of-range phase sample is detected, as shown below.



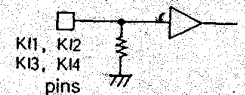
- After a new transmit/receive or channel selection, the $\overline{UL}$ line is asserted for 25 ms.
- While the PA switch is turned on, the $\overline{UL}$ line is asserted during PA mode.
- The $\overline{UL}$ pin is open while the device is in the PLL LOCK state (when the phase difference is < 3.2 µs).

(8) Key Matrix

It is normal to put diodes in series with the key scanning lines to avoid creating a short with the output lines. But KO1, KO2 and KO3 lines (key scan signal output) do not need diodes.



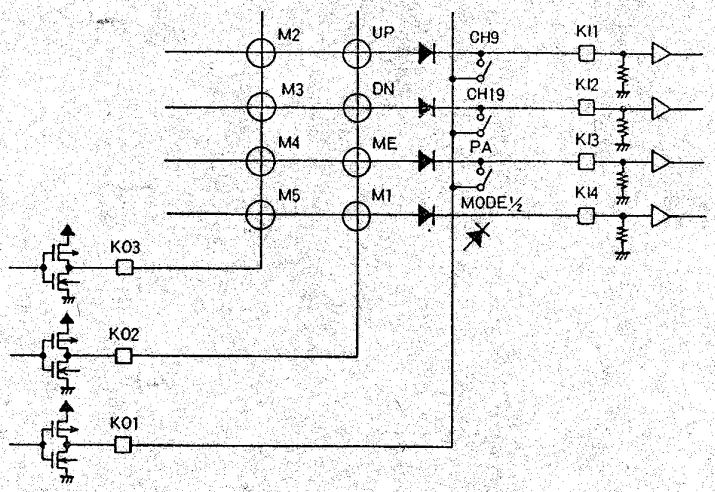
RONP, RONN : On impedance



RpdN : Pull-down resistor

unit : kΩ

Item	min	typ	max
RONP	0.5	1.0	2.0
RONN	30	50	70
RpdN	30	50	70



Explanation Regarding Power On and Hold Mode

(1) Operation in hold mode

When in hold mode ($\overline{HOLD}$ = 0), the LC7185-8750 does not accept any operation other than the $\overline{INIT}$ pin being asserted (reset). The primary function of hold mode is to maintain the contents of station memory.

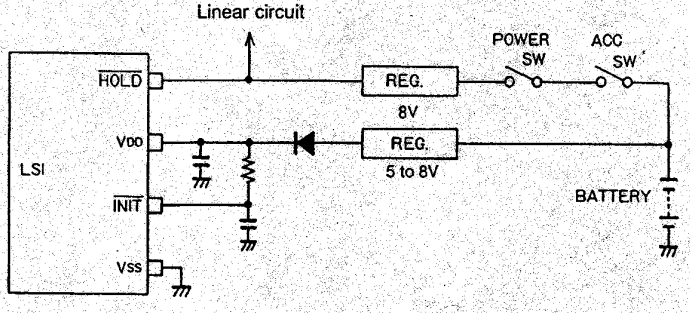
- In hold mode, the programmable divider, crystal oscillator and reference divider are all stopped. The PD pin (charge pump output) goes to high impedance. The $\overline{UL}$ pin goes to V_{SS}.
- The channel display pins D1 and D2 go to high impedance.
- The BEEP pin goes to V_{SS}.
- The key scan signal outputs (KO1 to KO3) go to V_{SS}.

When the LC7185-8750 leaves hold mode, the previously selected channel is reopened.

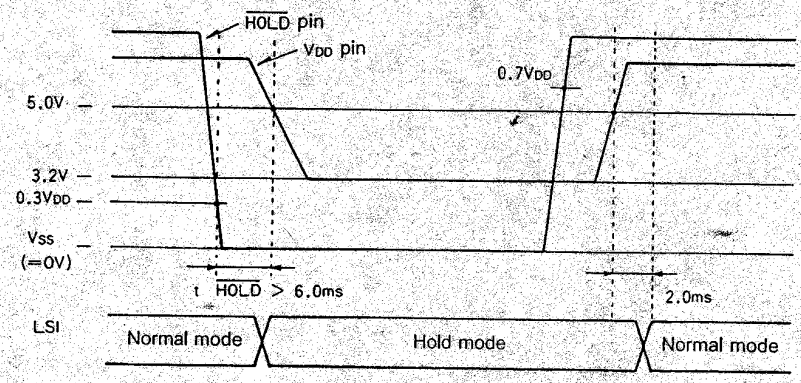
(2) Initial state settings

The LC7185-8750 can be reset to its initial state settings (reset) after the battery has been replaced, etc., by setting $\overline{INIT}$ = 0. The initial state that is established by an initial reset is as follows:

- When the V_{DD} pin turned on, CH9 or CH33 is selected.
- When the V_{DD} pin operate voltage already, CH9 is selected.
- All of station memory is set to CH33.



(3) Timing Requirements for Hold Mode

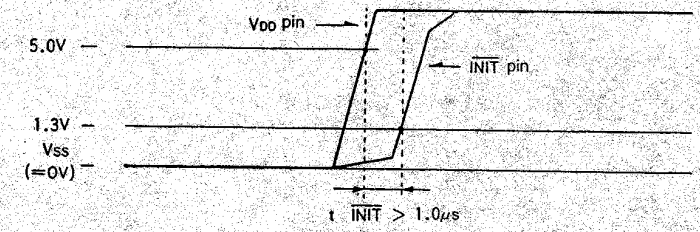


V_{DD} must remain at 5.0 V or higher (crystal oscillator requirement) for 6.0 ms (t $\overline{HOLD}$) after the $\overline{HOLD}$ line is asserted ($\overline{HOLD}$ = 0 (< 0.3 V_{DD}). After this, V_{DD} may go as low as 3.2 V.
There are no constraints on timing for the $\overline{HOLD}$ and V_{DD} pins when the chip is leaving hold mode.
The signal can be activated in one of two orders.

If $\overline{HOLD}$ is already deactivated (> 0.7 V_{DD}), the LC7185-8750 leaves hold mode within 2.0 ms after V_{DD} rises to >5.0 V.
If V_{DD} is > 5.0 V, the LC7185-8750 enters normal mode within 2.0 ms after $\overline{HOLD}$ is deactivated.

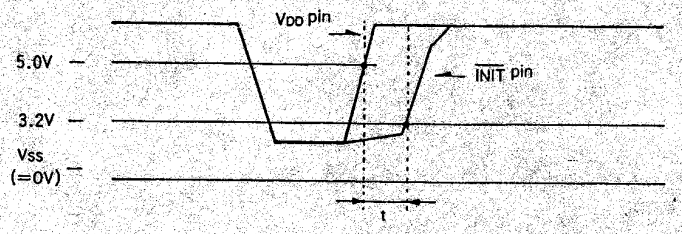
(4) Reset Timing

1. Reset timing (e.g. battery replacement)



Note: tINIT should be greater than 1.0 μs.

2. Reset caused by a sudden voltage (V_{DD}) drop



If V_{DD} drops momentarily down to less than 3.2 V and rises up to more than 5.0 V t > tINIT (t > 1.0 μs), a reset may be generated.

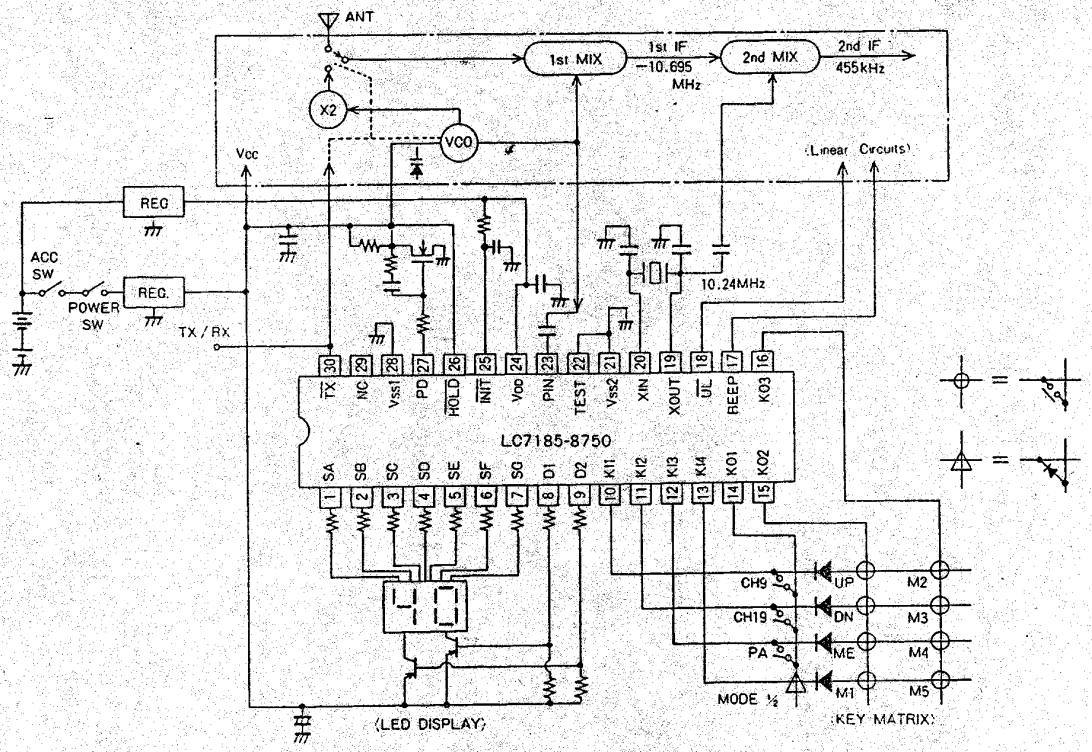
Frequency Table (U.S.A.: LC7185-8750)

Ref 25

CHANNEL	FREQUENCY (MHz)	RX ($\overline{TX}$ = 1)		TX ($\overline{TX}$ = 0)	
		N	Fvco	N	Fvco
1	26.965	6508	16.27	5393	13.4825 X2
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

V_{CO} (TX) = RF ÷ 2
V_{CO} (RX) = RF − 10.695 MHz (IF)
CH1: V_{CO} (TX) = 26.965 ÷ 2 = 13.4825
V_{CO} (RX) = 26.965 − 10.965 = 16.27

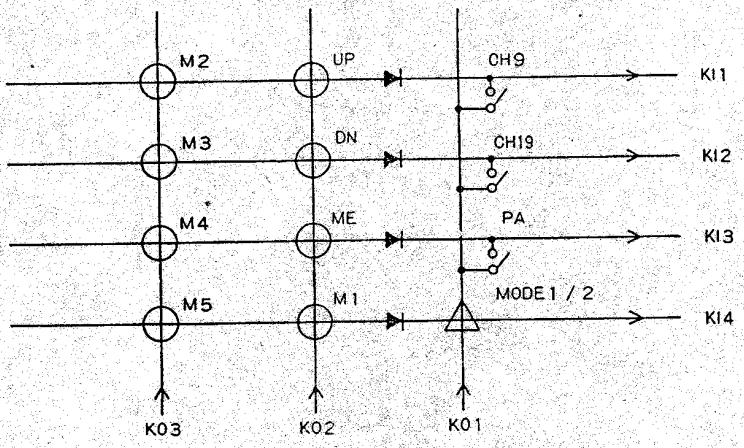
Sample Application Circuit



Pin Descriptions

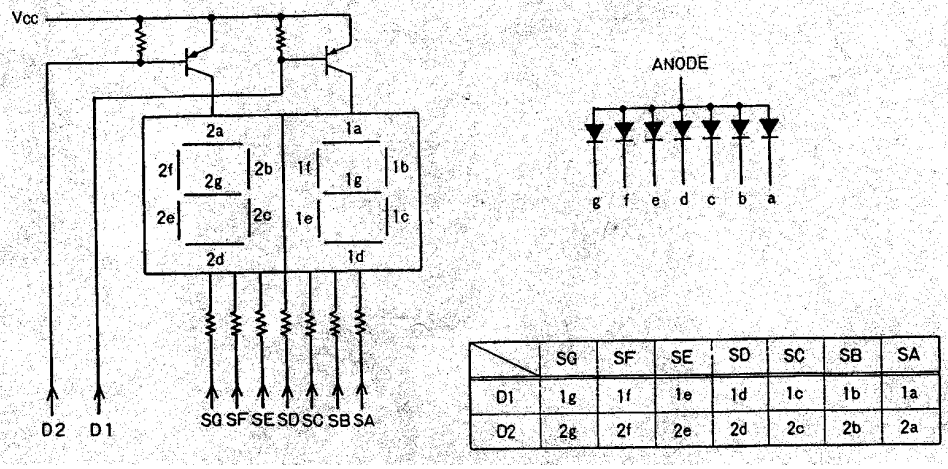
$\overline{TX}$	Transmit/receive select	PD	Charge pump output
$\overline{HOLD}$	Hold mode select	NC	NC pin
$\overline{INIT}$	Initial input	SA to SG	Segment driver (for display)
TEST	Test point (input)	D1, D2	Digit output (for display)
V_{DD}, $V_{SS}1$, $V_{SS}2$	Power supply	KI1 to KI4	Key inputs
PIN	Programmable divider input	KO1 to KO3	Key scan outputs
XIN, XOUT	Crystal oscillator input, output (10.240 MHz)	BEEP	Beep-tone control output
$\overline{UL}$	Unlock detection signal output		

Key Matrix



CH9	Emergency CH9 recall	ME	Station Memory Enable
CH19	Emergency CH19 recall	M1 to M5	Station Memory recall
PA	Public announcement display	UP/DN/ME/M1 to 5	Momentary SW
MODE 1/2	Display Mode	CH9/CH19/PA	Slide SW
UP	CH up/scan	MODE 1/2	Diode
DN	CH down/scan		

LED Display Configuration (Common anode/7 segment)



	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

APPENDIX 5

FINAL RF AMPLIFIER DATA SHEETS

FOUR(4) PAGES FOR KTC2075 FOLLOW THIS SHEET

SILICON NPN TRANSISTOR
EPITAXIAL PLANAR TYPE (PCT PROCESS)

KTC2075

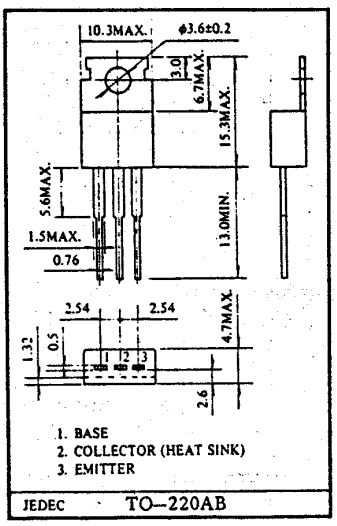
APPLICATIONS

■ 27MHz Power Amplifier Applications.

FEATURES

- Recommended for Output Stage Application of AM 4W Transmitter.
- High Power Gain.
- Wide Area of Stage Operation.

Unit in mm



■ MAXIMUM RATINGS (Ta=25℃)

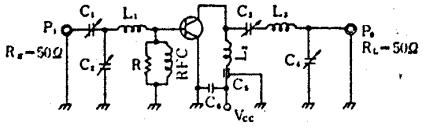
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	80	V
Collector-Emitter Voltage (R_{BE}=50Ω)	V_{CER}	80	V
Emitter-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	4	A

CHARACTERISTIC	SYMBOL	RATING	UNIT
Emitter Current	I_E	-4	A
Collector Power Dissipation (T_C=25℃)	P_C	10	W
Junction Temperature	T_j	150	℃
Storage Temperature Range	T_{stg}	-55~150	℃

■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	V_{CB}=30V, I_E=0	-	-	10	μA
Breakdown Voltage	Collector-Emitter	$V_{(BR)CER}$	I_C=10mA, R_{BE}=50Ω	80	-	-	V
	Emitter-Base	$V_{(BR)EBO}$	I_E=1.0mA, I_C=0	4.0	-	-	V
DC Current Gain		$h_{FE(1)}$	V_{CE}=5V, I_C=0.5A	25	-	-	
		$h_{FE(2)}$	V_{CE}=2V, I_C=3A	15	-	-	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=3A, I_B=0.3A	-	-	1.5	V
Transition Frequency		f_T	V_{CE}=5V, I_C=500mA	-	100	-	MHz
Collector Output Capacitance		Cob	V_{CE}=10V, I_E=0, f=1MHz	-	40	-	pF
Output Power (Fig. 1)		P_O	V_{CC}=12V, P_i=0.3W, f=27MHz	3.5	-	-	W

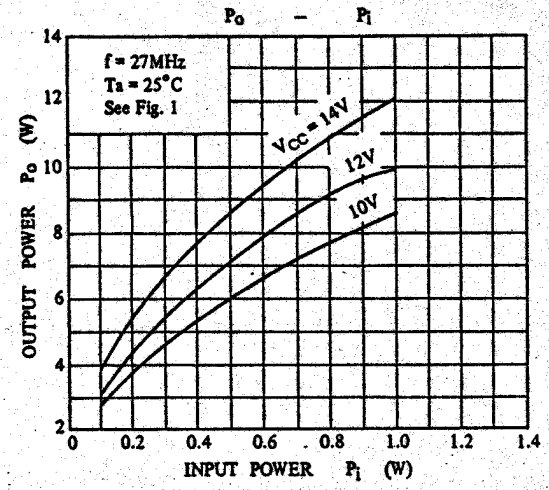
Fig. 1 P_O TEST CIRCUIT

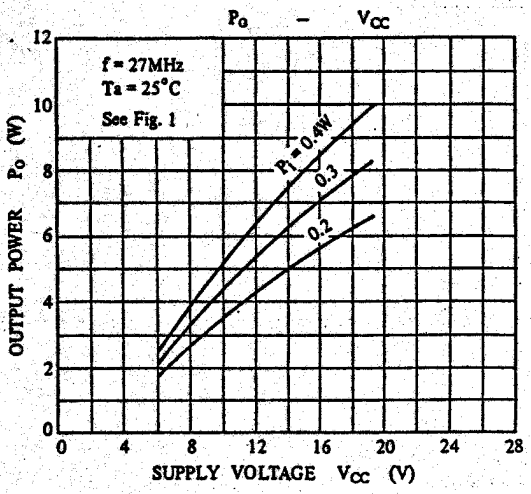


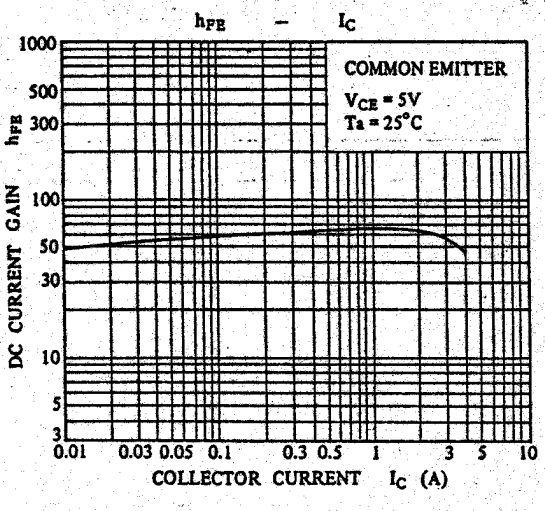
C_1 : ~100pF, C_2, C_3 : ~150pF, C_4 : ~300pF, C_5 : 1000pF
C_6 : 0.01μF R : 250Ω
L_1 : 0.8mmφ UEW, 7T, 8mm I.D L_2 : 0.8mmφ UEW, 5T, 8mm I.D
L_3 : 0.8mmφ UEW, 10T, 8mm I.D RFC : 0.35mmφ UEW, 17T, 5mm I.D

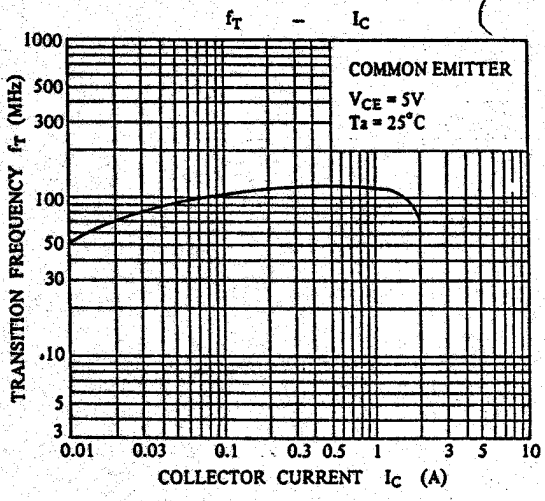
KEC

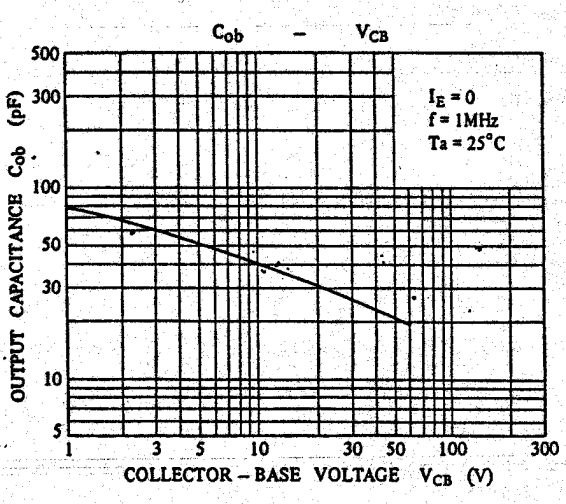
KTC2075


Po – Pi
f = 27MHz
Ta = 25°C
See Fig. 1
VCC = 14V
12V
10V
OUTPUT POWER Po (W)
INPUT POWER Pi (W)


Po – VCC
f = 27MHz
Ta = 25°C
See Fig. 1
Pi = 0.4W
0.3
0.2
OUTPUT POWER Po (W)
SUPPLY VOLTAGE VCC (V)


hFE – IC
COMMON EMITTER
VCE = 5V
Ta = 25°C
DC CURRENT GAIN hFE
COLLECTOR CURRENT IC (A)


fT – IC
COMMON EMITTER
VCE = 5V
Ta = 25°C
TRANSITION FREQUENCY fT (MHz)
COLLECTOR CURRENT IC (A)


Cob – VCB
IE = 0
f = 1MHz
Ta = 25°C
OUTPUT CAPACITANCE Cob (pF)
COLLECTOR – BASE VOLTAGE VCB (V)

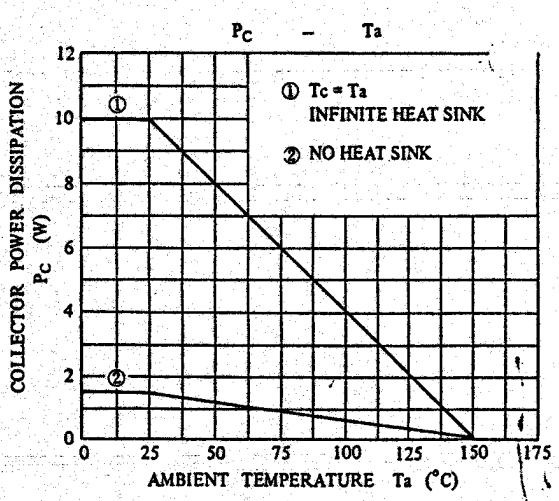
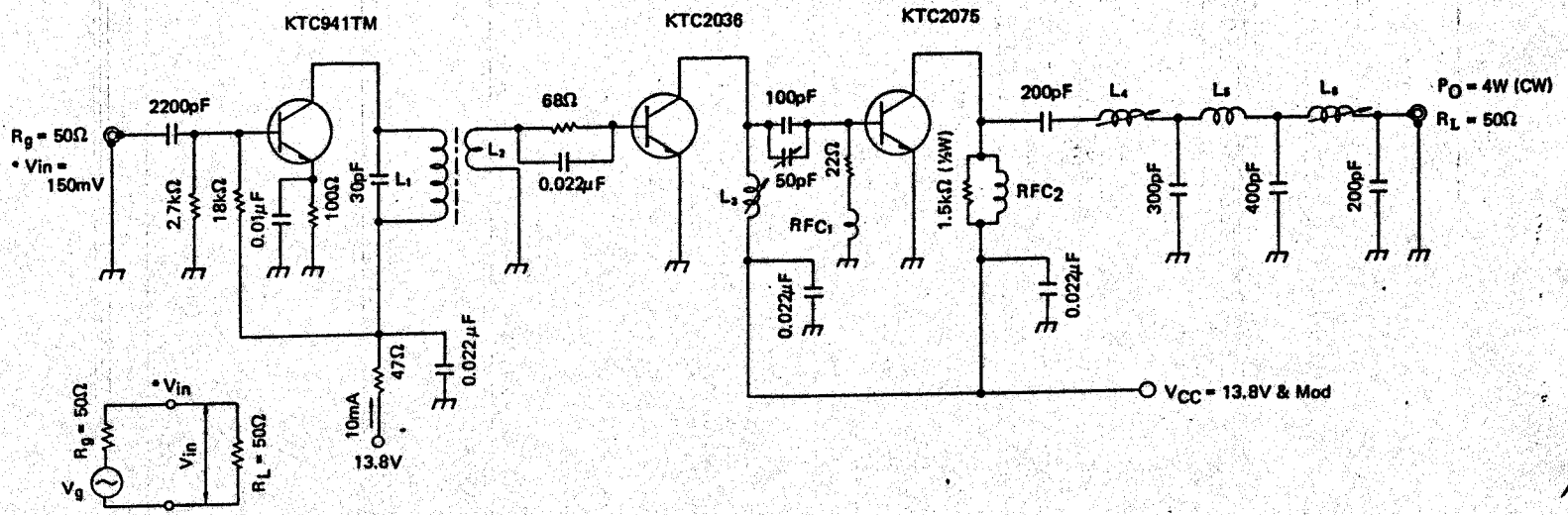

PC – Ta
① Tc = Ta
INFINITE HEAT SINK
② NO HEAT SINK
COLLECTOR POWER DISSIPATION PC (W)
AMBIENT TEMPERATURE Ta (°C)

Fig. 2. 27MHz 4W Output AM Transceiver Circuit



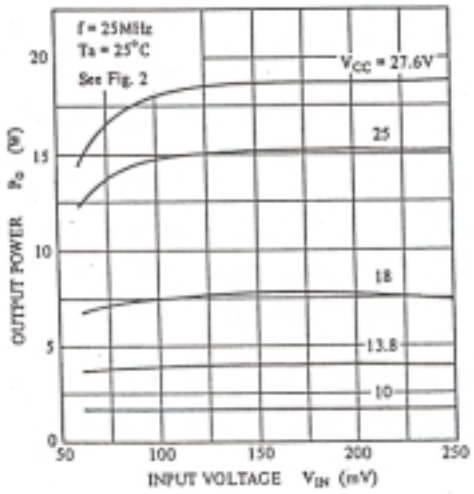
L_1 : 4mmϕ BOBBIN WITH FERRITE CORE, 0.08mmϕ UEW, 8 TURNS
L_2 : 4mmϕ BOBBIN WITH FERRITE CORE, 0.08mmϕ UEW, 2 TURNS
L_3, L_6 : 6.5mmϕ BOBBIN WITH FERRITE CORE, 0.6mmϕ Sn PLATED COPPER WIRE 6½ TURNS
L_4 : 6.5mmϕ BOBBIN WITH FERRITE CORE, 0.6mmϕ Sn PLATED COPPER WIRE 8½ TURNS
L_5 : 0.6mmϕ Sn PLATED COPPER WIRE, 6.5mm I.D, 8½ TURNS
RFC_1 : 47μH, 7BA–480k (TOKO)
RFC_2 : 0.2mmϕ UEW, 30 TURNS

RESISTER : ¼W CARBON
CAPACITER : CERAMIC

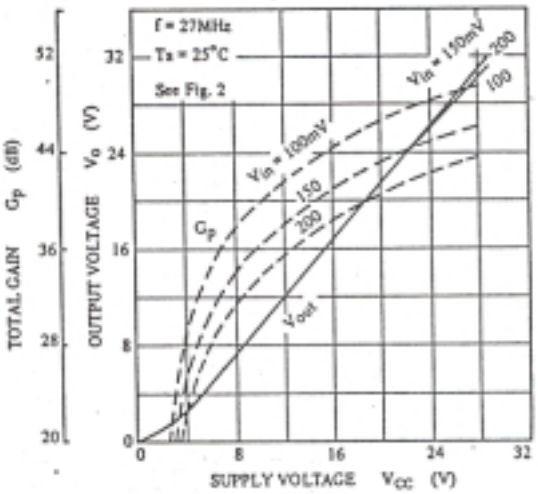
KTC2075

APPLICATION CIRCUIT CHARACTERISTIC

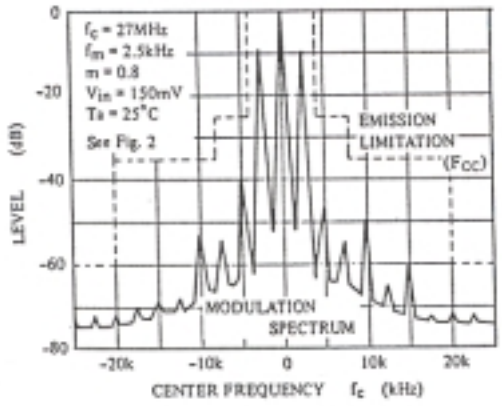
P_O – V_{IN}



V_O, G_p – V_{CC}



80% MODULATION SPECTRUM
EMISSION LIMITATION (F_{CC})



85% MODULATION SPECTRUM
EMISSION LIMITATION (F_{CC})