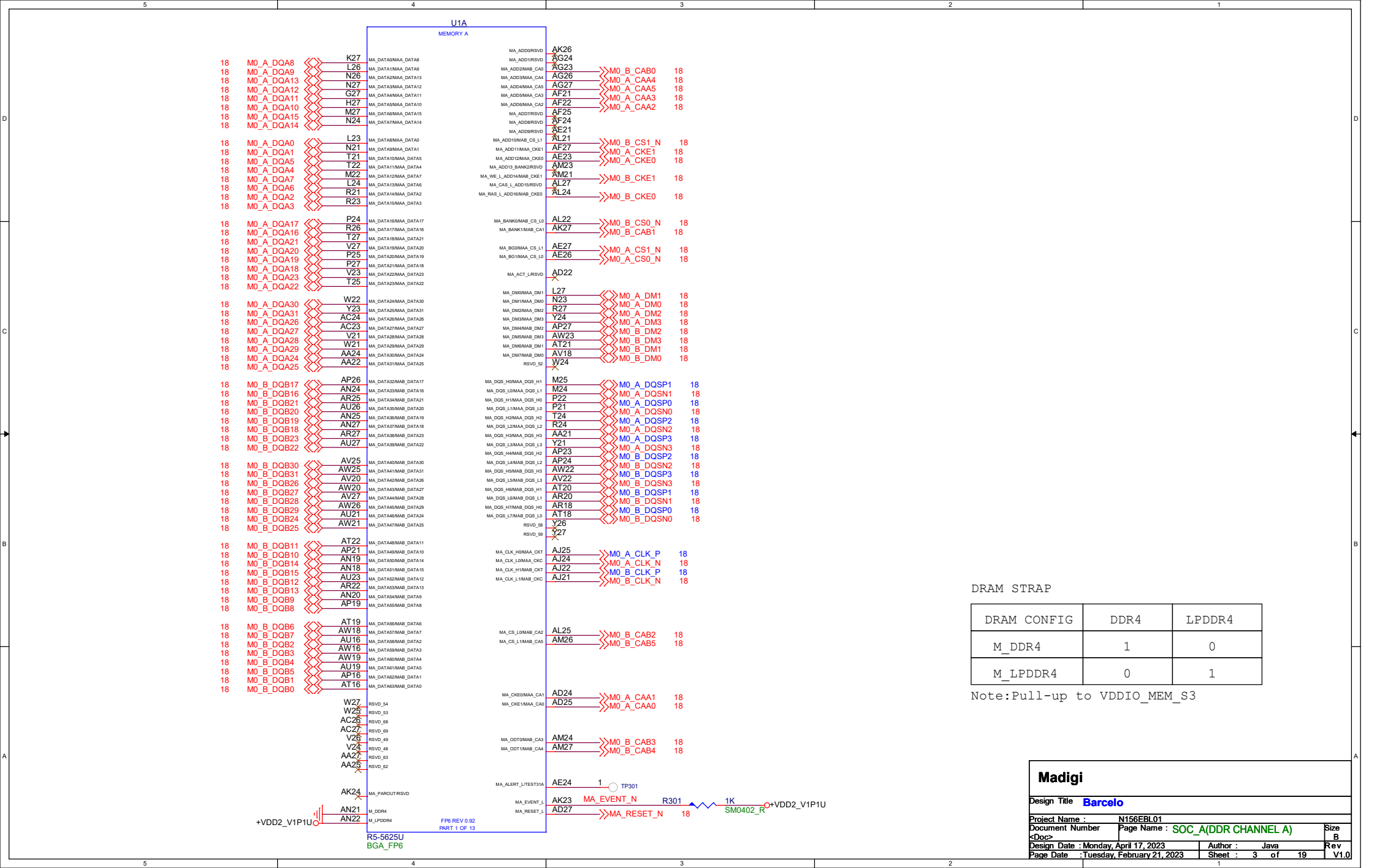
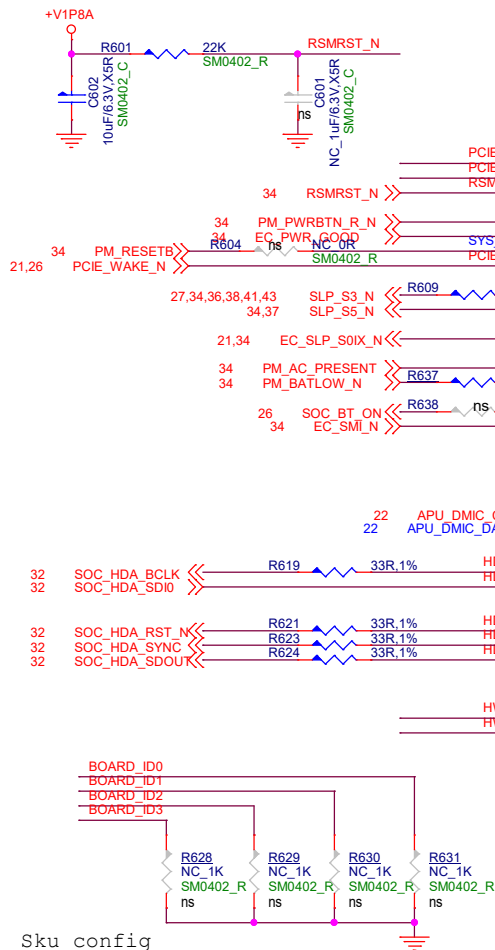




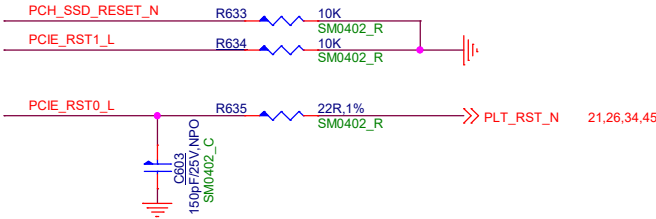


Sku config

SKU	Realtek R615	AC7265 R615
WIFI	1	0
SKU	1	0
SKU	1	0
SKU	1	0
SKU	1	0

Note:GPB5-8 BIOS Default 20K pull high.

STRAP	DEFINITION
SYS_RST#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

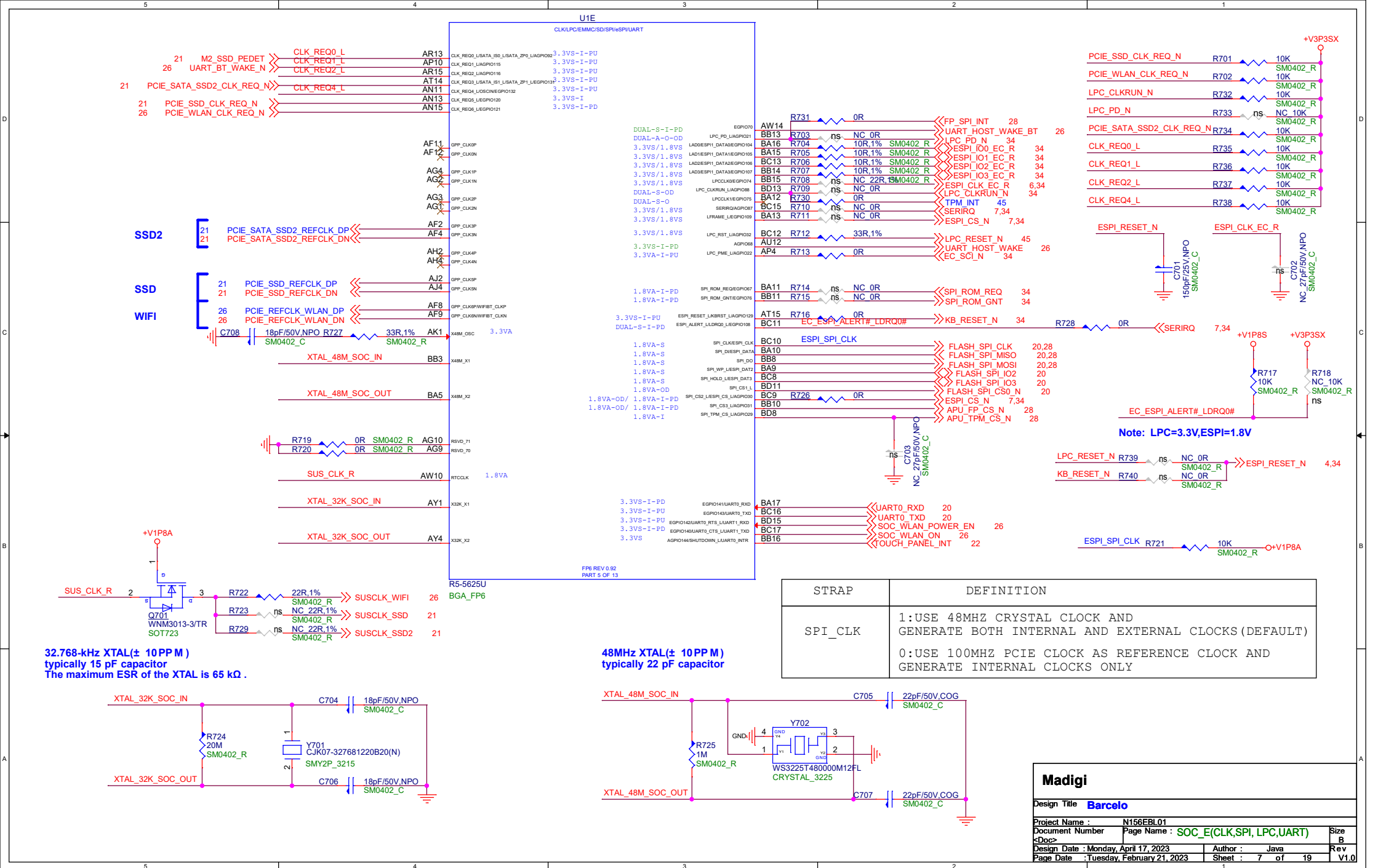


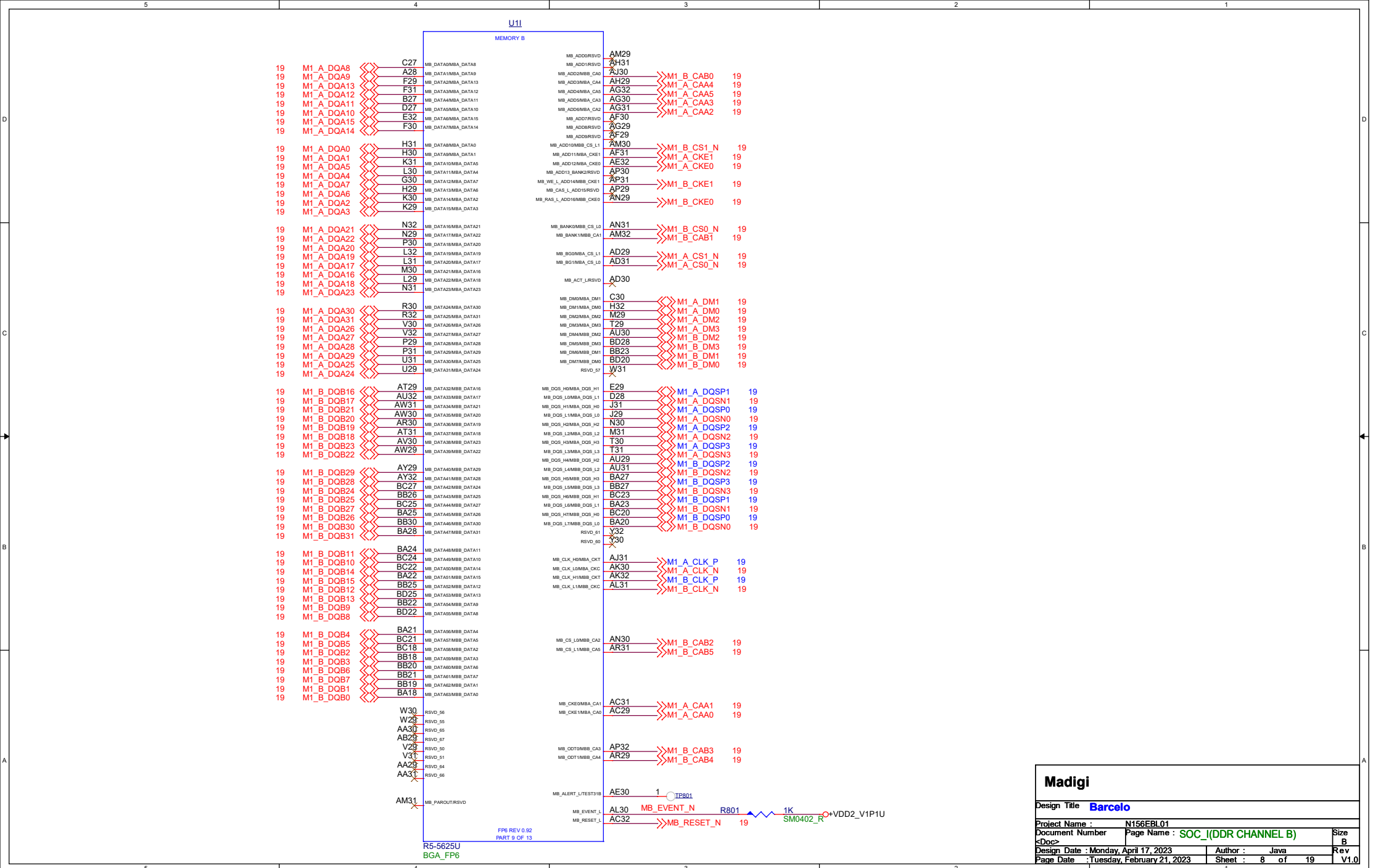
DRAM config

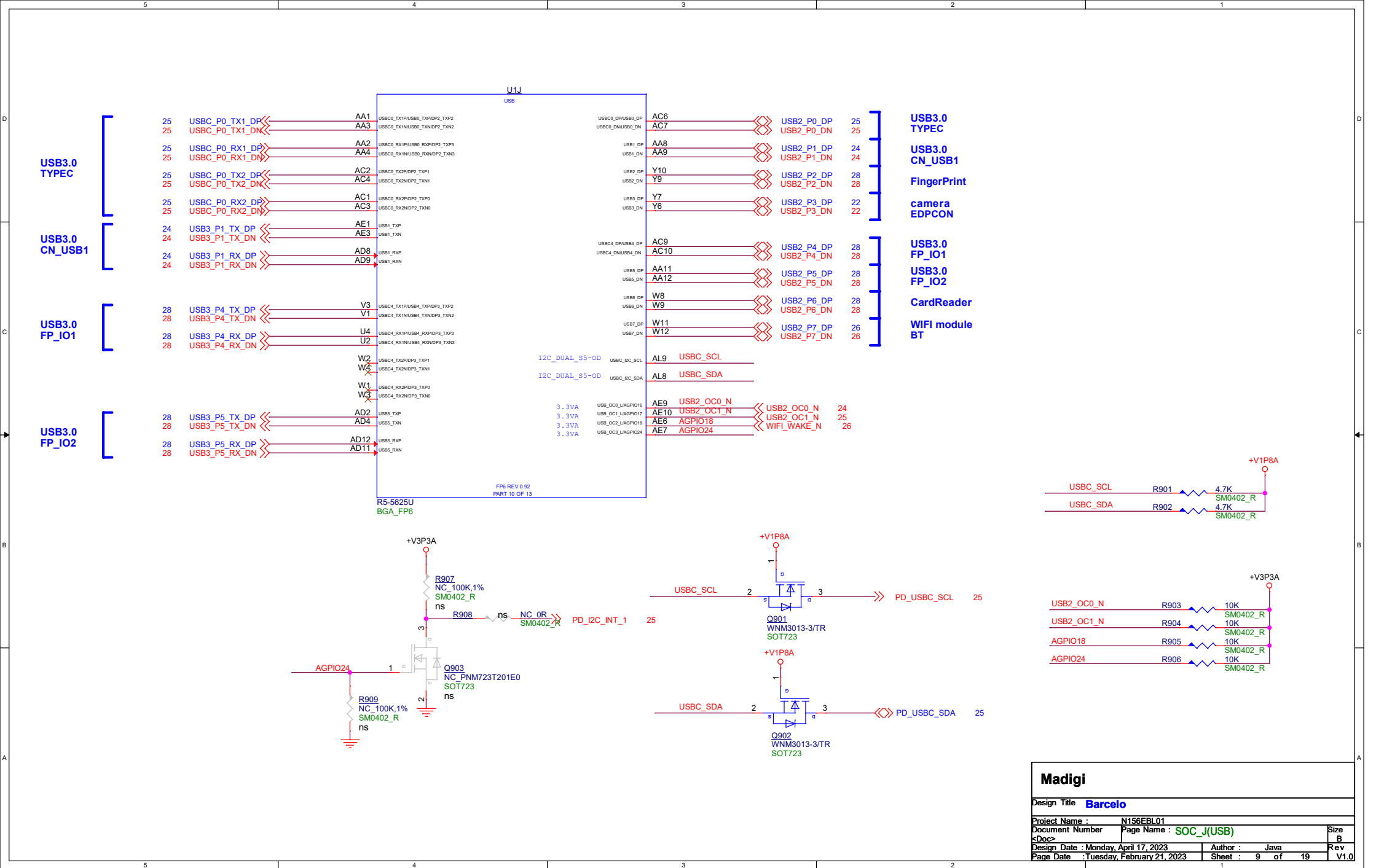
DRAM CONFIG	HW_ID1	HW_ID2
4x2GB	0	0
4x4GB	0	1
2x2GB	1	0
2x4GB	1	1

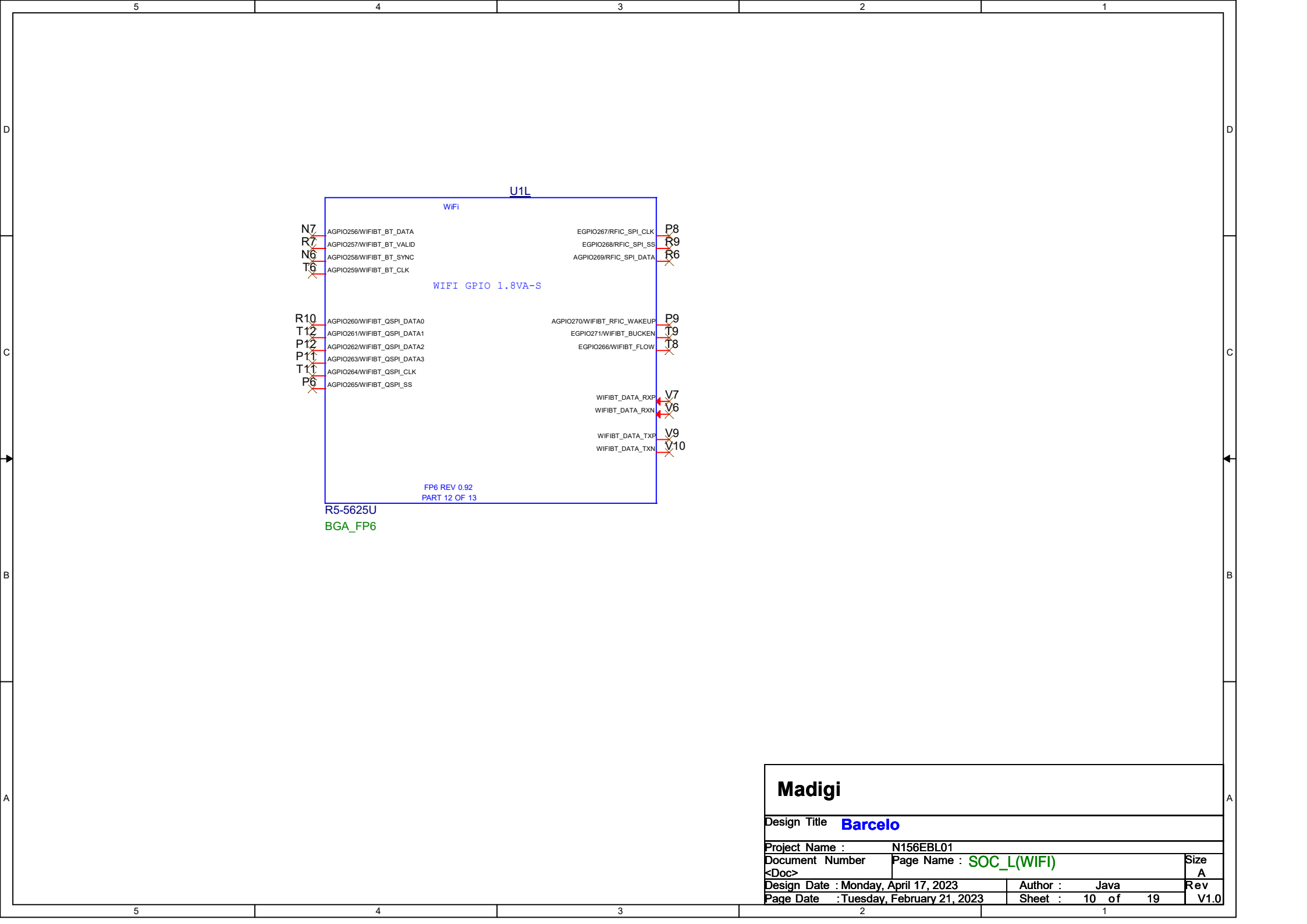
Madigi

Design Title	Barcelo
Project Name	N156EBL01
Document Number	Page Name : SOC_D(HDA, ACPI,I2C,GPIO)
Design Date	Monday, April 17, 2023
Author	Java
Page Date	Tuesday, February 21, 2023
Sheet	6 of 19
Rev	V1.0

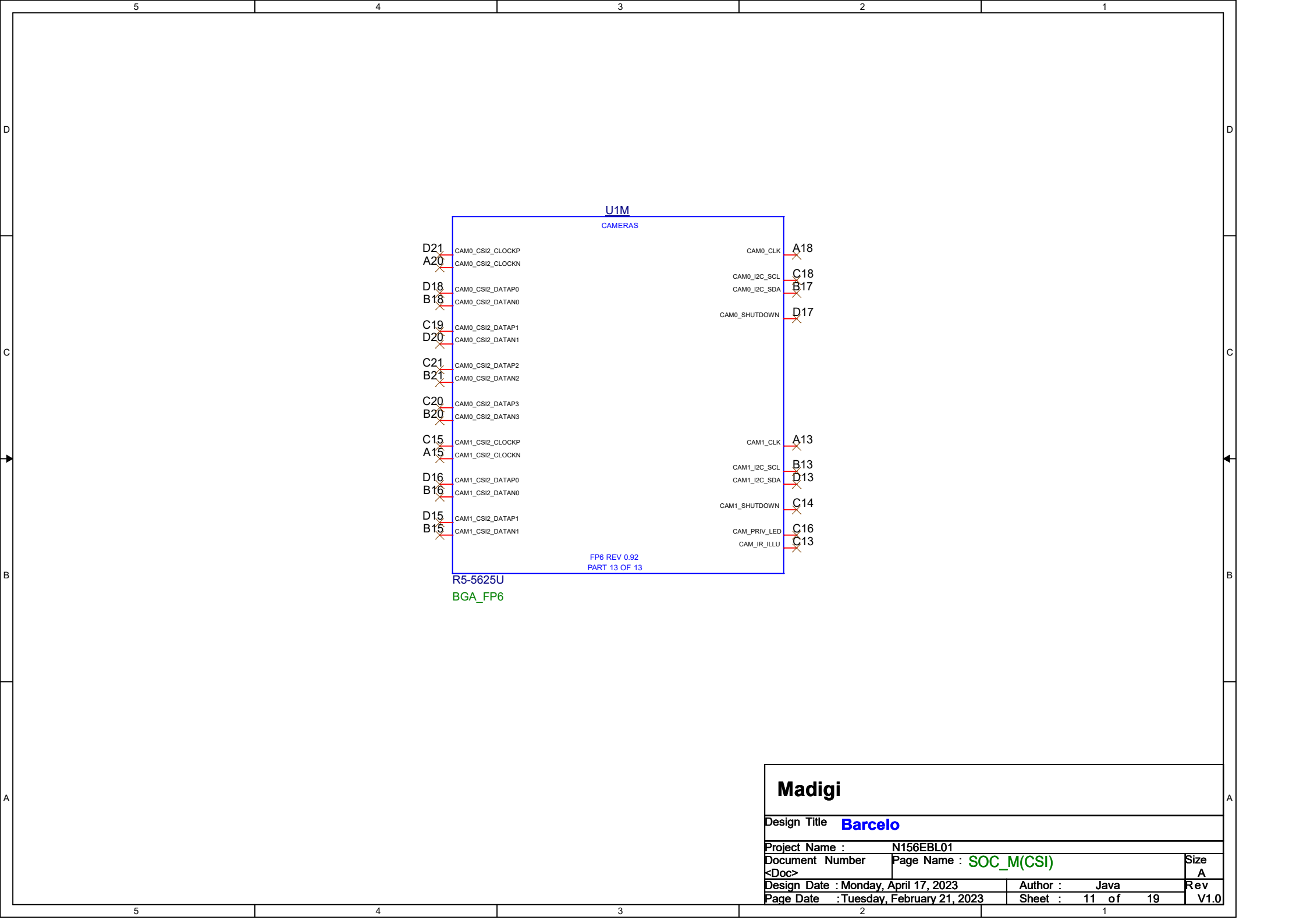




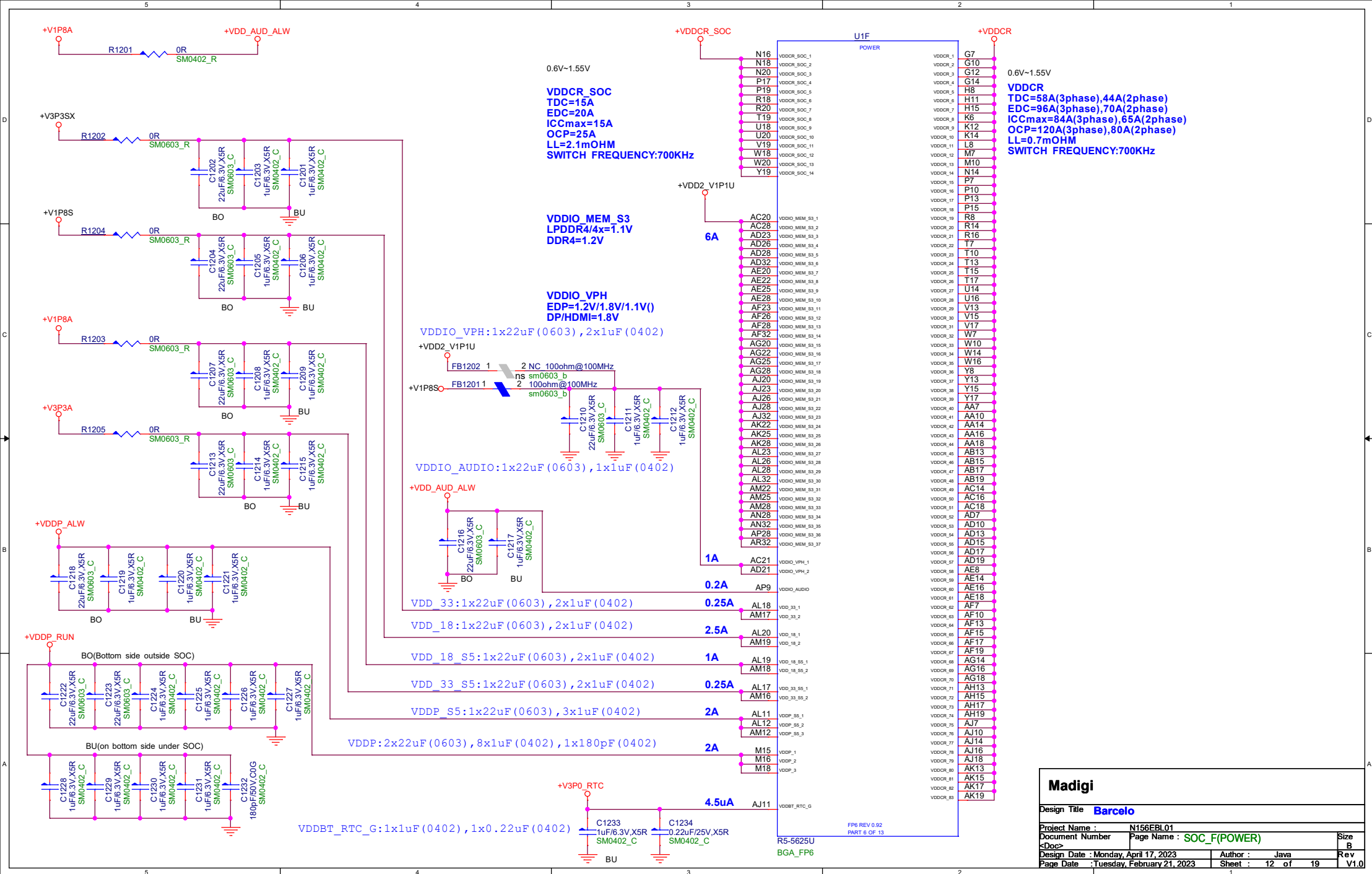


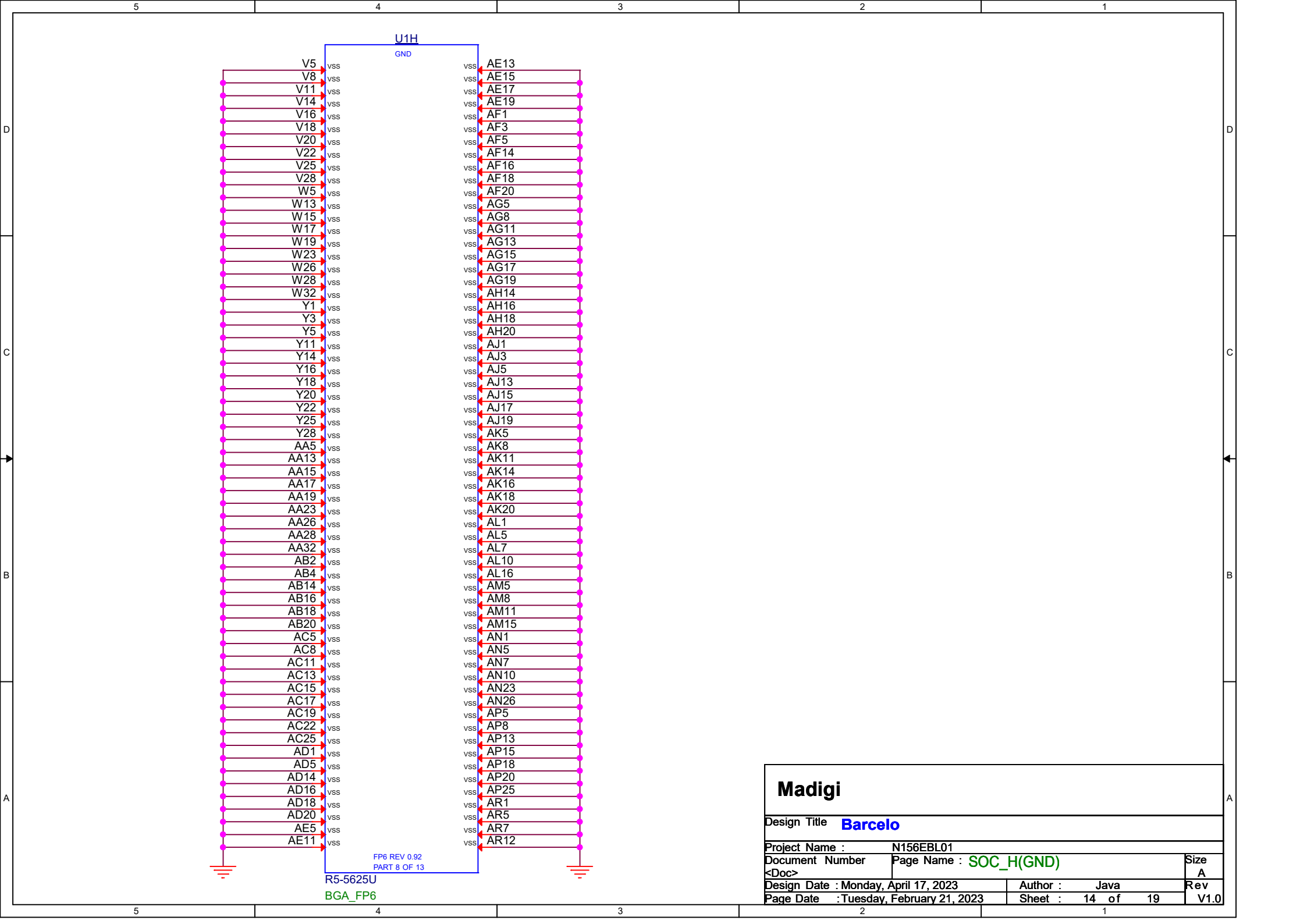


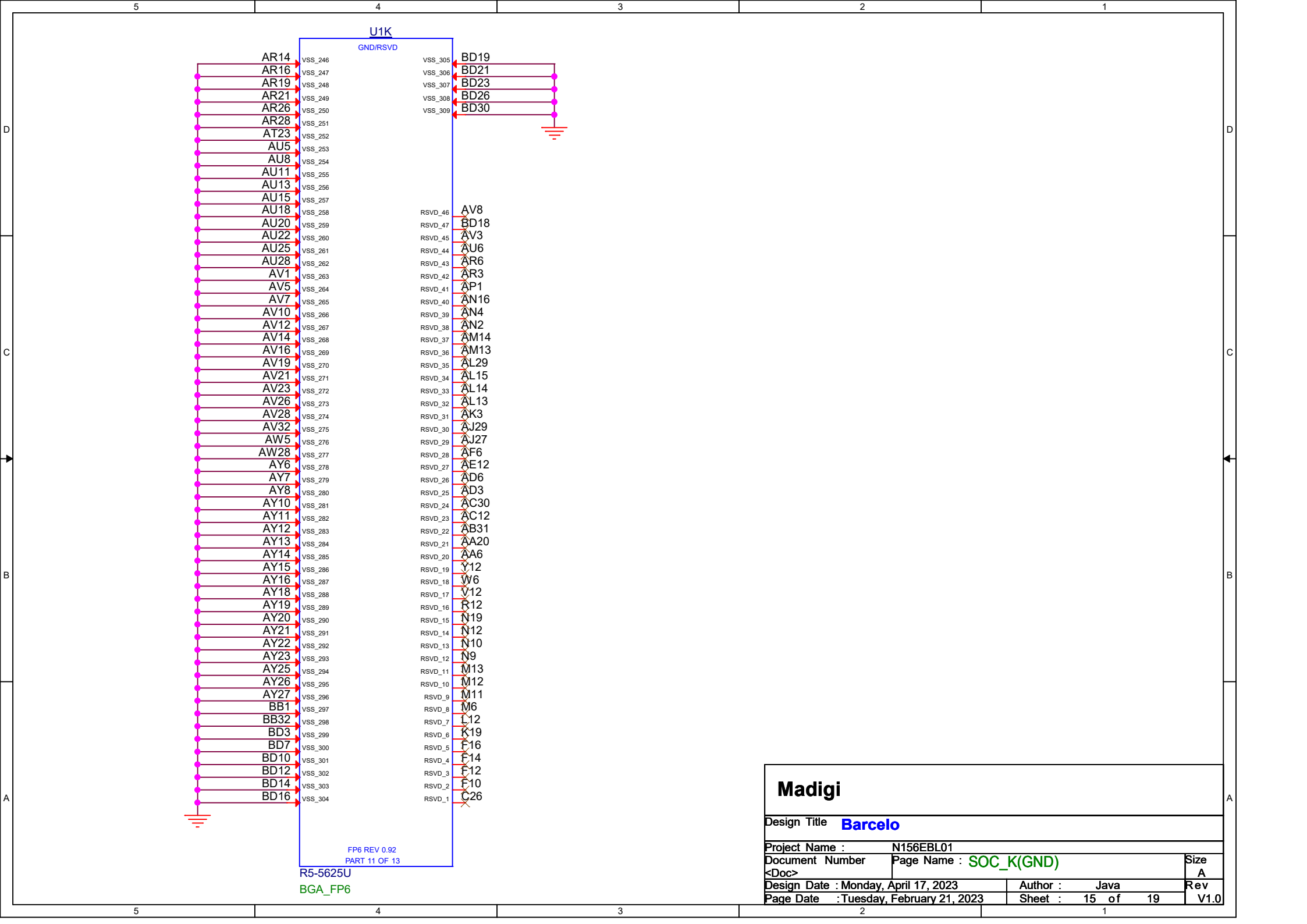
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Design Title Barcelo			
Project Name : N156EBL01			
Document Number	Page Name : SOC_L(WIFI)		Size A
<Doc>			Rev
Design Date : Monday, April 17, 2023		Author : Java	Rev
Page Date : Tuesday, February 21, 2023		Sheet : 10 of 19	V1.0



Madigi			
Design Title Barcelo			
Project Name : N156EBL01			
Document Number	Page Name : SOC_M(CSI)		Size A
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Design Date : Monday, April 17, 2023		Author : Java	
Page Date : Tuesday, February 21, 2023		Sheet : 11 of 19	V1.0

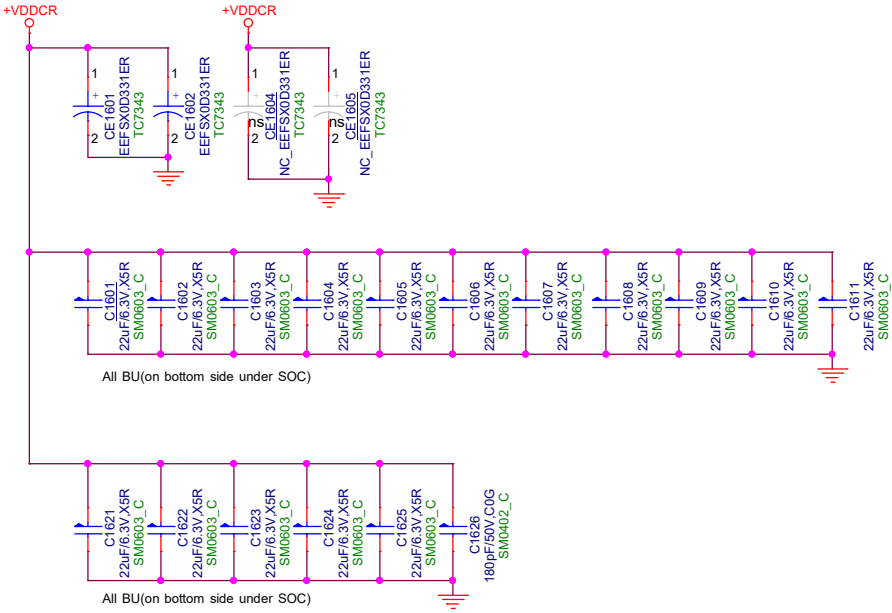




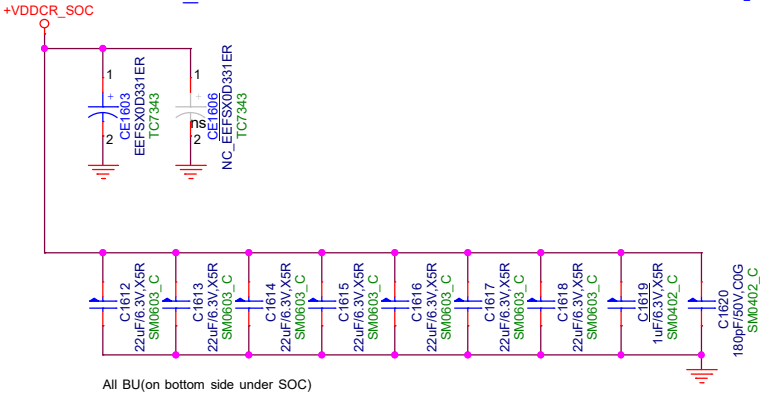


Madigi			
Design Title Barcelo			
Project Name : N156EBL01			
Document Number	Page Name : SOC_K(GND)		Size A
Design Date : Monday, April 17, 2023		Author : Java	Rev
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VDDCR:16x22uF (0603) ,1x180pF (0402)



VDDCR_SOC:7x22uF (0603) ,1x1uF (0402) ,1x180pF (0402)



Madigi

Design Title **Barcelo**

Project Name : N156EBL01

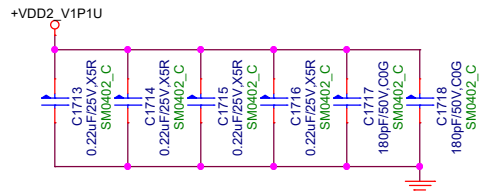
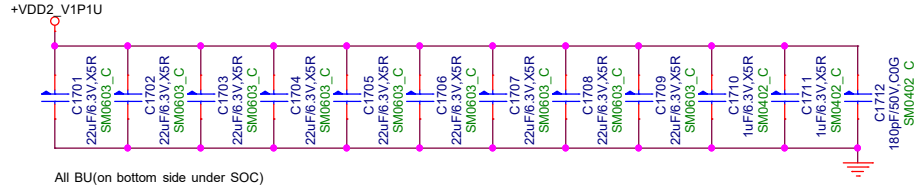
Document Number Page Name : **SOC (DECOUPLING - 1 OF 2)**

Design Date : Monday, April 17, 2023 Author : Java

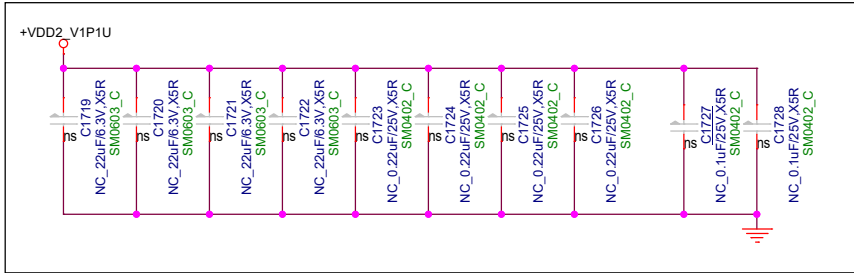
Page Date : Tuesday, February 21, 2023 Sheet : 16 of 19

Size
B
Rev
V1.0

VDDIO_MEM_S3: 9x22uF (0603), 2x1uF (0402), 4x0.22uF (0402), 1x180pF (0402)



VDDIO_MEM_S3(place hole): 4x22uF (0603), 4x0.22uF (0402), 2x0.1uF (0402)



Madigi

Design Title **Barcelo**

Project Name : N156EBL01

Document Number Page Name : **SOC (DECOUPLING - 2 OF 2)**

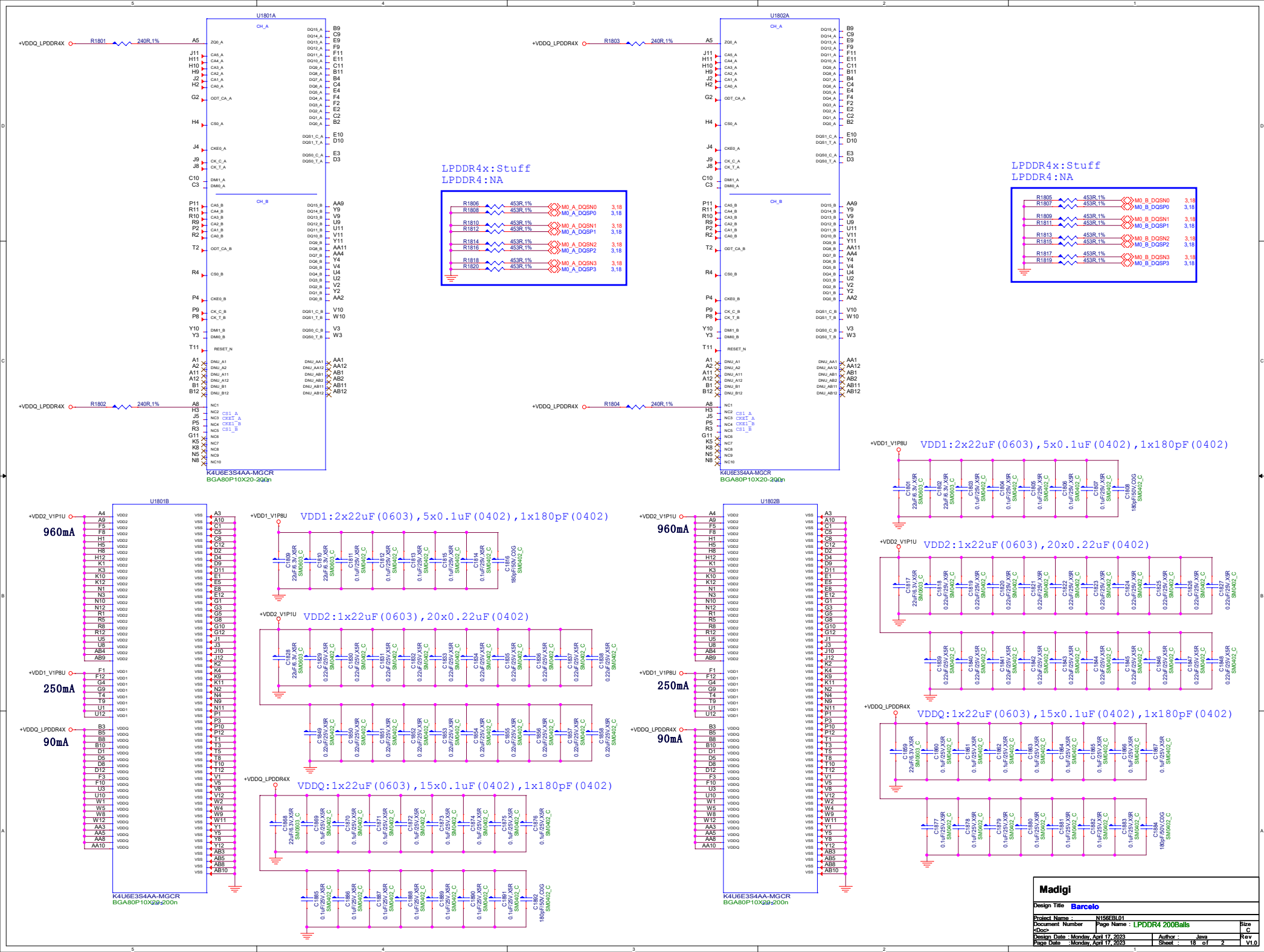
Design Date : Monday, April 17, 2023

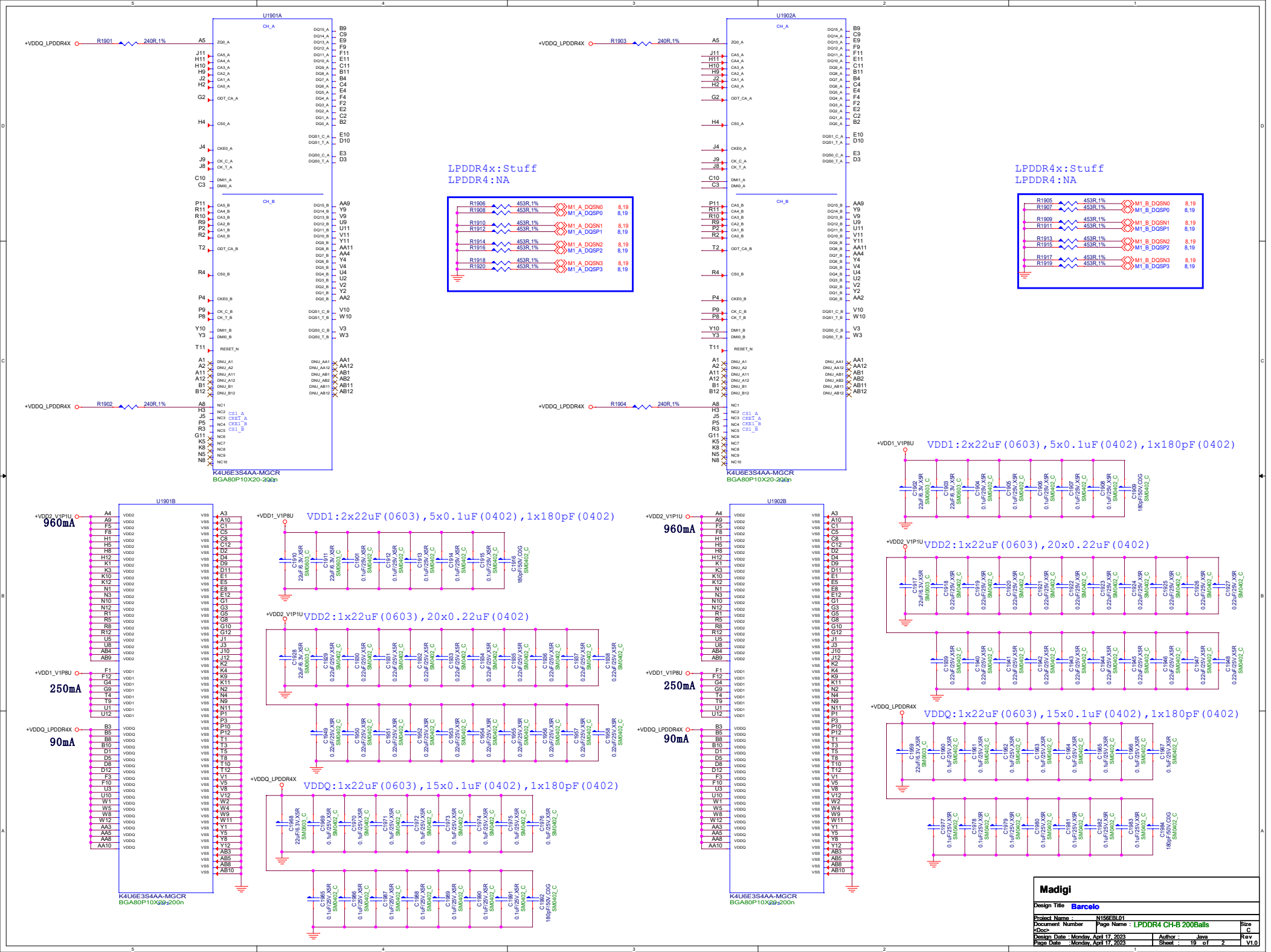
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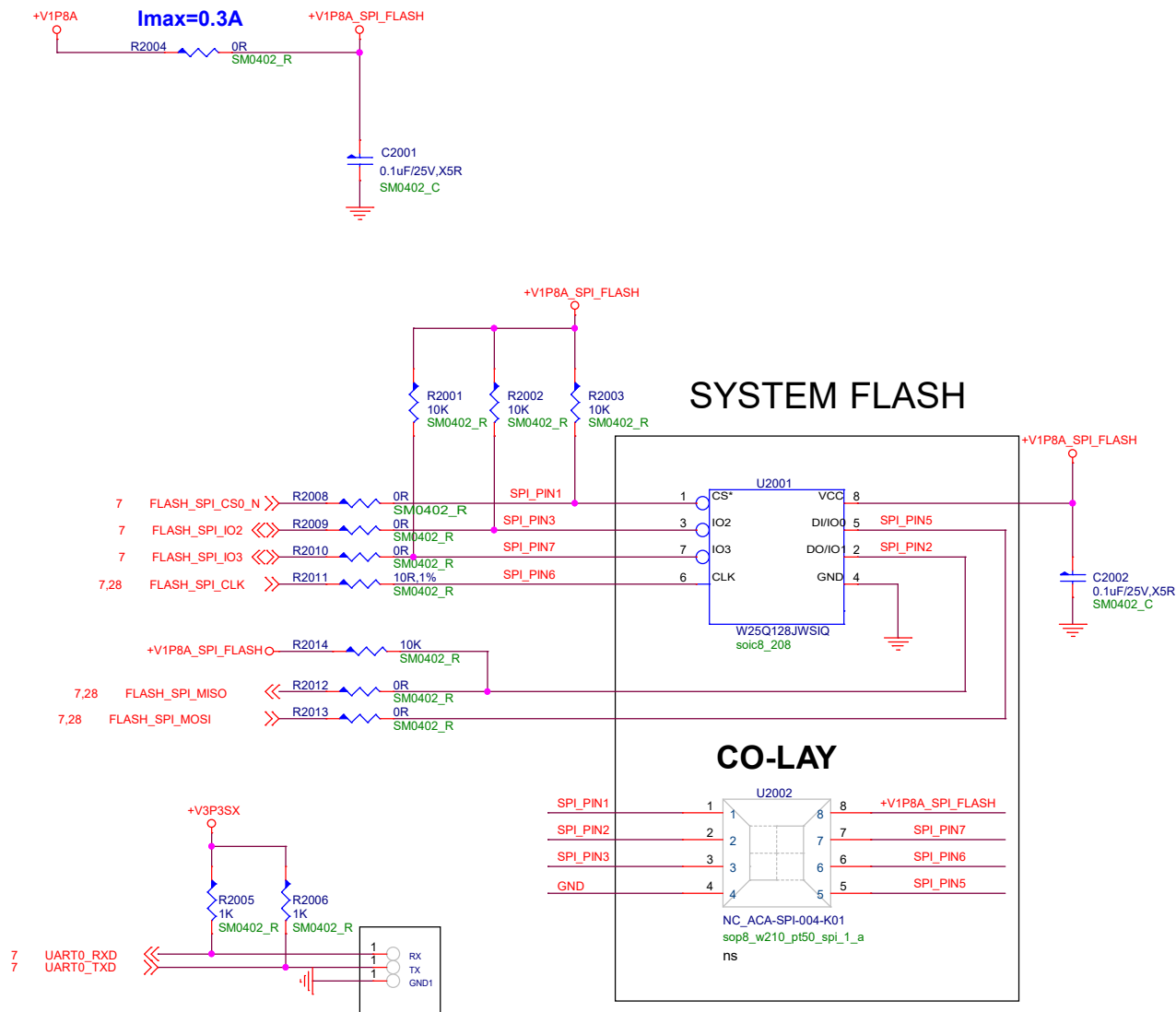
Author : Java

Sheet : 17 of 19

Size B Rev V1.0



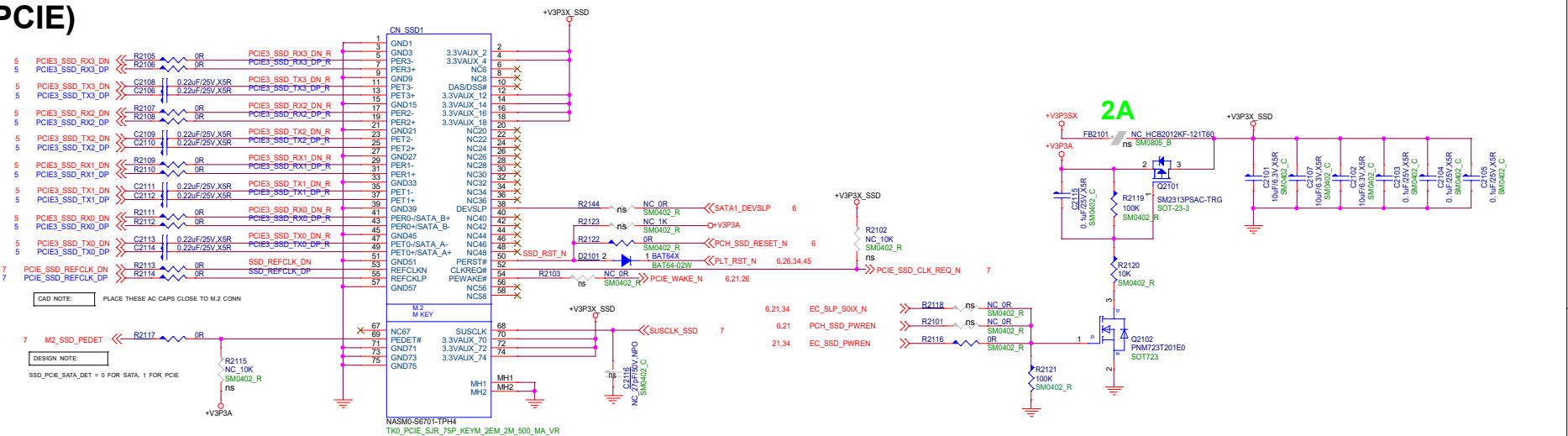




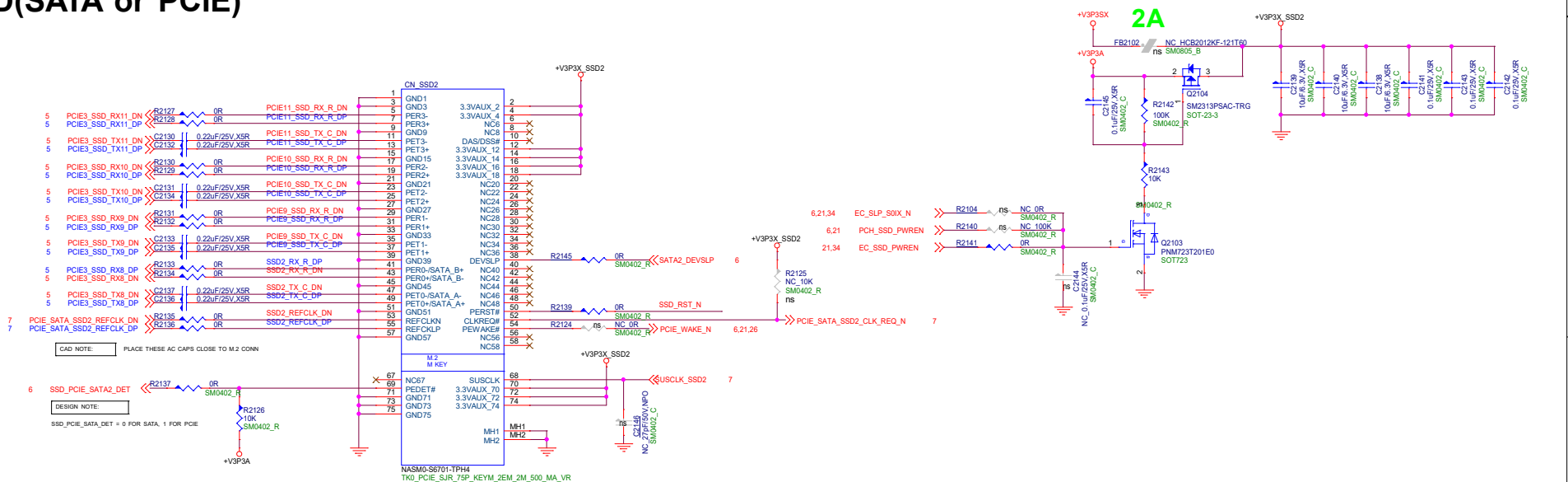
DVT/PVT/MP Stuff U2001
EVT Stuff U2002

Madigi			
Design Title Barcelo			
Project Name : N156EBL01			
Document Number	Page Name : SYSTEM FLASH		Size B
Design Date : Monday, April 17, 2023	Author : Java		Rev
Page Date : Tuesday, February 21, 2023	Sheet : 20 of 48		V1.0

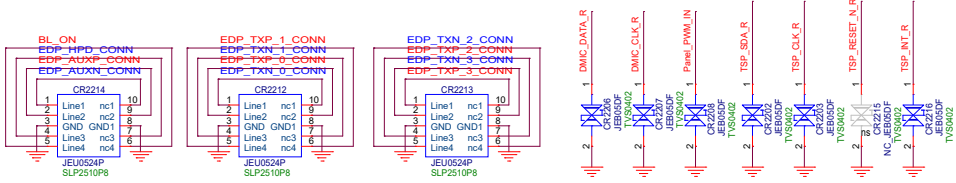
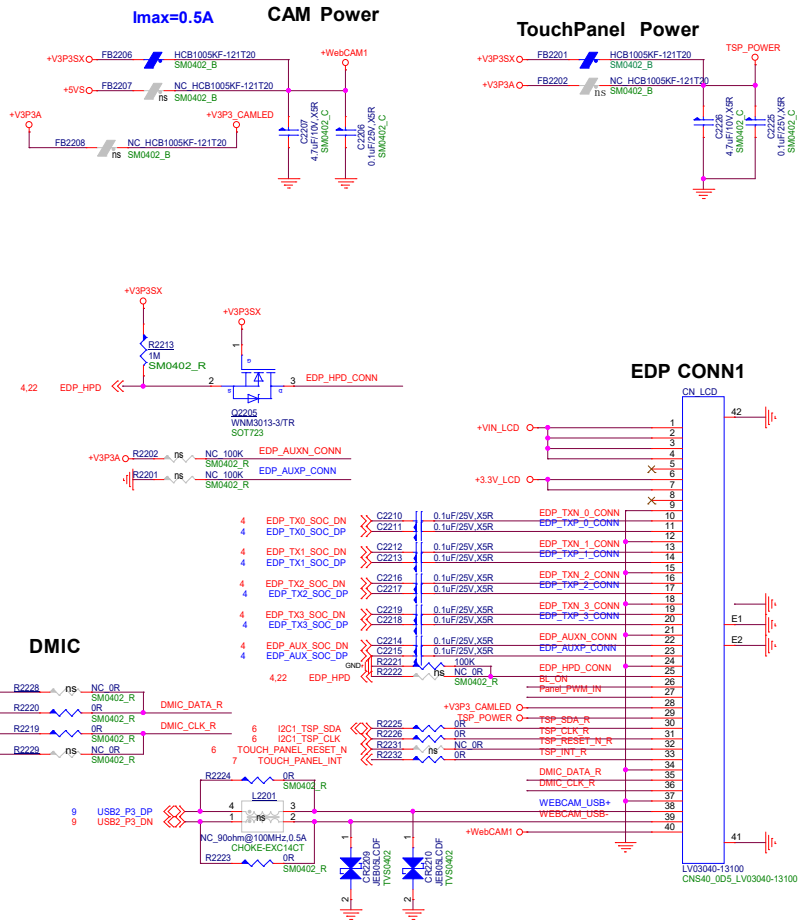
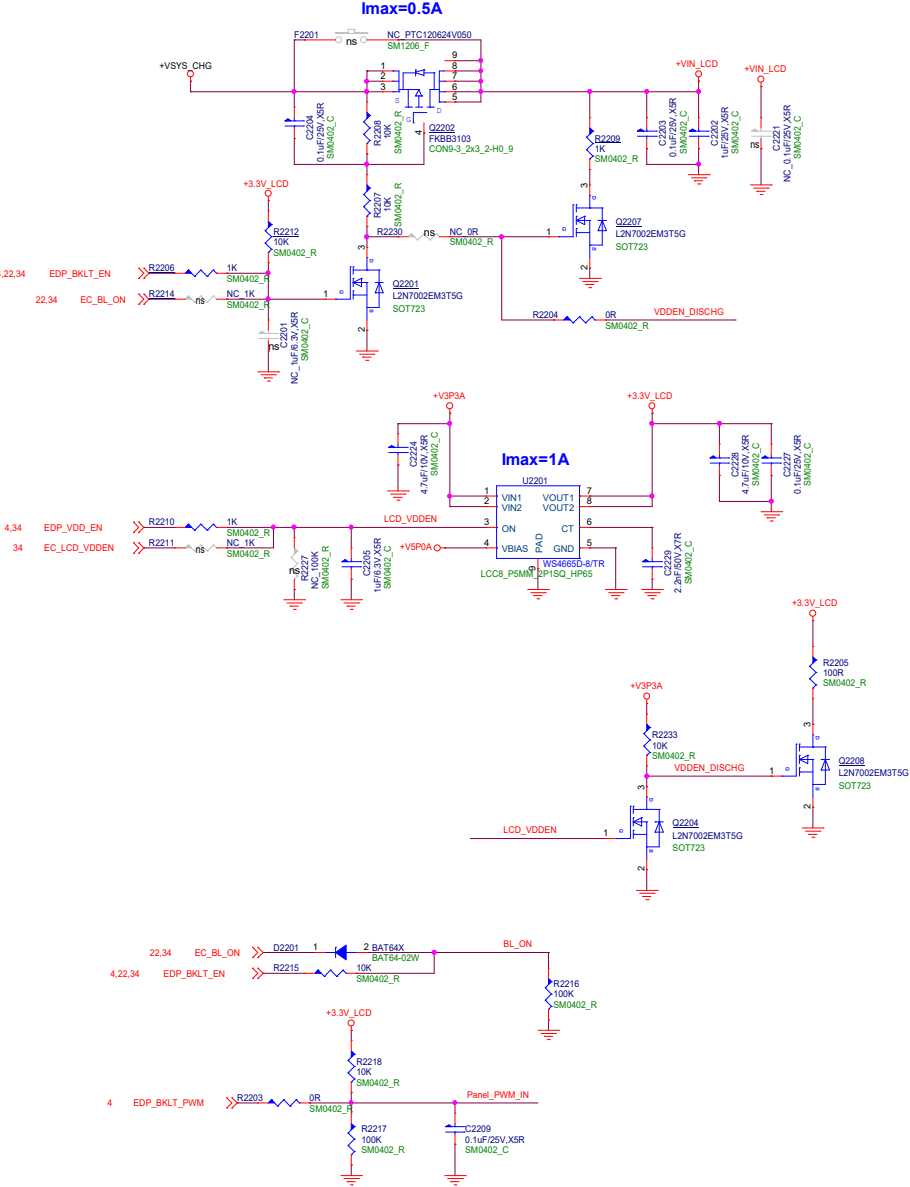
M.2 SSD(PCIE)



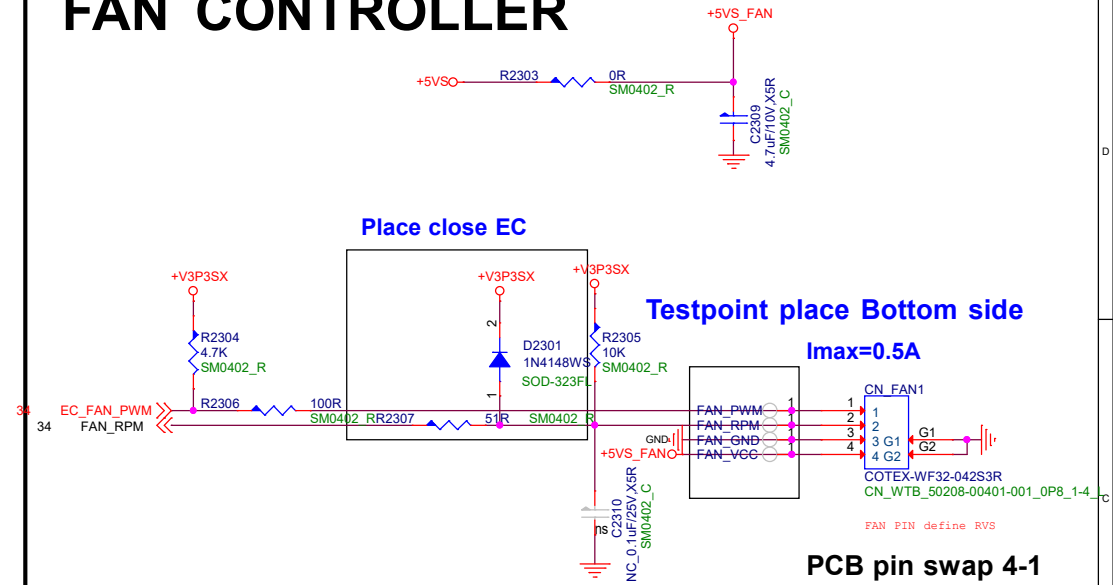
M.2 SSD(SATA or PCIE)



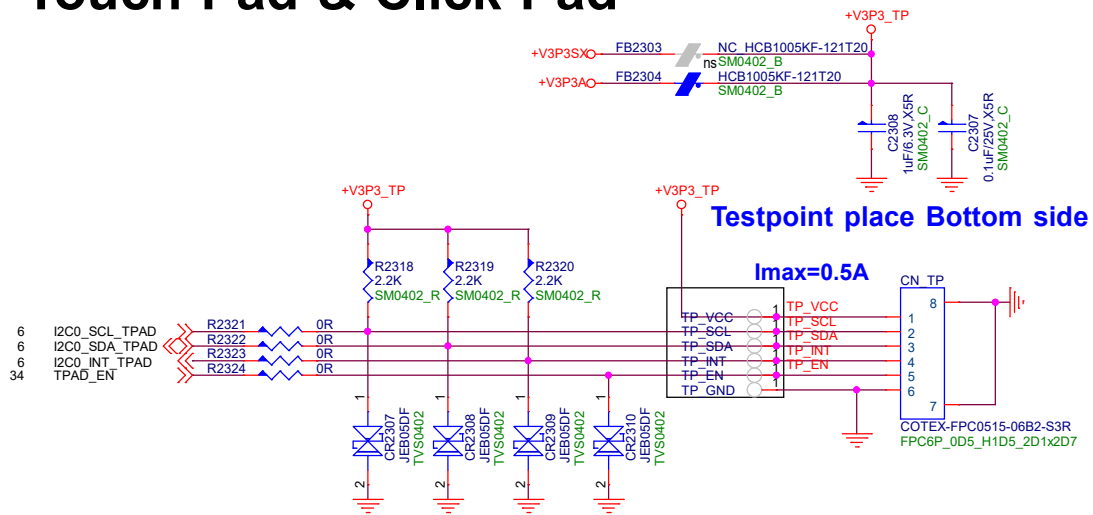
EDP Power



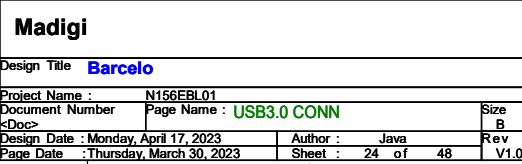
FAN CONTROLLER



Touch Pad & Click Pad

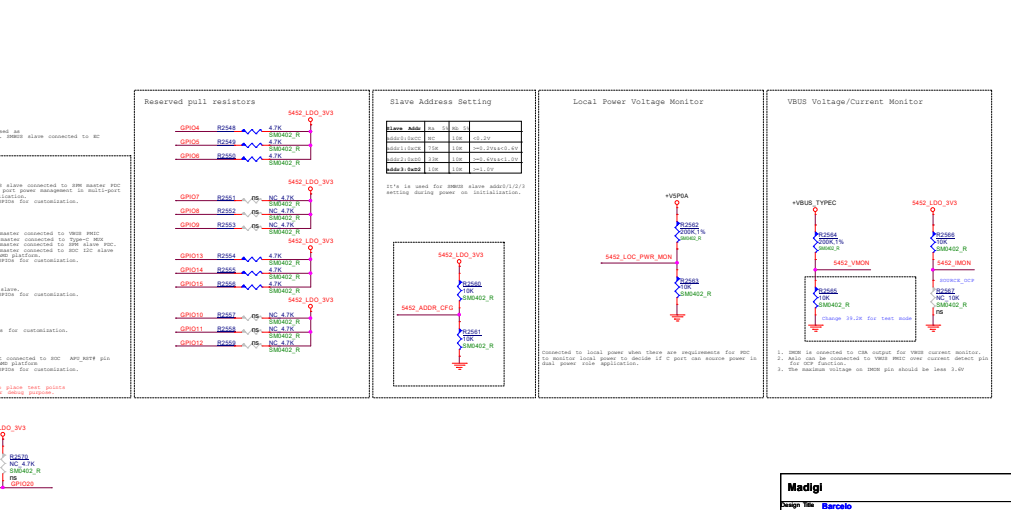
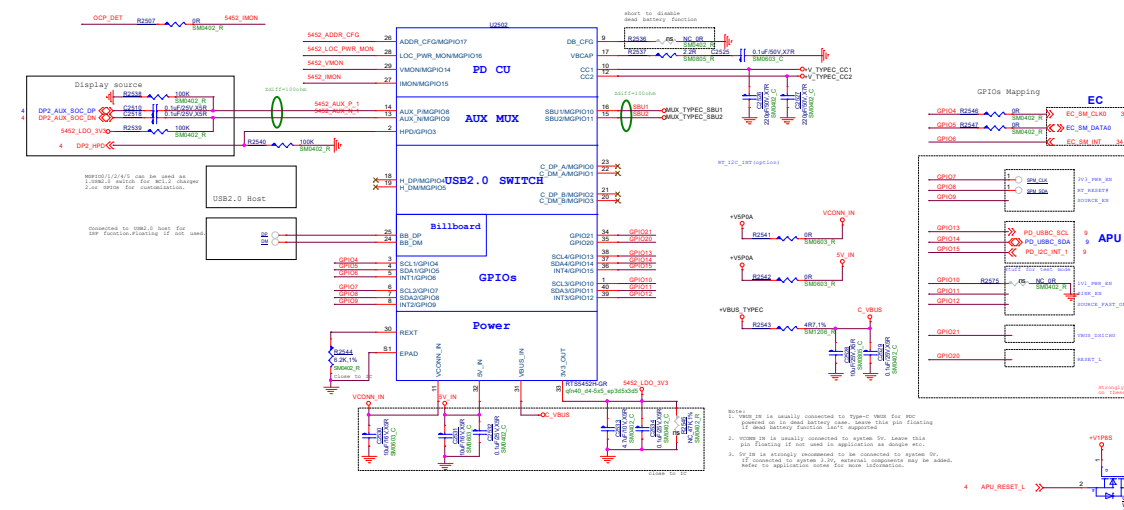
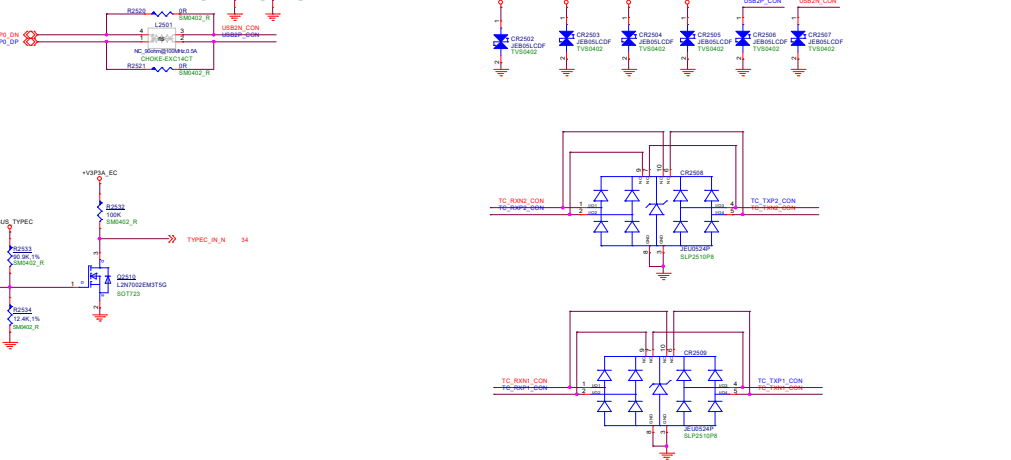
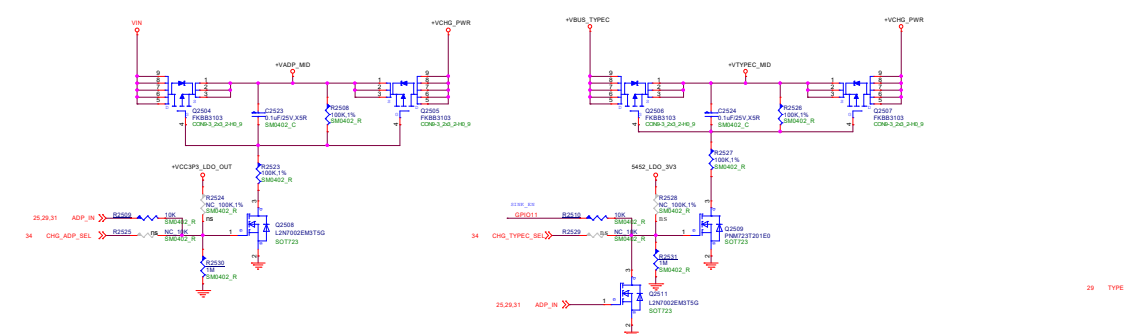
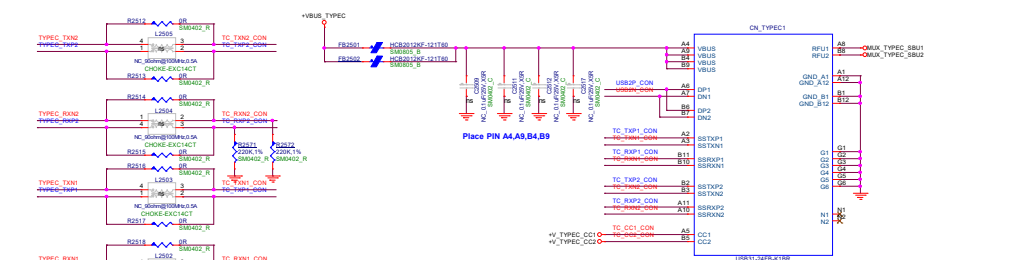
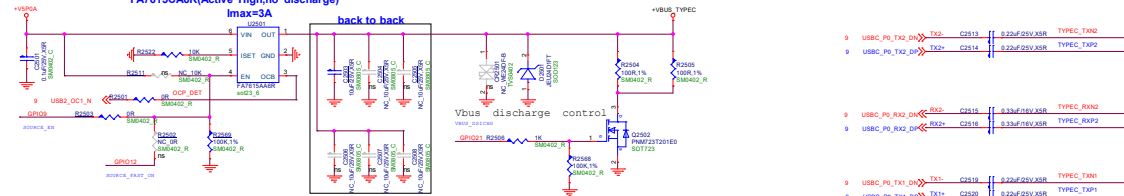


Madigi			
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Project Name : N156EBL01			
Document Number	Page Name : TPAD/FP/FAN		Size B
Design Date : Monday, April 17, 2023		Author : Java	
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FA7615CA6R(Active High,no discharge)

$I_{max}=3A$



Madrigal

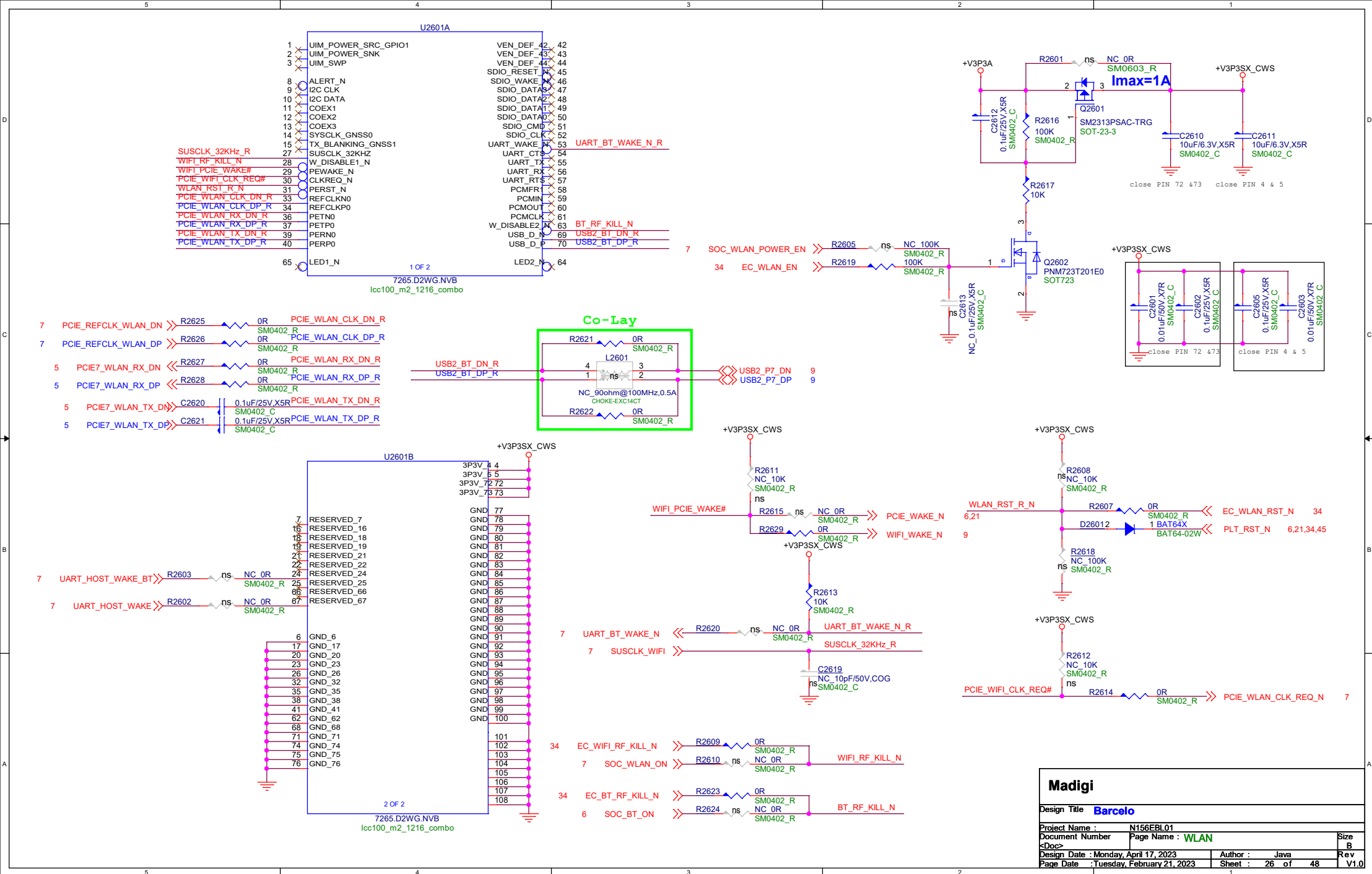
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Project Name: **N15466561**

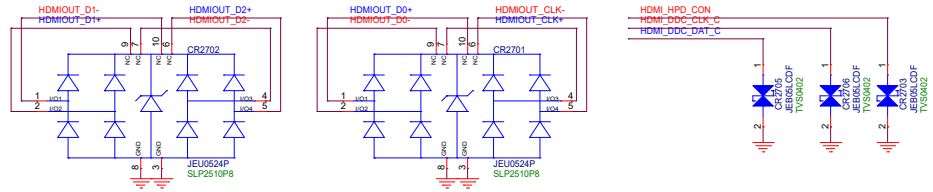
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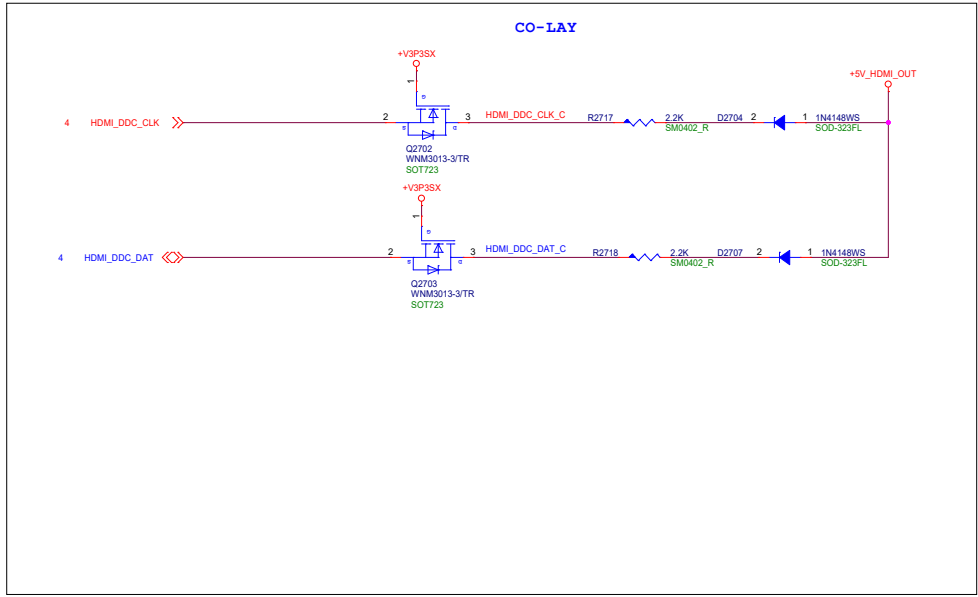
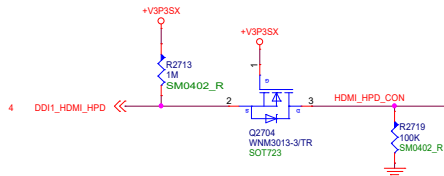
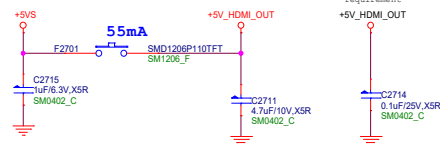
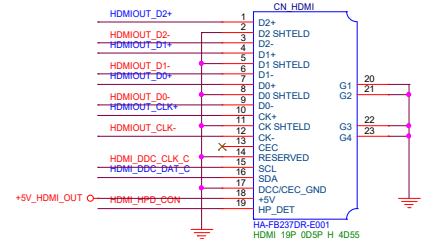
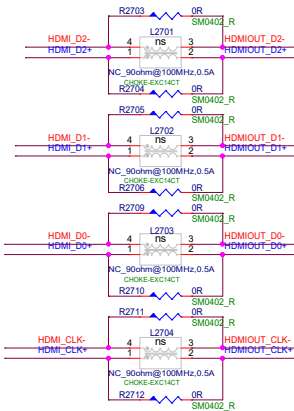
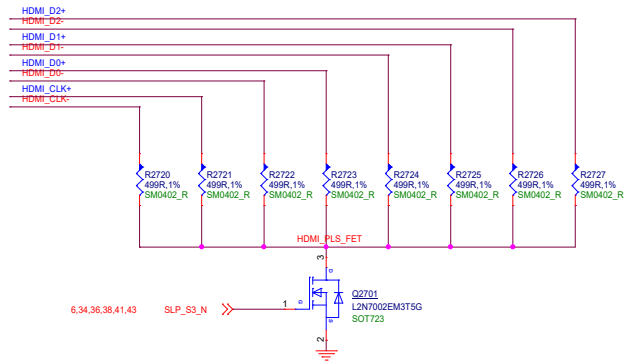
Design Date: Monday, April 17, 2023	Author: Anna
Draw Date: Sunday, February 26, 2023	Sheet: 25 of 48



HDMI



4	DDI1_LANE3_HDMI_DP	>>	C2708	0.1uF/25V X5R	HDMI_CLK+
4	DDI1_LANE3_HDMI_DN	>>	C2707	0.1uF/25V X5R	HDMI_CLK-
4	DDI1_LANE2_HDMI_DP	>>	C2706	0.1uF/25V X5R	HDMI_D0+
4	DDI1_LANE2_HDMI_DN	>>	C2705	0.1uF/25V X5R	HDMI_D0-
4	DDI1_LANE1_HDMI_DP	>>	C2704	0.1uF/25V X5R	HDMI_D1+
4	DDI1_LANE1_HDMI_DN	>>	C2703	0.1uF/25V X5R	HDMI_D1-
4	DDI1_LANE0_HDMI_DP	>>	C2702	0.1uF/25V X5R	HDMI_D2+
4	DDI1_LANE0_HDMI_DN	>>	C2701	0.1uF/25V X5R	HDMI_D2-



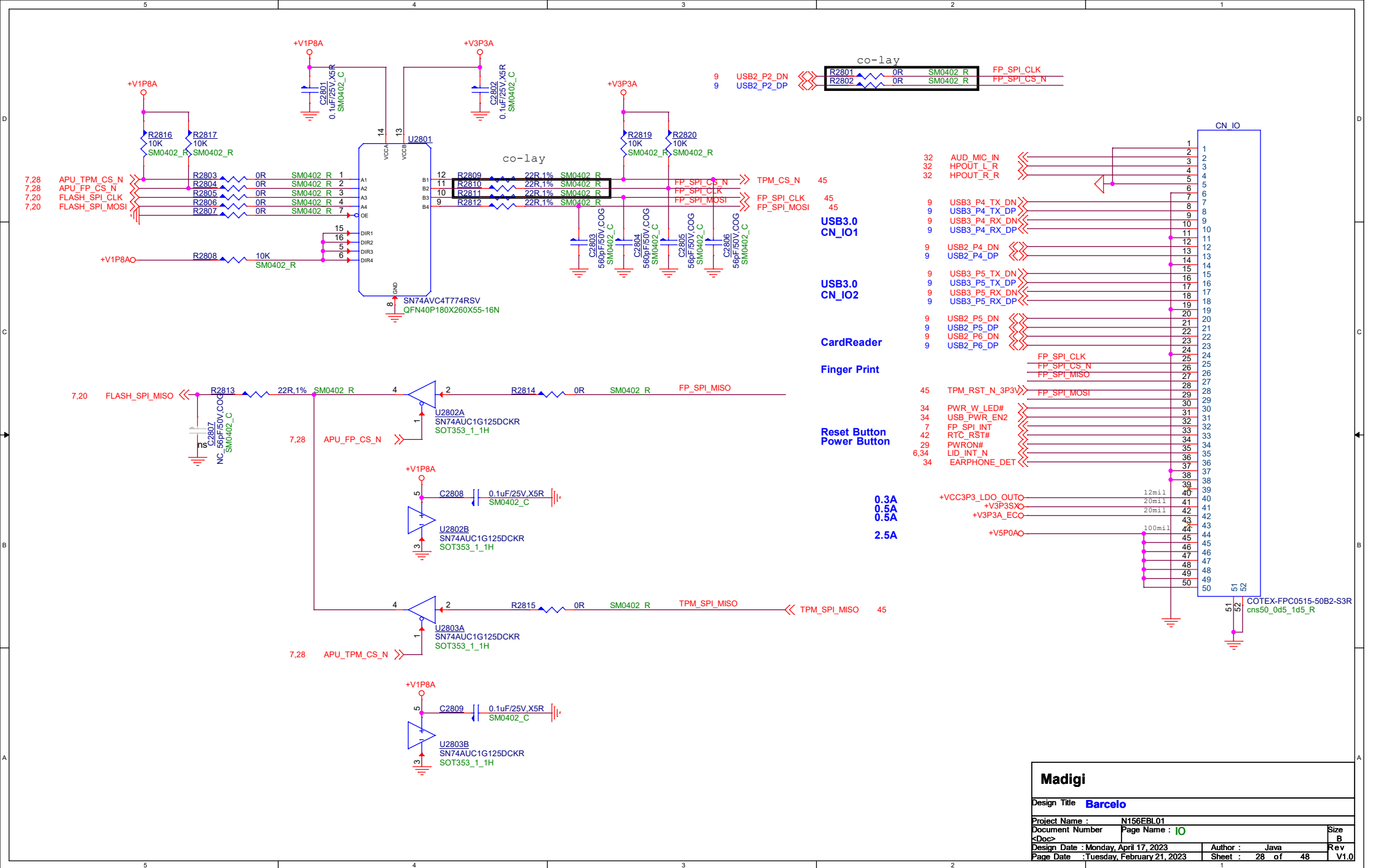


Figure 10 illustrates the pin connections for the Cortex-M0+ microcontroller. The diagram shows the pinout of the microcontroller, including power pins (VDD, GND), I/O pins (KEY_IN, KEY_OUT), and peripheral pins (KEY_IN0, KEY_OUT0, etc.). It also shows the connection of the microcontroller to the external circuit, including the power supply, ground, and the key matrix. The pin numbers are listed on the left, and the pin names are listed on the right. The connections are shown as lines between the pins and the external components.

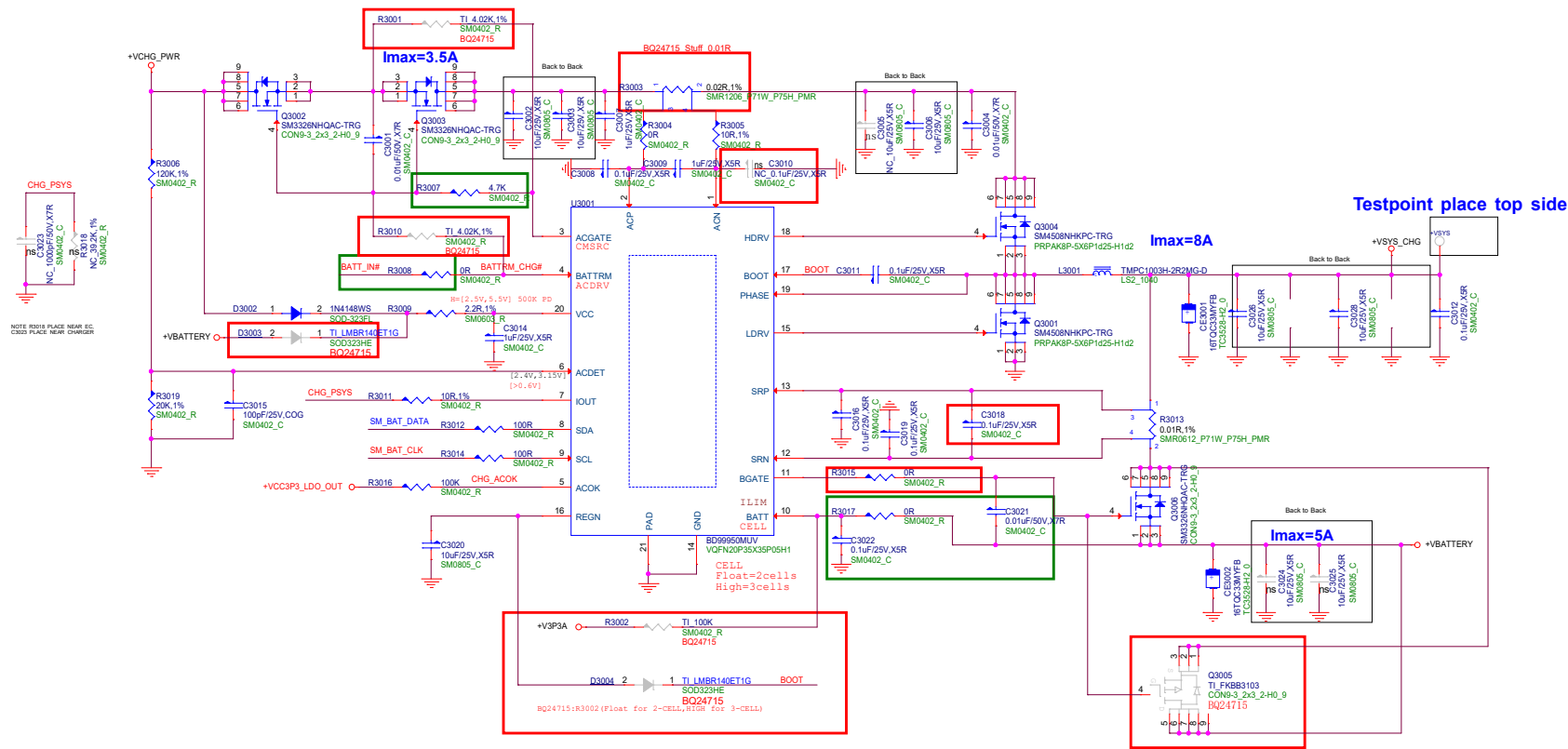
[illegible]

34 DCHG_W_LED# >>> 34

34 CAPS_W_LED# >>> CAPSLED-

Design Title				Barcelo			
Protect Name :				N156EBL01			
Document Number		Page Name :		KB/LED/PWR SW		Size	
<Doc>						C	
Design Date : Monday, April 17, 2023				Author :		Java	
Page Date : Thursday, March 30, 2023				Sheet :		29 of 48	
						Rev	
						V1.0	

BATTERY CHARGER



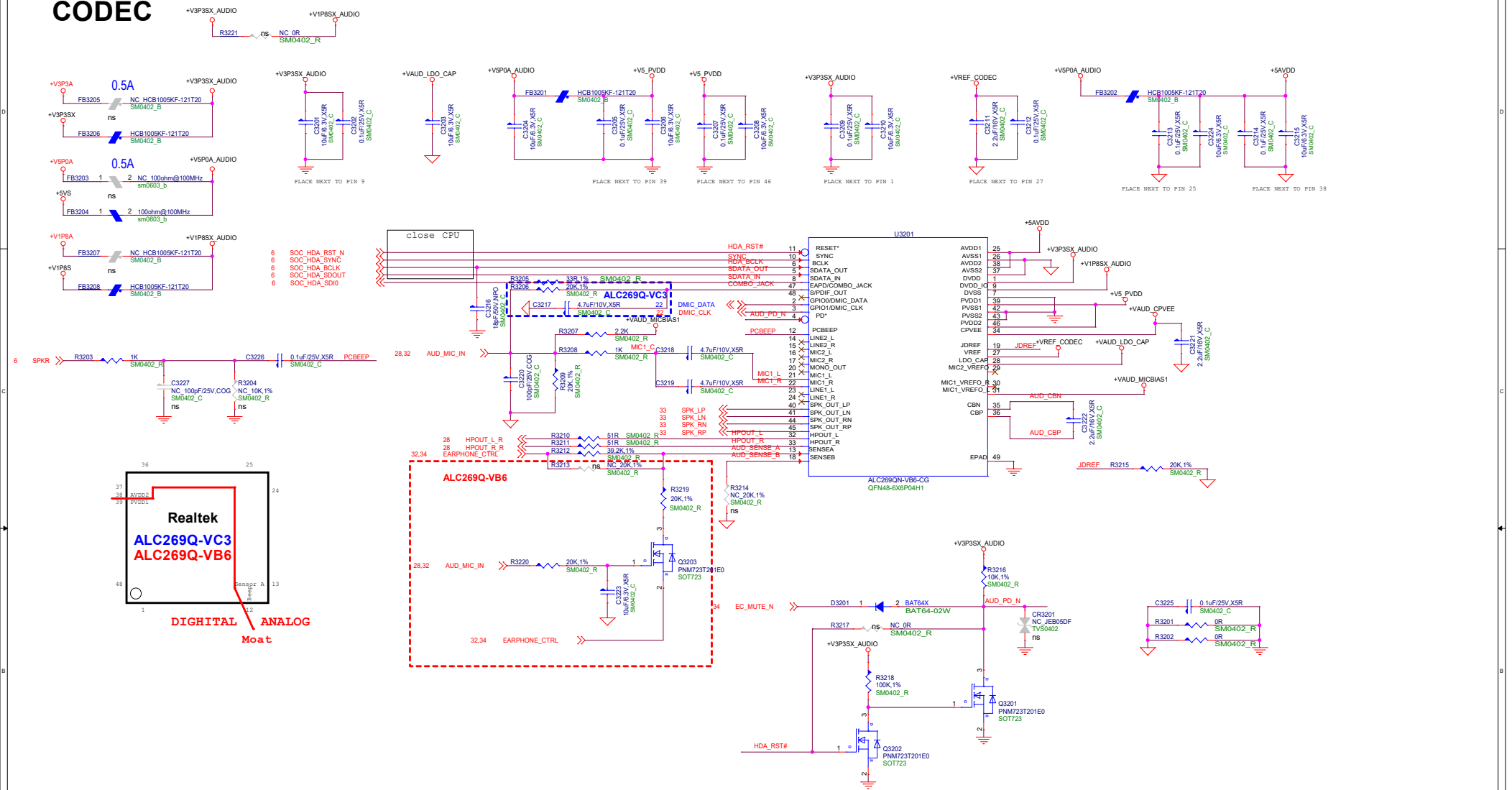
Register Address			BD99550
Register Address	Func	Value	Descrip
0x12	Charge Option	0xF302	DEFAULT
0x14	Charge Current	0x0640	1600mA
0x15	Charge Voltage	0x3300 0x2200	13056mV 8708mV
0x3E	Min Sys Voltage	0x2340 0x17C0	9024mV 6080mV
0x3F	Input Current	0x0800	2048mA

RED - 3Cell
BLUE - 2Cell

Chip Address		8D9950
Chip Address + R	0x13	
Chip Address + W	0x12	

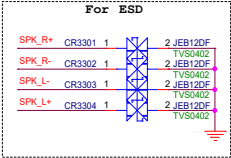
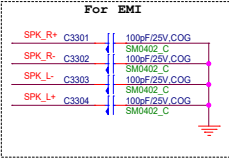
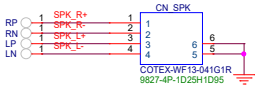
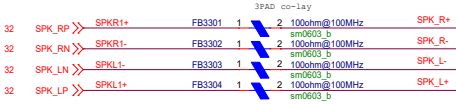
Net Interface			
34	CHG_PSYS	<<	CHG_PSYS
31,34	SM_BAT_DATA	<<>	SM_BAT_DATA
31,34	SM_BAT_CLK	>>	SM_BAT_CLK
29,31,34	CHG_ACOK	<<	CHG_ACOK
31,34	BATT_IN#	>>	BATT_IN#

CODEC



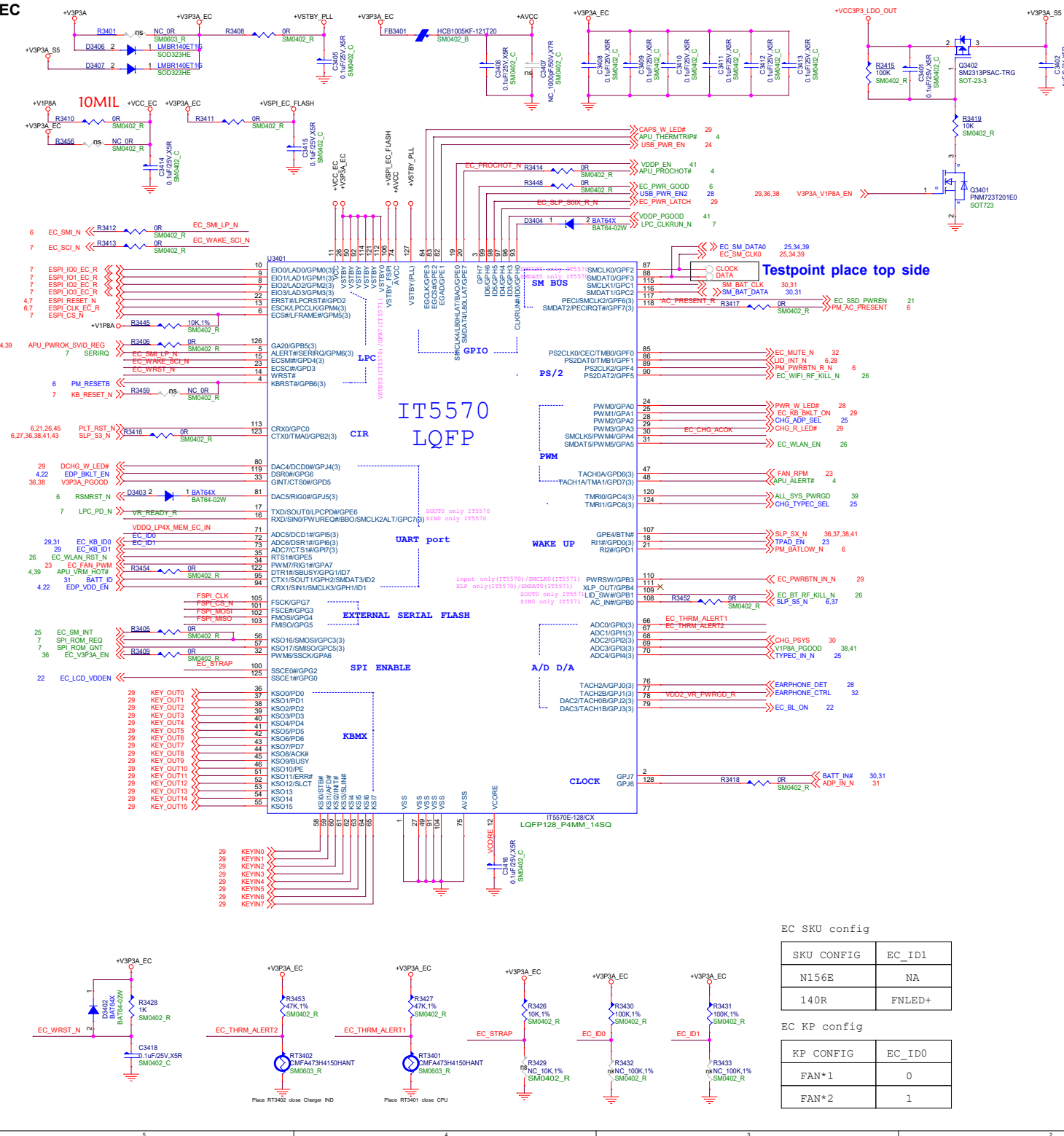
INT_SPEAKER

SPEAK: 2 W 4 Ω

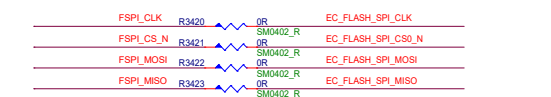


Madigi

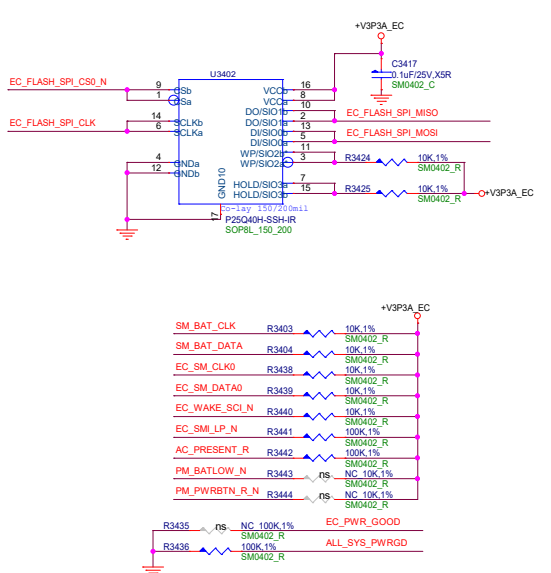
Design Title : Barcelo			
Project Name : N156EBL01			
Document Number : Doc	Page Name : SPEAK		Size : C
Design Date : Monday, April 17, 2023	Author : Java	Rev	
Page Date : Tuesday, February 21, 2023	Sheet : 33 of 48	Rev V1.0	



EEPROM



EC Flash 150&200 co-lay



Testpoint place top side

EC SKU config

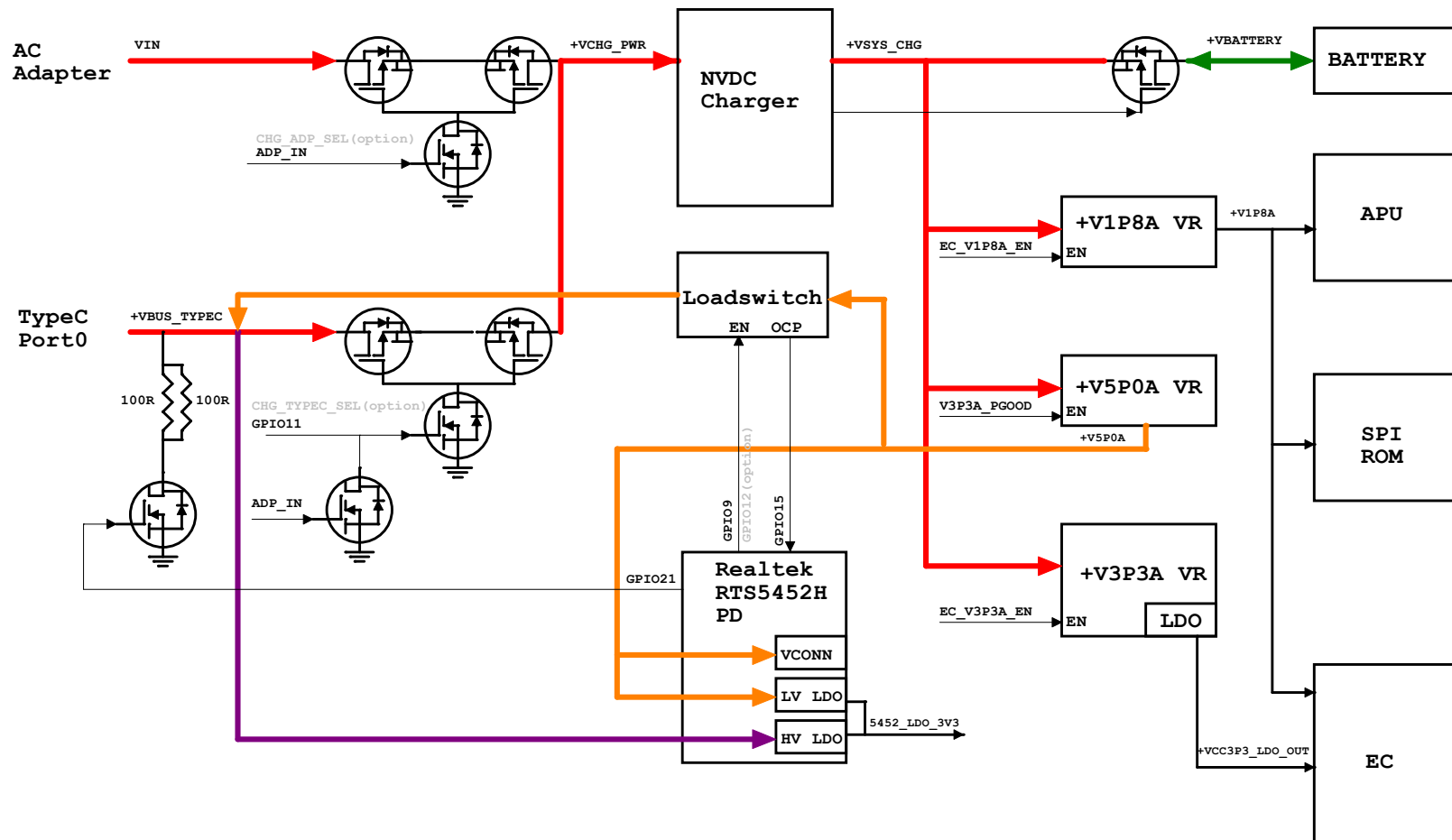
SKU CONFIG	EC_ID1
N156E	NA
140R	FNLED+

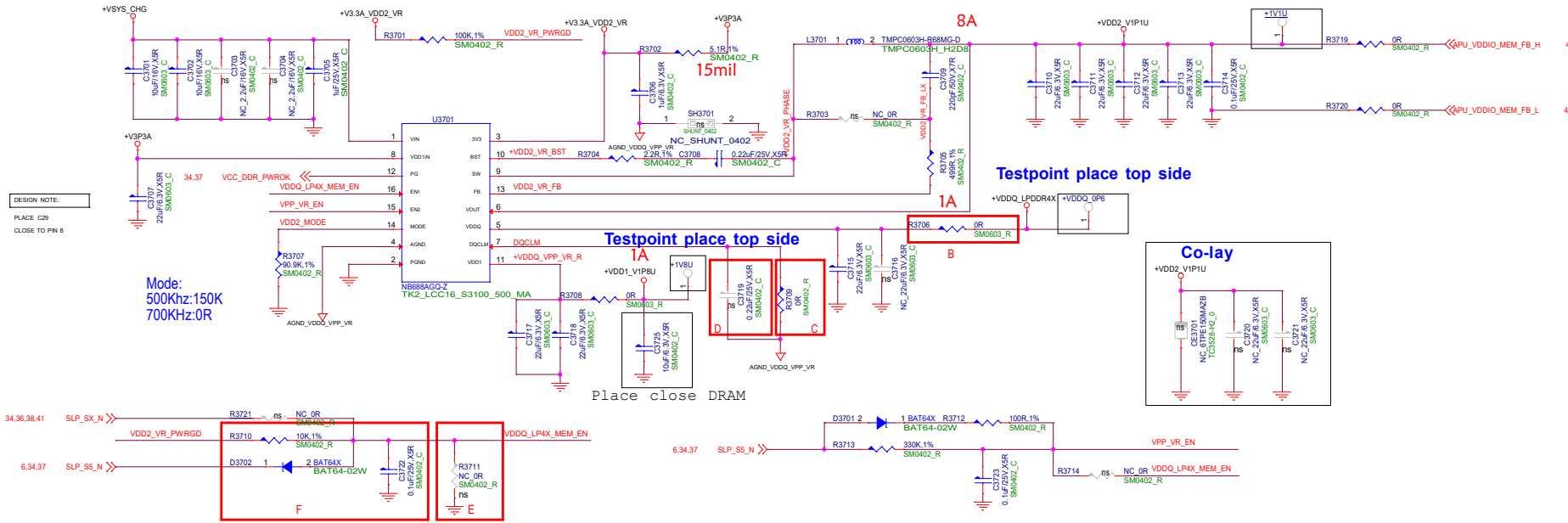
EC KP config

KP CONFIG	EC_ID0
FAN*1	0
FAN*2	1

Madigi

Design Title	Barcelona
Project Name	N156EBL01
Document Number	Page Name : EMBEDDED CONTROLLER
Doc	Size
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Author	Java
Page Date	Tuesday, February 28, 2023
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Rev	V1.0





DESIGN NOTE:
PLACE C29
CLOSE TO PIN 8

Mode:
500KHz:150K
700KHz:0R

Testpoint place top side

Testpoint place top side

Co-lay

Place close DRAM

Note:
LPDDR4:Stuff R3715,Unstuff R3706
LPDDR4X:Stuff R3706,Unstuff R3715

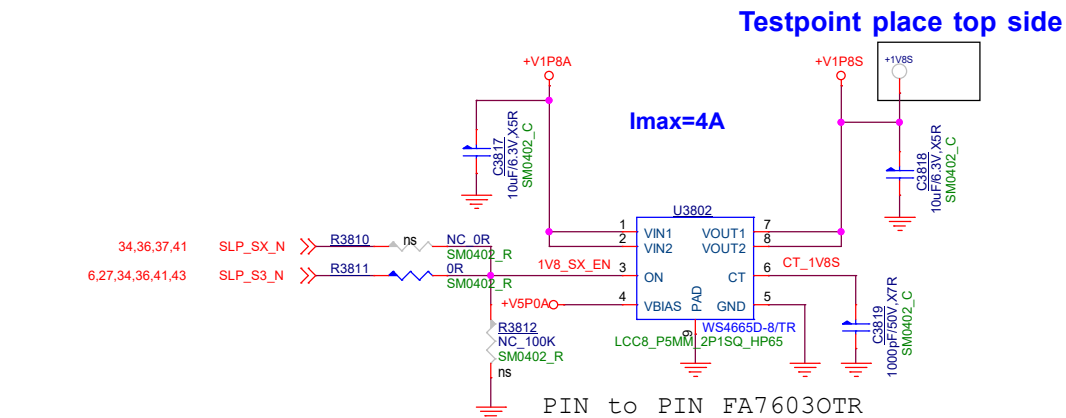
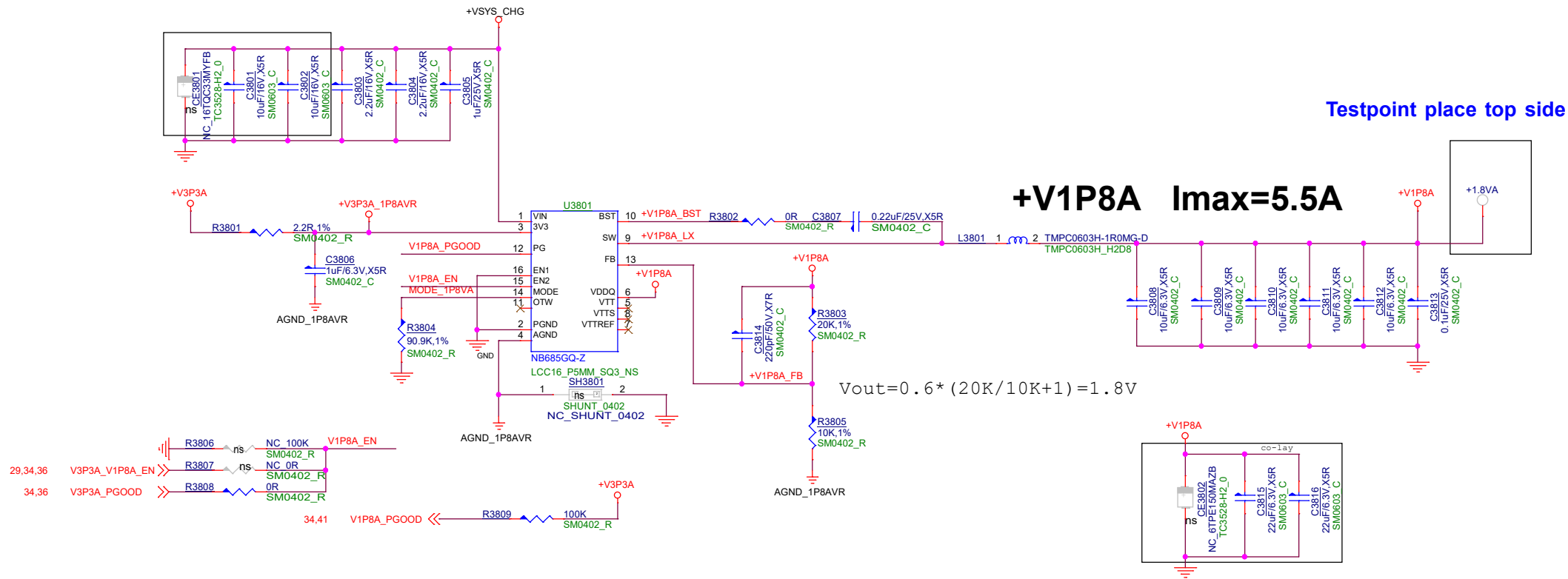
DESIGN NOTE:

LPDDR4X	LPDDR4
A TO BE EMPTY	A TO BE STUFF R2416
B TO BE STUFF	B TO BE EMPTY
C TO BE STUFF	C TO BE EMPTY
D TO BE EMPTY	D TO BE STUFF
E TO BE EMPTY	E TO BE STUFF
U4001:NB688A	U4001:NB688
F TO BE STUFF	F TO BE EMPTY

DESIGN NOTE:

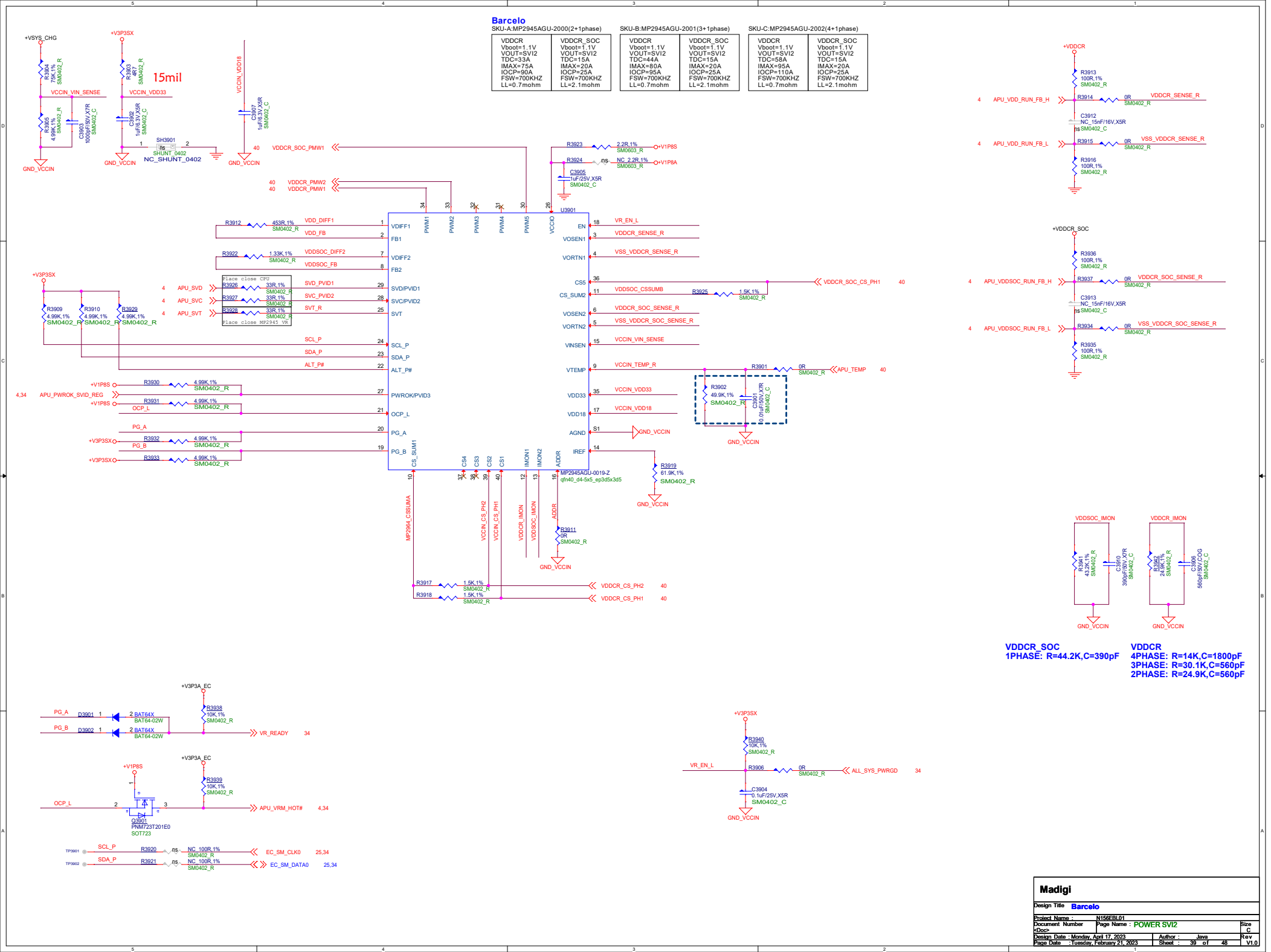
PARAMETER	SETTING
OUTPUT VOLTAGE	1.1V
LOAD CURRENT	9A
OCV	11.25A
FREQUENCY	700 KHZ
SOFT START	2.8 MILLI SEC

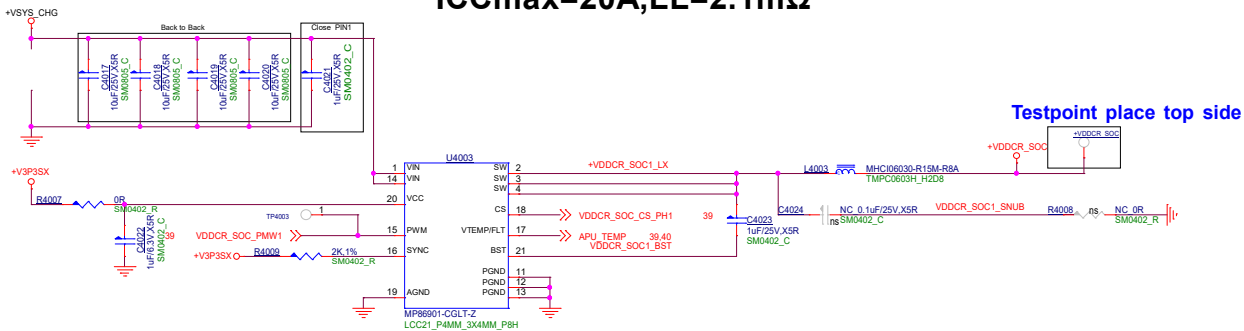
$$V_{out} = 0.6 * (16.9K / 20K + 1) = 1.107V$$

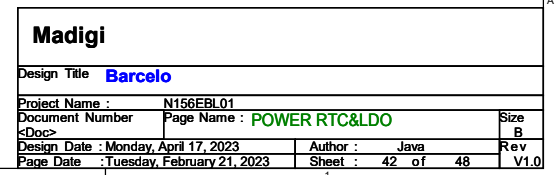


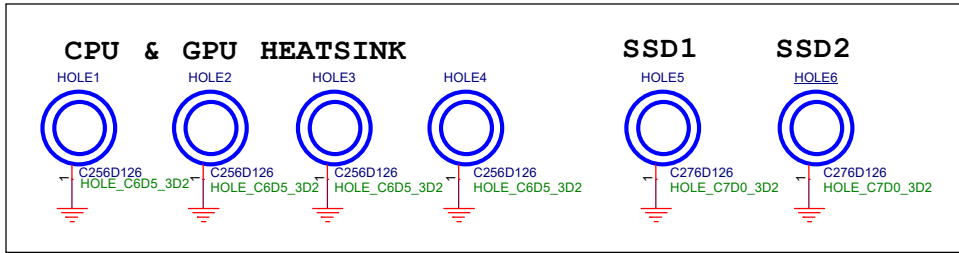
Madigi			
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Project Name : N156EBL01			
Document Number	Page Name : POWER 1.8VA/S	Size B	
Design Date : Monday, April 17, 2023	Author : Java	Rev	
Page Date : Tuesday, February 21, 2023	Sheet : 38 of 48	V1.0	

PIN to PIN GS7631ATD-R

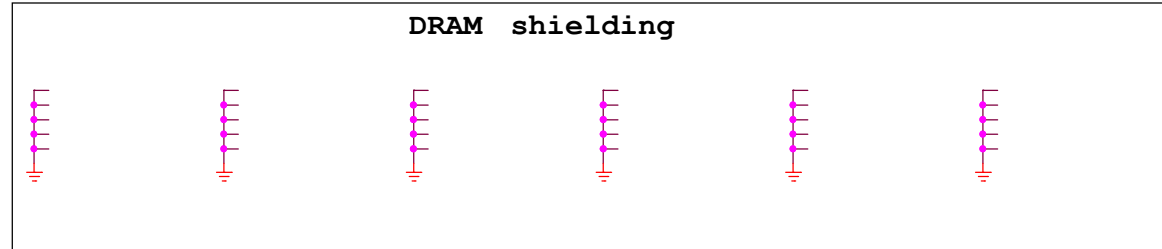
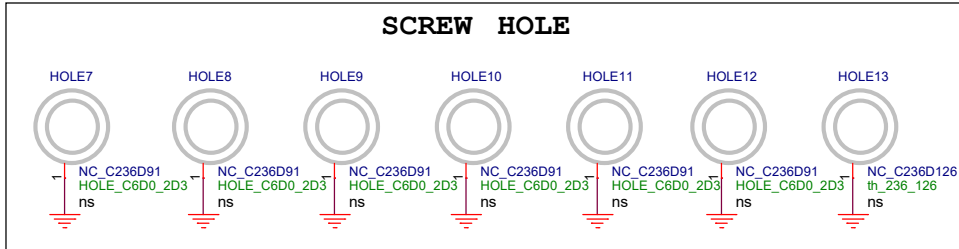
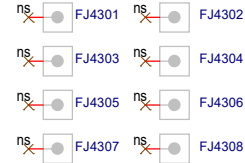








Mark Point EMI CAP



PCB
N156EBC01_MB_V11

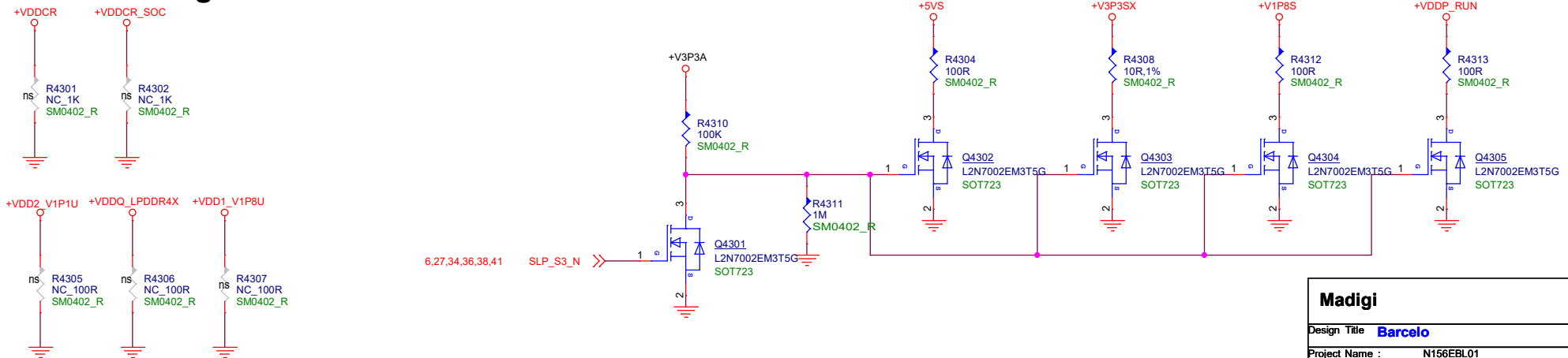


S/N :
SN
NC_Seril Number
ns



RTC_BATT
NC_CR2030 3.3V
ns

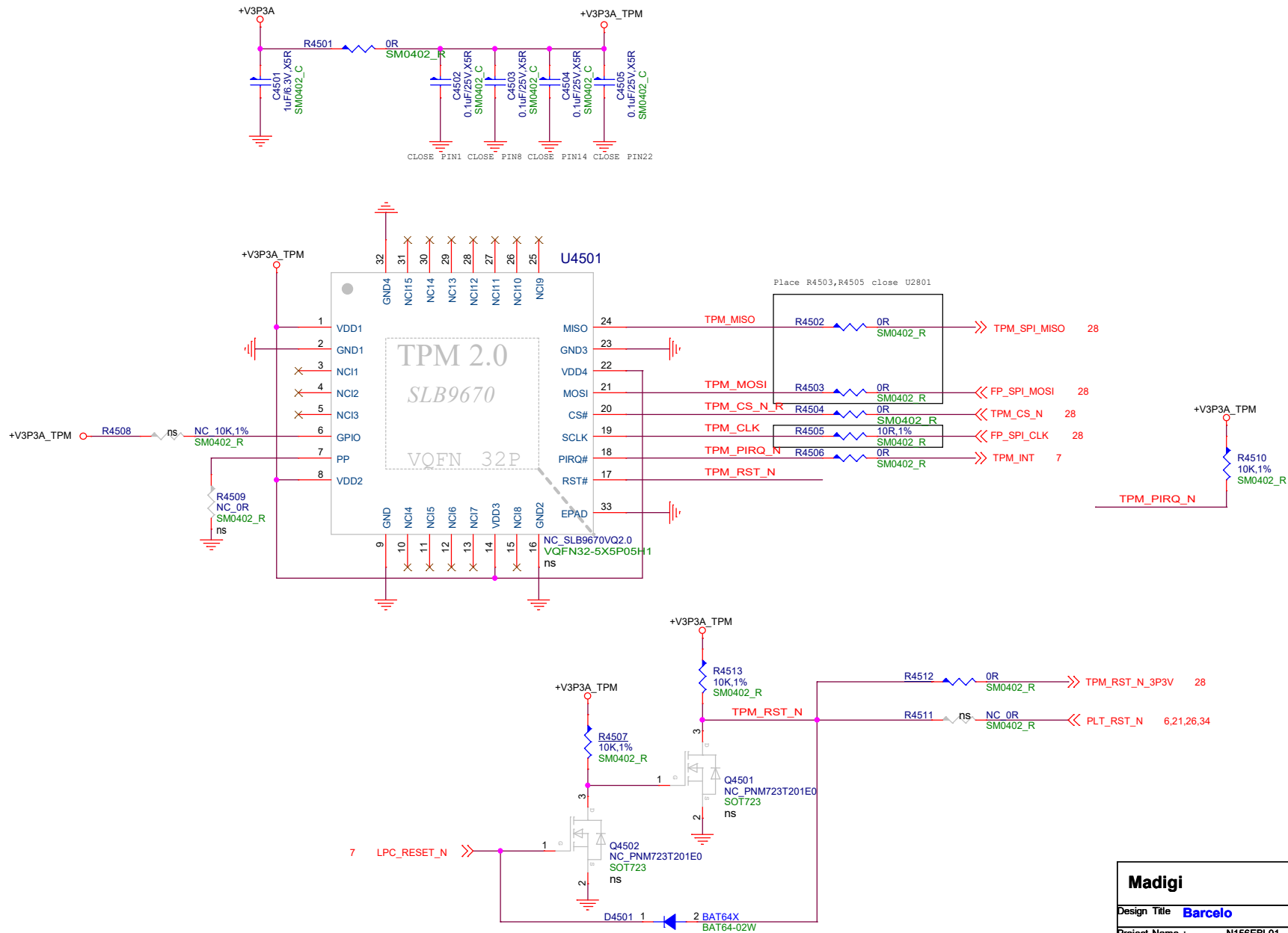
Discharge Resistor



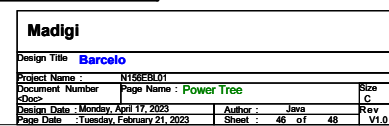
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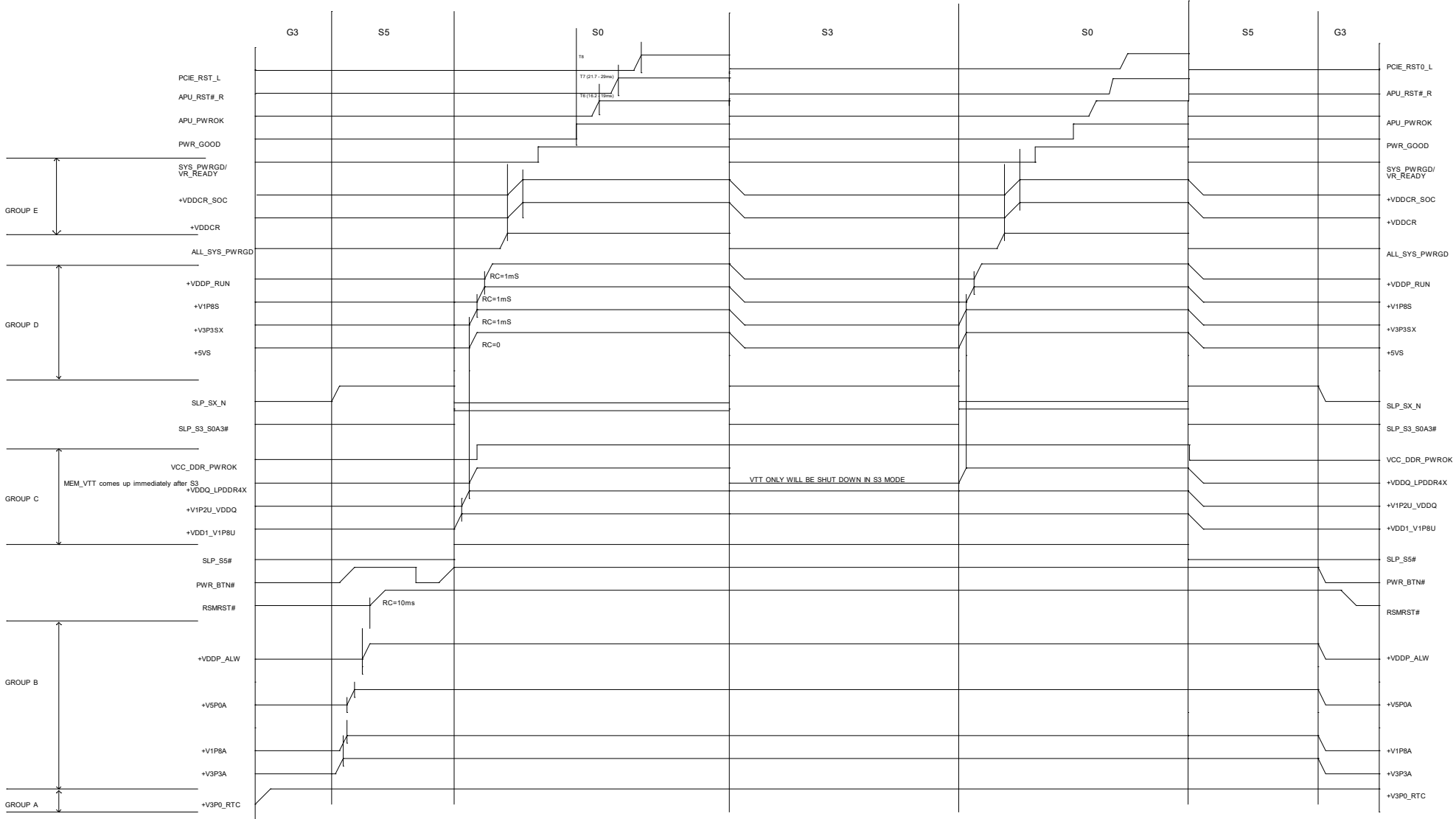
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Project Name : N156EBL01	Page Name : Discharge/HOLE	Rev V1.0
Document Number	Sheet : 43 of 48	
Design Date : Monday, April 17, 2023	Author : Java	
Page Date : Tuesday, February 28, 2023		

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Document Number	Page Name : BLANK		Size
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Design Date : Monday, April 17, 2023	Author : jms	Rev	
Page Date : Tuesday, February 21, 2023	Sheet : 44 of 48	V1.0	



Madigi			
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Page Date :	Tuesday, February 21, 2023	Sheet : 45 of 48	Rev V1.0

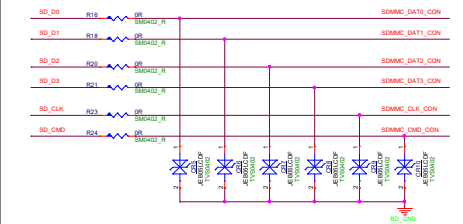
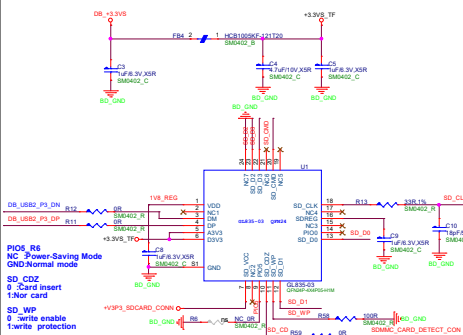




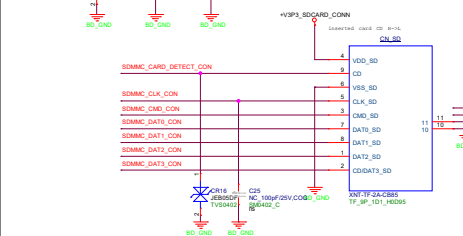
Power on Sequence required:

1. There is no sequencing requirement between power supplies within the individual power groups.
2. All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequencing Group B is greater than 10% of its specified minimum operating voltage.
3. All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 10% of its specified minimum operating voltage.
4. All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 10% of its specified minimum operating voltage.

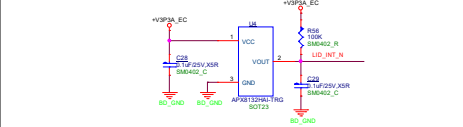
SD CardReader



Micro SD Socket



LID Sensor



FAN2



IO CONNECTOR

Headset

CN_USB1

CN_USB2

TF Card

FingerPrint

Reset Button

Power Button

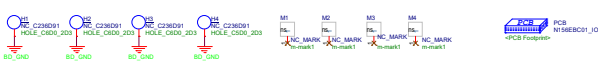
LED

Reset Button

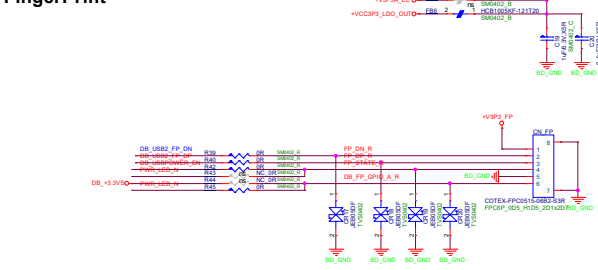
Power Button

LED

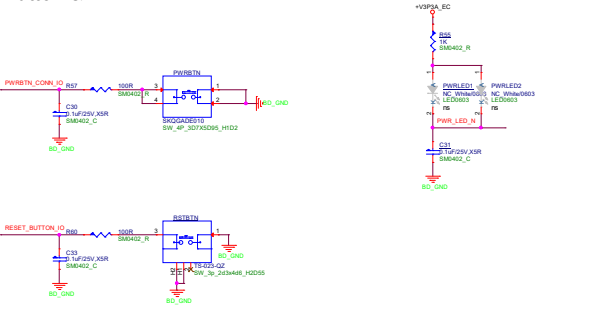
Screw Hole



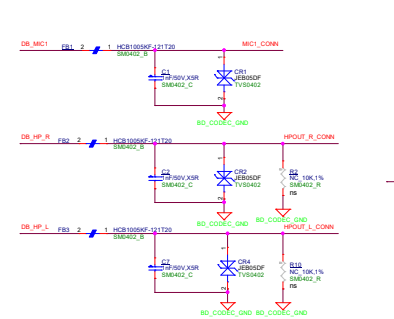
FingerPrint



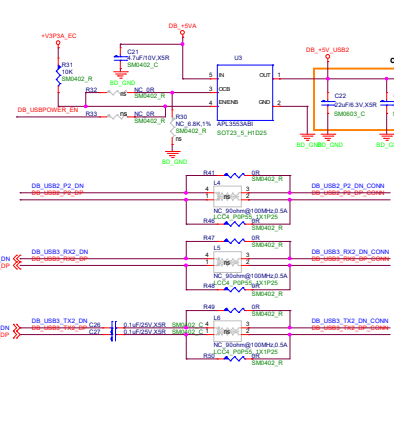
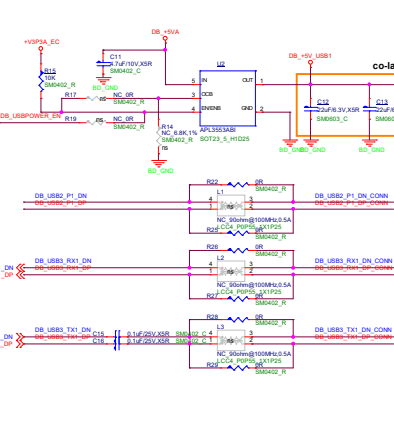
Button & LED



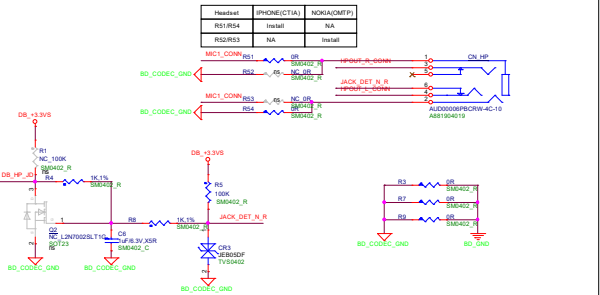
Headset



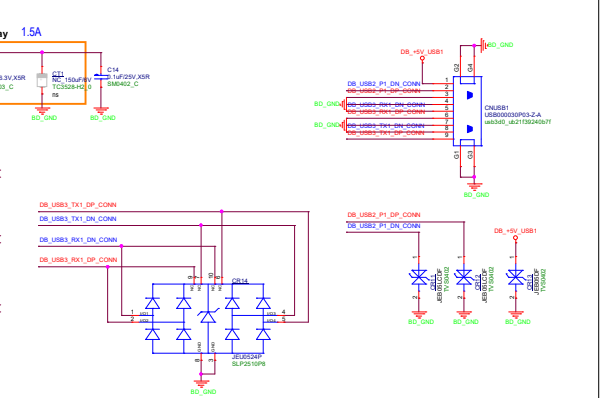
USB3 TypeA



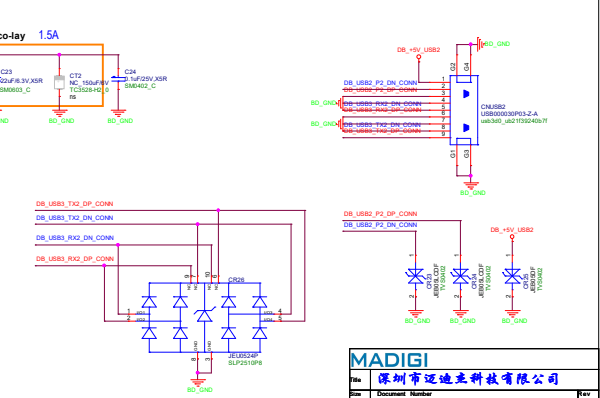
Audio Jack

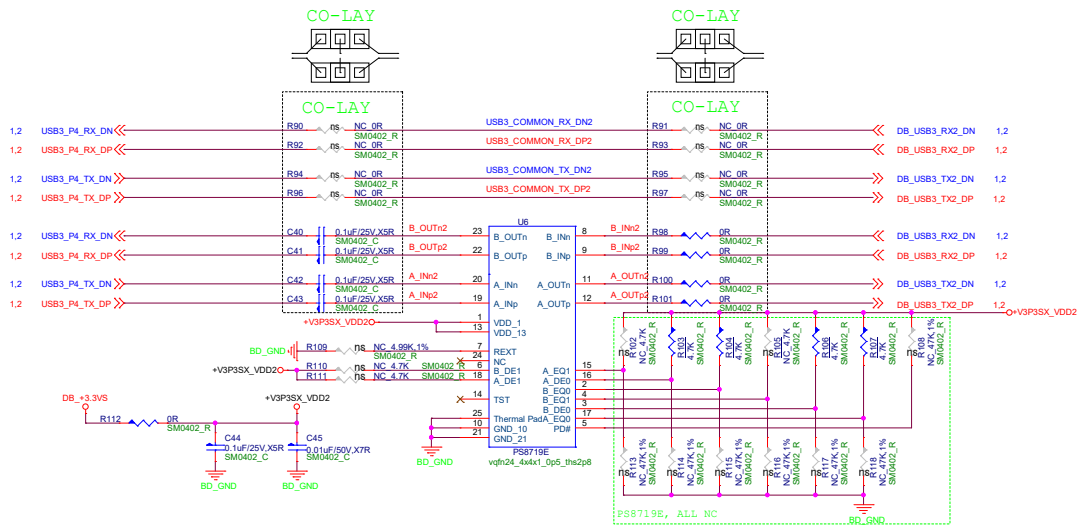
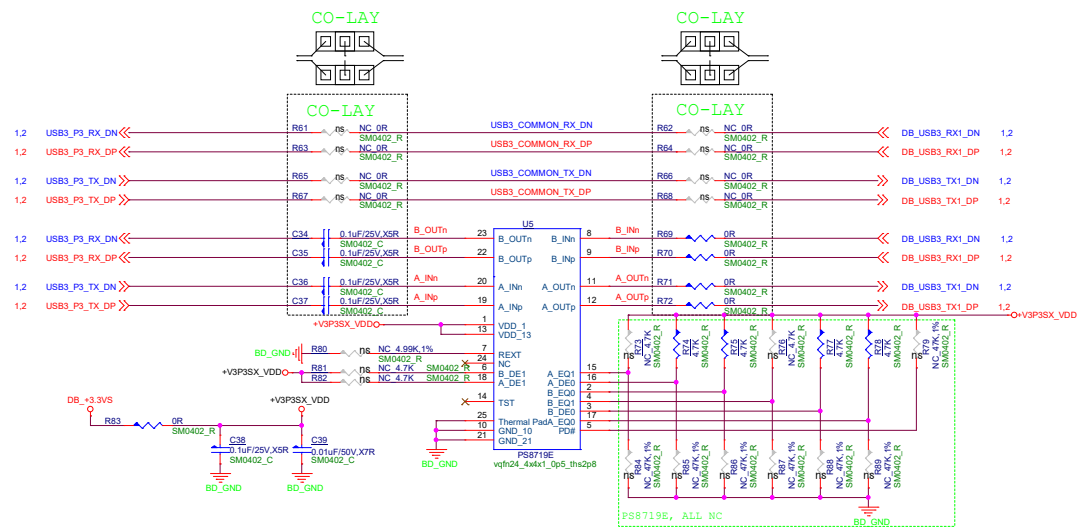


USB3 Jack



USB3 Jack





RX Receiver

Equalizer control and program for Channel A
3.3V tolerant.Integrated pulldown 150K resistors.
[A_EQ1,A_EQ0]==[PIN15,PIN17]
LL = program EQ for channel loss up to 9.5dB(default)
LH = program EQ for channel loss up to 13dB
HL = program EQ for channel loss up to 4.5dB
HH = program EQ for channel loss up to 7.5dB

Equalizer control and program for Channel B
3.3V tolerant.Integrated pulldown 150K resistors.
[B_EQ1,B_EQ0]==[PIN4,PIN2]
LL = program EQ for channel loss up to 9.5dB(default)
LH = program EQ for channel loss up to 13dB
HL = program EQ for channel loss up to 4.5dB
HH = program EQ for channel loss up to 7.5dB

TX Driver

Programmable output de-emphasis level setting for Channel A
3.3V tolerant.Integrated pulldown 150K resistors.
[A_DE1,A_DE0]==[PIN18,PIN16]
LL = 3.5dB de-emphasis(default)
LH = 0dB de-emphasis
HL = 2.7dB de-emphasis
HH = 5dB de-emphasis

Programmable output de-emphasis level setting for Channel B
3.3V tolerant.Integrated pulldown 150K resistors.
[B_DE1,B_DE0]==[PIN6,PIN3]
LL = 3.5dB de-emphasis(default)
LH = 0dB de-emphasis
HL = 2.7dB de-emphasis
HH = 5dB de-emphasis