THEORY OF OPERATION

This PLL-controlled VHF marine DSC base station radio provides an accurate and stable multi-channel operation.

- Transmitter
- Receiver
- Local oscillator PLL(phase lock loop) circuit
- Memory backup
- DSC feature
- ATIS function
- Large LCD
- GPS message

- Transmitter

The audio is picked up from the internal MIC. The audio signal is then amplified by audio amplifier, two of the quad operational amplifiers, U4 NJM3403, and filtered by low pass filter, two of the quad operational amplifiers, U5 NJM2904 .The audio level is adjusted by VR2 to obtain a suitable RF frequency deviation that then modulates the carrier of VCO, through varicap(VD1)

The modulated signal output from the VCO is pre-amplified by Q303, Q304 and IC1. When the supply voltage is 12V, this signal will be amplified up to 1W or 25W. This signal is filtered by low-pass filter circuit that consists of L1, L3, L4, L5, C1, C2, C4, C5, C6, C7, C8 and C9,C10,C11. These low pass filters are necessary to suppress the second and the third harmonics. The filtered signal is then fed into the antenna input and radiated out. It is also fed into another path consisting of C330, C331, D301, D302 for sampling, and is converted into a direct current voltage for the automatic power control (APC) circuit Q307,Q306,Q305 whose collector current is used to maintain the output power stability.

When the unit is transmitting, the channel control voltage is added to the TX VCO varicap VD2. The capacitance of VD1 is varied following the audio signal, thus the carrier is modulated to form the modulated signal.

- Receiver

The receiver uses a double frequency super-heterodyne circuit. The first immediate frequency (IF) is 21.4MHz and the second is 455KHz.

The RF signal is received by the antenna, and passes through a low-pass filter network L1, L3, L4, C1, C2, C4, C5, C7, C8, C10, C11 to filter out the unwanted signals. The received RF signal then passes through a high RF transformer T1 and is

amplified ty RF amplifier Q1, T2, T3, T4, C19, C20, C23 form the band pass filter. The RF signal then is mixed with the local oscillation frequency by the diode loop mixer that consists of D2, D3, T5 and T6. The first IF(immediate frequency) of 21.4MHz is produced. This IF passes through a pair of crystal filter F1,F2 to further filter out the other unwanted signals. The first IF then is amplified by Q2 and the IF amplifier U1(S1T3361). U1 is an integrated FM IF demodulation circuit which consists of a local oscillator, a demodulator, a second mixer, squelch control circuit, and RF amplifier. the 21.4MHz IF then is mixed here with signal of the second local oscillator and converted into 2^{nd} immediate frequency (IF) 455KHz. The 2^{nd} IF passes through a ceramic filter F3 to filter out the residue unwanted signal, at pin 5 of IC4 (S1T3361)this final IF signal is output and the audio signal is output at pin 9 of IC4(S1T3361).
The audio signal is amplified by U7B and passes through a volume control VR1, the amplified audio is then fed into de-emphasis circuit Q4 and finally amplified by audio amplifier U6(TDA2003) and heard from the speaker.

The squelch control is also controlled by U1(S1T3361). The audio signal passes through the low pass filter R16, C46 and U1(S1T3361) internal squelch control R11, R12, C33, C34 and R13 that form as a squelch amplifier to produce a squelch signal (RF noise). This signal is amplified ty Q5 and regulated by D7 to produce a direct current voltage as a control voltage. The control voltage then is input to pin12 of U1(S1T3361). Pin13 of IC4 sends the digital squelch control signal to the MCU to mute the audio speaker path and to indicate the RX status through LCD. R40 and VR2 form a variable resistor, which correspond to the squelch level.

◆ Local oscillator PLL (phase lock loop) circuit

The receiver and transmitter both share the same PLL (phase lock loop) circuitry to produce the carrier or the receiving frequency. The local oscillator consists of a phase lock loop(PLL) U3(LMX1511) Q401, Q402, Q502, Q503, and Q501. When Q501 is switched to saturation, the VCO will produce receiver local oscillator frequency. The fundamental frequency is determined by Y2(12.8MHz) and as the PLL reference oscillator. This signal is frequency-divided by U3 and a 12.5KHz signal is produced. When the VCO frequency applied to U3 pin10 and frequency-divided by U3 produces a frequency comparable to 12.5KHz, PLL will control the VCO. When these two frequencies are matched, a constant control voltage is output from PLL to lock VCO in desired frequency. Otherwise the PLL will also output an unlock indication to MCU to indicate that the PLL is in the frequency unlock state.

◆ Memory backup

U2 is an EEPROM S524A60X51 , which acts as a memory backup for the working channel code and the system parameters. Every time when the unit is switched on, the MCU will reset the system, clear the RAM, and recall the memory from the EEPROM to refresh the RAM in MCU U1.

◆ DSC feature

DSC is encoded by MCU U1, the passes through R18-R23 to produce D/A conversion and U4A low pass filter forms FSK signal. The FSK signal is amplified by U4C, U4B and filtered by U5A and U5B to modulate VCO frequency, thus the DSC signal is transmitted. The DSC signal is received and demodulated on the second receiver board. The demodulated signal is sent into main receiver U2 pin13, the signal from U2 pin 14 passes through U7D high-pass filter and U7C low-pass filter to get FSK signal and filter out residual unwanted signals. This FSK signal is decoded by U4. The DSC is restored and processed by MCU U1 with RX data from U4 pin7.

◆ Large LCD

All message through series bus from MCU to display driver U6 will be displayed through a 1”x1.5” LCD in 4x12 characters dot matrix.

◆ GPS message

External GPS message is input to MCU through phototransistor U10 TLP120. LCD will display the machine current location and time message in idle state.