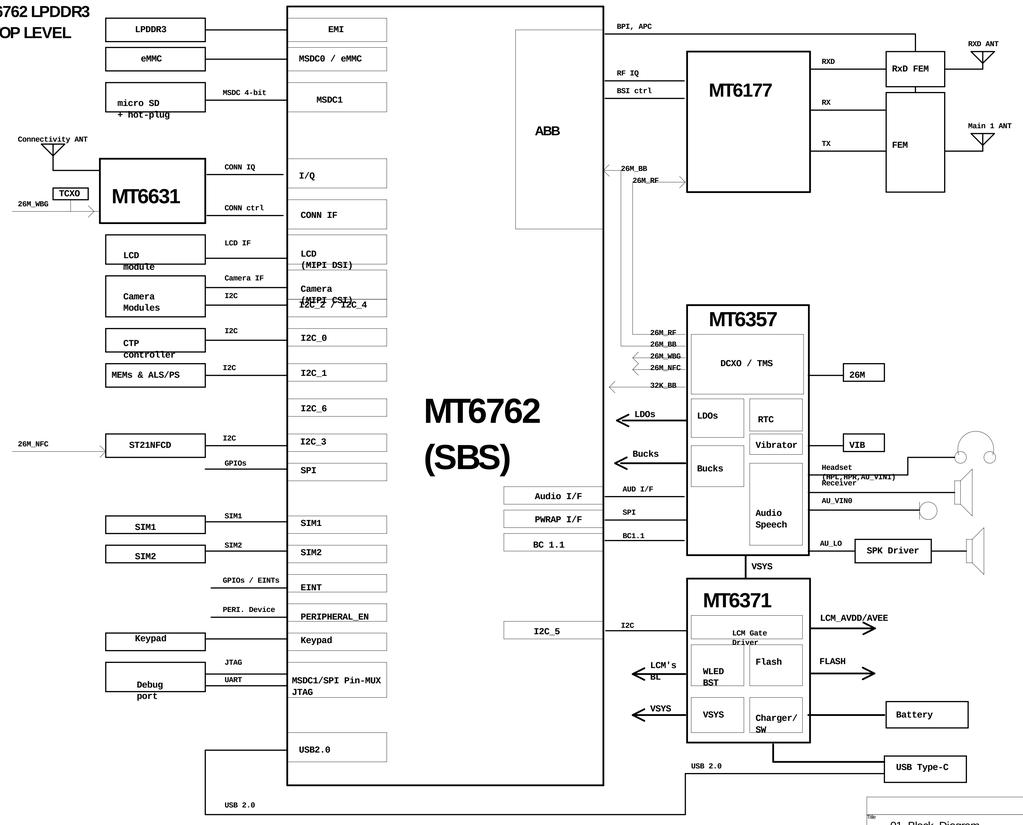
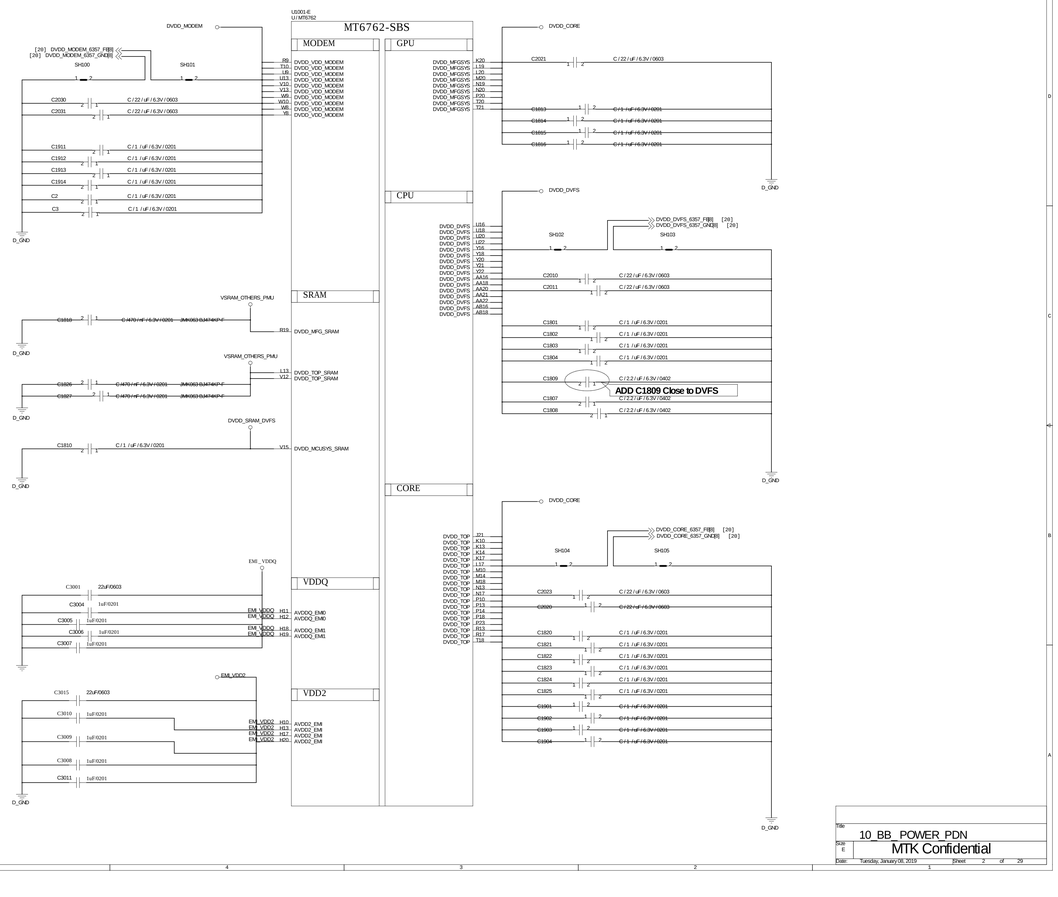
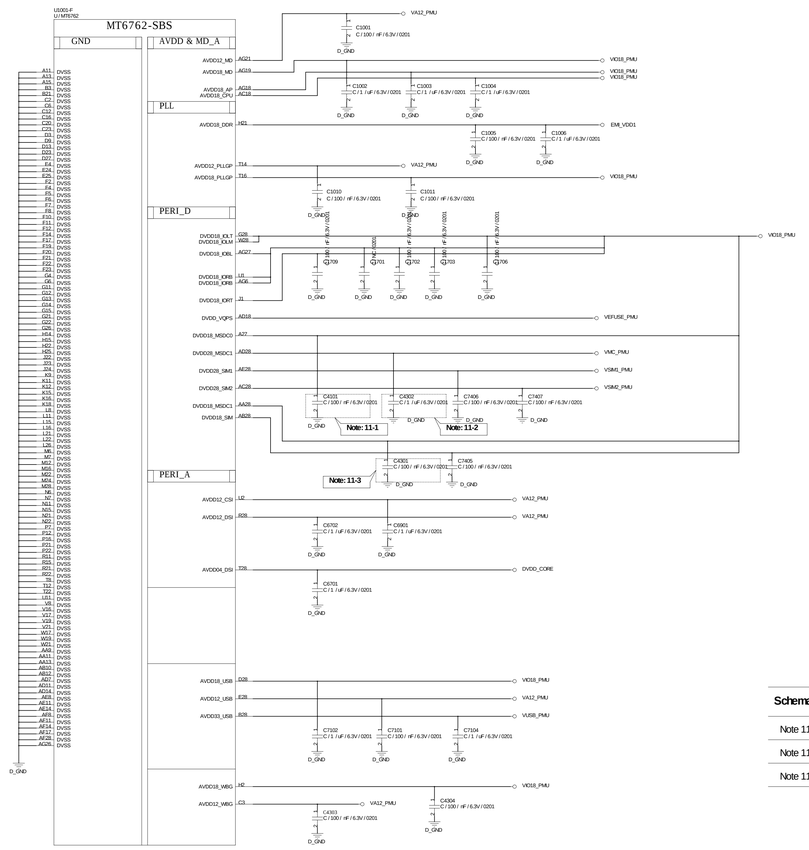
Project : MT6762 LPDDR3
REF_SCH TOP LEVEL



Title: 01_Block_Diagram
Size: E
MTK Confidential
Date: Tuesday, January 08, 2019
Sheet 1 of 29


U5001-E
U / MT6762
MT6762-SBS
MODEM
GPU
CPU
SRAM
VDDQ
VDD2
CORE
DVDD_MODEM
[29] DVDD_MODEM_6357_FB[6]
[29] DVDD_MODEM_6357_OA[6]
SH100
SH101
C2030 C / 22 / uF / 6.3V / 0603
C2031 C / 22 / uF / 6.3V / 0603
C1911 C / 1 / uF / 6.3V / 0201
C1912 C / 1 / uF / 6.3V / 0201
C1913 C / 1 / uF / 6.3V / 0201
C1914 C / 1 / uF / 6.3V / 0201
C2 C / 1 / uF / 6.3V / 0201
C3 C / 1 / uF / 6.3V / 0201
D_GND
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_VDD_MODEM
DVDD_CORE
DVDD_MFG1SYS
DVDD_MFG1SYS
DVDD_MFG1SYS
DVDD_MFG1SYS
DVDD_MFG1SYS
DVDD_MFG1SYS
DVDD_MFG1SYS
C2021 C / 22 / uF / 6.3V / 0603
C1813 C / 1 / uF / 6.3V / 0201
C1814 C / 1 / uF / 6.3V / 0201
C1815 C / 1 / uF / 6.3V / 0201
C1816 C / 1 / uF / 6.3V / 0201
D_GND
DVDD_DVFS
DVDD_DVFS_6357_FB[6] [29]
DVDD_DVFS_6357_OA[6] [29]
SH102
SH103
DVDD_DVFS
C2010 C / 22 / uF / 6.3V / 0603
C2011 C / 22 / uF / 6.3V / 0603
C1901 C / 1 / uF / 6.3V / 0201
C1902 C / 1 / uF / 6.3V / 0201
C1903 C / 1 / uF / 6.3V / 0201
C1904 C / 1 / uF / 6.3V / 0201
C1909 C / 2.2 / uF / 6.3V / 0402
ADD C1809 Close to DVFS
C1907 C / 2.2 / uF / 6.3V / 0402
C1908 C / 2.2 / uF / 6.3V / 0402
D_GND
VSRAM_OTHERS_PMU
C1810 C / 1 / uF / 6.3V / 0201
DVDD_MFG_SRAM
DVDD_TOP_SRAM
DVDD_TOP_SRAM
DVDD_SRAM_DVFS
DVDD_MCUSYS_SRAM
C1826 C / 470 / nF / 6.3V / 0201 JMK063 BJ474KH-F
C1827 C / 470 / nF / 6.3V / 0201 JMK063 BJ474KH-F
D_GND
DVDD_CORE
DVDD_TOP
DVDD_CORE_6357_FB[6] [29]
DVDD_CORE_6357_OA[6] [29]
SH104
SH105
C2023 C / 22 / uF / 6.3V / 0603
C2020 C / 22 / uF / 6.3V / 0603
C1820 C / 1 / uF / 6.3V / 0201
C1821 C / 1 / uF / 6.3V / 0201
C1822 C / 1 / uF / 6.3V / 0201
C1823 C / 1 / uF / 6.3V / 0201
C1824 C / 1 / uF / 6.3V / 0201
C1825 C / 1 / uF / 6.3V / 0201
C1901 C / 1 / uF / 6.3V / 0201
C1902 C / 1 / uF / 6.3V / 0201
C1903 C / 1 / uF / 6.3V / 0201
C1904 C / 1 / uF / 6.3V / 0201
D_GND
EMI_VDDQ
C3001 22uF/0603
C3004 1uF/0201
C3005 1uF/0201
C3006 1uF/0201
C3007 1uF/0201
EMI_VDDQ_H11
EMI_VDDQ_H12
EMI_VDDQ_H08
EMI_VDDQ_H09
AVDDQ_EMI
AVDDQ_EMI
AVDDQ_EMI
AVDDQ_EMI
EMI_VDD2
C3015 22uF/0603
C3010 1uF/0201
C3009 1uF/0201
C3008 1uF/0201
C3011 1uF/0201
EMI_VDD2_H10
EMI_VDD2_H11
EMI_VDD2_H07
EMI_VDD2_H05
AVDD2_EMI
AVDD2_EMI
AVDD2_EMI
AVDD2_EMI
D_GND
Title
10_BB_POWER_PDN
Size
E
MTK Confidential
Date: Tuesday, January 08, 2019
Sheet 2 of 29



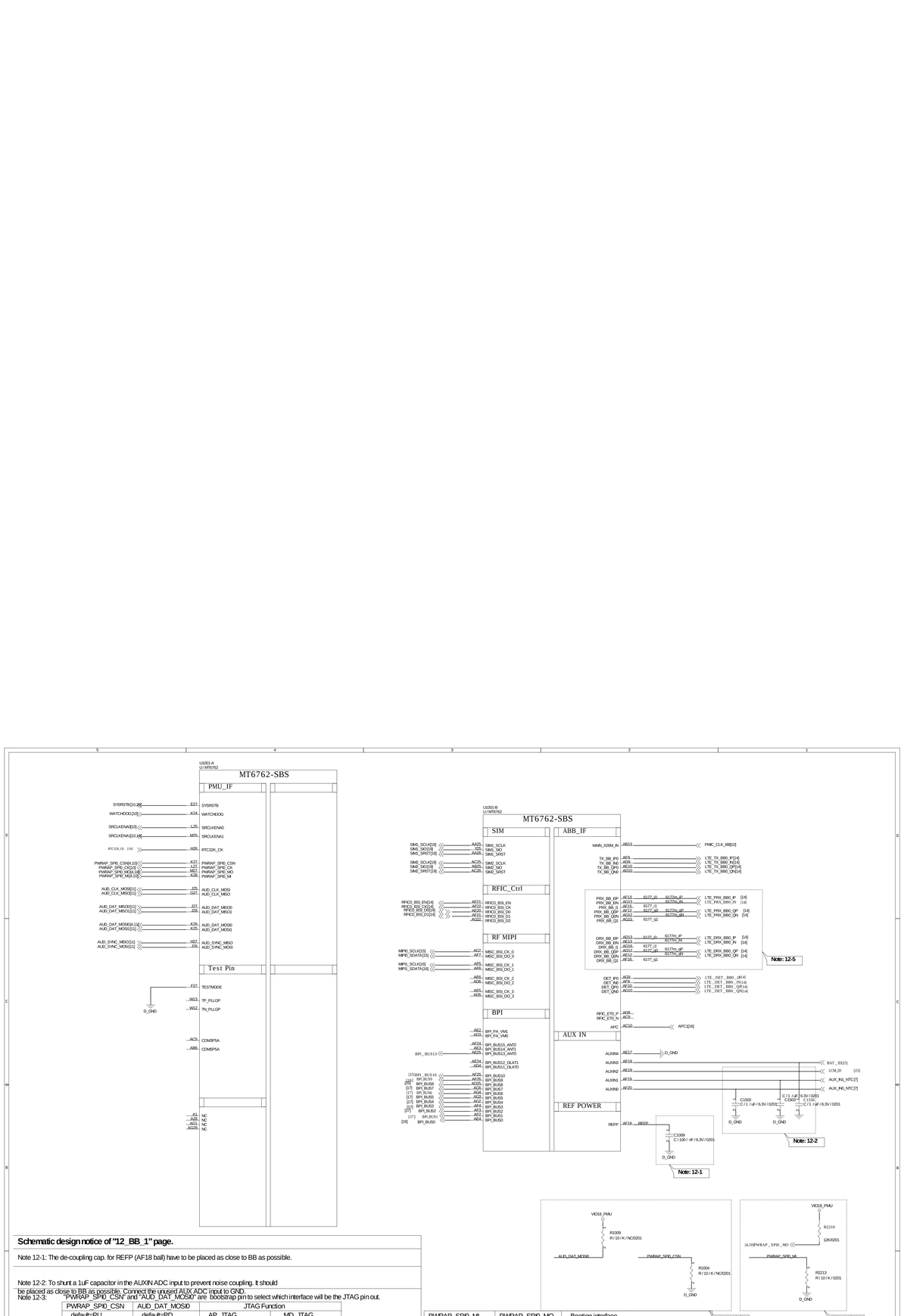
Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: C4101 closed DVDD18_MSDC0 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: C4301 closed DVDD18_MSDC1 150mil

Title	11_BB_POWER_PDN
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 3 of 29



Schematic design notice of "12_BB_1" page.

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by-ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by-ext. PD)	LO	SPI0+EINT8	N/A
LO (by-ext. PD)	HI (by-ext. PU)	MSDC1	N/A

Note 12-4: PWRAP_SPI0_MI is DDR type feature in bootstrap

PWRAP_SPI0_MI	Booting interface	
default=PU	DDR	MSDC0 pin mux
LO (by-ext. PD)	LPDDR3	follow LP3 Ref SCH.
HI	LPDDR4X	follow LP4X Ref SCH.

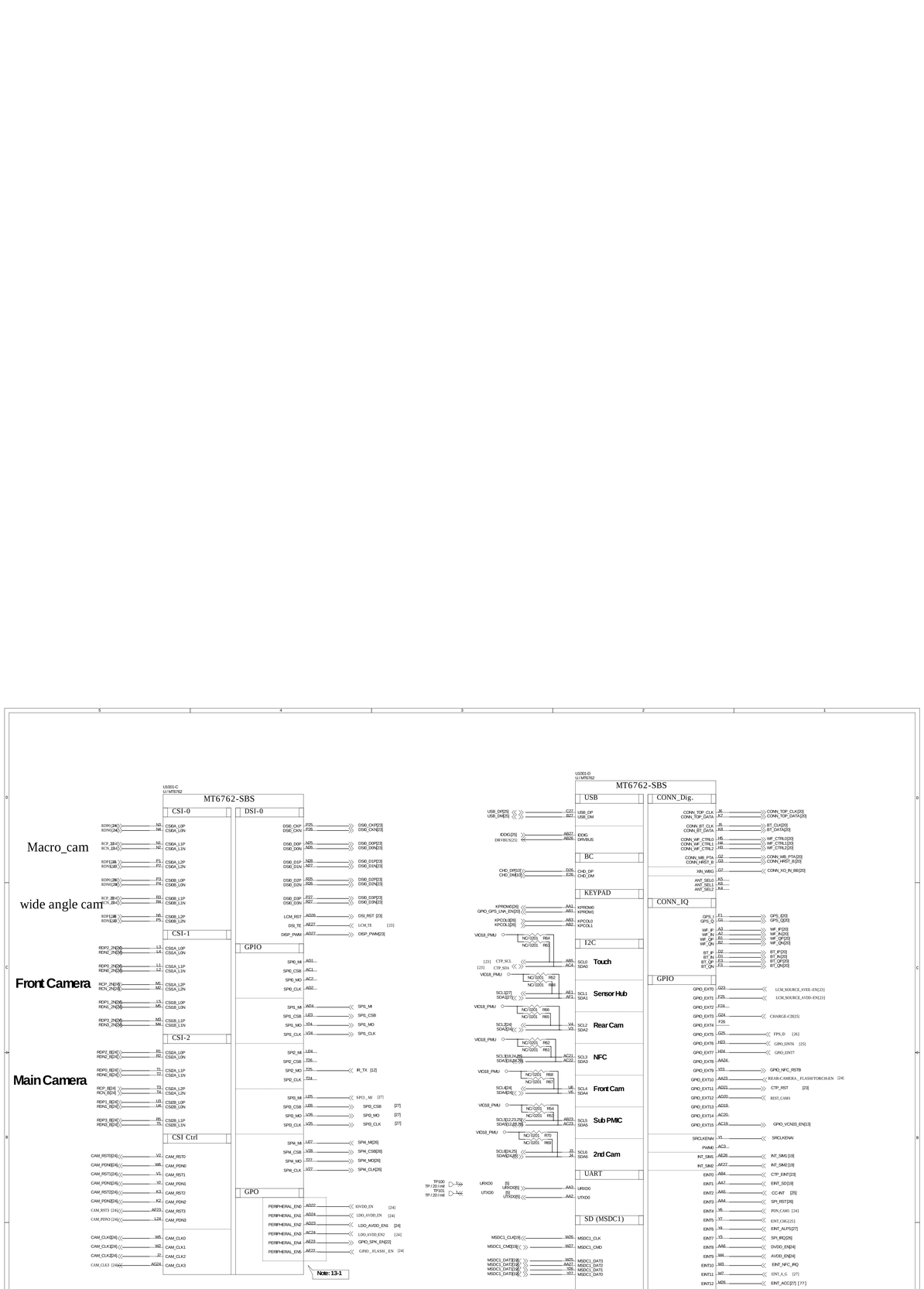
PWRAP_SPI0_MI	PWRAP_SPI0_MO	Booting interface	
default=PU	default=PD	DDR	MSDC0 pin mux
LO (by-ext. PD)	LO	LPDDR3	follow LPDDR3 Ref SCH.
LO (by-ext. PD)	HI (by-ext. PU)	N/A	N/A
HI	LO	LPDDR4X	follow LP4X/LP4 Ref SCH.
HI	HI (by-ext. PU)	LPDDR4	follow LP4X/LP4 Ref SCH.

Note 12-5: Please set unused IQ pins in NC

Title: 12_BB_1

Size: E | MTK Confidential

Date: Tuesday, January 08, 2019 | Sheet 4 of 29

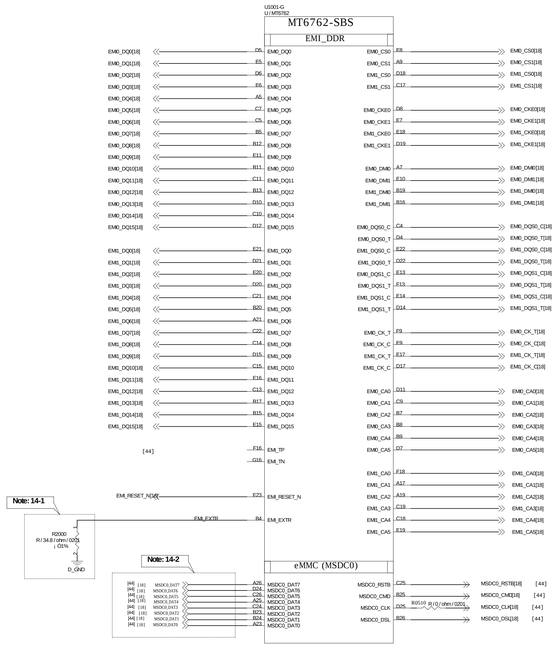


Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger

OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

Title	13_BB_2
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 5 of 29

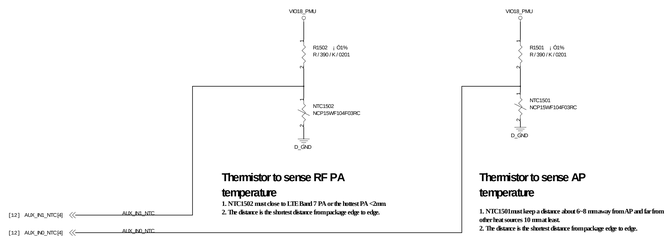


Schematic design notice of "14_BB_3" page.

Note 14-1: R4001 please select 34.8 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux

Title:	14_BB_3	
Size: E	MTK Confidential	
Date: Tuesday, January 08, 2019	Sheet 6 of 29	



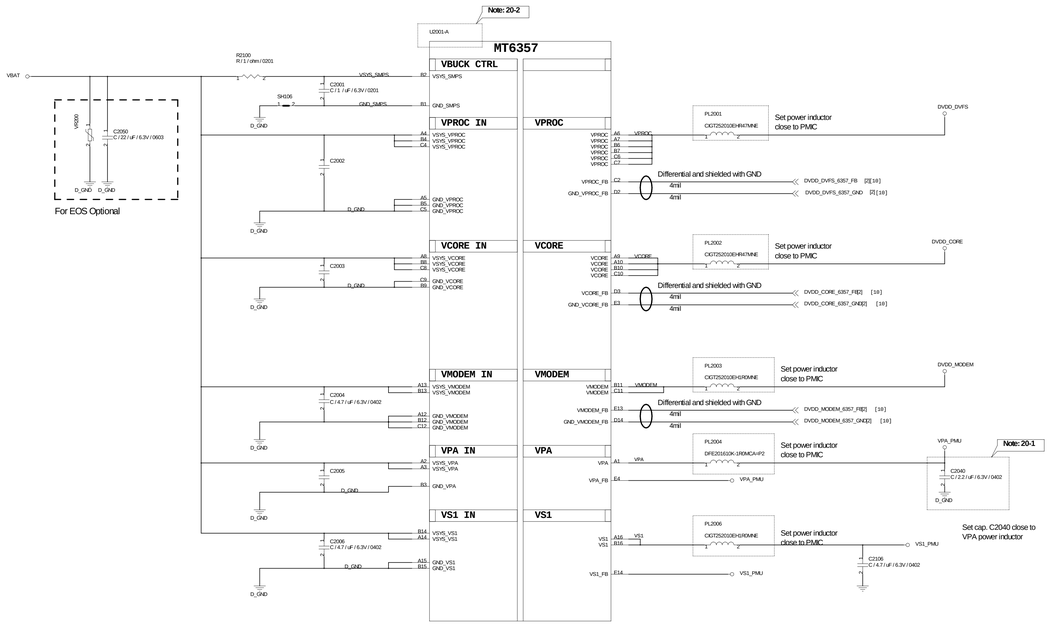
Thermistor to sense RF PA temperature

1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm
2. The distance is the shortest distance from package edge to edge.

Thermistor to sense AP temperature

1. NTC1501must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

Title	15_BB_AUXADC_Thermal	
Size: E	MTK Confidential	
Date: Tuesday, January 08, 2019	Sheet 7 of 29	



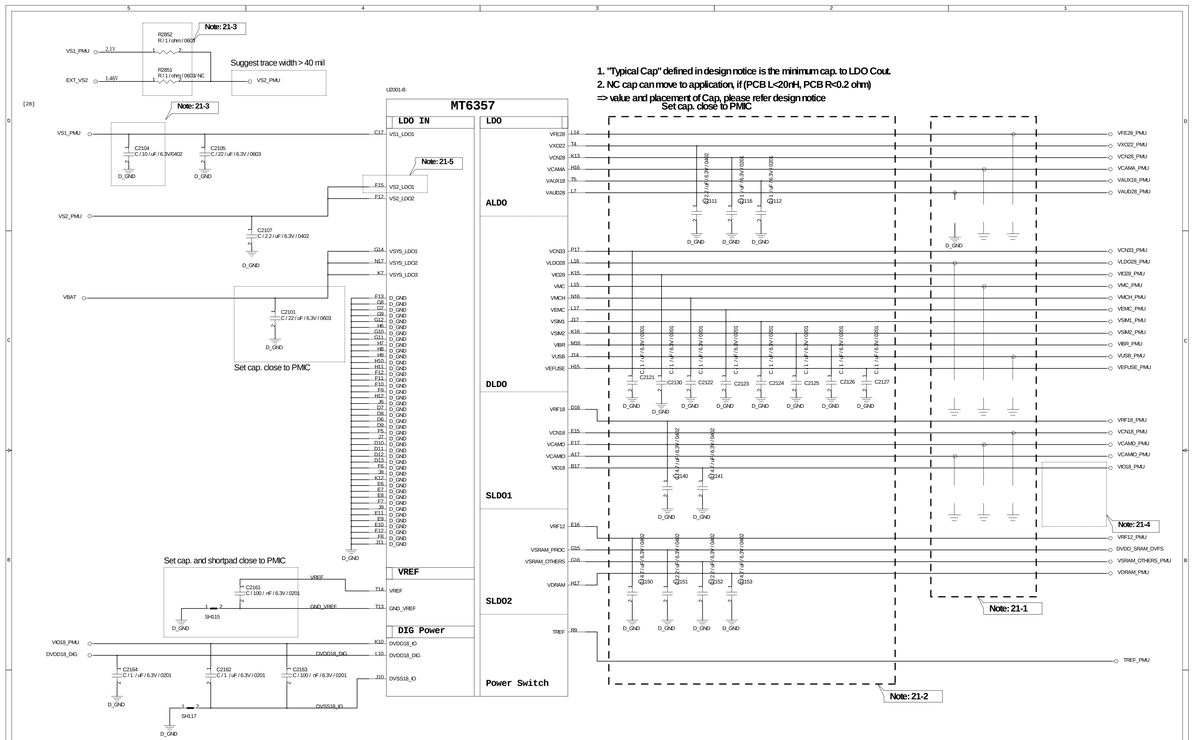
Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C2040, please choose 0402 size

Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357 CRV
MT6761	MT6357 MRV

Title	20_POWER_MT6357-Buck
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 8 of 29



Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1:
If these power trace can meet LDO layout constraint, these CAP can be NC or removed.

Note 21-2:
Please refer to MT6357 design notice.
Output cap range please follow MT6357CRV LDO design notice

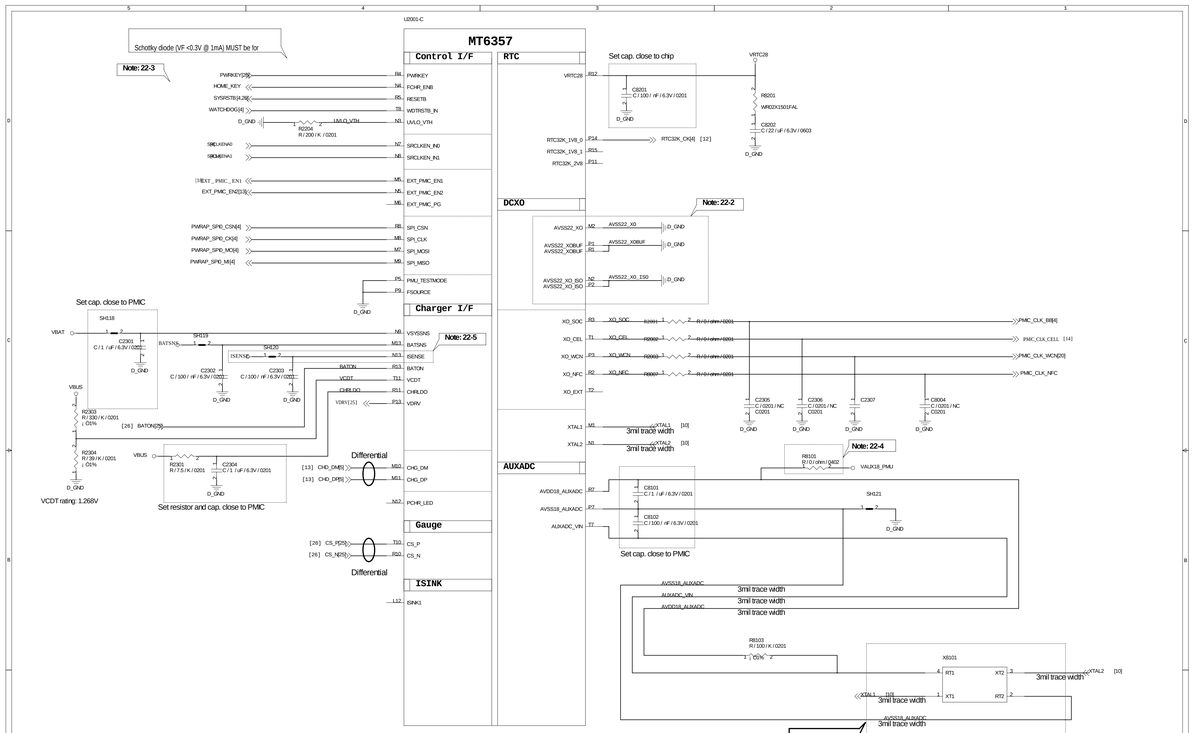
Note 21-3: Ext Buck BOM option

	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C2104	10uF , 0603	22uF , 0603
R2851	0-ohm , 0603	NC
R2852	NC	0-ohm , 0603

Note 21-4:
Please set SH2101 and SH2102 close to C2141, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C2141
Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

Title: 21_POWER_MT6357-LDO
Size: E
MTK Confidential
Date: Tuesday, January 08, 2019 Sheet 9 of 29



Schematic design notice of "22_POWER_MT6357-IF"

Note 22-1:
Please implement 2520 & 2016 Size TMS PCB co-layout.
Please refer to MT6762_MT6357 Co-Clock Design Notice for co-layout guide

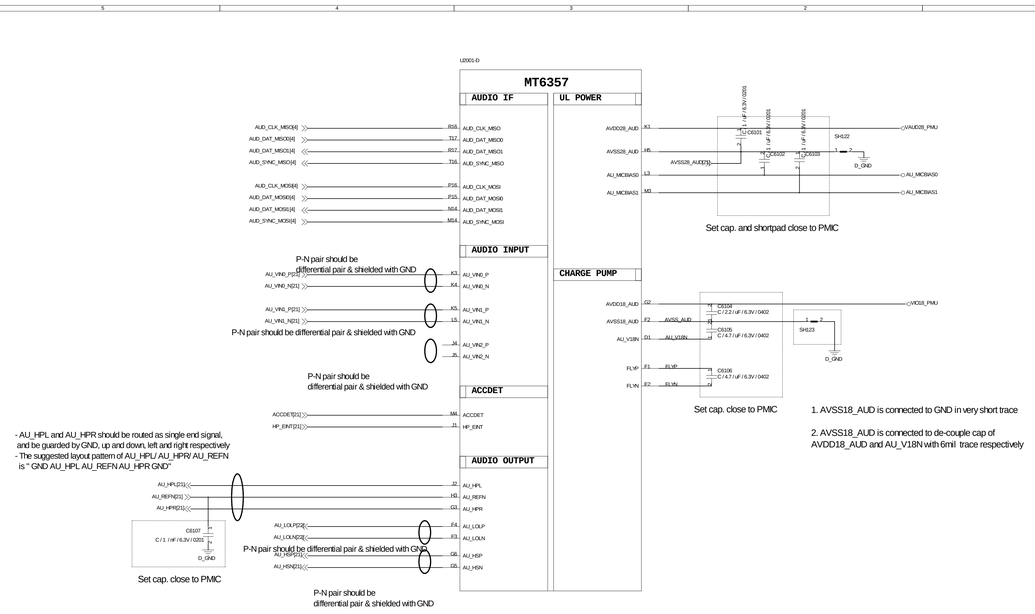
Note 22-2:
1. Please Connect P1 and R1 ball first and then to GND
2. Please Connect P2 and L2 ball first and then to GND
3. Please connect DCXO GND to main GND by independent L1-2 GND via.;
DO NOT connect it through L1 GND

Note 22-3:
For Schottky diode (VF <0.3V @ 1mA) MUST be for

Note 22-4:
Please follow MT6762_MT6357 Co-Clock Design Notice for Layout guide of VAUX18,
then R8101 can use 0 ohm to replace BEAD.

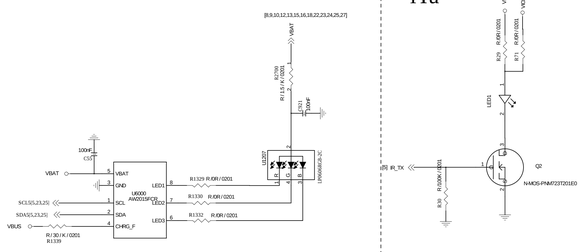
Note 22-5: Please connect to battery connector

Title	22_POWER_MT6357-IF
Size	E
	MTK Confidential
Date:	Tuesday, January 08, 2019
Sheet	10 of 29



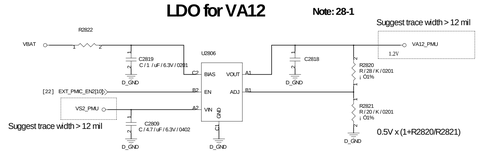
Title	23_POWER_MT6357-Audio	
Size: E	MTK Confidential	
Date: Tuesday, January 08, 2019	Sheet 11 of 29	

RGB_LED


[8,9,10,12,13,15,16,18,22,23,24,25,27]
VBAT
R1709
R1:2.7K / 0201
C1521
100nF
C1705
100nF
VBAT
GND
SCL
SDA
CHRG_F
U6000
AW20018FCR
LED1
LED2
LED3
R1329 R:0R / 0201
R1330 R:0R / 0201
R1332 R:0R / 0201
SCL3,5,21,23]
SDA3,5,21,25]
VBUS
R:/ 30.1K / 0201
R1339
LED5
LED6
LED7
LED8
LED9
LED10
LED11
LED12
LED13
LED14
LED15
LED16
LED17
LED18
LED19
LED20
LED21
LED22
LED23
LED24
LED25
LED26
LED27
LED28
LED29
LED30
LED31
LED32
LED33
LED34
LED35
LED36
LED37
LED38
LED39
LED40
LED41
LED42
LED43
LED44

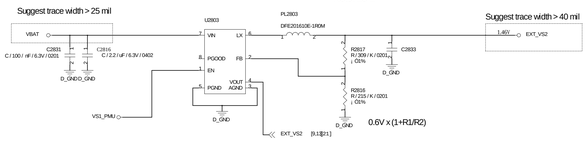
LDO for VA12

Note: 28-1



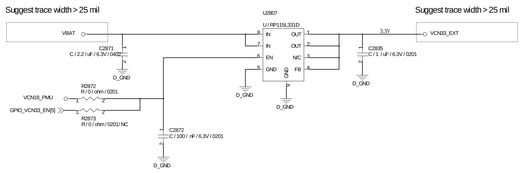
Ext. Bulk for VS2

Note: 28-2



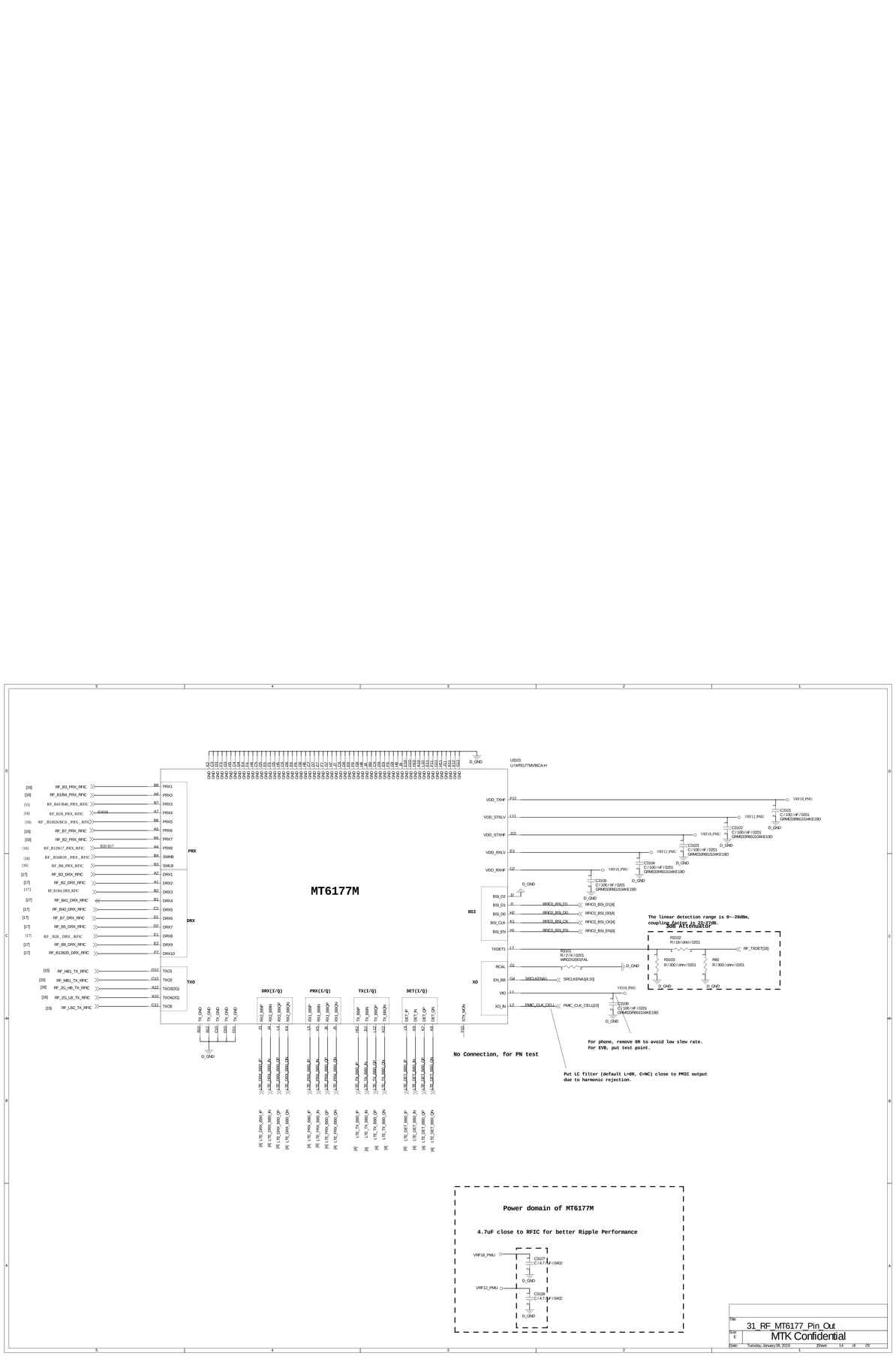
LDO for VCN33

Note: 28-3



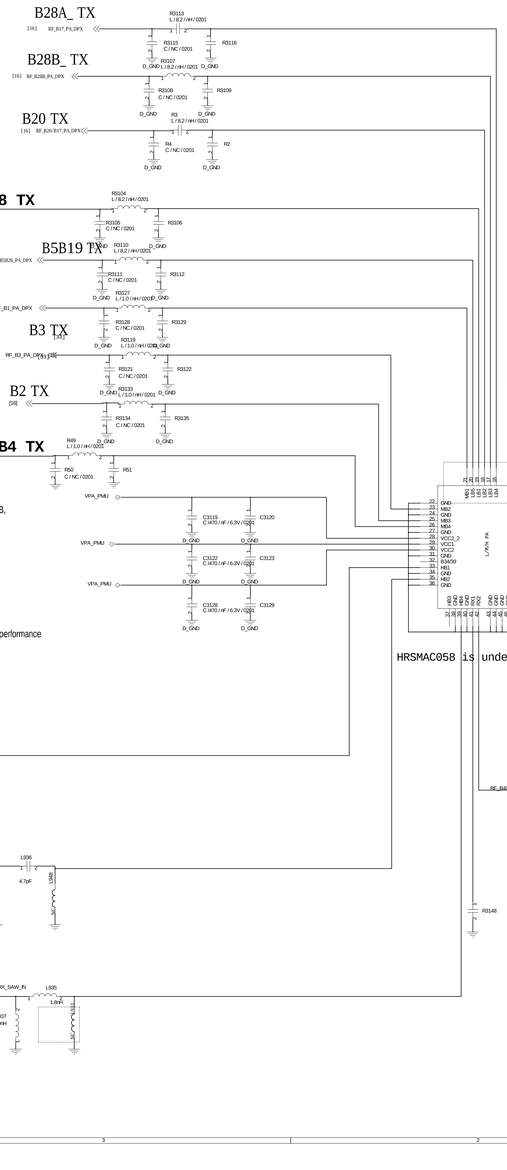
Schematic design notice of "28_POWER_ThirdParty-Power"	
Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631

Title: 28_POWER_ThirdParty_Powers
Size: E
MTK Confidential
Date: Tuesday, January 08, 2019 Sheet 13 of 29

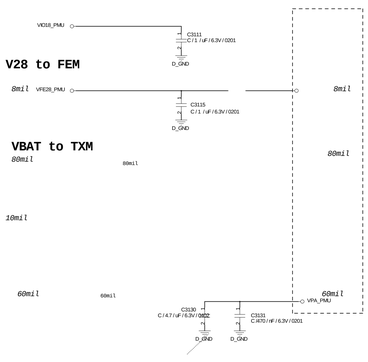


Title	31_RF_MT6177_Pin_Out
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 14 of 29

B1 TX



Power Net Connection



Note:
Refer to design notice

Reserve at least one tuning cap. For PMIC VPA total cap requirement,
Note:

the total cap at RF side should be in 6.2uF +7/-5%.

Note:
for GPS co-existence case and if the antenna isolation between GPS and B34 <30dB,
suggest not to use TXM reuse and use a BPF filter after B34 PA

For B39 Multi-cluster Application, sugget to use B39 standalone TX SAW(U3225) for beter SEM performance

Note:
Please use the phase3 HML PA to support B1/3 CA
4G PA input need LPF for harmonic rejection

HRSMAC058 is under verification

3/4G_PAIN_LB

3/4G_PAIN_MB

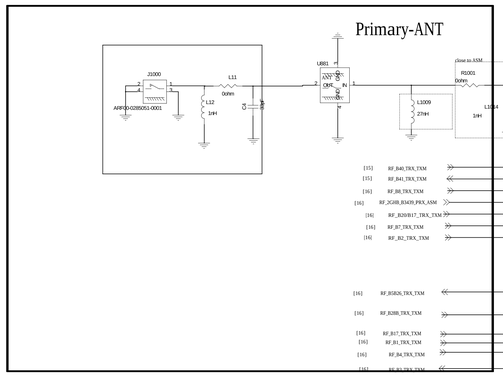
3/4G_PAIN_HB

Reserved Shunt C for MIPI C-load Tuning
Control the Total Capacitance to 25pF+-3pF

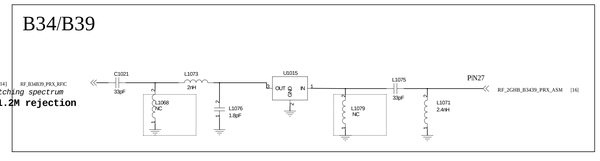
LPF for more margin on Tx spurious

Title	32_RF_MT6177_RF_TX
Size: C	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 15 of 29

LTE MAIN ANTENNA

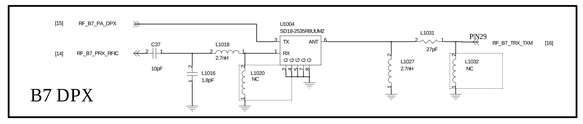


B34/B39

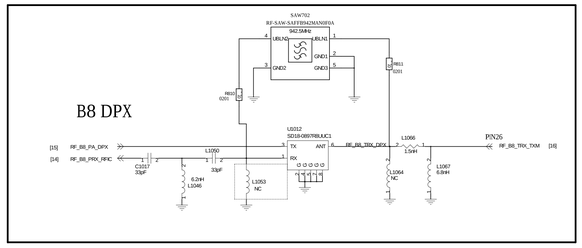


Reserve for GMSK 1.2M switching spectrum
RC=6.98K/220pF for 1.2M rejection

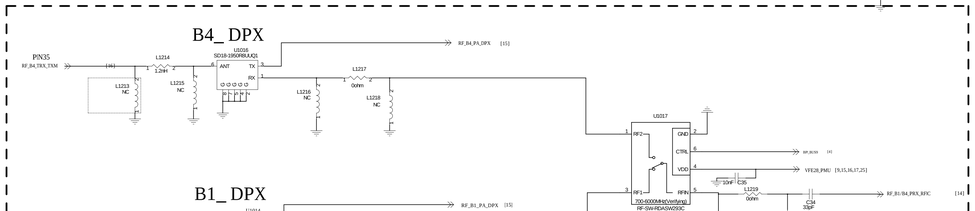
B7 DPX



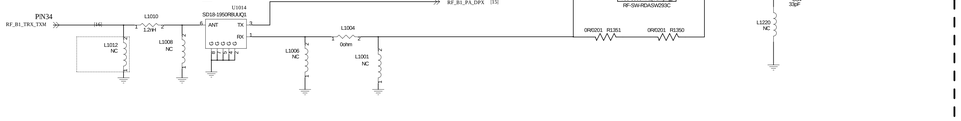
B8 DPX



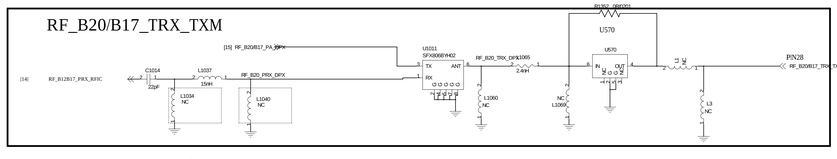
B4_ DPX



B1_ DPX

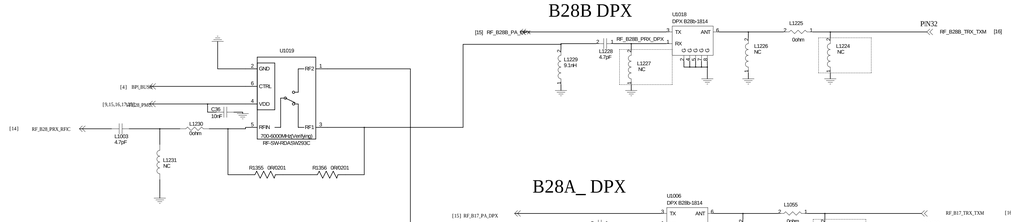


RF_B20/B17_TRX_TXM

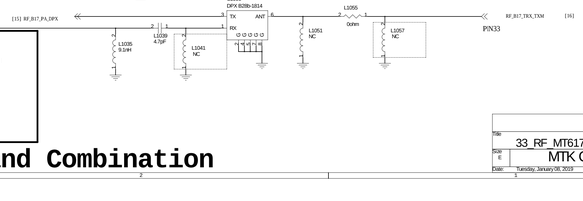


B17/28A/B28BÍ¬Ê± ´æÔÚÊ±×÷Îª B17Í¨µÀ

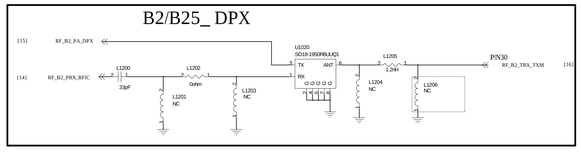
B28B DPX



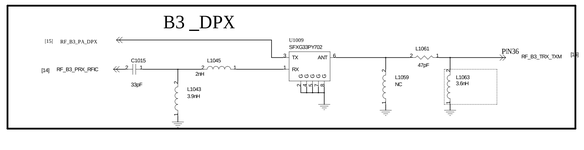
B28A_ DPX



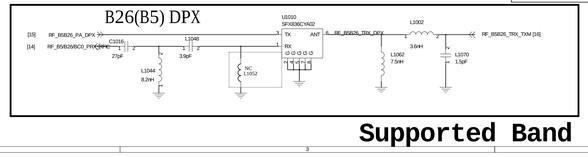
B2/B25_ DPX



B3 _DPX



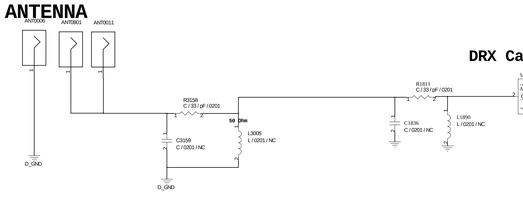
B26(B5) DPX



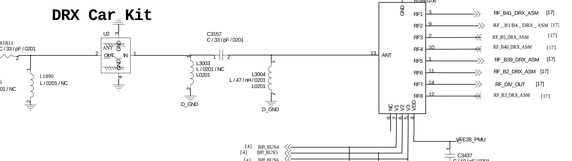
Supported Band Combination

Title	33_RF_MT6177_RF_PRX
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 16 of 29

LTE DRX ANTENNA

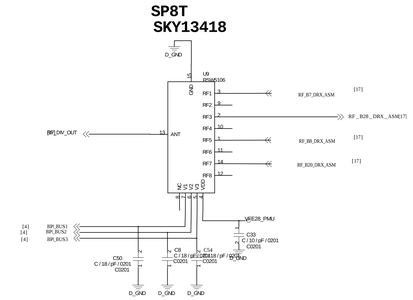


DRX Car Kit

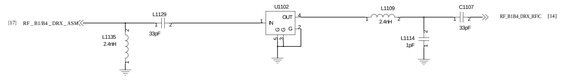


SP8T SKY13418

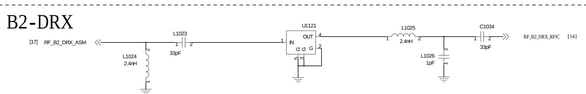
SP8T SKY13418



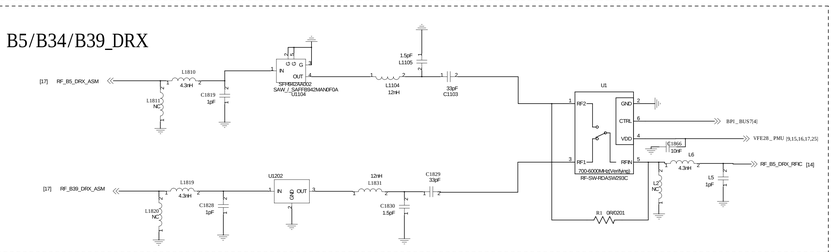
B1/B4_DRX



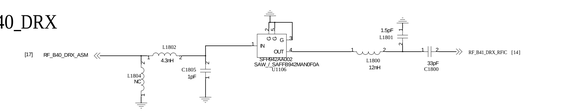
B2-DRX



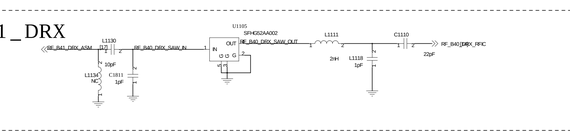
B5/B34/B39_DRX



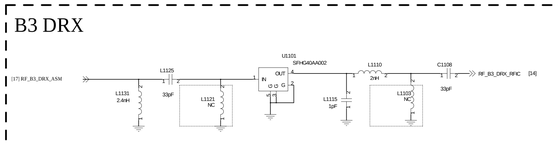
B40_DRX



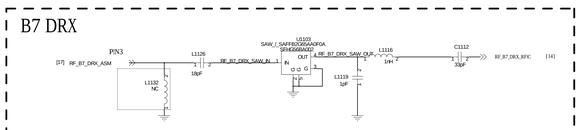
B41 _ DRX



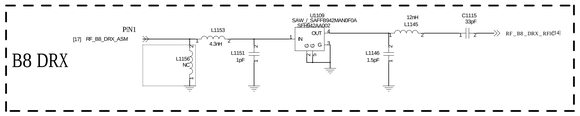
B3 DRX



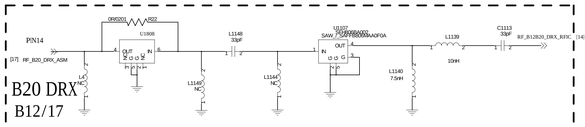
B7 DRX



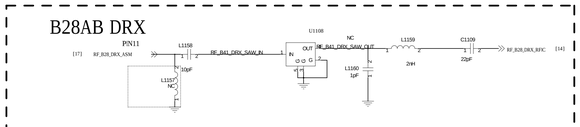
B8 DRX



B20 DRX
B12/17

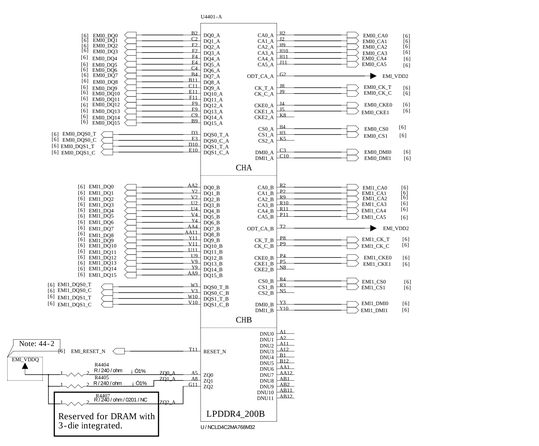


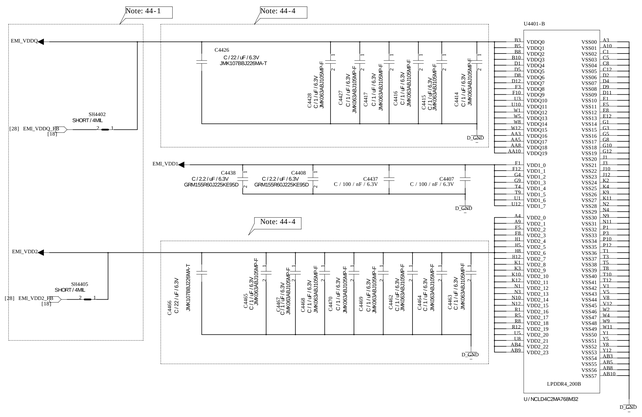
B28AB DRX

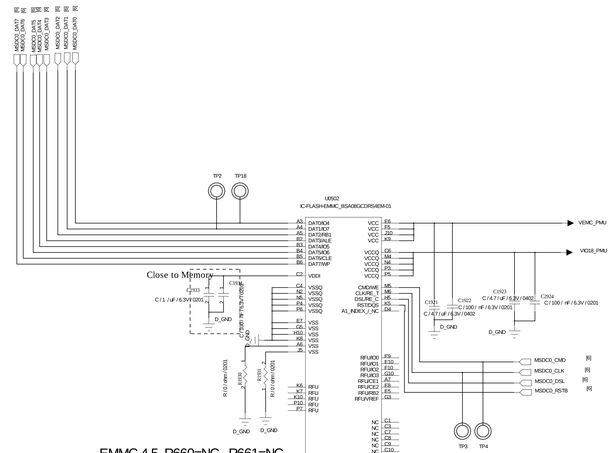


Title:	34_RF_MT6177_RF_DRX
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 17 of 29

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE

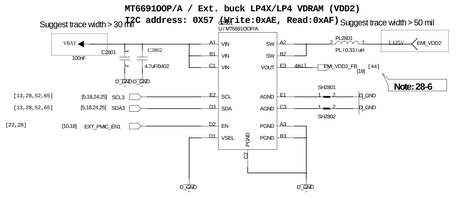






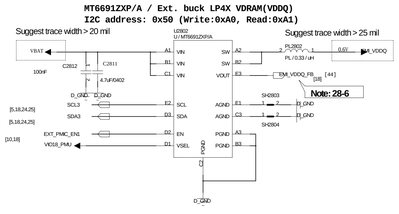
Ext. buck LPDDR4X/LPDDR4 VDRAM

Note: 28-4



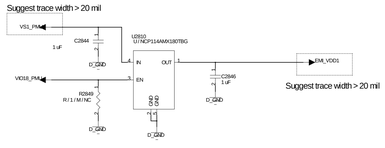
Ext. buck LPDDR4X VDDQ

Note: 28-4



LPDDR4X/LPDDR4 VDD1 1.8V LDO

Note: 28-5



Schematic design notice of "44_Memory_eMMC_LPDDR4"

Note 44-1: Please refer to power supply related page select output voltage properly for LPDDR4

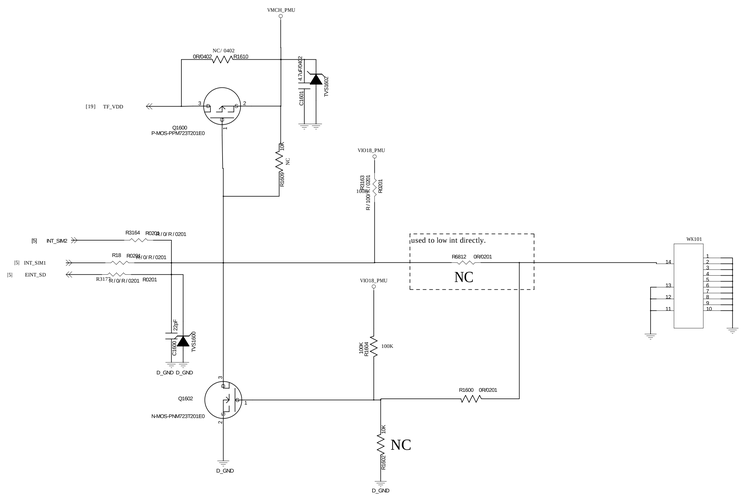
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

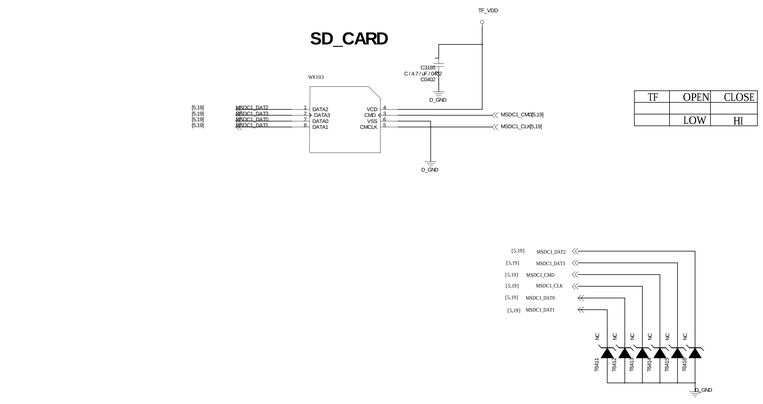
Note 44-5:

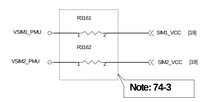
DRAM type	R4437, R4438
LPDDR4	Mount
LPDDR4X	NC

COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE: <Code>	SIZE: E	DRAWING NO: <Drawing Number><Revision>	REV:
SCALE: <Scale>		SHEET: 28 29	



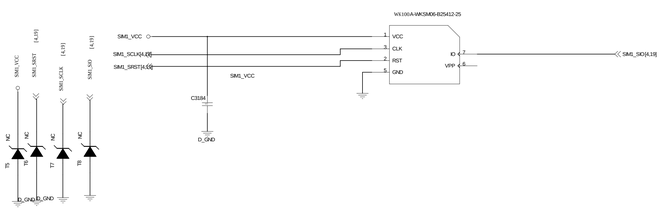
SD_CARD



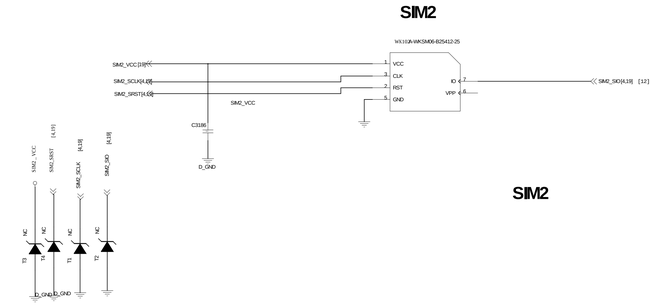


Note: 74-3

SIM1

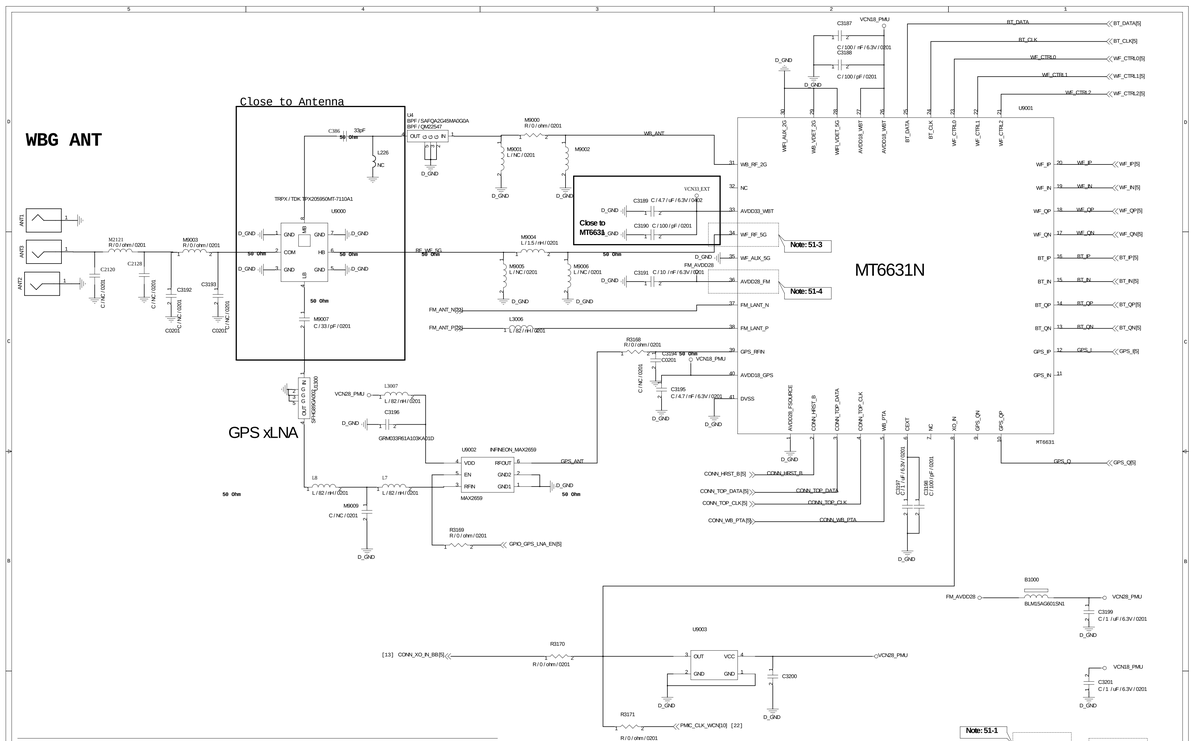


SIM2



Schematic design notice of "46_MEMORY_SD Card" page.

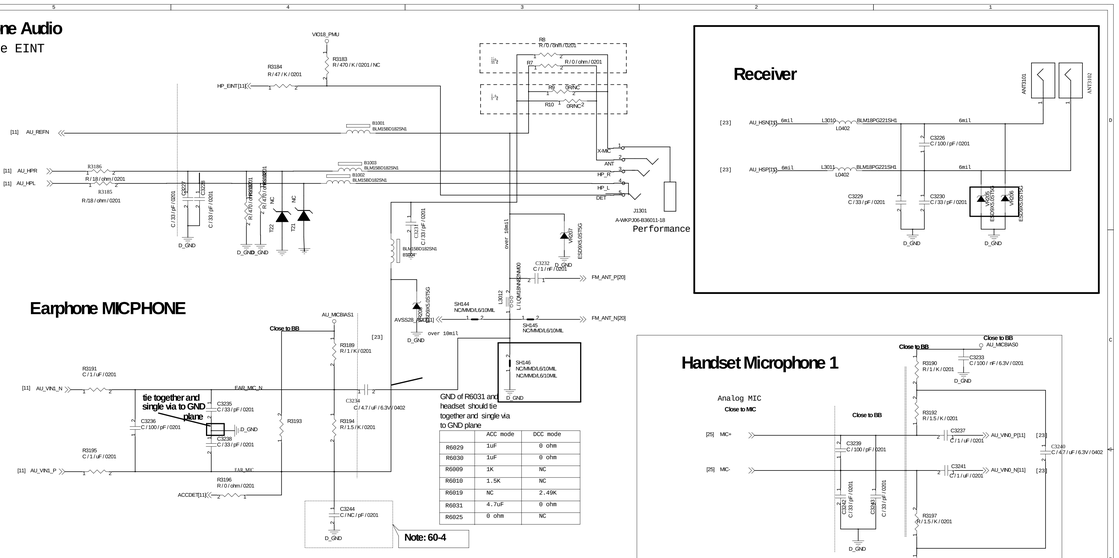
Note 46-1: For better ESD performance, please select suitable components for system protection.



Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"

Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6762 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support
Note 51-5:	Please refer "Design Guide MT6765_62_61_MT6631 removing VCN33 LDO" before using VCN33_PMU for WiFi

Title	51_CONNECTIVITY_CONSYS_MT6631
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 20 of 29



Schematic design notice of "62_PERI_AUDIO_IO" page.

Note 62-1:

Part # of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will

Note 62-2: results in FM RSSI 10dB degraded .

Note 62-3: Reserved Cap for CS/RS test, please double check multi-key function when used

	Earphone Jack @ Main board	Earphone Jack @ Sub board
R6513	0 ohm	100nF

Note 62-4:

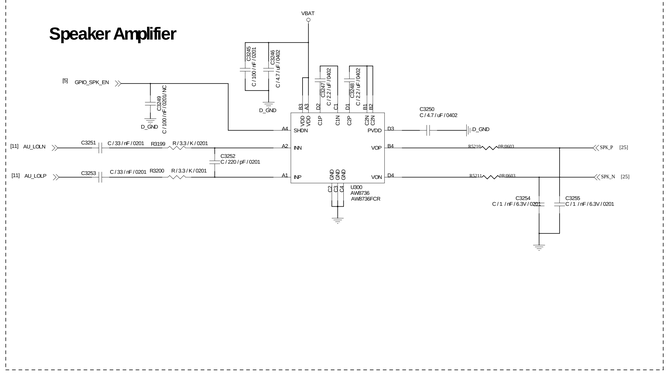
1. Please Select ACC Mode for Operator Project to Pass Electrical MOS Test; More Information refer to Audio/Speech Design Notice;
2. Need do SW configuration for ACC or DCC mode
3. Analog input impedance is as below, please customer check the detail requirement with mic vendor if the mic used has special requirement on the input impedance of analog input

MT6357	UL mode	Min	Typ	Max	Unit
R_{IN}	ACC	7K	-	-	ohm
C_{IN}	DCC	-	-	11p	F

Note 62-5: Please select C6231 with 0402 size

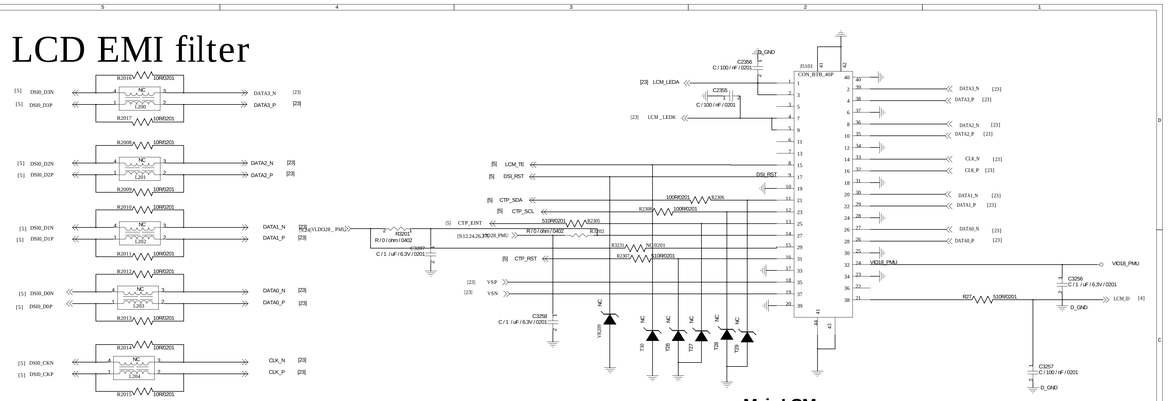
Title	62_PERI_AUDIO_IO
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 21 of 29

Speaker Amplifier

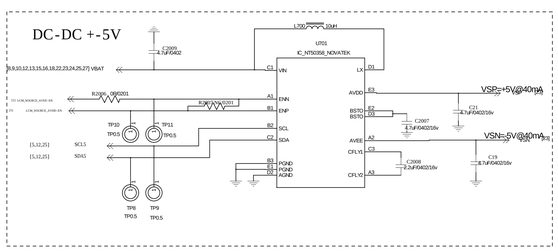


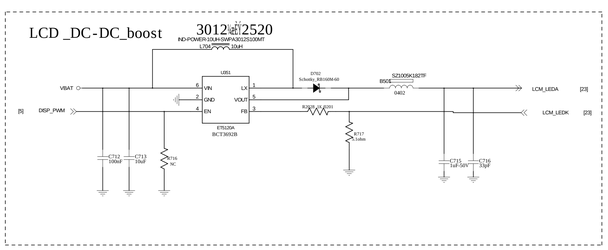
Title	65_PERI_SPEAKER_AMP	
Size: E	MTK Confidential	
Date: Tuesday, January 08, 2019	Sheet 22 of 29	

LCD EMI filter



Main LCM



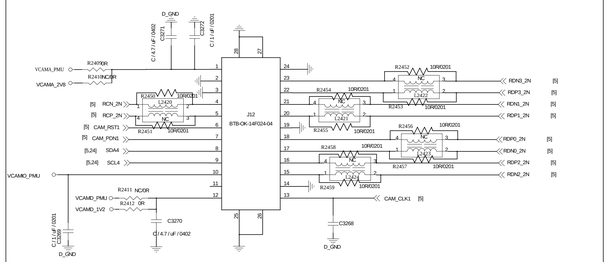


Schematic design notice of "67_PERI_LCD_CTP" page.

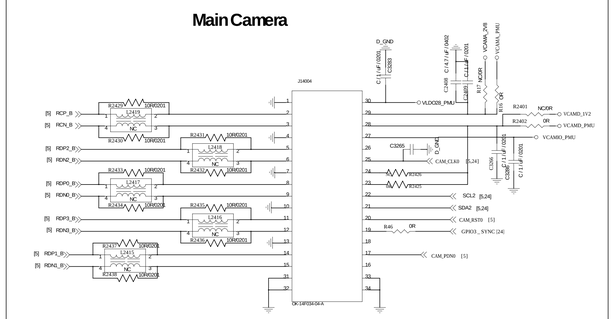
Note 67-1: It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.

Title	67_PERI_LCD_CTP
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 23 of 29

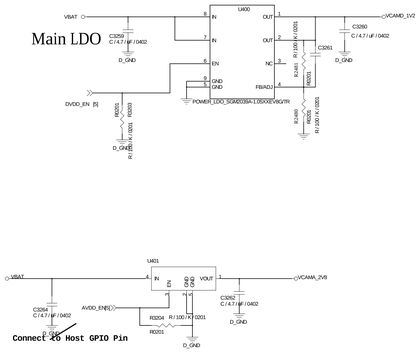
Front Camera



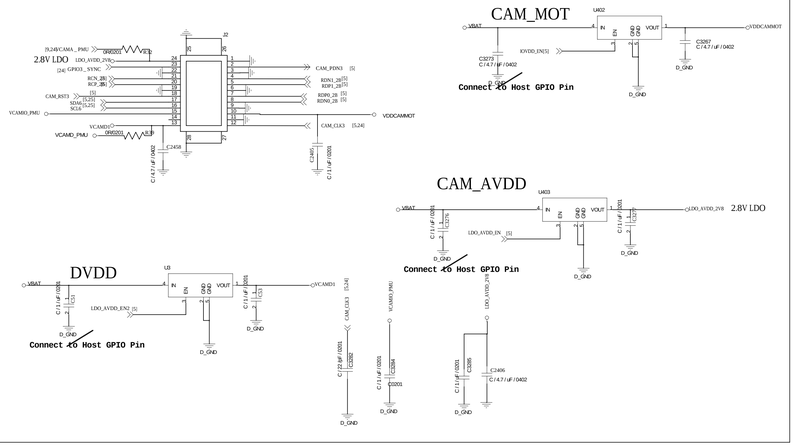
Main Camera



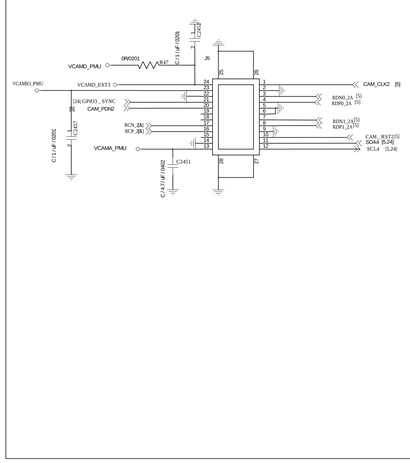
Main LDO



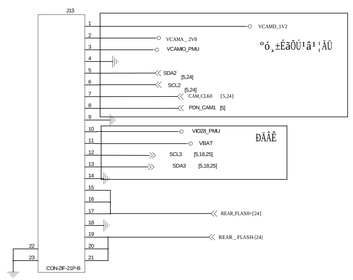
wide angle cam



Macro_cam

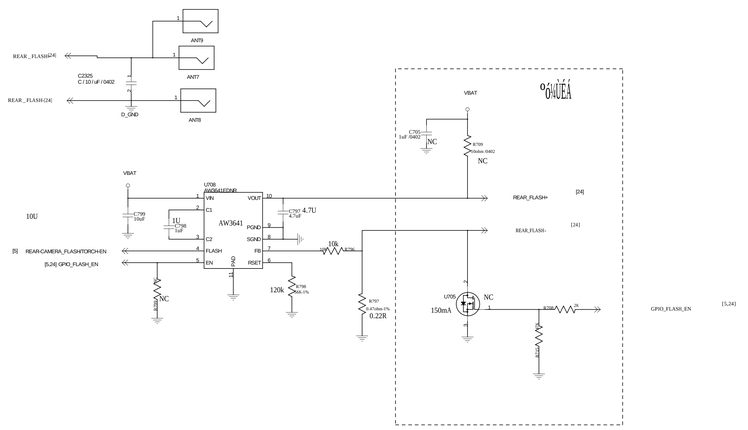


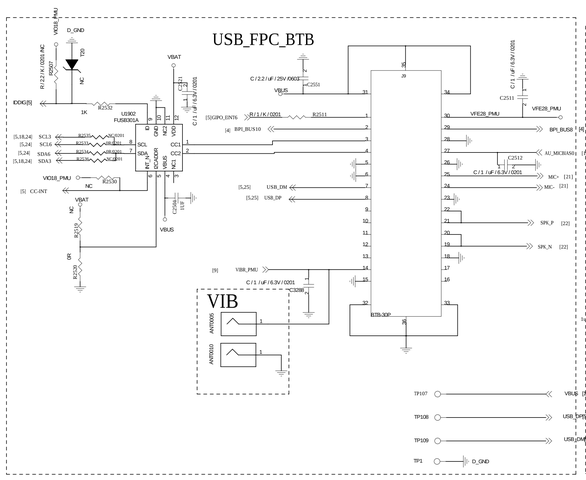
后副摄/遮光功能

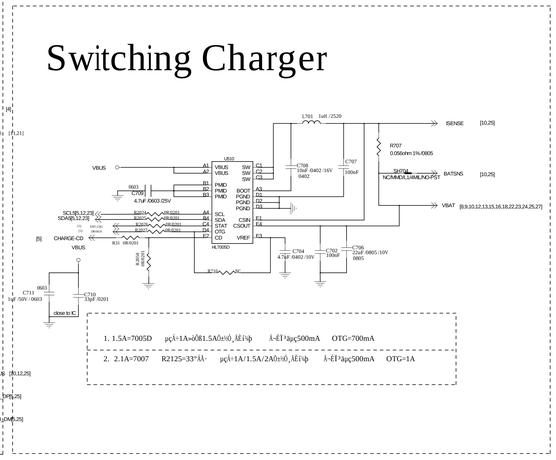


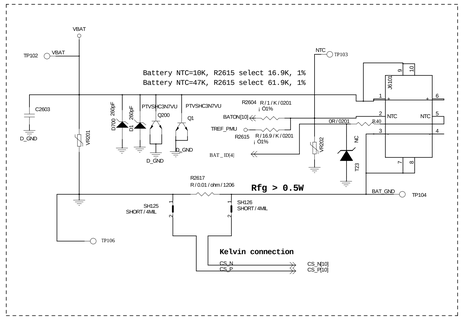
Back FLASH LED

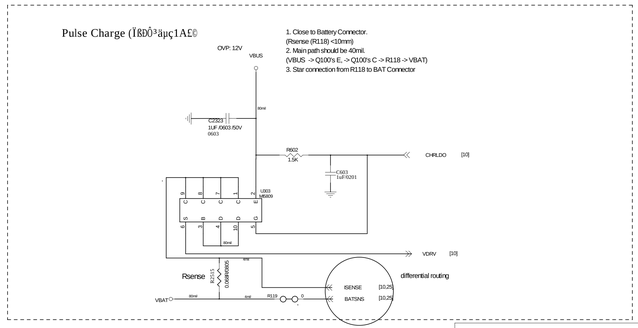
FLASH_LED











Title	71_PERI_USB 2.0	
Size: E	MTK Confidential	
Date: Tuesday, January 08, 2019	Sheet 25 of 29	

Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY

自定义键

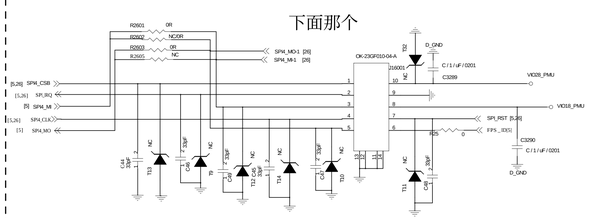
SHIELDING

Fiducial mark

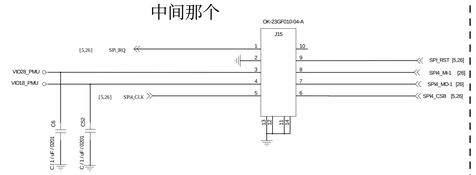
Fingerprint Sensor

Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)

下面那个



中间那个



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 75-1: DO NOT put pull-up resistor on PWRKEY

Note 75-2:
Volume Up : HOME Key / GND
Volume Down : KPROW0/KPCOL0

Note 75-3: For better ESD performance, please select suitable components for system protection.

Title	75_PERI_KEYPAD
Size: E	MTK Confidential
Date: Tuesday, January 08, 2019	Sheet 26 of 29

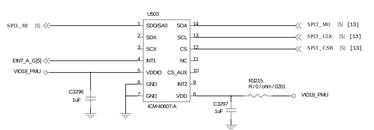
M-Sensor

AK09918 / M-Sensor I2C Address : 0x0C (Write:0x18, Read:0x19)

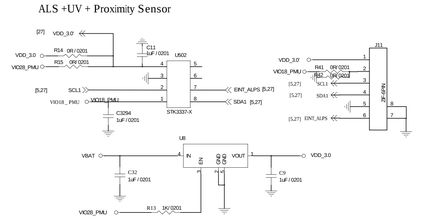
G-Sensor

Accerometer

default SPI (if sensor hub support)



ALS +UV + Proximity Sensor



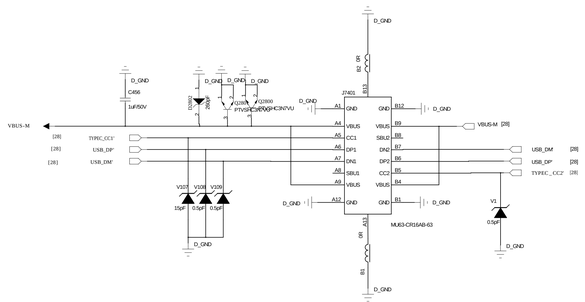
Schematic design notice of "77_PERI_SENSORS_MEMs_ALS/PS" page.

Note 77-1:	[M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail
Note 77-2:	[A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide
Note 77-3:	[A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C**
Note 77-4:	[A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.
Note 77-5:	[Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)
Note 77-6:	DO NOT share Sensor hub i2C to other non-SCP device
Note 77-7:	Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]

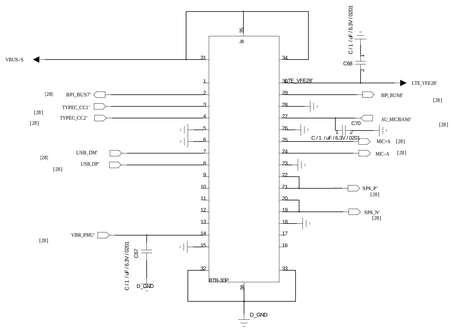
Title: 77_PERI_SENSORS_MEMs_ALS/PS
Size: E
MTK Confidential
Date: Tuesday, January 08, 2019 Sheet 27 of 29

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE

TYPE-C



USB_FPC_BTB



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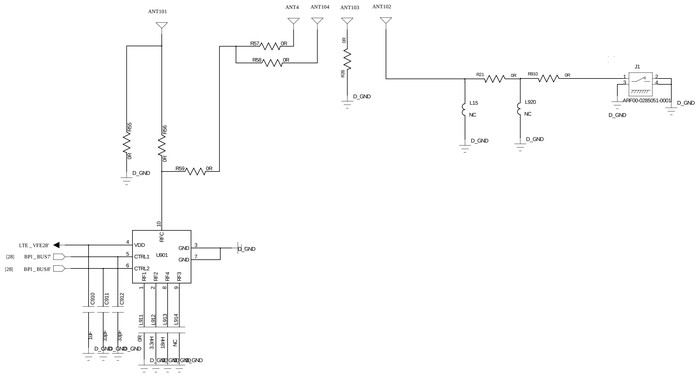
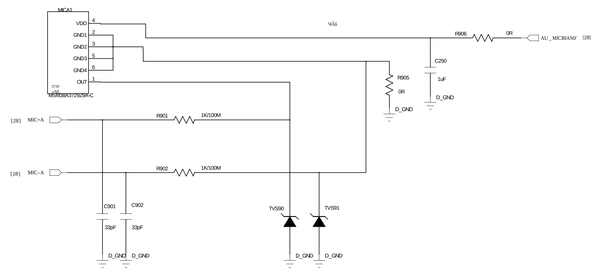
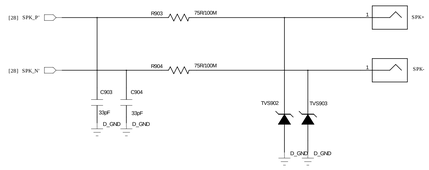


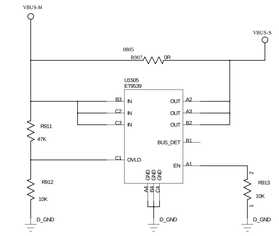
MIC1µ×³öÒô



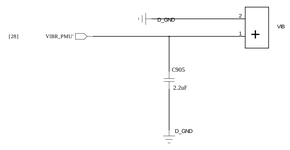
SPK



OVP



VIB



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RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE: <Scale>	SHEET: 28 29