SLM758 Hardware Design Guide

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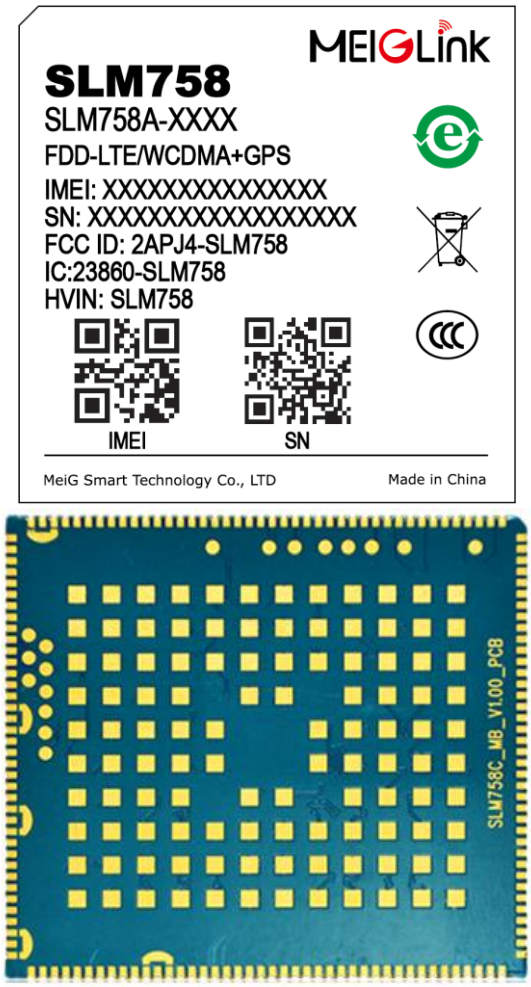

Foreword

Thank you for using the SLM758 module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

Before the announcement, the company has the right to modify the contents of this manual according to the needs of technological development.

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2018-11-21	1.08	Update information about reset,GPS	Zheng Lei

1. Introduction

This document describes the hardware application interface of the module, including the connection of the circuit and the RF interface.It can help users quickly understand the interface definition, electrical performance, and structural dimensions of the module.Combining this document with other application documents, users can quickly use modules to design mobile communication applications.

2.Module overview

SLM758 series core board, uses the MSM8953 of Qualcomm Snapdragon 600 series for its main chip, and its CPU is made of 14nm FinFET, built in 64bit ARM, 8 cores Cortex A-53, main frequency 2.0G processor, supporting LPDDR3 SDRAM memory.

Supporting board memory of 16GB/32GB global different mode multi-mode LTE intelligent communication module.This module is suitable for broadband intelligent wireless communication modules of TD-LTE/FDD-LTE/WCDMA/EVDO/TD-SCDMA/CDMA/GSM network standards.

The working frequency band supported by SLM758 module is:

- FDD-LTE: B2/4/5/7/12/13/17/28b
- WCDMA: B2/4/5

The SLM758 provides voice, SMS, address book, WiFi, BT and GPS functions while providing high-speed broadband data access; Product supports dual 1300W 3D camera or depth of field camera, and it can be widely used in VR Camera, intelligent robot, Video surveillance, security, automotive equipment, intelligent platform handheld terminals and other products.

The physical interface of the module is a 272-pin pad that provides the following hardware interfaces:

- Four 1.8V UART serial ports, supporting four or two wires.
- Main LCD（MIPI interface）+ Secondary LCD（MIPI interface）.
- LCD backlight interface.
- Three-way Camera interface（MIPI data）.
- Flashlight interface.
- A high-speed USB interface.
- Two Audio input interface.
- Three Audio output interface.
- Two-way UIM card interface.
- GPIO interface.
- Six groups of I2C interfaces.
- Two sets of SPI interfaces.
- One TF card interface.
- Support GNSS，WiFi，Bluetooth 4.1 functions.

2.1 Summary of features

Table 2.1：SLM758 features

Product characteristics		Description
Plateform		Qualcomm MSM8953
CPU		Octa-core A53 (64bit) 8*2.0GHz * Octa-core A53 (64bit) 8*1.8GHz * Octa-core A53 (64bit) 8*2.2GHz
GPU		Adreno506;650MHz
System memory		16GB eMMC + 2GB LPDDR3 933Mhz compatible with 32GB+3GB
OS		Android 7.1
Size		45.5x41.0x3.0mm，160pin LCC+112pin LGA
Networkband SLM758		FDD-LTE: B2/4/5/7/12/13/17/28b WCDMA: B2/4/5
Wi-Fi		WCN3660B:IEEE 802.11b/g/n/a 2.4G&5G
Bluetooth		BT 4.1
GNSS		GPS/Beidou/Glonass/Galileo
Data Access	TD-LTE	Cat4 TD-LTE 117/30Mbps
	FDD-LTE	Cat4 FDD-LTE 150/50Mbps
	DC-HSPA+	42/11.2Mbps
	TD-HSPA	2.8/2.3Mbps
	EVDO Rev.A	3.1/1.8Mbps
	EDGE	Class12, 236.8kbps/236.8kbps
	GPRS	Class12, 85.6kbps/85.6kbps
SIM		DSDS(Dual Sim-card Dual Stanby) 3.0/1.8V Support SIM hot plug L/W/G/T+G L/W/G/T+W L/W/G/T+1X L/EVDO/CDMA1X+G Don’t support dual CDMA SIM card
Display ((Home screen/subscreen))		Matrix: FULL HD: 1920*1200 60fps;
		LCD Size: User defined
		Interface: 1st LCM：MIPI DSI 4-lane; 2nd LCM：MIPI DSI 4-lane
Camera (Front and Rear)		Interface: Support three sets of CSI, each group is 4-Lane
		Camera Pixel:Rear 13-24Mp/Front up to 13Mp，Dual ISP can support dual

	13MP Camera at the same time	
	Video decode	4K 30fps, 1080p 60fps, H.264/H.265 MP4/ WMV9/ VC1/ DivX/ VP8/VP9
	Video encode	4K 30fps,1080p 60 fps: H.264/ H.265/ MP4/ VP8 1080P 60fps De +1080p 30fps En
Input Device	Key（Power on/off, Home, Volume+, Volume-）	
	Capacitive TP	
Reset	Support HW reset	
Application interface	Interface name	Main function description
	VBAT	3pin，Power input，3.4V～4.2V，Nominal value3.8V
	SDIO *1	TF Card，Support 128GB max
	USB2.0(3.0)	Support OTG USB_BOOT（Force USB boot for emergency downloads）
	BLSP ports	7 ports(BLSP2-8), 4-bits each, multiplexed serial interface functions
	UART*4	BLSP2,BLSP4-6 support UART，up to 4 Mbps
	I2C*6	BLSP2-6&BLSP8 support I2C, These BLSPs use bits [1:0] for I2C
	SPI(master only)	SPI is only support via BLSP
	ADC*3	Support
	Charge	Support5V/2A
	Vibrator	Support
	GPIO	25 GPIOs，Excluded BLSP multiplexing GPIO and GPIO involved in LCM、 TP and CAMERA
	VCOIN	Real time clock backup battery
	RF Interface	Multimode LTE main antenna Multimode LTE diversity antenna The GPS antenna 2.4G WiFi/BT antenna 5G WIFI- antenna
	Audio	One main MIC One noise reduction MIC One Handsfree speaker（Built in 0.8W Class D amplifier） One earpiece One stereo headphone(With headphone MIC) One audio output Two I2S signal

2.2 Block diagram

The following figure lists the main functional parts of the module:

- MSM8953 baseband chip
- PM8953 power management chip
- PMI8952 power management chip
- WCN3660B(Compatible with WCN3680B)-WIFI/BT/FM three in one chip
- Antenna interface
- LCD/CAM-MIPI interface
- EMCP memory chip
- AUDIO interface
- UART、SD card interface，SIM card interface，I2Cinterface,etc.

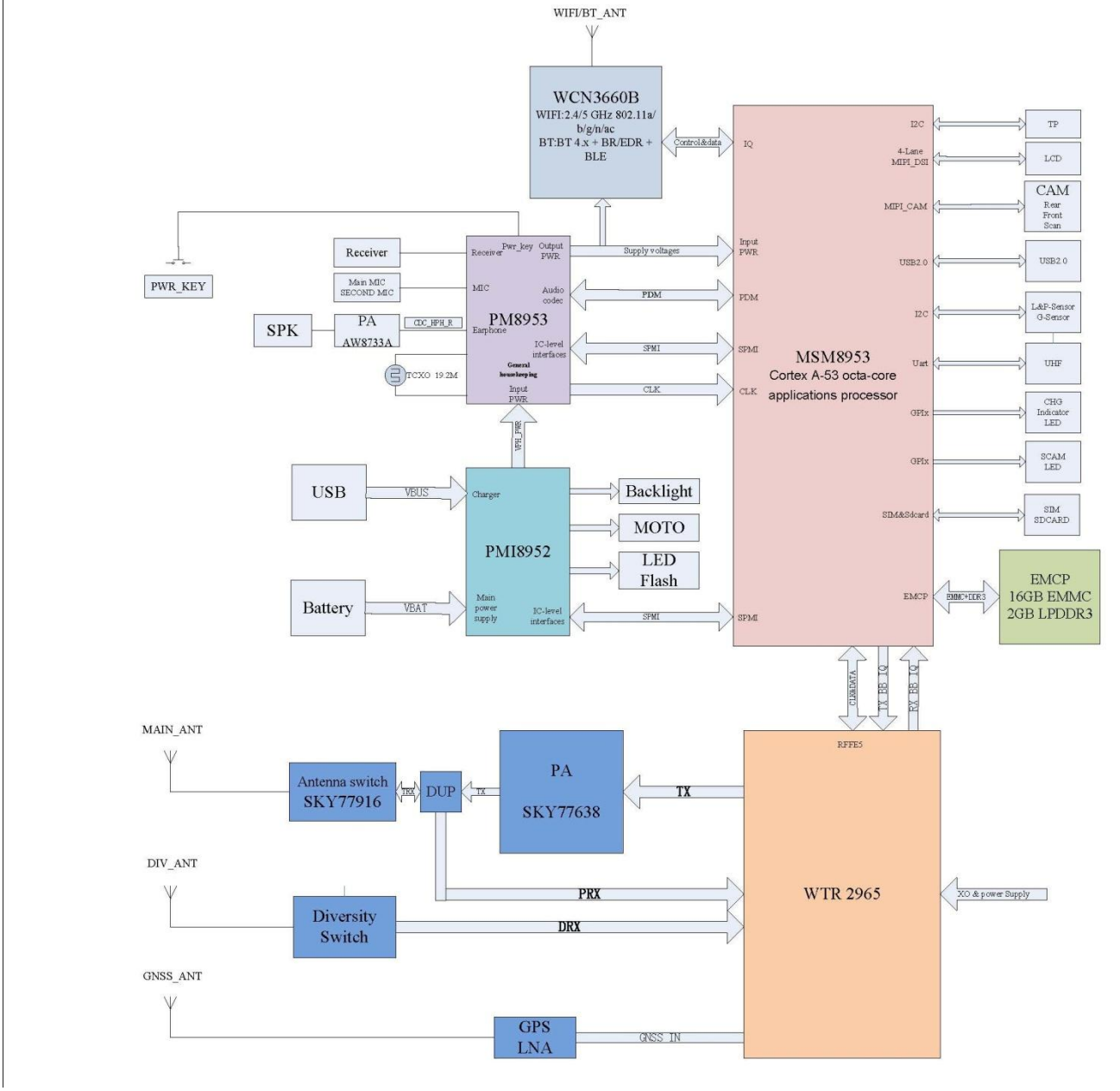


Figure 2.1: module function block diagram

3. Module Package

3.1.Pin distribution diagram

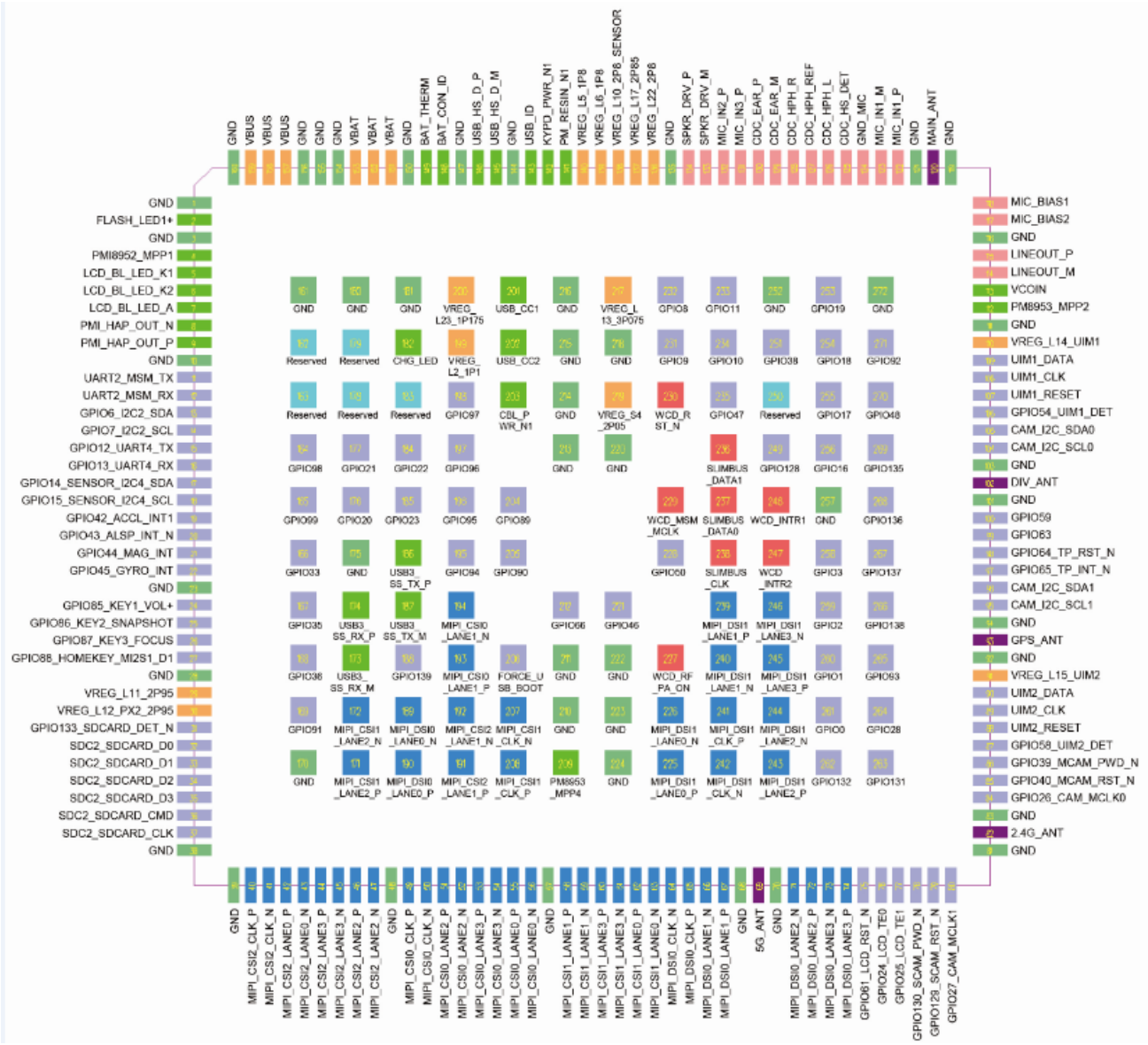


Figure 3.1： module pin diagram (top view)

3.2. Pin definitions

table 3.1： Pin description

Pin number	Pin number	I/O	Description	Comment
The power supply				

VBAT	151、152、153	I	The module provides three VBAT power pin pins. The SLM758 operates from a single supply with a voltage range from 3.4V to 4.2V for VBAT.	Externally, capacitors and Zener diodes must be added for surge protection.
VBUS	157、158、159	I/O	5V charging input power.	
VCOIN	113	I/O	When the VBAT of the system power is absent, the external backup battery provides power to the system real-time clock.When VBAT is present, the backup battery is charged.	VCOIN pins connect 3V button batteries or large capacitors.
VREG_L5_1P8	140	O	1.8V power output, always available for CPU, Memory, IO and other power supply.	100mA
VREG_L6_1P8	139	O	1.8 V power output, standby will be closed, used for Camera, LCD and other small current power supply.	100mA
VREG_L10_2P8_SENSOR	138	O	2.8V power output, will be turned off during standby, used for Sensor, TP power supply.	150mA
VREG_L17_2P85	137	O	2.85 V power output, for LCD, C	400mA
VREG_L11_2P95	29	O	TF card power supply pin	500mA
VREG_L12_PX2_2P95	30	O	TF card signal pull-up power supply pin	100mA
VREG_L14_UIM1	110	O	UIM power supply pins	50mA
VREG_L15_UIM2	91	O	UIM power supply pins	50mA
VREG_L22_2P8_AVDD	136	O	Camera AVDD	300mA
VREG_L2_1P1	199	O	Main Camera DVDD	300mA
VREG_L23_1P2_DVDD	200	O	Secondary camera DVDD	300mA
GND	1、3、10、23、28、38、39、48、57、68、70、81、83、92、94、101、103、111、116、119、121、135、144、147、150、154、155、156、160、161、170、175、180、181、210、211、213、214、215、216、218、220、222、223、224、252、257、272		GND	

Main display interface (MIPI)				
MIPI_DSI0_CLK_N	64	O	MIPI_LCD clock	
MIPI_DSI0_CLK_P	65	O		
MIPI_DSI0_LANE0_N	189	I/O	MIPI_LCD data	
MIPI_DSI0_LANE0_P	190	I/O		
MIPI_DSI0_LANE1_N	66	I/O		
MIPI_DSI0_LANE1_P	67	I/O		
MIPI_DSI0_LANE3_N	73	I/O		
MIPI_DSI0_LANE3_P	74	I/O		
MIPI_DSI0_LANE2_N	71	I/O		
MIPI_DSI0_LANE2_P	72	I/O		
GPIO61_LCD_RST_N	75	O	LCD reset	
GPIO24_LCD_TE0	76	I/O	LCD frame sync signal	
The main display backlight interface				
LCD_BL_LED_K1	5	AI	LCD Series backlight negative1	Each normal 20mA， max 30mA
LCD_BL_LED_K2	6	AI	LCD Series backlight negative2	
LCD_BL_LED_A	7	PO	LCD Series backlight positive	
Sub display interface (MIPI)				
MIPI_DSI1_CLK_N	242	O	MIPI_LCD2 clock	
MIPI_DSI1_CLK_P	241	O		
MIPI_DSI1_LANE0_N	226	I/O	MIPI_LCD2 data	
MIPI_DSI1_LANE0_P	225	I/O		
MIPI_DSI1_LANE1_N	240	I/O		
MIPI_DSI1_LANE1_P	239	I/O		
MIPI_DSI1_LANE2_N	244	I/O		
MIPI_DSI1_LANE2_P	243	I/O		
MIPI_DSI1_LANE3_N	246	I/O		
MIPI_DSI1_LANE3_P	245	I/O		
GPIO63_LCD2_RST_N	99	O	LCD2 reset	
GPIO25_LCD_TE1	77	I/O	LCD2 frame sync signal	
UART(1.8V)				
UART2_MSM_TX	11	I	UART2 data transmit	
UART2_MSM_RX	12	O	UART2 data receive	
GPIO13_UART4_RX	16	O	UART4 data receive	
GPIO12_UART4_TX	15	I	UART4 data transmit	
GPIO17_UART5_RX	255	O	UART5 data receive	

GPIO16_UART5_TX	256	I	UART5 data transmit	
GPIO21_UART6_RX	177	I	UART6 data receive	
GPIO20_UART6_TX	176	O	UART6 data transmit	
UIM card Interface				
UIM1_DET	106	I	UIM1 insert detect	
UIM1_RESET	107	O	UIM1 reset	
UIM1_CLK	108	O	UIM1 clock	
UIM1_DATA	109	I/O	UIM1 data	
UIM2_DET	87	I	UIM2 insert detect	
UIM2_RESET	88	O	UIM2 reset	
UIM2_CLK	89	O	UIM2 clock	
UIM2_DATA	90	I/O	UIM2 data	
Front Camera				
MIPI_CSI2_CLK_P	40	I	Front Camera MIPI clock	
MIPI_CSI2_CLK_N	41	I		
MIPI_CSI2_LANE0_P	42	I	Front Camera MIPI data	
MIPI_CSI2_LANE0_N	43	I		
MIPI_CSI2_LANE1_P	191	I		
MIPI_CSI2_LANE1_N	192	I		
MIPI_CSI2_LANE2_P	46	I		
MIPI_CSI2_LANE2_N	47	I		
MIPI_CSI2_LANE3_P	44	I		
MIPI_CSI2_LANE3_N	45	I		
GPIO27_SCAM_MCLK	80	I/O	Front Camera main clock	
GPIO129_SCAM_RST_N	79	I/O	Front Camera reset	
GPIO130_SCAM_PWD_N	78	I/O	Front Camera dormancy	
Rear Camera				
MIPI_CSI0_CLK_N	50	I	Rear Camera MIPI clock	
MIPI_CSI0_CLK_P	49	I		
MIPI_CSI0_LANE0_N	56	I	Rear Camera MIPI data	
MIPI_CSI0_LANE0_P	55	I		
MIPI_CSI0_LANE1_N	194	I		
MIPI_CSI0_LANE1_P	193	I		
MIPI_CSI0_LANE2_N	52	I		
MIPI_CSI0_LANE2_P	51	I		
MIPI_CSI0_LANE3_N	54	I		

MIPI_CSI0_LANE3_P	53	I		
GPIO26_MCAM_MCLK	84	I/O	Rear Camera main clock	
GPIO40_MCAM_RST_N	85	I/O	Rear Camera reset	
GPIO39_MCAM_PWD_N	86	I/O	Rear Camera dormancy	
Depth Camera				
MIPI_CSI1_CLK_N	207	I	Depth Camera clock	
MIPI_CSI1_CLK_P	208	I		
MIPI_CSI1_LANE0_N	63	I	Depth Camera MIPI data	
MIPI_CSI1_LANE0_P	62	I		
MIPI_CSI1_LANE1_N	59	I		
MIPI_CSI1_LANE1_P	58	I		
MIPI_CSI1_LANE2_N	172	I		
MIPI_CSI1_LANE2_P	171	I		
MIPI_CSI1_LANE3_N	61	I		
MIPI_CSI1_LANE3_P	60	I		
GPIO132_DCAM_PWD_N	262	I/O	Depth Camera dormancy	
GPIO131_DCAM_RST_N	263	I/O	Depth Camera reset	
GPIO28_CAM_MCLK2	264	I/O	Depth Camera main clock	
Audio Interface				
MIC_IN1_M	123	I	The main MIC negative	
MIC_IN1_P	122	I	The main MIC positive	
MIC_IN2_P	132	I	Headphone MIC positive	
GND_MIC	124	I	Headphone MIC、Noise reduction MIC negative	
MIC_IN3_P	131	I	Noise reduction MIC positive	
MIC_BIAS1	118	O	The BIAS voltage of main MIC is used in the design of silicon wheat	
MIC_BIAS2	117	O	The BIAS voltage of the earphone MIC is used in the design of silicon wheat	
CDC_HPH_R	128	O	Right channel of earphone	
CDC_HPH_L	126	O	Left channel of earphone	
CDC_HS_DET	125	I	Headphone plug and unplug detection	
CDC_HPH_REF	127	I	Earphone reference GND	
CDC_EAR_M	129	O	Earpiece output negative	
CDC_EAR_P	130	O	Earpiece output positive	
SPKR_DRV_M	133	O	Power amplifier (0.85 W) output negative	Class_D

SPKR_DRV_P	134	O	Power amplifier (0.85 W) output positive	Class_D
SD card Interface				
GPIO133_SDCARD_DET_N	31	I/O	SD card insertion detection	
SDC2_SDCARD_CMD	36	I/O	SD CMD	
SDC2_SDCARD_CLK	37	I/O	SD clock	
SDC2_SDCARD_D0	32	I/O	SD data	
SDC2_SDCARD_D1	33	I/O		
SDC2_SDCARD_D2	34	I/O		
SDC2_SDCARD_D3	35	I/O		
I2C				
CAM_I2C_SDA0	105	I/O	Special I2C signal can only be used for CAM	Pullup to VREG_L6_1P8
CAM_I2C_SCL0	104	I/O		
GPIO14_SENSOR_I2C4_SDA	17	I/O	Special I2C signal can only be used for SENSOR	
GPIO15_SENSOR_I2C4_SCL	18	I/O		
GPIO6_I2C2_SDA	13	I/O	Universal I2C signal	
GPIO7_I2C2_SCL	14	I/O		
CAM_I2C_SDA1	96	I/O	Special I2C signal can only be used for CAM	
CAM_I2C_SCL1	95	I/O		
GPIO18_NFC_I2C5_SDA	254	I/O	Universal I2C signal, which is used by default for NFC	Pullup to VREG_L5_1P8
GPIO19_NFC_I2C5_SCL	253	I/O		
TP				
GPIO10_TP_I2C3_SDA	234	I/O	I2C data	Pullup to VREG_L5_1P8
GPIO11_TP_I2C3_SCL	233	I/O	I2Cclock	
GPIO65_TP_INT_N	97	I	TP interrupt	
GPIO64_TP_RST_N	98	O	TP reset	
USB				
USB_HS_D_M	145	I/O	USB DM	
USB_HS_D_P	146	I/O	USB DP	
USB_ID	143	I	USB ID	
Antenna interface				
RF_MAIN	120	I/O	The main antenna	
RF_WIFI/BT	82	I/O	WIFI/BT antenna	
RF_DIV	102	I	Diversity antenna	
RF_GPS	93	I	GPS antenna	
5G_ANT	69	I/O	5GWIFI antenna	

GPIOand default function				
GPIO0_SPI_MOSI	261	O	The default configuration is the SPI interface	
GPIO1_SPI_MISO	260	O		
GPIO2_SPI1_CS	259	I		
GPIO3_SPI1_CLK	258	O		
GPIO8	232	I/O	Generic GPIO, without default configuration	
GPIO9	231	I/O	Generic GPIO, without default configuration	
GPIO33	166	I/O	Generic GPIO, without default configuration	
GPIO35	167	I/O	Generic GPIO, without default configuration	
GPIO36	168	I/O	Generic GPIO, without default configuration	
GPIO38	251	I/O	The default configuration is the gyroscope interrupt signal.	
GPIO42_ACCL_INT1	19	I/O	The default configuration is G-sensor interrupt	
GPIO43_ALSP_INT_N	20	I/O	The default configuration is Ps-sensor interrupt signal	
GPIO44_MAG_INT	21	I/O	The default configuration is the compass interrupt signal.	
GPIO45_GYRO_INT	22	I/O	The default configuration is the gyroscope interrupt signal.	
GPIO46_PRESSURE_INT	221	I/O	The default configuration is the pressure sensor interrupt signal	
GPIO47	235	I/O	Generic GPIO, without default configuration	
GPIO48_FP_INT_N	270	I/O	The default configuration is the interrupt signal for fingerprint recognition.	
GPIO59	100	I/O	General purpose GPIO, no default configuration	
GPIO63	99	I/O	General purpose GPIO, no default configuration	
GPIO66	212	I/O	General purpose GPIO, no default configuration	
GPIO85_KEY1_VOL+	24	I/O	Control volume increase	
GPIO86_KEY2_SNAPSHOT	25	I/O	The default configuration is the button	
GPIO87_KEY3_FOCUS	26	I/O	The default configuration is the button	
GPIO88_KEY4_HOME	27	I/O	HOME key，Compatible with MI2S_1_D1	
GPIO89_DMIC0_CLK	204	I/O	General purpose GPIO, no default configuration	
GPIO90_DMIC0_DATA	205	I/O	General purpose GPIO, no default configuration	
GPIO96_WSA_EN	197	I/O	The default configuration is AUDIO enable signal	

GPIO128	249	I/O	General purpose GPIO, no default configuration	
GPIO138_FP_SPI_MISO	266	O	The default configuration is SPI interface for fingerprint recognition.	
GPIO137_FP_SPI_MOSI	267	O		
GPIO136_FP_SPI_CS	268	I		
GPIO135_FP_SPI_CLK	269	O		
Other functional pin				
FORCE_USB_BOOT	206	I	Pull up to 1.8 V (VREG_L5_1P8) into the emergency download mode	
FLASH_LED1+	2	O	Flashlight positive, 1A output	
CHG_LED	182	I	The charging indicator light negative	
PMI_HAP_OUT_N	8	O	motor output negative	
PMI_HAP_OUT_P	9	O	motor output positive	
BAT_THERM	149	I	Battery temperature detection, the battery NTC terminal (battery terminal NTC resistance is 10K), such as no battery temperature detection requirement, need to increase 10K resistance to GND.	
PMI8952_MPP1	4	I/O	Analog voltage input/output can be used as PWM output or ADC input	
PM8953_MPP2	112	I/O	Analog voltage input/output can be used as PWM output or ADC input	
PM8953_MPP4	209	I/O	Analog voltage input/output can be used as PWM output or ADC input	
KYPD_PWR_N1	142	I/O	Power key	
PM_RESIN_N1	141	I/O	Reset key, android device for volume reduction	
LCD_BL_LED_A	7	O	LCD Backlight anode	
LCD_BL_LED_K1	5	I	LCD Backlight cathode1	
LCD_BL_LED_K2	6	I	LCD Backlight cathode2	

Table 3.2: Pin Characteristics

PIN #	SLM758 Pin name	GPIO Interrupt	Pad characteristics	Functional description
1	GND		GND	GND

2	FLASH_LED1+		AO	FLASH LED anode(1A)
3	GND		GND	GND
4	PMI8952_MPP1		AO-Z,AI,DO	Configurable MPP,PWM,ADC
5	LCD_BL_LED_K1		AI	LCD Backlight cathode1(20mA)
6	LCD_BL_LED_K2		AI	LCD Backlight cathode2(20mA)
7	LCD_BL_LED_A		PO	LCD Backlight anode
8	PMI_HAP_OUT_N		AO	Haptics driver output negative
9	PMI_HAP_OUT_P		AO	Haptics driver output positive
10	GND		GND	GND
11	UART2_MSM_TX	GPIO_4	B-PD:nppukp	Configurable I/O,UART2 TX
12	UART2_MSM_RX	GPIO_5*	B-PD:nppukp	Configurable I/O,UART2 RX
13	GPIO6_I2C2_SDA	GPIO_6	B-PD:nppukp	Configurable I/O, I2C SDA
14	GPIO7_I2C2_SCL	GPIO_7	B-PD:nppukp	Configurable I/O, I2C SCL
15	GPIO12_UART4_TX	GPIO_12*	B-PD:nppukp	Configurable I/O,UART4 TX
16	GPIO13_UART4_RX	GPIO_13*	B-PD:nppukp	Configurable I/O,UART4 RX
17	GPIO14_SENSOR_I2C4_SDA	GPIO_14	B-PD:nppukp	Configurable I/O,SENSOR I2C SDA
18	GPIO15_SENSOR_I2C4_SCL	GPIO_15	B-PD:nppukp	Configurable I/O, SENSOR I2C SCL
19	GPIO42_ACCL_INT1	GPIO_42*	B-PD:nppukp	Configurable I/O,ACC INT
20	GPIO43_ALSP_INT_N	GPIO_43*	B-PD:nppukp	Configurable I/O,ALSP INT
21	GPIO44_MAG_INT	GPIO_44*	B-PD:nppukp	Configurable I/O,MAG INT
22	GPIO45_GYRO_INT	GPIO_45*	B-PD:nppukp	Configurable I/O,GYRO INT
23	GND		GND	GND
24	GPIO85_KEY1_VOL+	GPIO_85*	B-PD:nppukp	Configurable I/O,KEY VOL+
25	GPIO86_KEY2_SNAPSHOT	GPIO_86*	B-PD:nppukp	Configurable I/O,KEY VOL- or SNAPSHOT
26	GPIO87_KEY3_FOCUS	GPIO_87*	B-PD:nppukp	Configurable I/O,KEY HOME or FOCUS
27	GPIO88_HOMEKEY_MI2S1_D1	GPIO_88	B-PD:nppukp	Configurable I/O,KEY HOME or MI2S1_D1
28	GND		GND	GND
29	VREG_L11_2P95		PO	PMIC output 2.95V for SD-card power
30	VREG_L12_PX2_2P95		PO	PMIC output 2.95V for SDC2 signal
31	GPIO133_SDCARD_DET_N	GPIO_133*	B-PD:nppukp	Configurable I/O,SD card detection
32	SDC2_SDCARD_D0		BH-NP:pdpukp	Secure digital controller 2 data bit 0
33	SDC2_SDCARD_D1		BH-NP:pdpukp	Secure digital controller 2 data bit 1
34	SDC2_SDCARD_D2		BH-NP:pdpukp	Secure digital controller 2 data bit 2

35	SDC2_SDCARD_D3		BH-NP:pdpukp	Secure digital controller 2 data bit 3
36	SDC2_SDCARD_CMD		BH-NP:pdpukp	Secure digital controller 2 command
37	SDC2_SDCARD_CLK		BH-NP:pdpukp	Secure digital controller 2 clock
38	GND		GND	GND
39	GND		GND	GND
40	MIPI_CSI2_CLK_P		AI	MIPI camera serial interface 2 clock+
41	MIPI_CSI2_CLK_N		AI	MIPI camera serial interface 2 clock-
42	MIPI_CSI2_LANE0_P		AI	MIPI camera serial interface 2 lane0+
43	MIPI_CSI2_LANE0_N		AI	MIPI camera serial interface 2 lane0-
44	MIPI_CSI2_LANE3_P		AI	MIPI camera serial interface 2 lane3+
45	MIPI_CSI2_LANE3_N		AI	MIPI camera serial interface 2 lane3-
46	MIPI_CSI2_LANE2_P		AI	MIPI camera serial interface 2 lane2+
47	MIPI_CSI2_LANE2_N		AI	MIPI camera serial interface 2 lane2-
48	GND		GND	GND
49	MIPI_CSI0_CLK_P		AI	MIPI camera serial interface 0 clock+
50	MIPI_CSI0_CLK_N		AI	MIPI camera serial interface 0 clock-
51	MIPI_CSI0_LANE2_P		AI	MIPI camera serial interface 0 lane2+
52	MIPI_CSI0_LANE2_N		AI	MIPI camera serial interface 0 lane2-
53	MIPI_CSI0_LANE3_P		AI	MIPI camera serial interface 0 lane3+
54	MIPI_CSI0_LANE3_N		AI	MIPI camera serial interface 0 lane3-
55	MIPI_CSI0_LANE0_P		AI	MIPI camera serial interface 0 lane0+
56	MIPI_CSI0_LANE0_N		AI	MIPI camera serial interface 0 lane0-
57	GND		GND	GND
58	MIPI_CSI1_LANE1_P		AI	MIPI camera serial interface 1 lane1+
59	MIPI_CSI1_LANE1_N		AI	MIPI camera serial interface 1 lane1-
60	MIPI_CSI1_LANE3_P		AI	MIPI camera serial interface 1 lane3+
61	MIPI_CSI1_LANE3_N		AI	MIPI camera serial interface 1 lane3-
62	MIPI_CSI1_LANE0_P		AI	MIPI camera serial interface 1 lane0+
63	MIPI_CSI1_LANE0_N		AI	MIPI camera serial interface 1 lane0-
64	MIPI_DSI0_CLK_N		AO	MIPI display serial interface 0 clock-
65	MIPI_DSI0_CLK_P		AO	MIPI display serial interface 0 clock+
66	MIPI_DSI0_LANE1_N		AO	MIPI display serial interface 0 lane1-
67	MIPI_DSI0_LANE1_P		AO	MIPI display serial interface 0 lane1+
68	GND		GND	GND
69	5G_ANT		AI	RF signal for 5G WIFI

70	GND		GND	GND
71	MIPI_DSI0_LANE2_N		AO	MIPI display serial interface 0 lane2-
72	MIPI_DSI0_LANE2_P		AO	MIPI display serial interface 0 lane2+
73	MIPI_DSI0_LANE3_N		AO	MIPI display serial interface 0 lane3-
74	MIPI_DSI0_LANE3_P		AO	MIPI display serial interface 0 lane3+
75	GPIO61_LCD_RST_N	GPIO_61*	B-PD:nppukp	Configurable I/O, primary LCD RESET
76	GPIO24_LCD_TE0	GPIO_24	B-PD:nppukp	Configurable I/O, primary LCD TE
77	GPIO25_LCD_TE1	GPIO_25*	B-PD:nppukp	Configurable I/O, secondary LCD TE
78	GPIO130_SCAM_PWD_N	GPIO_130*	B-PD:nppukp	Configurable I/O, front CAM PWDN
79	GPIO129_SCAM_RST_N	GPIO_129*	B-PD:nppukp	Configurable I/O, front CAM RESET
80	GPIO27_CAM_MCLK1		B-PD:nppukp	Configurable I/O, front CAM MCLK
81	GND		GND	GND
82	2.4G_ANT		AI	RF signal for 2.4G WIFI&BT
83	GND		GND	GND
84	GPIO26_CAM_MCLK0	GPIO_26	B-PD:nppukp	Configurable I/O, main CAM MCLK
85	GPIO40_MCAM_RST_N	GPIO_40	B-PD:nppukp	Configurable I/O, main CAM RESET
86	GPIO39_MCAM_PWD_N	GPIO_39	B-PD:nppukp	Configurable I/O, main CAM PWDN
87	GPIO58_UIM2_DET	GPIO_58*	B-PD:nppukp	Configurable I/O,UIM2 removal detection
88	UIM2_RESET		B-PD:nppukp	Configurable I/O,UIM2 reset
89	UIM2_CLK		B-PD:nppukp	Configurable I/O,UIM2 clock
90	UIM2_DATA		B-PD:nppukp	Configurable I/O,UIM2 data
91	VREG_L15_UIM2		PO	PMIC output for UIM2
92	GND		GND	GND
93	GPS_ANT		AI	RF signal for GPS ANT
94	GND		GND	GND
95	CAM_I2C_SCL1	GPIO_32	B-PD:nppukp	Configurable I/O, Dedicated camera I2C1 SCL
96	CAM_I2C_SDA1	GPIO_31*	B-PD:nppukp	Configurable I/O, Dedicated camera I2C1 SDA
97	GPIO65_TP_INT_N	GPIO_65*	B-PD:nppukp	Configurable I/O,TP INT
98	GPIO64_TP_RST_N	GPIO_64	B-PD:nppukp	Configurable I/O,TP RESET
99	GPIO63	GPIO_63*	B-PD:nppukp	Configurable I/O,
100	GPIO59	GPIO_59*	B-PD:nppukp	Configurable I/O,
101	GND		GND	GND
102	DIV_ANT		AI	RF signal for diversity ANT
103	GND		GND	GND

104	CAM_I2C_SCL0		B-PD:nppukp	Configurable I/O, Dedicated camera I2C0 SCL
105	CAM_I2C_SDA0		B-PD:nppukp	Configurable I/O, Dedicated camera I2C0 SDA
106	GPIO54_UIM1_DET	GPIO_54*	B-PD:nppukp	Configurable I/O,UIM1 removal detection
107	UIM1_RESET		B-PD:nppukp	Configurable I/O,UIM1 reset
108	UIM1_CLK		B-PD:nppukp	Configurable I/O,UIM1 clock
109	UIM1_DATA		B-PD:nppukp	Configurable I/O,UIM1 data
110	VREG_L14_UIM1		PO	PMIC output for UIM1
111	GND		GND	GND
112	PM8953_MPP2		AO-Z,DI,DO	Configurable MPP,PWM,ADC
113	VCOIN		AI,AO	Coin-cell battery or backup battery
114	LINEOUT_M		AO	Audio lineout minus for audio PA
115	LINEOUT_P		AO	Audio lineout plus for audio PA
116	GND		GND	GND
117	MIC_BIAS2		AO	Microphone bias #2 for earphone mic
118	MIC_BIAS1		AO	Microphone bias #1
119	GND		GND	GND
120	MAIN_ANT		AI	RF signal for main ANT
121	GND		GND	GND
122	MIC_IN1_P		AI	Microphone 1 input plus
123	MIC_IN1_M		AI	Microphone 1 input minus
124	GND_MIC		GND	Microphone bias filter ground
125	CDC_HS_DET		AI	MBHC mechanical insertion/removal-detection
126	CDC_HPH_L		AO	Headphone output, left channel
127	CDC_HPH_REF		AI	Headphone ground reference
128	CDC_HPH_R		AO	Headphone output, right channel
129	CDC_EAR_M		AO	Earpiece output, minus
130	CDC_EAR_P		AO	Earpiece output, plus
131	MIC_IN3_P		AI	Microphone input 3
132	MIC_IN2_P		AI	Microphone input 2
133	SPKR_DRV_M		AO	Class-D speaker driver output, minus
134	SPKR_DRV_P		AO	Class-D speaker driver output, plus
135	GND		GND	GND
136	VREG_L22_2P8		PO	PMIC output 2.8V for camera AVDD
137	VREG_L17_2P85		PO	PMIC output 2.8V for LCD,CAM,TP

138	VREG_L10_2P8_SENSOR		PO	PMIC output 2.8V for sensor
139	VREG_L6_1P8		PO	PMIC output 1.8V for LCD,CAM,TP, sensor
140	VREG_L5_1P8		PO	PMIC output 1.8V for digital I/Os
141	PM_RESIN_N1		DI	KEY VOL-(default) or RESET
142	KYPD_PWR_N1		DI	KEY POWER ON/OFF
143	USB_ID		AI	USB ID
144	GND		GND	GND
145	USB_HS_D_M		AI,AO	USB data minus
146	USB_HS_D_P		AI,AO	USB data plus
147	GND		GND	GND
148	BAT_CON_ID		AI	Battery ID input to ADC
149	BAT_THERM		AI	Battery temperature input to ADC
150	GND		GND	GND
151	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
152	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
153	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
154	GND		GND	GND
155	GND		GND	GND
156	GND		GND	GND
157	VBUS		PI,PO	USB Voltage
158	VBUS		PI,PO	USB Voltage
159	VBUS		PI,PO	USB Voltage
160	GND		GND	GND
161	GND		GND	GND
162	Reserved			Reserved
163	Reserved			Reserved
164	GPIO98_I2C8_SDA	GPIO_98	B-PD:nppukp	Configurable I/O, I2C SDA
165	GPIO99_I2C8_SCL	GPIO_99	B-PD:nppukp	Configurable I/O, I2C SCL
166	GPIO33	GPIO_33	B-PD:nppukp	Configurable I/O
167	GPIO35	GPIO_35*	B-PD:nppukp	Configurable I/O
168	GPIO36	GPIO_36*	B-PD:nppukp	Configurable I/O
169	GPIO91_MI2S_1_SCK	GPIO_91*	B-PD:nppukp	Configurable I/O,MI2S1_SCK
170	GND		GND	GND
171	MIPI_CSI1_LANE2_P		AI	MIPI camera serial interface 1 lane2+
172	MIPI_CSI1_LANE2_N		AI	MIPI camera serial interface 1 lane2-

173	USB3_SS_RX_M		AI	USB super-speed receive – minus
174	USB3_SS_RX_P		AI	USB super-speed receive – plus
175	GND		GND	GND
176	GPIO20_UART6_TX	GPIO_20	B-PD:nppukp	Configurable I/O,UART6 TX
177	GPIO21_UART6_RX	GPIO_21*	B-PD:nppukp	Configurable I/O,UART6 RX
178	Reserved			Reserved
179	Reserved			Reserved
180	GND		GND	GND
181	GND		GND	GND
182	CHG_LED		AO	Current sink for charging indication
183	Reserved			Reserved
184	GPIO22_I2C6_SDA	GPIO_22	B-PD:nppukp	Configurable I/O, I2C SDA
185	GPIO23_I2C6_SCL	GPIO_23	B-PD:nppukp	Configurable I/O, I2C SCL
186	USB3_SS_TX_P		AO	USB super-speed transmit – plus
187	USB3_SS_TX_M		AO	USB super-speed transmit – minus
188	GPIO139_USB_SS_SEL	GPIO_139	B-PD:nppukp	Configurable I/O, USB Type C switch control
189	MIPI_DSI0_LANE0_N		AO	MIPI display serial interface 0 lane0-
190	MIPI_DSI0_LANE0_P		AO	MIPI display serial interface 0 lane0+
191	MIPI_CSI2_LANE1_P		AI	MIPI camera serial interface 2 lane1+
192	MIPI_CSI2_LANE1_N		AI	MIPI camera serial interface 2 lane1-
193	MIPI_CSI0_LANE1_P		AI	MIPI camera serial interface 0 lane1+
194	MIPI_CSI0_LANE1_N		AI	MIPI camera serial interface 0 lane1-
195	GPIO94	GPIO_94	B-PD:nppukp	Configurable I/O
196	GPIO95	GPIO_95	B-PD:nppukp	Configurable I/O
197	GPIO96	GPIO_96	B-PD:nppukp	Configurable I/O
198	GPIO97	GPIO_97*	B-PD:nppukp	Configurable I/O
199	VREG_L2_1P1		PO	PMIC output 1.1V for main camera DVDD
200	VREG_L23_1P175		PO	PMIC output 1.175V for front camera DVDD
201	USB_CC1		AI;AO	USB type C connector configuration channel1
202	USB_CC2		AI;AO	USB type C connector configuration channel2
203	CBL_PWR_N1		DI	Cable power-on; initiates power on when grounded
204	GPIO89	GPIO_89	B-PD:nppukp	Configurable I/O
205	GPIO90	GPIO_90*	B-PD:nppukp	Configurable I/O
206	FORCE_USB_BOOT		DI	pullup with VREG_L5 to forced USB

				boot
207	MIPI_CSI1_CLK_N		AI	MIPI camera serial interface 1 clock-
208	MIPI_CSI1_CLK_P		AI	MIPI camera serial interface 1 clock-
209	PM8953_MPP4		AO-Z,DI,DO	Configurable MPP,PWM,ADC
210	GND		GND	GND
211	GND		GND	GND
212	GPIO66	GPIO_66	B-PD:nppukp	Configurable I/O
213	GND		GND	GND
214	GND		GND	GND
215	GND		GND	GND
216	GND		GND	GND
217	VREG_L13_3P075		PO	PMIC output 3.075V for audio codec
218	GND		GND	GND
219	VREG_S4_2P05		PO	PMIC output 2.05V for audio codec
220	GND		GND	GND
221	GPIO46_PRESSURE_INT	GPIO_46*	B-PD:nppukp	Configurable I/O, Pressure INT
222	GND		GND	GND
223	GND		GND	GND
224	GND		GND	GND
225	MIPI_DSI1_LANE0_P		AO	MIPI display serial interface 1 lane0+
226	MIPI_DSI1_LANE0_N		AO	MIPI display serial interface 1 lane0-
227	Reserved （WCD_RF_PA_ON）			Reserved
228	GPIO50	GPIO_50	B-PD:nppukp	Configurable I/O, WCD_ELDO_EN
229	Reserved （WCD_MSM_MCLK）			Reserved
230	Reserved （WCD_RST_N）			Reserved
231	GPIO9	GPIO_9*	B-PD:nppukp	Configurable I/O,
232	GPIO8	GPIO_8	B-PD:nppukp	Configurable I/O,
233	GPIO11_TP_I2C3_SCL	GPIO_11	B-PD:nppukp	Configurable I/O, CTP I2C SCL
234	GPIO10_TP_I2C3_SDA	GPIO_10	B-PD:nppukp	Configurable I/O, CTP I2C SDA
235	GPIO47	GPIO_47	B-PD:nppukp	Configurable I/O,
236	Reserved （SLIMBUS_DATA1）			Reserved
237	Reserved （SLIMBUS_DATA0）			Reserved
238	Reserved （SLIMBUS_CLK）			Reserved

239	MIPI_DSI1_LANE1_P		AO	MIPI display serial interface 1 lane1+
240	MIPI_DSI1_LANE1_N		AO	MIPI display serial interface 1 lane1-
241	MIPI_DSI1_CLK_P		AO	MIPI display serial interface 1 clock+
242	MIPI_DSI1_CLK_N		AO	MIPI display serial interface 1 clock-
243	MIPI_DSI1_LANE2_P		AO	MIPI display serial interface 1 lane2+
244	MIPI_DSI1_LANE2_N		AO	MIPI display serial interface 1 lane2-
245	MIPI_DSI1_LANE3_P		AO	MIPI display serial interface 1 lane3+
246	MIPI_DSI1_LANE3_N		AO	MIPI display serial interface 1 lane3-
247	Reserved（WCD_INTR2）			Reserved
248	Reserved （WCD_INTR1）			Reserved
249	GPIO128	GPIO_128	B-PD:nppukp	Configurable I/O,
250	Reserved			Reserved
251	GPIO38	GPIO_38*	B-PD:nppukp	Configurable I/O,
252	GND		GND	GND
253	GPIO19_NFC_I2C5_SCL	GPIO_19	B-PD:nppukp	Configurable I/O,NFC I2C SCL
254	GPIO18_NFC_I2C5_SDA	GPIO_18	B-PD:nppukp	Configurable I/O, NFC I2C SDA
255	GPIO17_UART5_RX	GPIO_17*	B-PD:nppukp	Configurable I/O,UART5 RX
256	GPIO16_UART5_TX	GPIO_16	B-PD:nppukp	Configurable I/O,UART5 TX
257	GND		GND	GND
258	GPIO3_SPI1_CLK	GPIO_3	B-PD:nppukp	Configurable I/O, SPI CLK
259	GPIO2_SPI1_CS	GPIO_2	B-PD:nppukp	Configurable I/O, SPI CS
260	GPIO1_SPI_MISO	GPIO_1*	B-PD:nppukp	Configurable I/O, SPI MISO
261	GPIO0_SPI_MOSI	GPIO_0	B-PD:nppukp	Configurable I/O, SPI MOSI
262	GPIO132_DCAM_PWD_N	GPIO_132*	B-PD:nppukp	Configurable I/O, Depth camera pwdn
263	GPIO131_DCAM_RST_N	GPIO_131*	B-PD:nppukp	Configurable I/O, Depth camera reset
264	GPIO28_CAM_MCLK2	GPIO_28*	B-PD:nppukp	Configurable I/O, Depth camera MCLK
265	GPIO93_MI2S_1_D0	GPIO_93*	B-PD:nppukp	Configurable I/O, MI2S1_D0
266	GPIO138_FP_SPI_MISO	GPIO_138	B-PD:nppukp	Configurable I/O, fingerprint SPI MISO，MI2S_2_D1
267	GPIO137_FP_SPI_MOSI	GPIO_137*	B-PD:nppukp	Configurable I/O, fingerprint SPI MOSI，MI2S_2_D0
268	GPIO136_FP_SPI_CS	GPIO_136	B-PD:nppukp	Configurable I/O, fingerprint SPI CS，MI2S_2_WS
269	GPIO135_FP_SPI_CLK	GPIO_135	B-PD:nppukp	Configurable I/O, fingerprint SPI CLK，MI2S_2_SCK
270	GPIO48_FP_INT_N	GPIO_48*	B-PD:nppukp	Configurable I/O, fingerprint INT
271	GPIO92_MI2S_1_WS	GPIO_92	B-PD:nppukp	Configurable I/O, MI2S1_WS
272	GND		GND	GND

*：Wake-up system interrupt pin

B：Bidirectionaldigital with CMOS input

H：High-voltage tolerant

NP：pdpukp=defaultno-pull with programmable options following the colon (:)

PD：nppukp=defaultpulldown with programmable options following the colon (:)

PU：nppdkp=defaultpullup with programmable options following the colon (:)

KP：nppdpu=defaultkeeper with programmable options following the colon (:)

3.3. Mechanical Dimensions

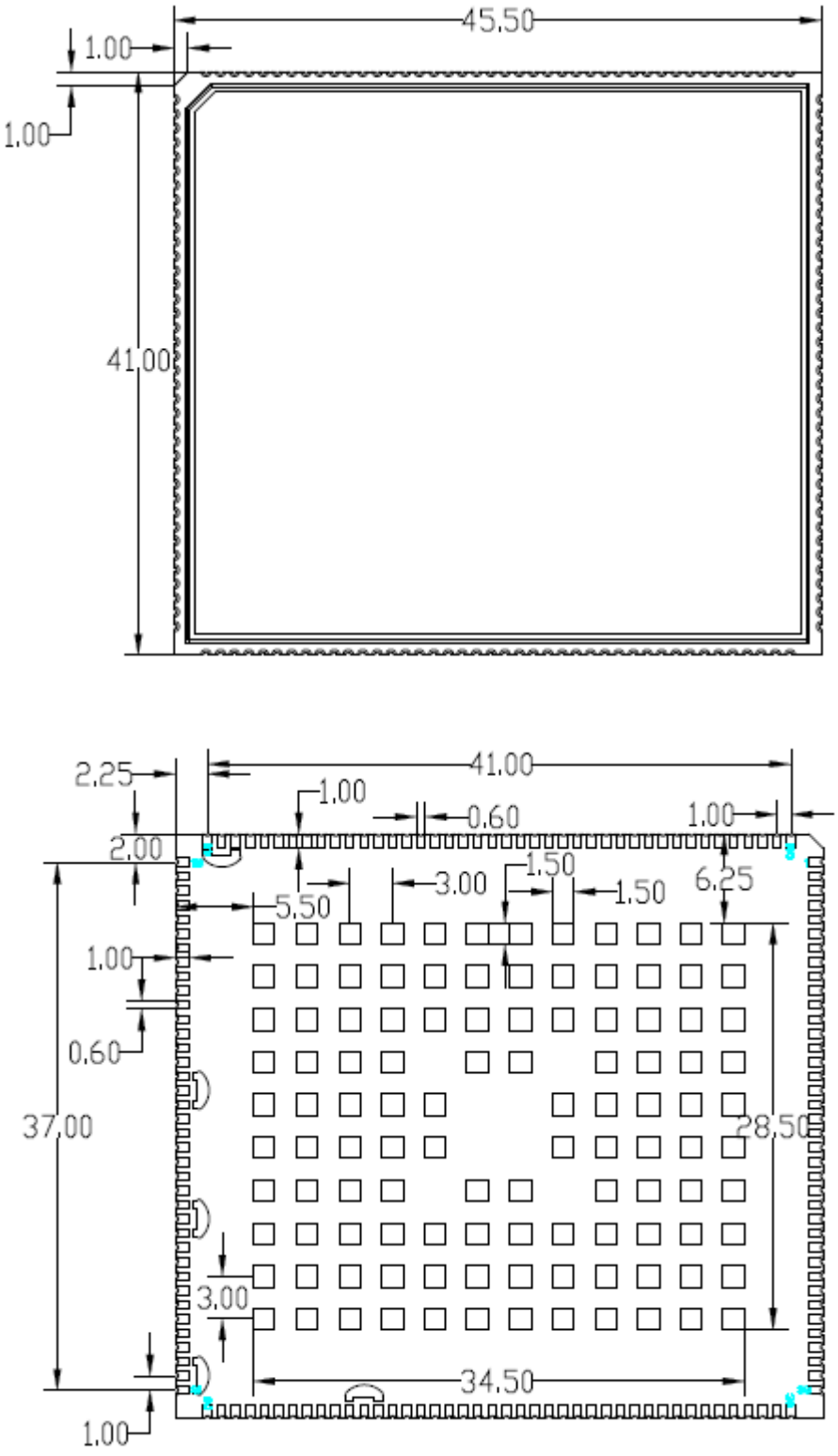


Figure 3.2：Module 3D size（unit： mm）

4. Interface application

4.1. Power Supply

In the case of a battery device, the voltage input range of the module VBAT is 3.4V to 4.2V, and the recommended voltage is 3.8V. In the GSM band, when the module is transmitting at maximum power, the peak current can reach up to 3A, resulting in a large voltage drop on VBAT.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to use a suitable TVS tube and a 5.6V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.7V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

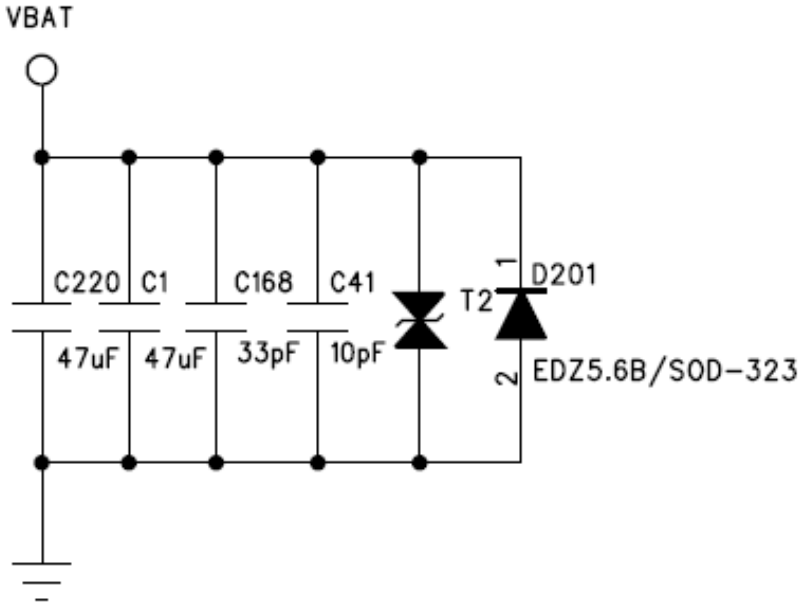


Figure 4.1： VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 5V-12V. The recommended circuit that can be powered by DC-DC is shown below:

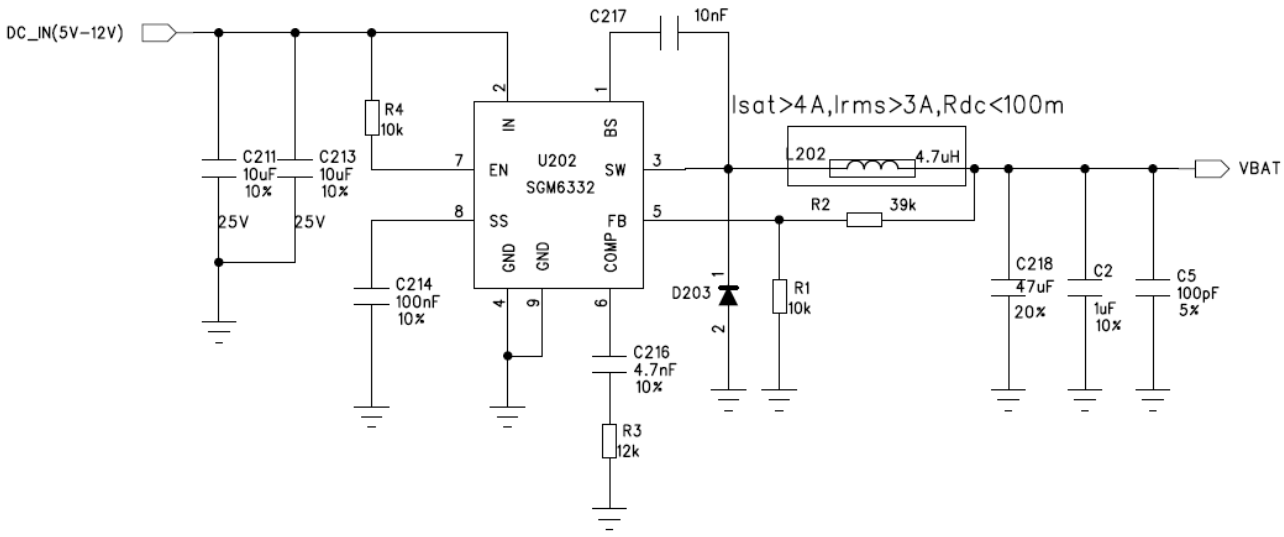


Figure 4.2：DC-DC power supply circuit

Note：If the user does not use battery power, please note that a 10K resistor is connected to the 149 pin (BAT_THERM) of the module and pulled down to GND to prevent the software from judging the abnormal battery temperature after the module is turned on, resulting in shutdown. The connection diagram is as follows:

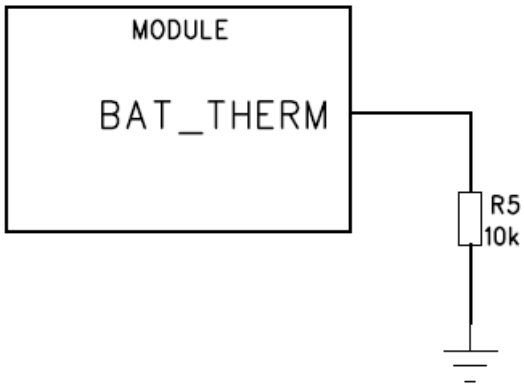


Figure 4.3：Connection diagram when not powered by battery

4.1.1. Power Pin

The VBAT pin (151, 152, 153) is used for power input. In the user's design, pay special

attention to the design of the power supply section to ensure that the VBAT does not fall below 3.4V even when the module consumes 2A. If the voltage drops below 3.4V, the module may shut down. The PCB layout from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

Figure4.4：VBAT lowest voltage drop

4.2. Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In extreme cases, such operations can cause permanent damage to the module.

4.2.1. Module Boot

The user can power on the module by pulling the KYPD_PWR_N1 pin (142) low. The pull-down time is at least 5 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows; or the CBL_PWR_N pin (203) is pulled low. CBL_PWR_N can be powered on by 10K pull-down resistor to GND. It does not need to release this signal after booting.

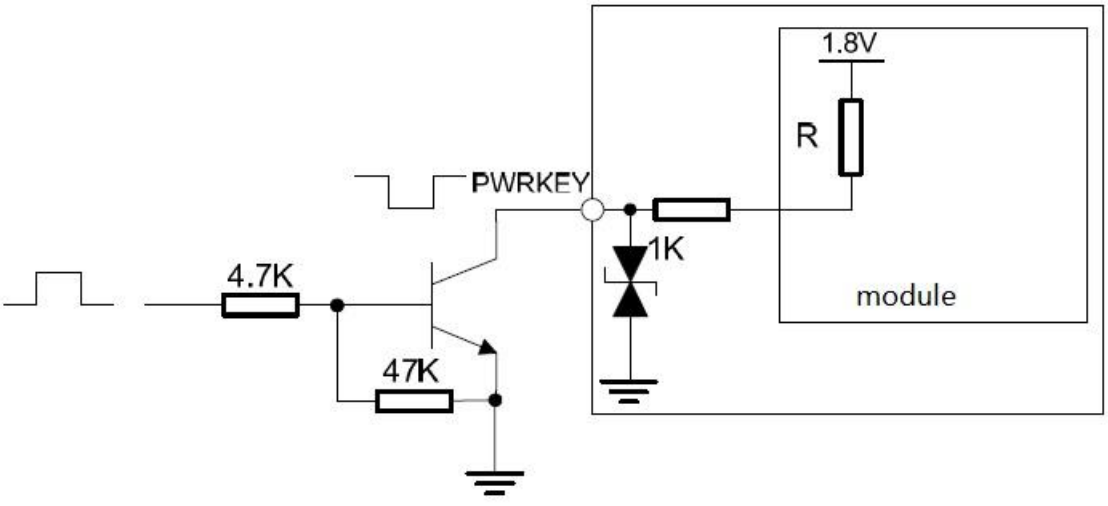


Figure 4.5：Using an external signal to drive the module to boot

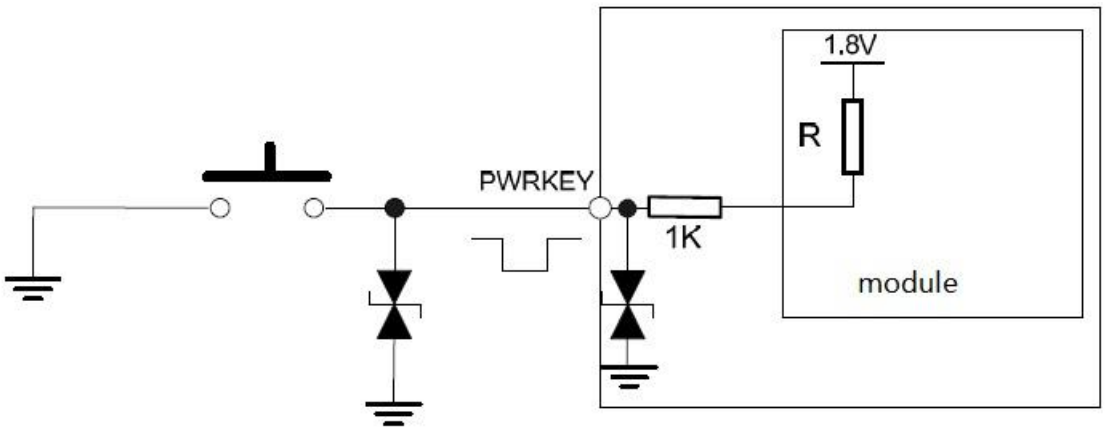


Figure 4.6：Booting with the button circuit

The following figure is the boot timing description:

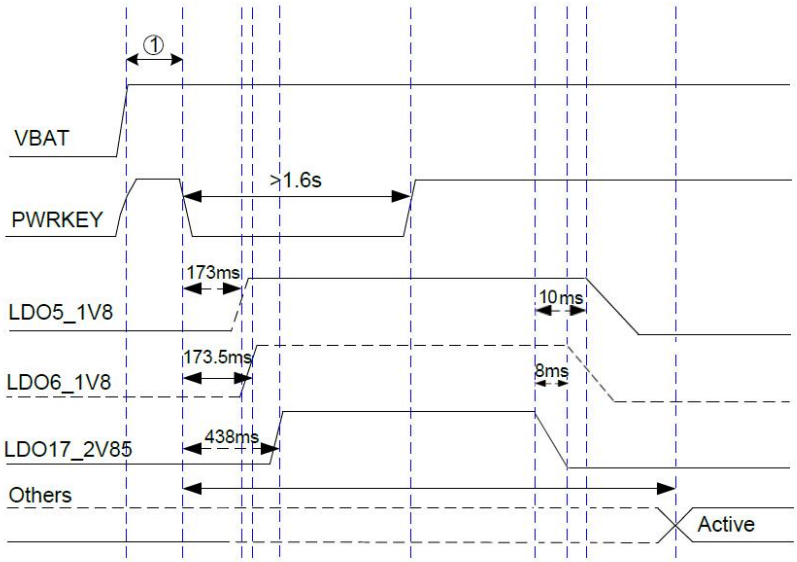


Figure 4.7：Using PWRKEY boot timing diagram

4.2.2. Module Shutdown

Users can use the PWRKEY pin to shutdown.

4.2.2.1 PWRKEY Shutdown

The user can turn off the PWRKEY signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the boot circuit. After the module detects the shutdown action, a prompt window pops up on the screen to confirm whether to perform the shutdown action.

The user can achieve a forced shutdown by pulling PWRKEY down for a long time, pulling down for at least 15 seconds.

4.2.3.Module Reset

The SLM758 module supports a reset function that allows the user to quickly restart the module by pulling the RESET pin of the module low. The recommended circuit is as follows:

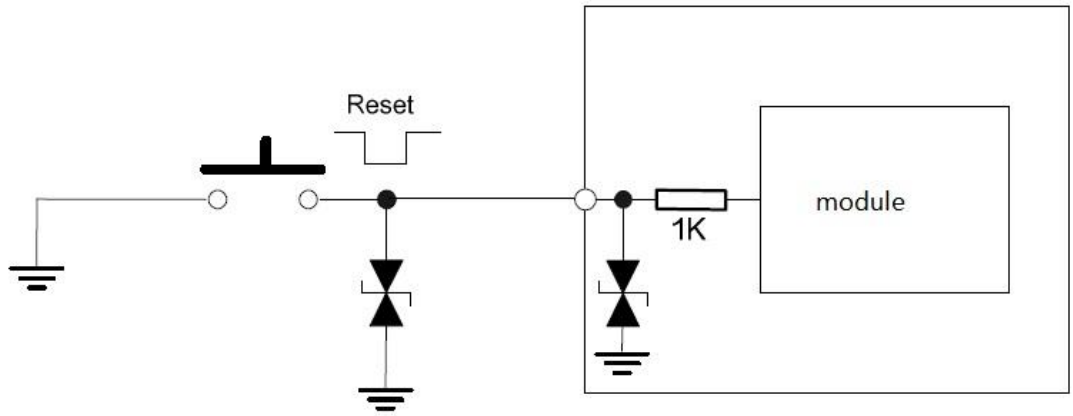


Figure 4.8：Reset using the key circuit

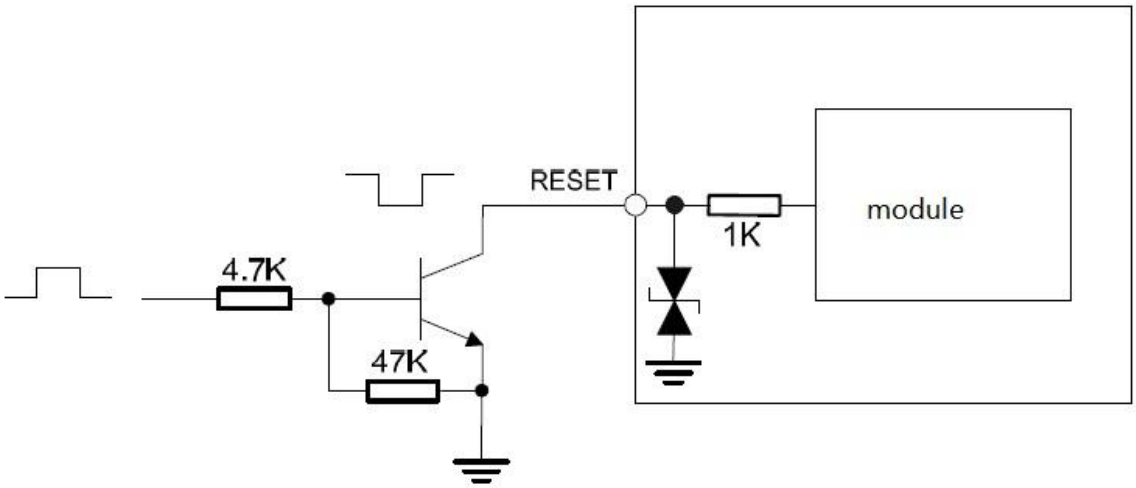


Figure 4.9： Reset Module Using External Signal

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or

3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET can refer to the following table:

Table 4.1：RESET Hardware Parameters

Pin	Description	Minimum	Typical	Maximum	Unit
RESET	Input high level	1	-	-	V
	Input low level	-	-	0.65	V
	Pull down effective time	500		-	ms

4.3. VCOIN Power

When VBAT is disconnected, the user needs to save the real-time clock. The VCOIN pin cannot be left floating. It should be connected to a large capacitor or battery. When external capacitor is connected, the recommended value is 100uF, and the real-time clock can be kept for 1 minute. The reference design circuit is used when the RTC power supply uses an external large capacitor or battery to power the RTC inside the module:

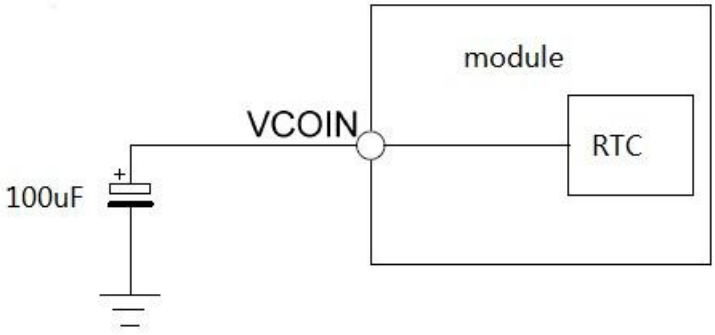


Figure 4.10：External Capacitor Powering the RTC

Non-rechargeable battery powered:

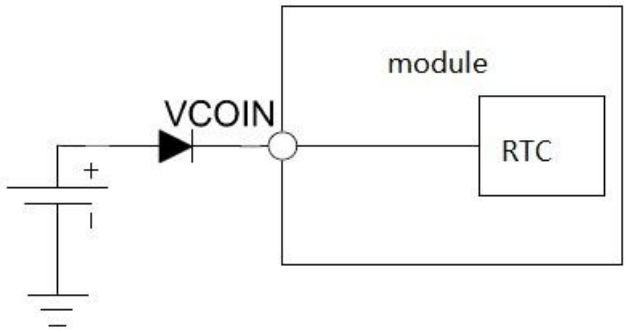


Figure 4.11：Non-rechargeable battery to power the RTC

Rechargeable battery powered:

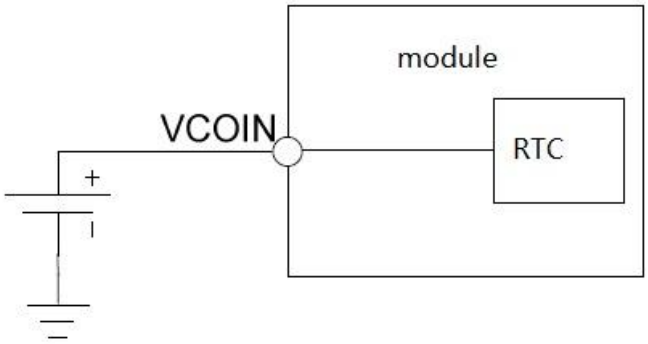


Figure 4.12： Rechargeable Battery Powers RTC

This VCOIN power supply is typically 3.0V and consumes approximately 3uA when VBAT is disconnected.

4.4. Power Output

The SLM758 has multiple power outputs. For LCD, Camera, touch panel, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high frequency interference.

Table 4.2：Power Description

Signal	Programmable Range（V）	Default Voltage(V)	Drive Current(mA)
VREG_L2_1P1	0.375~1.5375	1.2	
VREG_L5_1P8	1.75~3.337	1.80	500
VREG_L6_1P8	1.75~3.337-	1.80	300
VREG_L11_SDC	1.75~3.337	2.95	500
VREG_L12_SDC	1.75~3.337	1.8	100
VREG_L14_UIM1	1.75~3.337	1.8/3.3	50
VREG_L15_UIM2	1.75~3.337	1.8/3.3	50
VREG_L10_2P8_SENSOR	1.75~3.337	2.8	150
VREG_L17_2P85	1.75~3.337	2.85	600
VREG_L18_2P7	1.75~3.337	2.70	150
VREG_L22_2P8_AVDD	1.75~3.337	2.8	300
VREG_L23_1P175	0.375-1.5375	1.3	300

4.5. Serial Port

The SLM758 provides four serial ports for communication. And corresponding to three groups of I2C interfaces can be multiplexed into hardware flow control, note that the I2C interface can not be added to the UART_RTS/CTS when the pull resistor can be added.

Table 4.3：UART Pin Description

Name	Pin	Direction	Function
UART2_MSM_TX	11	I	UART2 Data Transmission
UART2_MSM_RX	12	O	UART2 Data Reception
GPIO6_I2C2_SDA	13	I	UART2 Clear To Send（CTS）
GPIO7_I2C2_SCL	14	O	UART2 Request To Send（RTS）
GPIO12_UART4_TX	15	I	UART4 Data Transmission
GPIO13_UART4_RX	16	O	UART4 Data Reception
GPIO14_SENSOR_I2C4_SDA	17	I	UART4 Clear To Send（CTS）
GPIO15_SENSOR_I2C4_SCL	18	O	UART4 Request To Send（RTS）
GPIO16_UART5_TX	256	I	UART5 Data Transmission
GPIO17_UART5_RX	255	O	UART5 Data Reception
GPIO18_NFC_I2C5_SDA	254	I	UART5 Clear To Send（CTS）
GPIO19_NFC_I2C5_SCL	253	O	UART5 Request To Send（RTS）
GPIO20_UART6_TX	176	O	UART6 Data Transmission
GPIO21_UART6_RX	177	I	UART6 Data Reception
GPIO22_I2C6_SDA	184	I	UART6 Clear To Send（CTS）
GPIO23_I2C6_SCL	185	O	UART6 Request To Send（RTS）

Please refer to the following connection method:

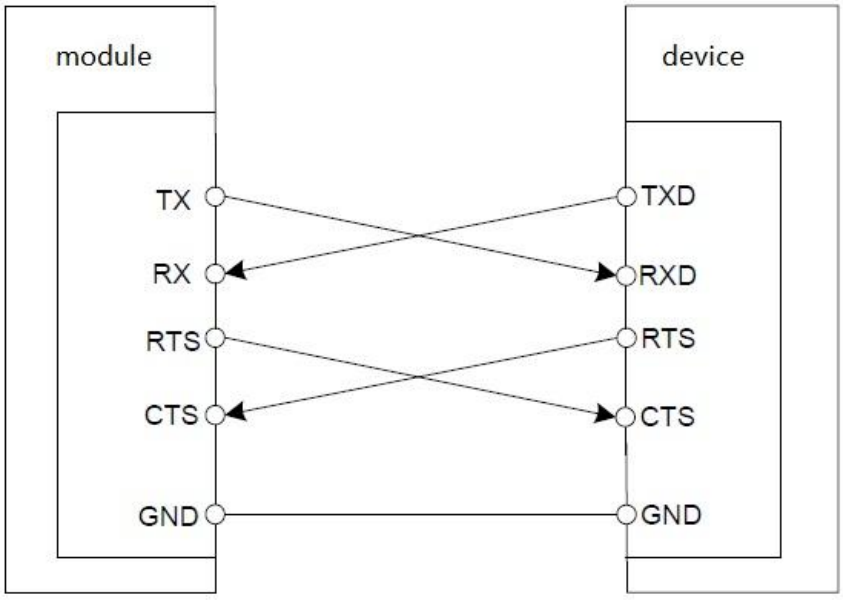


Figure 4.13：Serial Port Connection Diagram

When the serial level used by the user does not match the module, in addition to adding the

level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to this two circuits.

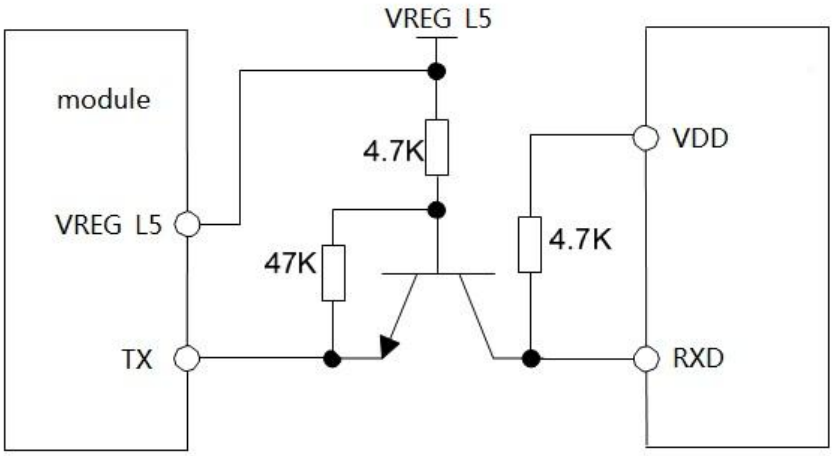


Figure 4.14：TX Connection Diagram

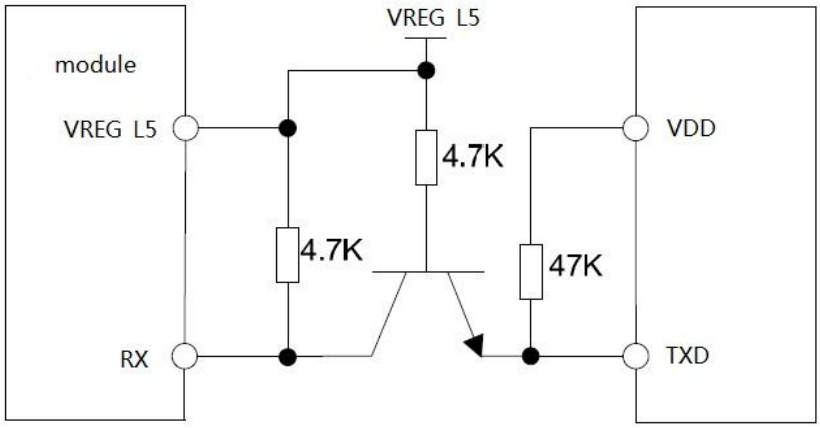


Figure 4.15：RX Connection Diagram

Note： When using Levels Isolation in Figures 14 and 15, it is necessary to use VREG_L5_1P8 as the pull-up power supply. VREG_L6_1P8 will enter the low power mode during sleep. It is not recommended.

Table 4.4：Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Input low level	-	0.45	V
Input high level	1.35	-	V

Note: 1. The serial port of the module is a CMOS interface, and the RS232 signal cannot be directly connected. If necessary, please use the RS232 conversion chip.

2. If the 1.8V output of the module cannot meet the high level range of the user terminal, please add a level shifting circuit.

4.6. MIPI Interface

The SLM758 supports the Moble Industry Processor Interface (MIPI) interface for Camera and LCD. The module supports FULL HD (1920*1200) display. The MIPI interface Main Camera supports up to 16MP, and the Front Camera supports 8MP.

MIPI is a high-speed signal line. In the Layout stage, please follow the impedance and length requirements strictly, and control the length of the differential pair within the group and the group length. The total length should be as short as possible.

Metrics			Information/design guidance	Comments
General information	CLK frequency		750 MHz	
	Data rate		1.5 Gbit/s per lane	
Impedance	Differential	Main route	100 Ω ± 3%	Inspected by TDR simulation @ 150 ps (20-80%). No manufacturing variation considered.
		Break-out	100 Ω ± 10%	
		Connector	100 Ω ± 20%	
	Single-ended	Main route	50 Ω ± 20%	
		Break-out	50 Ω ± 30%	
		Connector	50 Ω ± 30%	
Length match	Intra-lane length match		0.7 mm (5 ps)	It is important to maintain differential lines; single line meandering should not be used other than at Tx breakout.
	Data to clock slew		1.4 mm (10 ps)	This target is for compliance mode. For mission mode while data rate is 1 Gbps or less, inter-pair skew may be relaxed to 100 ps; consider 100 ps for extra-cable inter-pair time skew. At 1.0-1.5 Gbps, this value is 50 ps. (Refer to the MIPI Alliance Specfication for D-PHY 9.2.1 for mission-mode target).
	Max trace length		30 cm	This max length guidance is practical level of definition. (Refer to the MIPI Alliance Specfication for D-PHY 7.6.1).
Spacing	Spacing to all other signal	Main route	4x line width	If not practical, may be relaxed to x3 line width by accepting potential risk. (Refer to the MIPI Alliance Specfication for D-PHY 7.6.5).
	Spacing data lane to lane		3x line width	If not practical, may be relaxed to x2 line width by accepting potential risk. (Refer to the MIPI Alliance Specfication for D-PHY 7.6.5).

4.6.1. LCD Interface

The SLM758 module supports the MIPI interface of two LCD displays, supports dual-screen display, and has a compatible screen identification signal. The resolution of the screen can be up to 1920*1200. The signal interface is shown in the following table. In the Layout, the MIPI signal line should strictly control the differential 100 ohm impedance and the equal length between the signal line group and the group.

The module's MIPI interface is a 1.2V power domain. When the user needs a compatible screen design, the module's LCD_ID pin or ADC pin can be used. At the same time, the module can provide 2.8V power to the LCD. The LCD interface is as follows:

Table 4.5: Primary and secondary screen interface definition

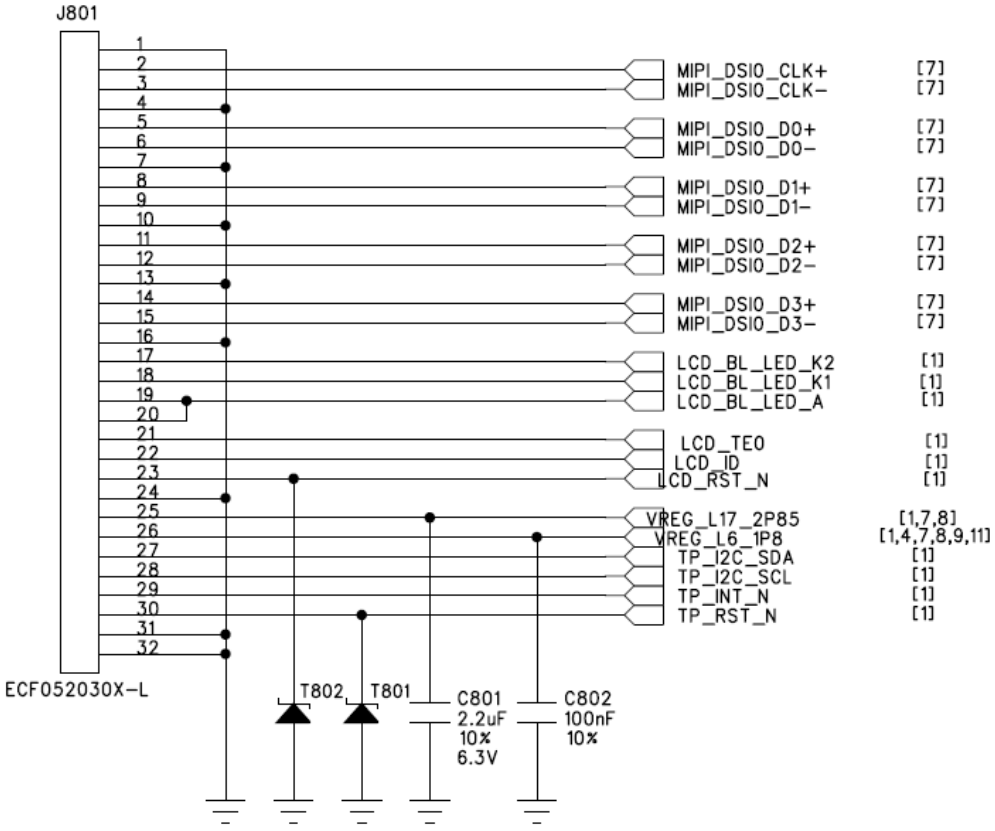
Main screen interface			
MIPI_DSI0_CLK_N	64	O	MIPI_LCD clock line
MIPI_DSI0_CLK_P	65	O	
MIPI_DSI0_LANE0_N	189	I/O	MIPI_LCD data line
MIPI_DSI0_LANE0_P	190	I/O	
MIPI_DSI0_LANE1_N	66	I/O	
MIPI_DSI0_LANE1_P	67	I/O	
MIPI_DSI0_LANE3_N	73	I/O	
MIPI_DSI0_LANE3_P	74	I/O	
MIPI_DSI0_LANE2_N	71	I/O	
MIPI_DSI0_LANE2_P	72	I/O	
GPIO61_LCD_RST_N	75	O	LCD reset pin
GPIO24_LCD_TE0	76	I/O	LCD frame sync signal
LCD_BL_LED_K1	5	AI	LCD series backlight negative pole 1
LCD_BL_LED_K2	6	AI	LCD series backlight negative pole 2
LCD_BL_LED_A	7	PO	LCD series backlight positive pole
VREG_L6_1P8	139	O	1.8V power supply
VREG_L17_2P85	137	O	2.8V power supply

Secondary screen interface			
MIPI_DSI1_CLK_N	242	O	MIPI_LCD2 clock line
MIPI_DSI1_CLK_P	241	O	
MIPI_DSI1_LANE0_N	226	I/O	MIPI_LCD2 data line
MIPI_DSI1_LANE0_P	225	I/O	
MIPI_DSI1_LANE1_N	240	I/O	
MIPI_DSI1_LANE1_P	239	I/O	
MIPI_DSI1_LANE2_N	244	I/O	
MIPI_DSI1_LANE2_P	243	I/O	
MIPI_DSI1_LANE3_N	246	I/O	
MIPI_DSI1_LANE3_P	245	I/O	
GPIO63_LCD2_RST_N	99	O	LCD2 reset pin
GPIO25_LCD_TE1	77	I/O	LCD2 frame sync signal
PM8953_MPP2	112	I/O	Screen backlight PWM control
VREG_L6_1P8	139	O	1.8V power supply
VREG_L17_2P85	137	O	2.8V power supply

LCD_ID of the module, this pin is internally GPIO. When used as LCD_ID, please confirm

the internal circuit of LCD. If the internal divider of the LCD uses resistor divider, please pay attention to the voltage to meet the high or low range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor near the LCD side.



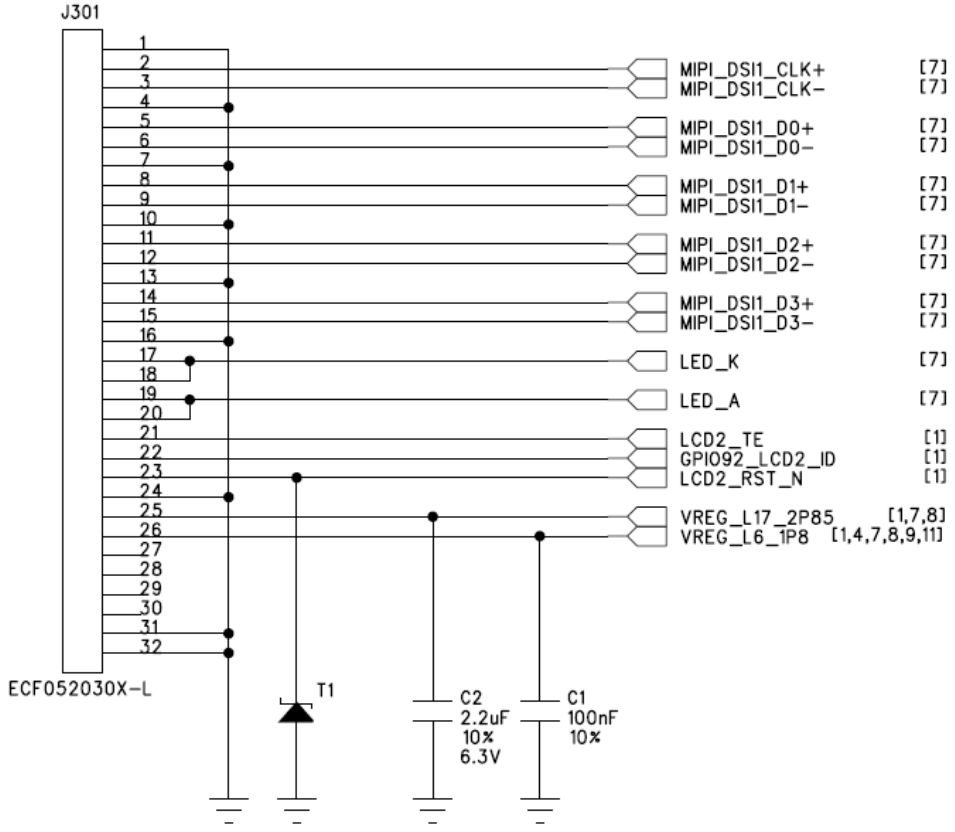


Figure 4.16: Main LCD and sub LCD interface circuit

Both the primary and secondary LCDs require a backlight circuit. The backlight of the main LCD is driven inside the module. It can directly use LCD_BL_LED_A, LCD_BL_LED_K1, LCD_BL_LED_K2 to support up to 2 strings of 8 LEDs in total. The backlight driving circuit of the secondary LCD can refer to Figure 4.17. Adjusting the brightness of the backlight can be realized by PM8953_MPP2 of the module. The modulation method is PWM mode.

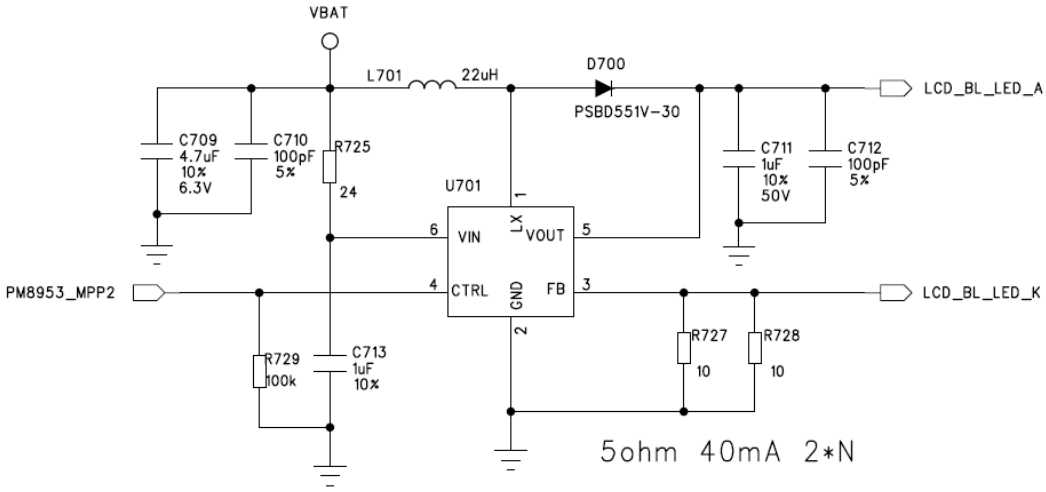


Figure 4.17: Backlight drive schematic

Note: 1. The backlight circuit should select the chip according to the backlight circuit of the LCD. Users should carefully read the LCD document and select the correct driver chip. The reference circuit provided in this document is a series-type PWM dimming backlight driver circuit; if it is a series-type one-line dimming backlight driver circuit, it needs to be controlled by GPIO.

4.6.2.MIPI Camera Interface

The SLM758 module supports the MIPI interface Camera and provides a dedicated camera power supply. The main camera is a CSI0 interface that supports four sets of data lines and can support up to 24M pixels. The front camera is a CSI2 interface that supports four sets of data lines and can support 8M pixels. There is also a set of CSI1 interface, which can do dual 13M dual camera design with the main camera, or as a dual camera design for the depth of field camera; it can also be used as the MIPI interface scan head design. The module provides the power required by the Camera, including AVDD-2.8V, IOVDD-1.8V\AFVDD-2.8V (powered by the focus motor) and D-VDD1.2V (CAM core voltage).

Table 4.6: MIPI Camera Interface Definition

Main camera interface			
Name	Pin	Input/output	Description
MIPI_CSI0_CLK_N	50	I/O	Main camera MIPI clock signal
MIPI_CSI0_CLK_P	49	I/O	
MIPI_CSI0_LANE0_N	56	I/O	Main camera MIPI data signal
MIPI_CSI0_LANE0_P	55	I/O	
MIPI_CSI0_LANE1_N	194	I/O	
MIPI_CSI0_LANE1_P	193	I/O	
MIPI_CSI0_LANE2_N	52	I/O	
MIPI_CSI0_LANE2_P	51	I/O	
MIPI_CSI0_LANE3_N	54	I/O	
MIPI_CSI0_LANE3_P	53	I/O	
GPIO26_MCAM_MCLK	84	O	Main camera clock signal
GPIO40_MCAM_RST_N	85	O	Main camera reset signal
GPIO39_MCAM_PWD_N	86	O	Main camera sleep signal
CAM_I2C_SDA0	105	I/O	I2C data
CAM_I2C_SCL0	104	I/O	I2C clock
VREG_L6_1P8	139	O	1.8V IOVDD
VREG_L17_2P85	137	O	2.8V AFVDD（Focus motor power
VREG_L22_2P8	136	O	2.8V AVDD
VREG_L2_1P1	199	O	1.2V DVDD

Front camera interface			
Name	Pin	Input/output	Description
MIPI_CSI2_CLK_P	40	I/O	Front camera MIPI clock signal
MIPI_CSI2_CLK_N	41	I/O	
MIPI_CSI2_LANE0_P	42	I/O	Front camera MIPI data signal
MIPI_CSI2_LANE0_N	43	I/O	
MIPI_CSI2_LANE1_P	191	I/O	
MIPI_CSI2_LANE1_N	192	I/O	
MIPI_CSI2_LANE2_P	46	I/O	
MIPI_CSI2_LANE2_N	47	I/O	
MIPI_CSI2_LANE3_P	44	I/O	
MIPI_CSI2_LANE3_N	45	I/O	
GPIO27_SCAM_MCLK	80	O	Front camera clock signal
GPIO129_SCAM_RST_N	79	O	Front camera reset signal
GPIO130_SCAM_PWDN	78	O	Front camera sleep signal
CAM_I2C_SDA1	96	I/O	I2C data
CAM_I2C_SCL1	95	I/O	I2C clock
VREG_L6_1P8	139	O	1.8V IOVDD
VREG_L17_2P85	137	O	2.8V AFVDD（Focus motor power
VREG_L22_2P8	136	O	2.8V AVDD
VREG_L23_1P175	200	O	1.2V DVDD

Depth camera interface			
Name	Pin	Input/output	Description
MIPI_CSI1_CLK_N	207	I/O	Depth camera MIPI clock signal
MIPI_CSI1_CLK_P	208	I/O	
MIPI_CSI1_LANE0_N	63	I/O	Depth camera MIPI data signal
MIPI_CSI1_LANE0_P	62	I/O	
MIPI_CSI1_LANE1_N	59	I/O	
MIPI_CSI1_LANE1_P	58	I/O	
MIPI_CSI1_LANE2_N	172	I/O	
MIPI_CSI1_LANE2_P	171	I/O	
MIPI_CSI1_LANE3_N	61	I/O	
MIPI_CSI1_LANE3_P	60	I/O	
GPIO28_CAM_MCLK2	264	O	Depth camera clock signal
GPIO131_DCAM_RST_N	263	O	Depth camera reset signal
GPIO132_DCAM_PWD_N	262	O	Depth camera sleep signal
CAM_I2C_SDA1	96	I/O	I2C date
CAM_I2C_SCL1	95	I/O	I2C clock
VREG_L6_1P8	139	O	1.8V IOVDD
VREG_L17_2P85	137	O	2.8V AFVDD（Focus motor power
VREG_L22_2P8	136	O	2.8V AVDD
VREG_L2_1P1	199	O	1.2V DVDD

If the user designs to use the CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the driver chip of CAMERA, and the correct connection is as follows:

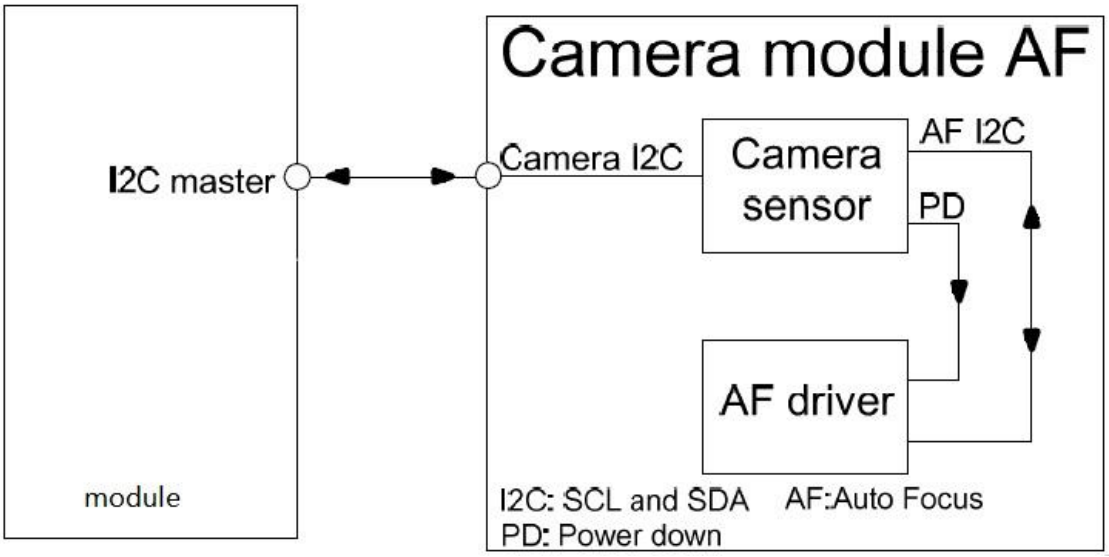
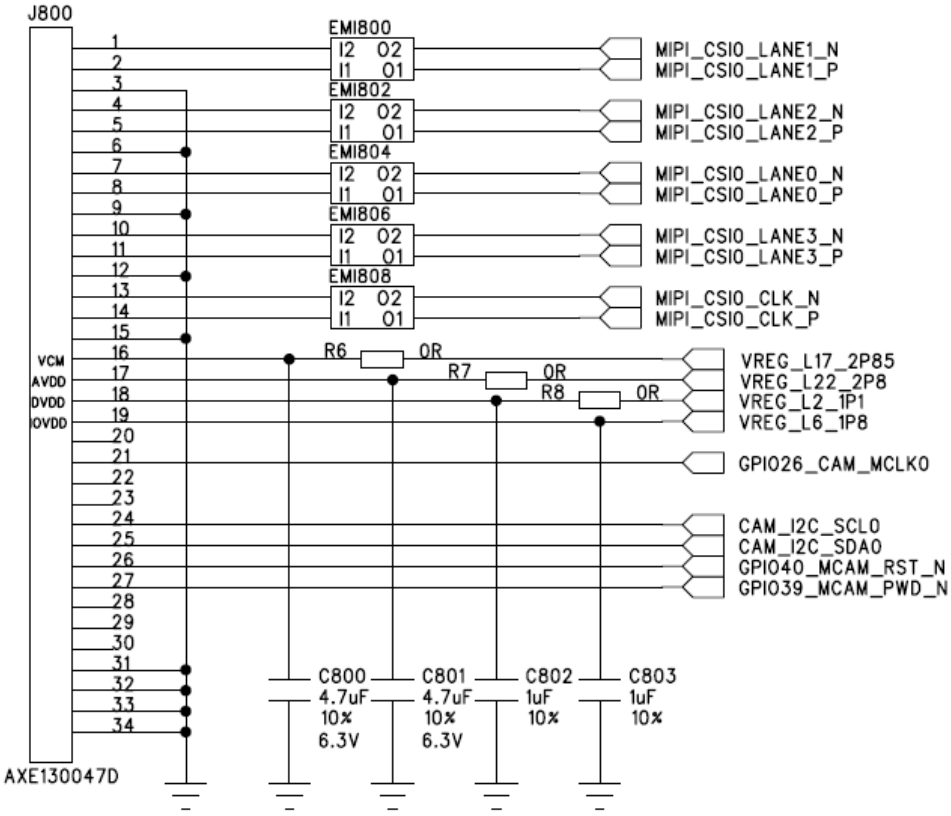


Figure 18： Correct CAMERA connection diagram

The MIPI interface has a high rate. The user should control the impedance by 100 ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.



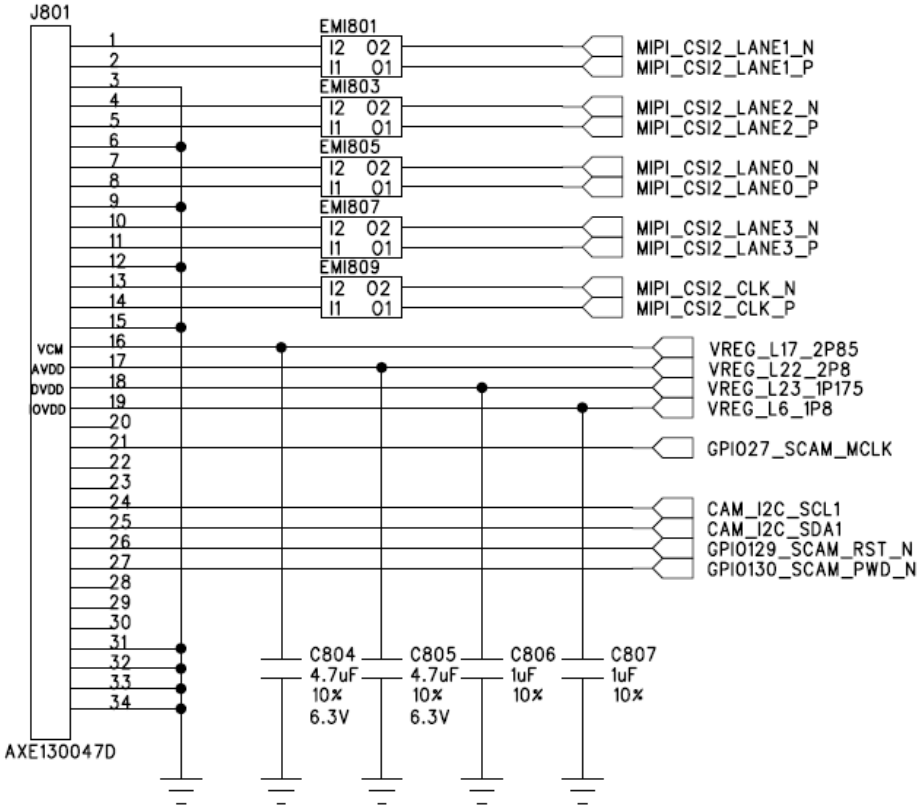


Figure 4.19: MIPI Camera Reference Circuit

Important note: When designing the camera function, you need to pay attention to the position of the connector. There will be a small person in the specification of the camera to indicate the imaging direction. You need to ensure that the villain is standing on the long side of the LCD, otherwise the camera will be flipped. The software cannot be adjusted at 90°. As shown in the two figures below.

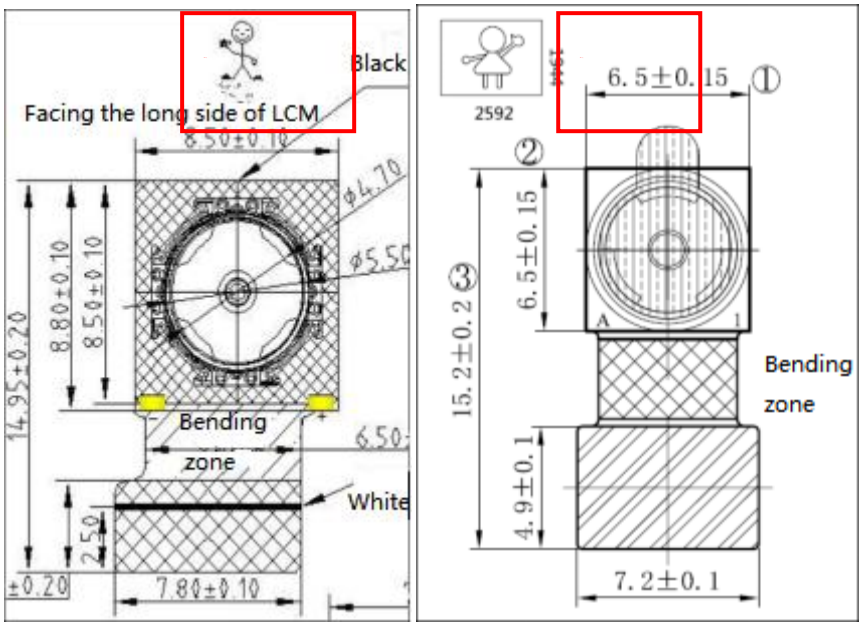


Figure 4.20: Camera imaging diagram

4.7.Resistive Touch Interface

The module does not provide a resistive touch screen interface. If the user needs to use a resistive touch, an external dedicated chip is required. The module can provide an I2C interface.

4.8.CapacitiveTouch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touches while providing the required power and interrupt pins. The default interface pins for capacitive touch software are defined as follows:

Table 4.7：Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO10_TP_I2C3_SDA	234	I/O	The capacitive touch I2C interface needs to be pulled up toVREG_L5_1P8
GPIO11_TP_I2C3_SCL	233	I/O	
GPIO65_TP_INT_N	97	I	Interrupt
GPIO64_TP_RST_N	98	O	Reset
VREG_L5_1P8	140	O	1.8V Power supply
VREG_L10_2P8_SENSOR	138	O	2.8V Power supply

Note: The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.9.Audio Interface

The module provides three analog audio inputs, MIC_IN1_P/M for the main microphone, MIC_IN2_P for the microphone, and MIC_IN3_P for the noise reduction microphone. The module also provides three analog audio outputs (HPH_L/R, REC_P/N, SPK_P/N). The audio pin is defined as follows:

Table 4.8：Audio Pin Definitions

Name	Pin	Input/Output	Description
MIC_IN1_M	123	I	Main MIC negative, grounded at MIC
MIC_IN1_P	122	I	Main MIC positive
MIC_IN2_P	132	I	Headphone MIC positive
GND_MIC	124	I	Headphone MIC, noise reduction MIC
MIC_IN3_P	131	I	Noise reduction MIC positive
MIC_BIAS1	118	O	BIAS voltage of the main MIC for silicon wheat
MIC_BIAS2	117	O	BIAS voltage of the headphone MIC for silicon wheat design
CDC_HPH_R	128	O	Headphone right channel

CDC_HPH_L	126	O	Headphone left channel
CDC_HS_DET	125	I	Headphone plug detection
CDC_HPH_REF	127	I	Headphone reference ground
CDC_EAR_M	129	O	Earpiece output negative
CDC_EAR_P	130	O	Earpiece output positive
SPKR_DRV_M	133	O	Amplifier (0.85W) output negative
SPKR_DRV_P	134	O	Amplifier (0.85W) output positive

Users are advised to use the following circuit according to the actual application to get better sound effects.

4.9.1Receiver Interface Circuit

The receiver interface circuit places the following devices near the REC end, and B302 and B303 can be changed to magnetic beads according to actual effects.

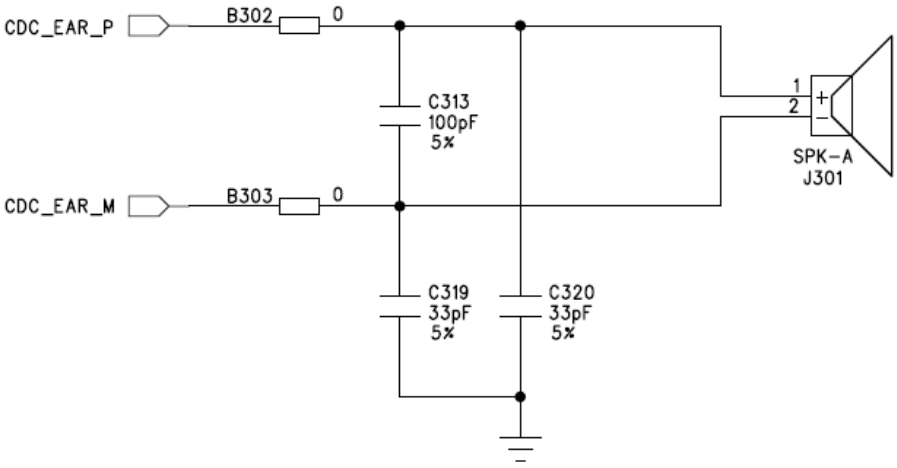


Figure 4.21： Receiver Interface Circuit

4.9.2 Microphone receiving Circuit

On the right is the MEMS microphone interface circuit, which has more BIAS power than the electret MIC. The negative signal of the main MIC must be designed from 0R to ground resistance near the MIC. As shown in Figure R301.

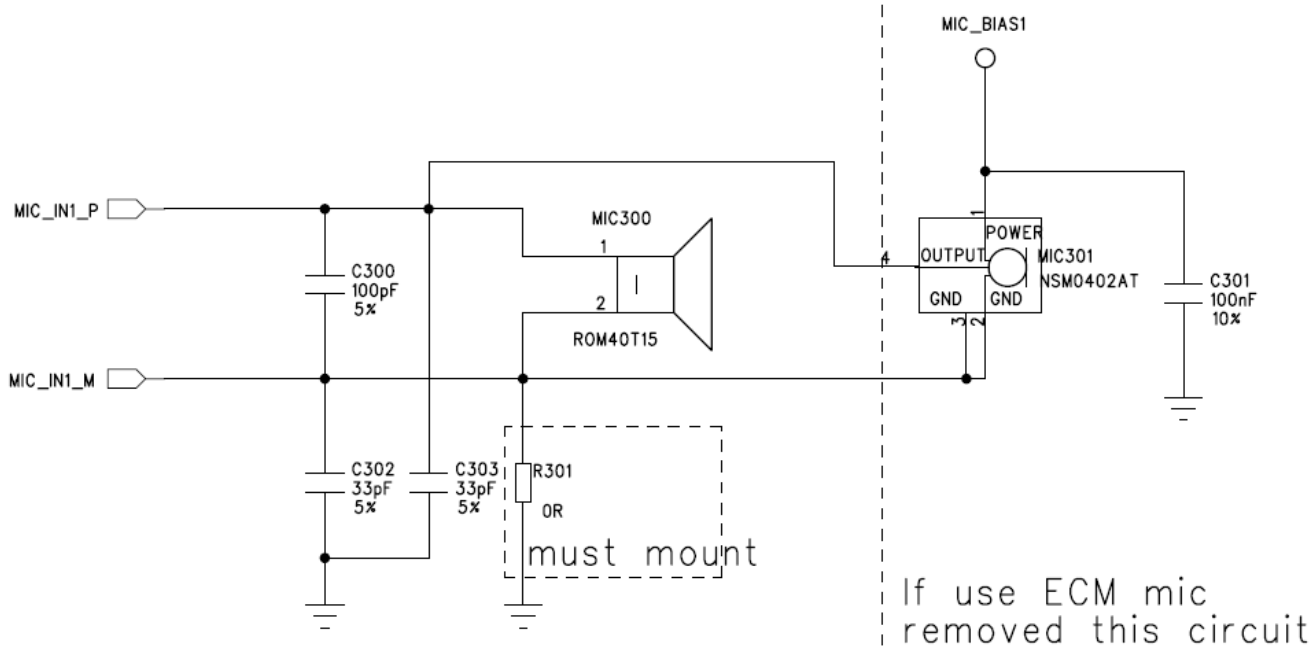


Figure 4.22： Microphone Differential Interface Circuit

4.9.3.Headphone Interface Circuit

The module integrates a stereo headphone jack. Users are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as an interrupt. In software, this pin is the earphone interrupt by default. The user can use this pin to detect the plugging and unplugging of the earphone.

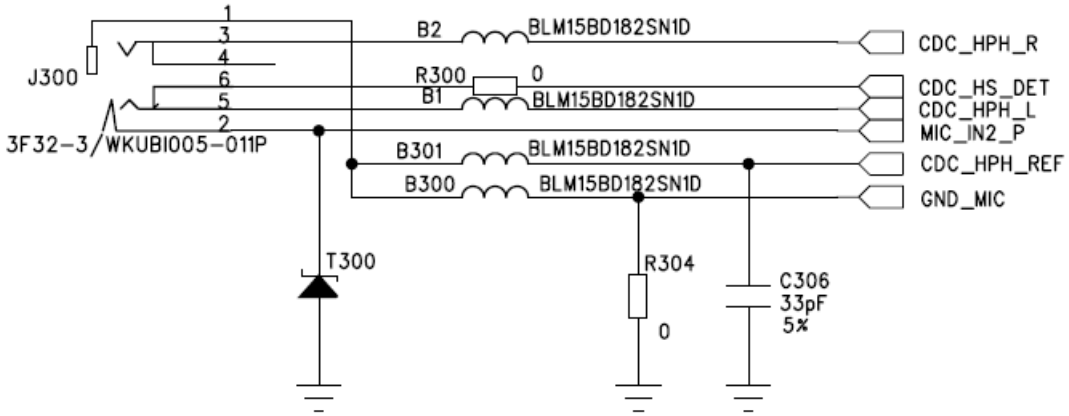


Figure 4.23：Headphone Interface Circuit

Note:

1. The earphone holder in Figure 4.24 is normally closed. If the user is using the normally open mode earphone holder, please modify the detection circuit according to the actual pin and modify the software accordingly.

2. We recommend that the headphone detection pin HS_DET and HPH_L form a detection circuit (the connection method in the above figure), because HPH_L has a pull-down resistor inside the chip, which can ensure that HS_DET is low when connected with HPH_L, if the user will HS_DET and HPH_R To connect, please reserve a 1K pull-down resistor on HPH_R.
3 The standard of the headphone interface is the European standard OMPT. If you need to design the American standard CTIA interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headset standards, you need an external dedicated chip, such as the TI-TS3A226AE.

4.9.4.Speaker Interface Circuit

The module integrates a Class-D audio amplifier with an output power of 0.85W and an output signal of SPKR_OUT_P / SPKR_OUT_M.

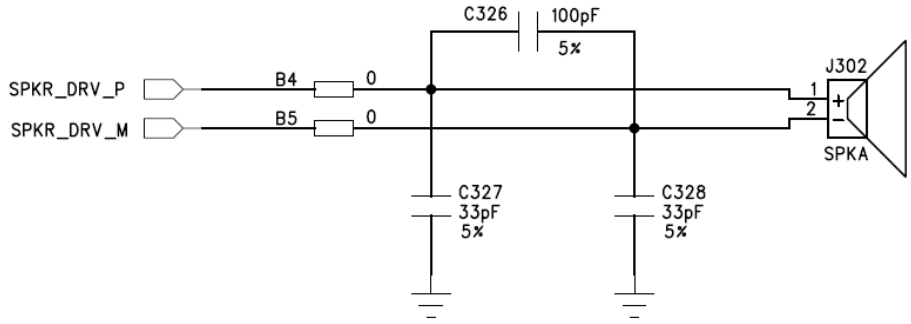


图 4.24：用内部音频功放推荐电路

It is also possible to add an audio amplifier externally, using CDC_HPH_R as a single-ended input signal, and the reference circuit is shown below.

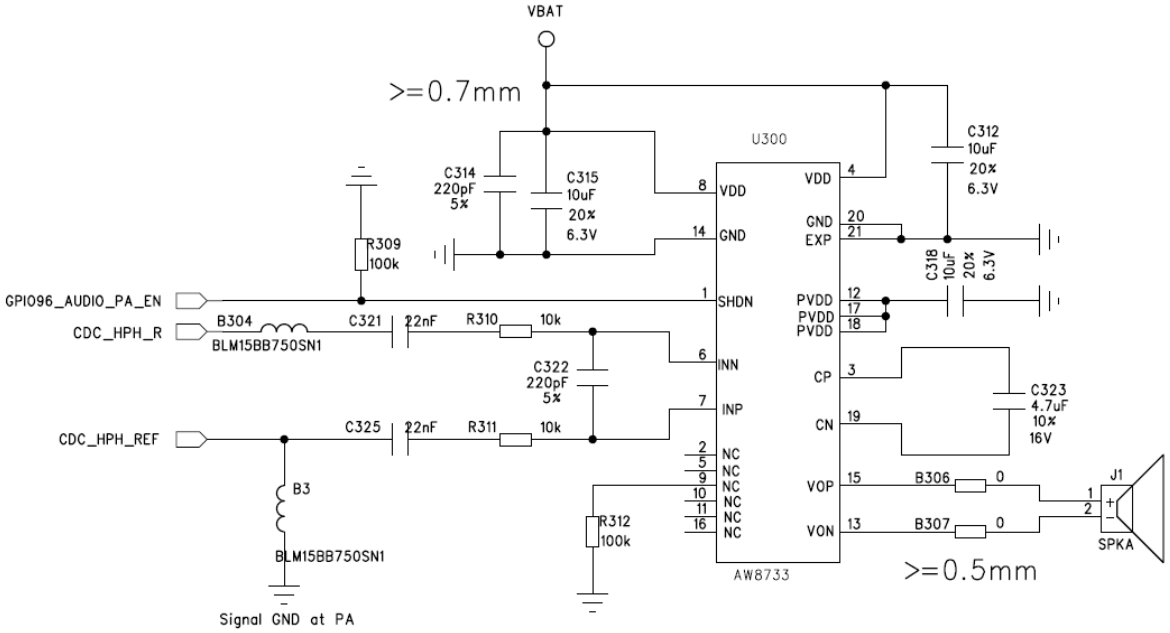


Figure 4.25：Recommended circuit with external audio amplifier

4.9.5.I2S Interface

There are two sets of GPIO-compatible I2S interfaces inside the module. The pins used by this function are as follows:

Name	Pin	Intput/Output	Description
GPIO88_HOMEKEY_MI2S1_D1	27	I	I2S1 input DATA
GPIO93_MI2S_1_D0	265	O	I2S1 output DATA
GPIO92_MI2S_1_WS	271	O	I2S1_ WS
GPIO91_MI2S_1_SCK	169	O	I2S1_ SLK
GPIO138_FP_SPI_MISO	266	I	I2S2 input DATA
GPIO137_FP_SPI_MOSI	267	O	I2S2 output DATA
GPIO136_FP_SPI_CS	268	O	I2S2_WS
GPIO135_FP_SPI_CLK	269	O	I2S2_SCK

4.10. USB Interface

The SLM758 supports a USB 2.0 /3.0High/Super speed interface. It must control the 90 ohm differential impedance during Layout and control the external trace length.

The module supports OTG function at the same time and can output 5V/1A current.

The voltage input range during charging is as follows:

Table 4.9: Voltage input range during charging

Name	Description	Minimum	Typical	Maximum	Unit
VBUS	Input range	4	-	6.3	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. The DM/DP must add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting the TVS, the user should pay attention to the load capacitance of less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand, it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

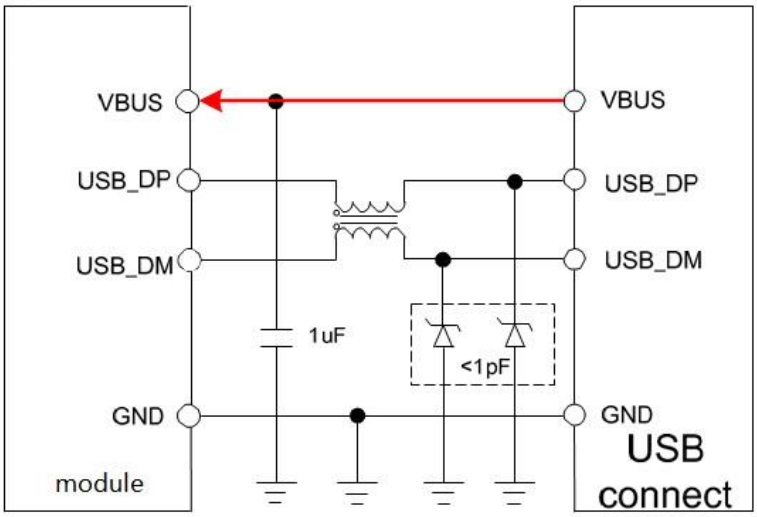


Figure 4.26: USB Connection Diagram

4.10.1. USB OTG

The SLM758 module can provide USB OTG function. The pins used in this function are as follows:

Table 4.10: USB OTG Pin Description

Pin name	Pin	Description
VBUS	157、158、159	5V charging input / OTG output power.
USB_HS_D_M	145	USB Date-
USB_HS_D_P	146	USB Date+
USB_ID	143	USB ID

The recommended circuit diagram of USB OTG is as follows:

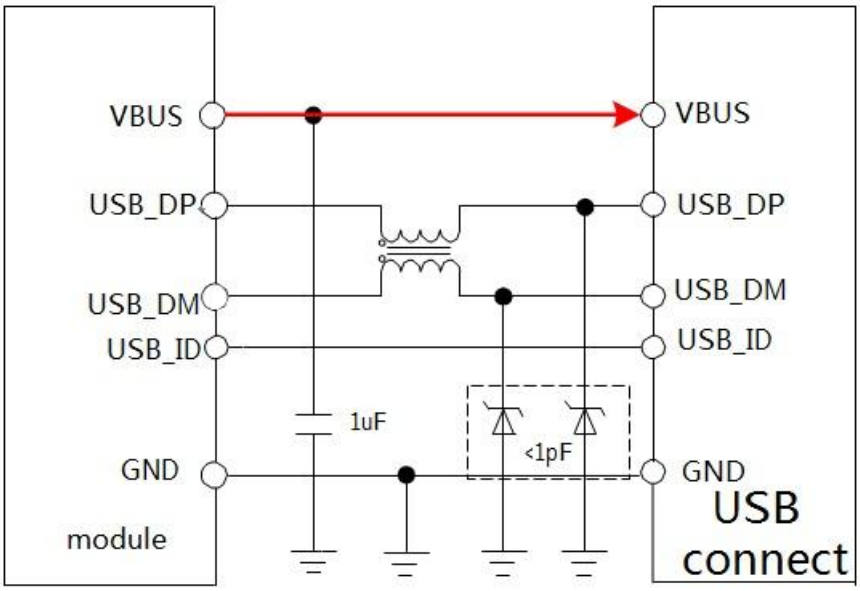


Figure 4.27: USB-OTG Connection Diagram

4.11. Charging Interface

The SLM758 module integrates a 2A charging solution. The charging related content of this manual is only described by the internal charging scheme. The MSM8953 platform uses the Qualcomm PMI8952 internal integrated charging chip by default. The chip is in switching mode and has high efficiency. It integrates a 15-bit battery voltage detection ADC and a 15-bit current detection ADC. The charging current can be up to 2A.

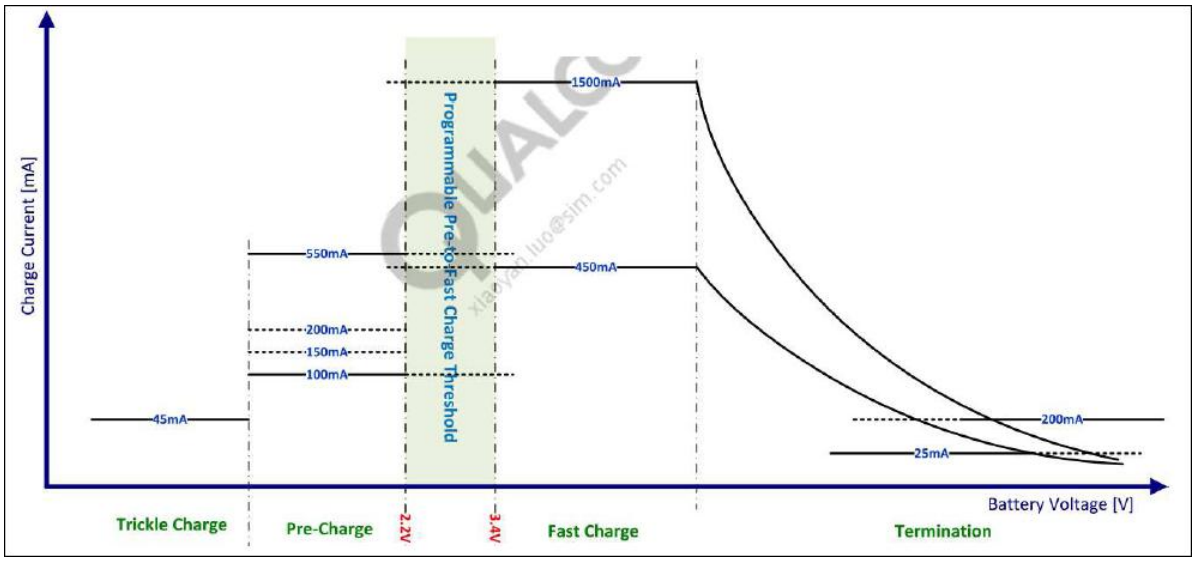


Figure 4.28: Charging diagram

4.11.1. Charging Detection

When the VBUS pin voltage is higher than 4.0V, a hardware interrupt will be generated inside the module. The software determines whether the charger is inserted or the USB data cable is inserted by judging the status of USB_DP/USB_DM.

4.11.2. Charge Control

The SLM758 module can charge the over-discharged battery. The charging process includes trickle charge, pre-charge, constant current, and constant-voltage charge. When the VBAT voltage is lower than 3.4V, the module is pre-charged; when VBAT is between 3.4V and 4.2V, it is charged by the constant current plus constant voltage method optimized for the lithium battery. At present, the software's charge cut-off voltage is 4.2V, and the back-off voltage is 4.05V.

4.11.3. BAT_CON_TEM

The SLM758 module has battery temperature detection and can be implemented by BAT_THERM (149PIN). This requires the internal integration of a 10KΩ thermistor (negative temperature coefficient) inside the battery to connect the thermistor to the BAT_THERM pin. During the charging process, the software reads the voltage of the BAT_THERM pin to determine if the battery temperature is too high. If the temperature is too high or too low, the battery will stop charging immediately to prevent battery damage. The battery charging connection diagram is shown below:

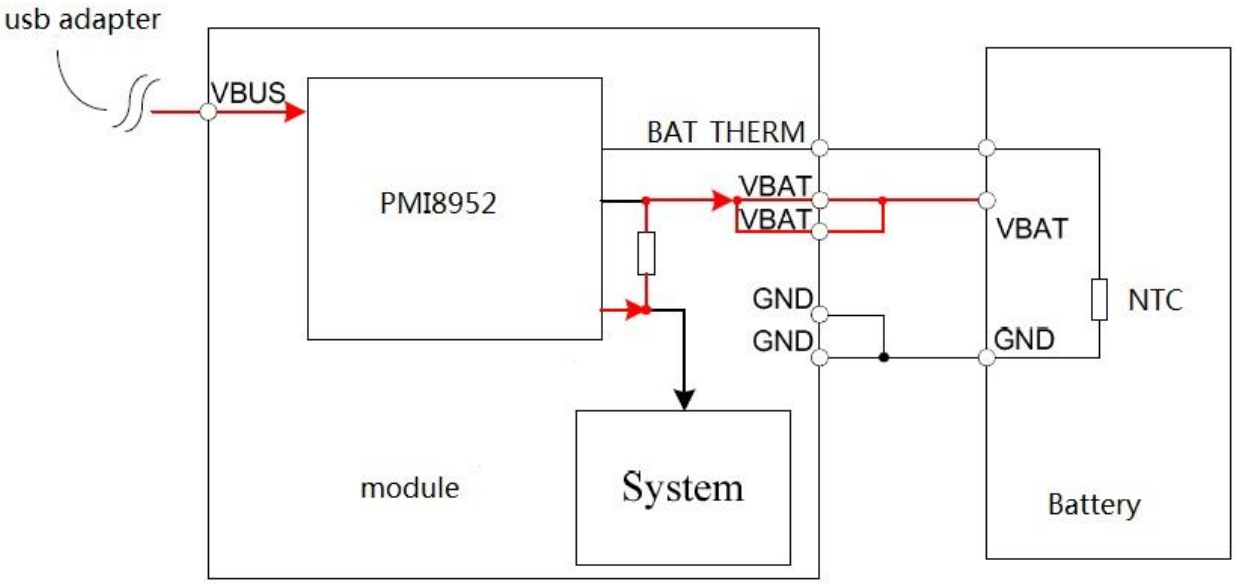


Figure 4.29: Charging circuit connection diagram

4.12 UIM Card Interface

The SLM758 can support two SIM cards at the same time to achieve dual card dual standby. Support SIM card hot swap, can automatically recognize 1.8V and 3.0V cards. The figure below is the SIM recommended interface circuit. In order to protect the SIM card, it is recommended to use TVS devices for electrostatic protection. The device of the peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

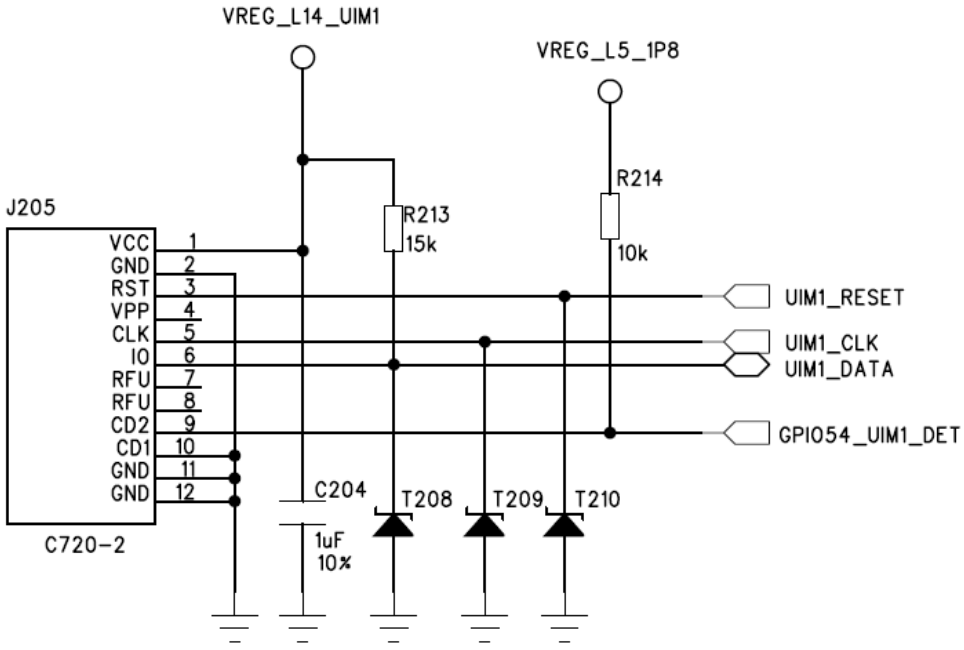


Figure 4.30: UIM card interface circuit

4.13. SD Card Interface

SLM758 supports SD card interface and supports up to 64GB.

The reference circuit is as follows:

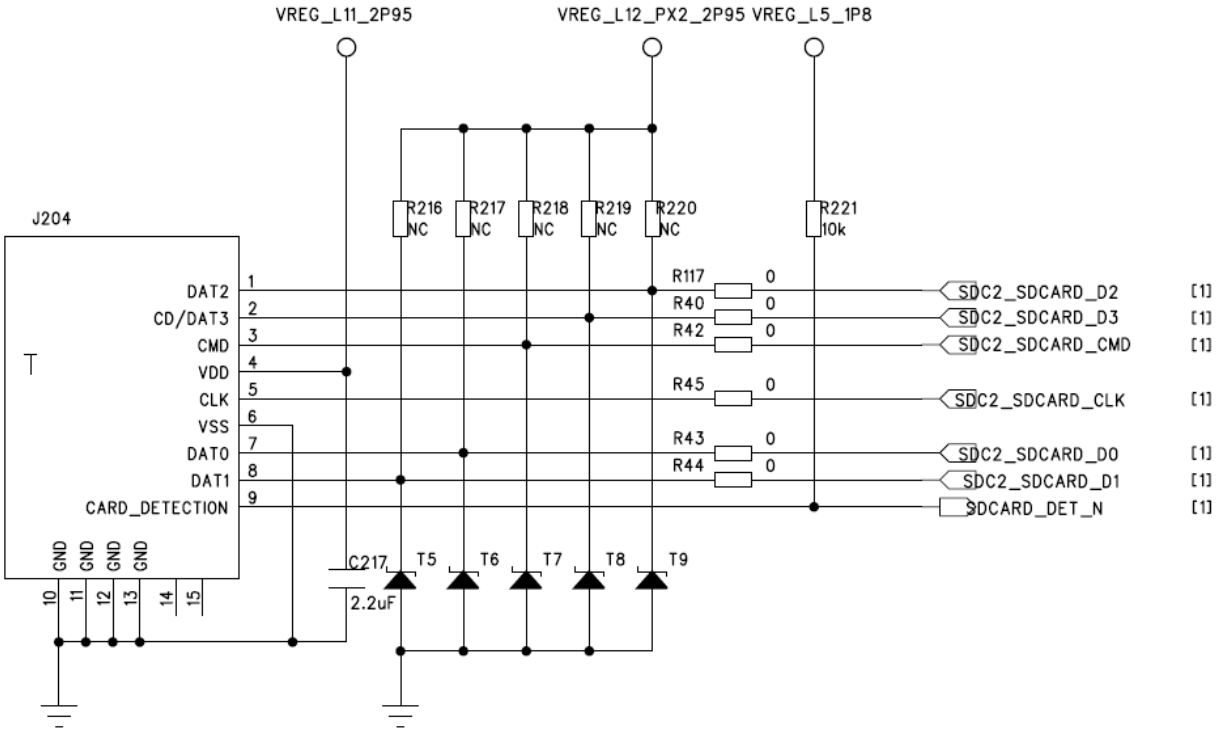


Figure 4.31: SD Card Interface Circuit

4.14 I2C Bus Interface

The SLM758 module supports four hardware I2C bus interfaces and one camera-specific CCI interface. The pin definitions and default functions are as follows:

Table 4.11: I2C Interface Pin Description

Name	Pin	Default function
CAM_I2C_SDA0	105	Camera dedicated
CAM_I2C_SCL0	104	
GPIO14_SENSOR_I2C4_SDA	17	General purpose I2C, default for sensor
GPIO15_SENSOR_I2C4_SCL	18	
GPIO6_I2C2_SDA	13	General purpose I2C
GPIO7_I2C2_SCL	14	
CAM_I2C_SDA1	96	Camera dedicated
CAM_I2C_SCL1	95	
GPIO10_TP_I2C3_SDA	234	General purpose I2C, default for TP
GPIO11_TP_I2C3_SCL	233	
GPIO18_NFC_I2C5_SDA	254	Universal I2C, default for NFC
GPIO19_NFC_I2C5_SCL	253	

Note: To use the 2.2KΩ pull-up resistor to 1.8V when used as an I2C bus interface, refer to Table 3.1 - I2C Interface.

4.15 Analog to Digital Converter (ADC)

The SLM758 module provides three MPP function signals from the power management chip: PMI8953_MPP1 (4PIN) and PM8953_MPP2 (112PIN), PM8953_MPP4 (209PIN) MPP can be configured as an ADC or PWM signal. Note: PM8953_MPP2 and PM8953_MPP4 cannot be configured as PWM functions at the same time.

The ADC signal is 16 bit resolution, and its performance parameters are as follows:

Table 4.12: ADC Performance Parameters

Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	-	1.8	-	V
ADC Resolution	-	-	15	bits
Analog Input Bandwidth	-	100	-	kHz
Sampling Frequency	-	2.4	-	MHz
INL	-	-	±8	LSB
DNL	-	-	±4	LSB
Offset error	-	-	±1	%
Gain error	-	-	±1	%

4.16. PWM

The PWM pin can be used as a backlight adjustment for the LCD to adjust the backlight brightness by adjusting the duty cycle.

4.17. Motor

The SLM758 supports motor functions and can be implemented by the user via PMI_HAP_OUT_N (8PIN) and PMI_HAP_OUT_P (9PIN). The reference schematic diagram is as follows. Note that the uF-level capacitor cannot be placed on the signal line.

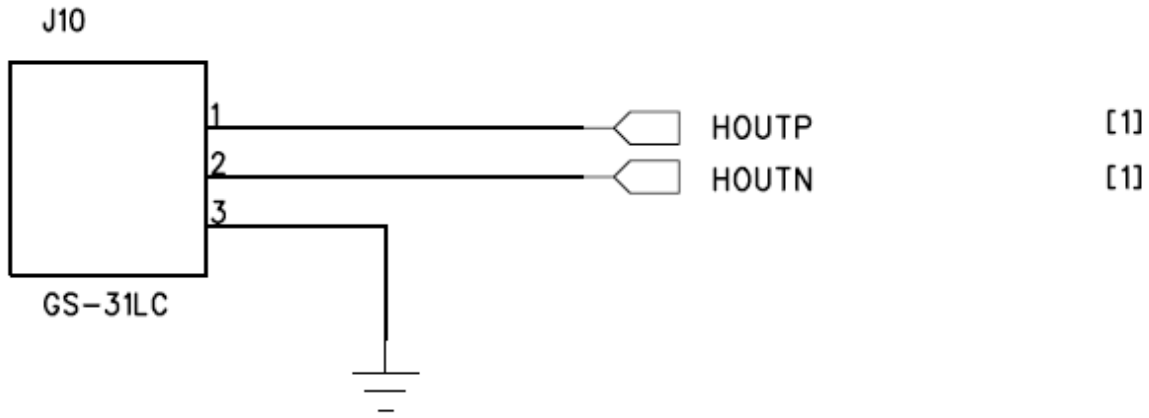


Figure 4.32: Motor interface circuit

4.18 Antenna Interface

The module provides four antenna interfaces: MAIN antenna, DRX antenna, GPS antenna and WiFi/BT antenna. In order to ensure that the user's products have good wireless performance, the antenna selected by the user should meet the requirement that the input impedance is 50 ohms in the working frequency band and the VSWR is less than 2.

4.18.1 Main Antenna

The module provides the MAIN antenna interface pin Pin1 RF_MAIN. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

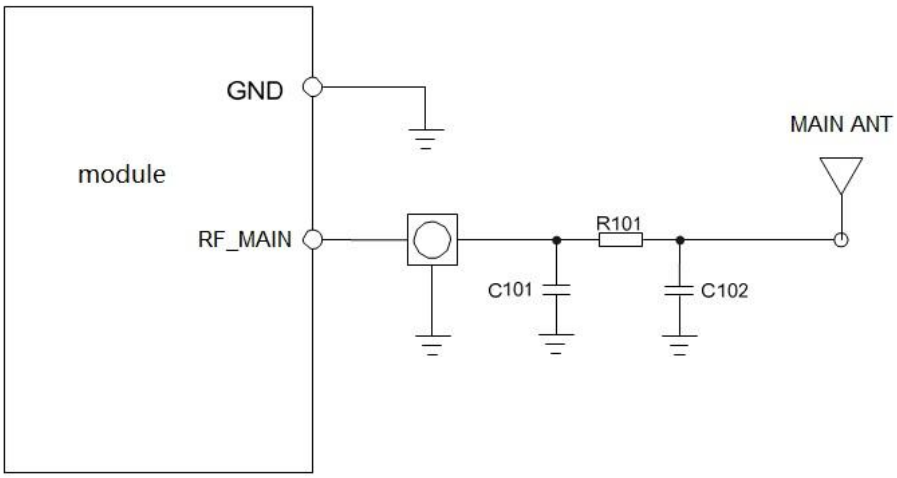


Figure 4.34: MAIN Antenna Interface Connection Circuit

In the figure, R101, C101, and C102 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R101 defaults to 0R, C101 and C102 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

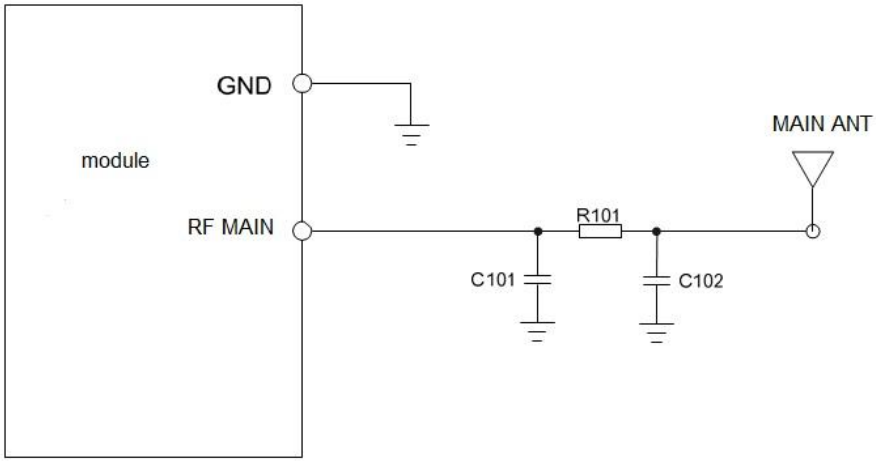


Figure 4.35: MAIN Antenna Interface Simplified Connection Circuit

In the above figure, R101 defaults to 0R, and C101 and C102 do not paste by default.

4.18.2 DRX Antenna

The module provides the DRX antenna interface pin RF_DIV, and the antenna on the user's motherboard should be connected to the module's antenna pins using a 50-ohm characteristic microstrip or stripline.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

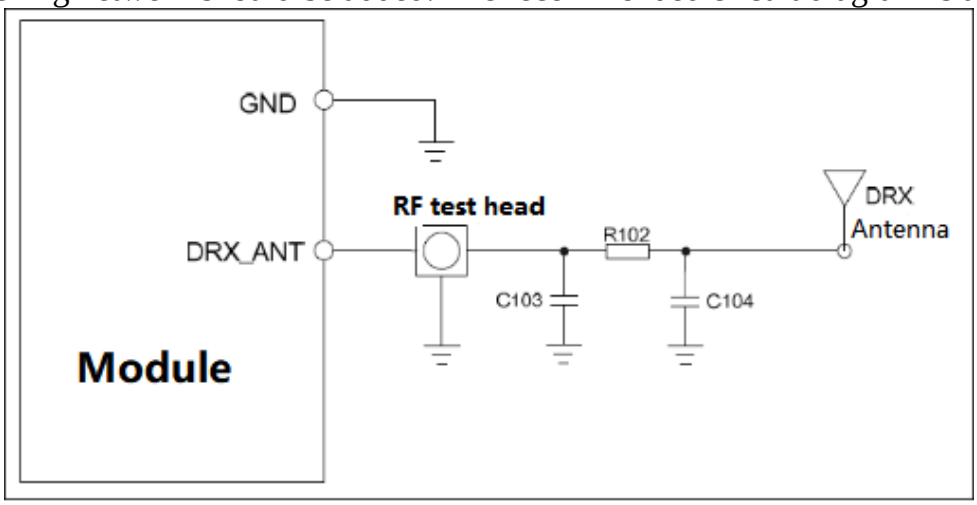


Figure 4.36: DRX Antenna Interface Connection Circuit

In the figure, R102, C103, and C104 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R102 defaults to 0R, C103 and C104 are not posted by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

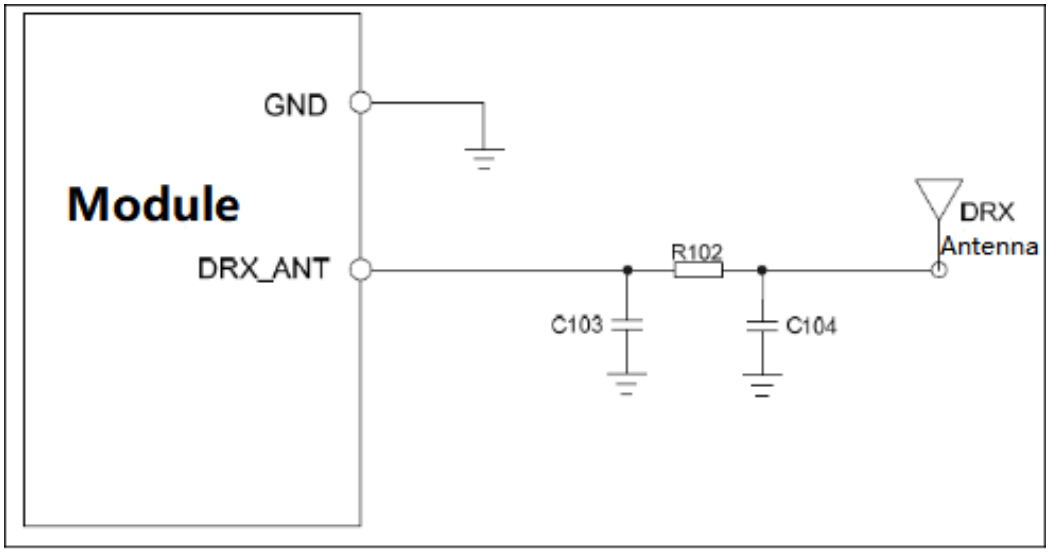


Figure 4.37: DRX Antenna Interface Simplified Connection Circuit

In the above figure, R102 defaults to 0R, C103 and C104 are not attached by default.

4.18.3 GPS Antenna

The module provides the GNSS antenna pin RF_GPS. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.

The LNA is integrated inside the module.

To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connections are as follows:

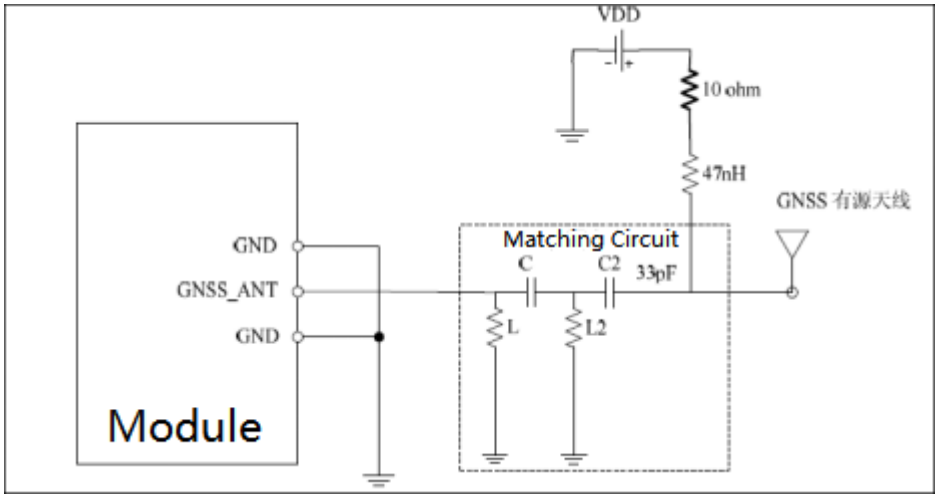


Figure 4.38: Connecting Active Antennas

4.18.4 WiFi/BT antenna

The module provides the WiFi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50 ohm microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

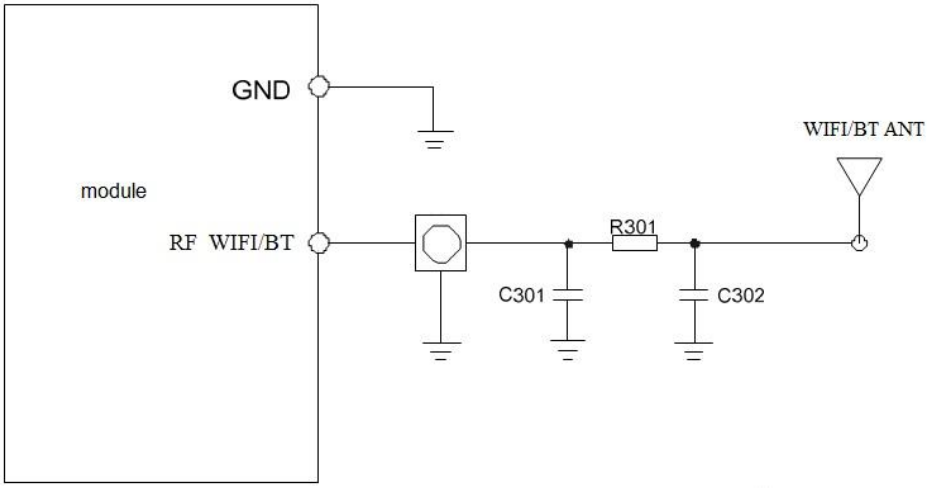


Figure 4.40: WiFI_BT antenna interface connection circuit

In the figure, R301, C301, and C302 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C301 and C302 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

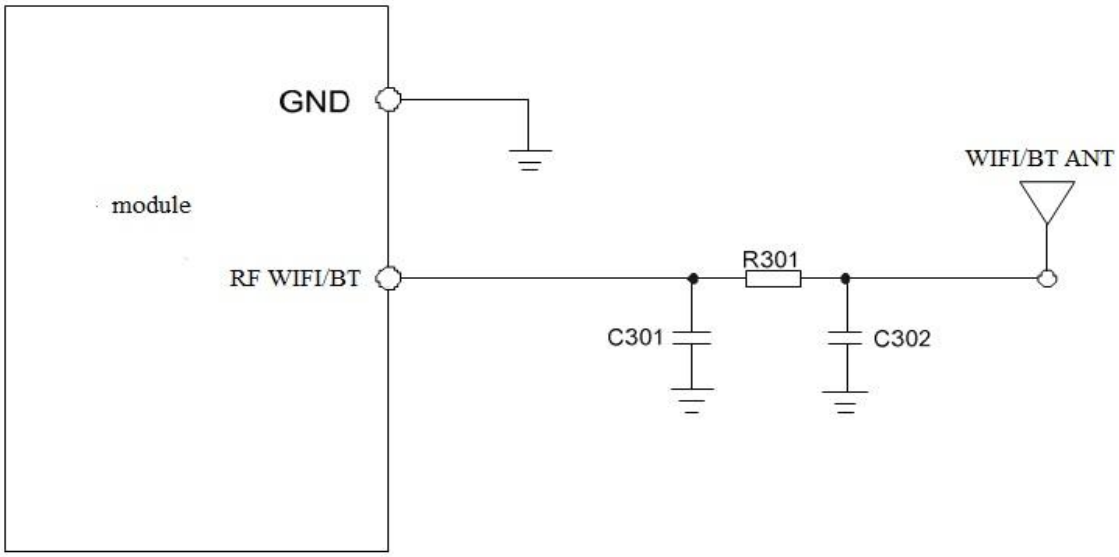


Figure 4.41: WIFI_BT antenna interface simplified connection circuit

In the above figure, R301 defaults to 0R, and C301 and C302 do not paste by default.

5.PCB Layout

The performance of a product depends largely on the PCB trace. As mentioned above, if the PCB layout is unreasonable, it may cause interference problems such as card loss. The way to solve these interferences is often to redesign the PCB. If you can plan a good PCB layout in the early stage, the PCB traces smoothly, saving a lot of time. Of course, it can also save a lot of costs. This chapter mainly introduces some things that users should pay attention to during the PCB layout stage, minimizing interference problems and shortening the user's development cycle.

The SLM758 module is an intelligent module with its own Android operating system. It includes sensitive data lines such as high-speed USB and MIPI. It also has strict requirements on the length and impedance of the signal line. If the high-speed signal processing is not good, it will cause serious EMI. The problem, more serious will also affect the USB identification, LCD display, so the PCB design requirements when using the SLM758 module is much higher than the previous 2G module, please read this chapter carefully, reduce the subsequent hardware debugging cycle.

When using the SLM758 module, the user is required to use at least 4 layers of via holes for the PCB to facilitate impedance control and signal line shielding.

5.1. Module PIN distribution

Before the PCB layout, first understand the pin distribution of the module, and rationally layout the related devices and interfaces according to the distribution defined by the pin. Please refer to Figure 2 to determine the distribution of the function feet of the module.

5.2. PCB Layout Principles

Several aspects of the main attention during the PCB layout phase:

5.2.1. Antenna

Antenna part design, SLM758 module has a total of 4 antenna interfaces, they are: ANT_MAIN, ANT_DRX, ANT_GNSS, ANT_WIFI. Pay attention to component placement and RF routing:

The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pins of the module.

The antenna matching circuit needs to be placed close to the antenna end;

The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;

The device and wiring between the antenna pin and the antenna connector of the module must be away from high-speed signal lines and strong interference sources to avoid crossing or parallel with any signal lines in adjacent layers.

The length of the RF cable between the antenna pin of the module and the antenna connector should be as short as possible. The situation of crossing the entire PCB should be absolutely avoided.

If the antenna is connected by a coaxial RF line, care should be taken to avoid the coaxial RF line spanning the SIM card, power supply circuit, and high-speed digital circuits to minimize the effects of each other.

5.2.2 Power Supply

Power traces must consider not only VBAT, but also the return GND of the power supply. The trace of the VBAT positive must be short and thick, the trace must first pass through the large capacitor, Zener diode and then the power PIN of the module. There are multiple PAD exposed copper at the bottom of the module. Make sure that the GND path of these exposed copper areas to the power supply is the shortest and smoothest. This ensures that the current path of the entire power supply is the shortest and the interference is minimal.

5.2.3. SIM Card

The SIM card has a large area and does not have an anti-EMI interference device. It is relatively susceptible to interference. Therefore, in the layout, first ensure that the SIM card is away from the antenna and the antenna extension cable inside the product. Place it as close as possible to the module. When the PCB is routed, pay attention to it. The SIM_CLK signal is protected, and the SIM_DATA, SIM_RST, and SIM_VDD signals of the SIM card are away from the power source and away from the high-speed signal line. If the processing is not easy, it may cause problems such as not knowing the card or dropping the card. Therefore, please follow the following principles when designing:

- Keep the SIM card holder away from the GSM antenna during the PCB layout phase;
- SIM card routing should be as far away as possible from RF line, VBAT and high-speed signal lines, and the SIM card should not be too long;
- The GND of the SIM card holder should be in good communication with the GND of the module to make the GND equipotential between the two.
- To prevent SIM_CLK from interfering with other signals, it is recommended to protect SIM_CLK.
- It is recommended to place a 100nF capacitor on the SIM_VDD signal line near the SIM card holder;
- Place TVS near the SIM card holder. The parasitic capacitance of the TVS should not exceed 50pF, and the 51Ω resistor in series with the module can enhance ESD protection.
- The SIM card signal line increases the capacitance of 22pF to ground to prevent radio frequency interference.
- The return path of VBAT has a large current, so the SIM card trace should avoid the return path of VBAT as much as possible.

5.2.4. MIPI

MIPI is a high-speed signal line. Users must pay attention to protection during the layout stage, so that they are away from the signal lines that are easily interfered. The GND processing must be performed on the upper and lower sides, and the traces are differential pairs. 100 ohm differential impedance matching is performed. Ensure impedance consistency and do not bridge different GND planes as much as possible.

The MIPI interface selects a small-capacity TVS when selecting an ESD device. It is recommended that the parasitic capacitance be less than 1pF.

The MIPI routing requirements are as follows:

The total length of the cable does not exceed 300mm

It is required to control 100 ohm differential impedance with an error of ±10%.

The error of the differential line length within the group is controlled within 0.7mm.

The length error between groups is controlled within 1.4mm.

5.2.5. USB

The module supports high-speed USB interface at a rate of 480Mbps. The user recommends adding a common-mode inductor during the schematic design phase to effectively suppress EMI interference. If you need to increase the static protection, please select a TVS tube with a parasitic capacitance of less than 1pF. Please refer to the following notes when planning Layout:

- The common mode inductor should be close to the side of the USB connector.
- Requires control of 90 ohm differential impedance with an error of ±10%.
- The differential line length error is controlled within 6mm.
- If the USB has a charging function,please note that the VBUS cable is as wide as possible.
- If there is a test point, try to avoid the split line and put the test point on the path of the trace.

Table 5.1: Internal USB cable length of the module

Pin	Signal	Length mm)	Length Error（P-N）
14	USB_DP	46.3	0.2mm
13	USB_DM	46.4	

5.2.6.Audio

The module supports 3 analog audio signals. Analog signals are susceptible to interference from high speed digital signals. So stay away from high-speed digital signal lines. The module supports the GSM system, and the GSM signal can interfere with the audio by coupling and conduction. Users can add 33pF and 10pF capacitors to the audio path to filter out coupling interference. The 33pF capacitor mainly filters out the interference of the GSM850/EGSM900 band, and the 10pF capacitor mainly filters out the interference of the DCS1800 band. The coupling interference of TDD has a great relationship with the PCB design of the user. In some cases, the TDD of the GSM850/EGSM900 frequency band is more serious, and in some cases,

the TDD interference of the DCS1800 frequency band is more serious. Therefore, the user can select the required filter capacitor according to the actual test result, and sometimes even do not need to paste the filter capacitor.

The GSM antenna is the main source of coupling interference for TDD, so users should pay attention to keeping the audio trace away from the GSM antenna and VBAT during PCB layout and routing. The filter capacitor of the audio is preferably placed close to the module end and placed next to the interface end. The audio output should be routed according to the differential signal rules.

The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the “zizi” sound at the SPK output. Therefore, it is better to connect in parallel with the input of the Audio PA in the schematic design. Some large capacitance capacitors and series magnetic beads.

The conducted interference is also strongly related to TDD and GND. If GND is not handled well, many high-frequency interference signals will interfere with MIC and Speaker through devices such as bypass capacitors, so users should ensure good performance of GND during PCB design.

5.2.7. Other

The serial port interface of the module should also be kept as short as possible. It is best to walk in a group when routing, and do not distract the wires.

6. Electrical, Reliability

6.1 Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 6.2: Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	-	-	6	V
VBUS	-	-	10.5	V
Peak current	-	-	3	A

6.2 Working Temperature

The table below shows the operating temperature range of the module:

Table 6.2: Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	℃
Storage temperature	-40	-	90	℃

6.3 Working Voltage

Table 6.3: Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.4		4.35	V
VBUS	4	5	6	V
Hardware shutdown voltage	2.5	2.8	-	V

6.4 Digital Interface Features

Table 6.4: Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	1.17	-	-	V
V_{IL}	Input low level voltage	-	-	0.63	V
V_{OH}	Output high level voltage	1.35	-	-	V
V_{OL}	Output low level voltage	-	-	0.45	V

6.5 SIM_VDD Characteristics

Table 6.5: SIM_VDD Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
V_O	Output voltage	-	3	-	V
		-	1.8	-	
I_O	Output current	-	-	55	mA

6.6 PWRKEY Feature

Table 6.6: PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	2000			ms

6.7 VCOIN Feature

Table 6.7: VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
$VCOIN_{-IN}$	VCOIN input voltage	2	3	3.25	V
I_{RTC-IN}	VCOIN Current consumption	-		3	uA
$VCOIN_{-OUT}$	VCOIN Output voltage	-	3	-	V
$I_{RTC-OUT}$	VCOIN Output current	-		2	mA

6.8 Current Consumption (VBAT = 3.8V)

Table 6.8: Current consumption

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
VBAT	voltage	Voltage must be between the maximum and minimum values	3.4	3.8	4.2	V
Ivbat	Average	Shutdown mode	-	-	65	uA

	current	GSM Standby power consumption	-	-	4.0	mA
		WCDMA Standby power consumption	-	-	3.9	mA
		TD-S Standby power consumption	-	-	4.0	mA
		CDMA Standby power consumption	-	-	3.8	mA
		FDD Standby power consumption			4.45	mA
		TDD Standby power consumption			3.5	mA
	Call Current consumption	GSM900 CH62 32dBm	-	-	250	mA
		WCDMA2100 CH10700 22.5 dBm	-	-	550	mA
	Digital transmission	GPRS GSM900 CH62 PCL5 1DL 4UL	-	-	TBD	mA
		EGPRS GSM900 CH62 PCL8 1DL 4UL	-	-	TBD	mA
Imax	Peak current	Power control at maximum output power	-	-	3	A

6.9 Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling, and operating modules.

6.10 Module Operating Frequency Band

The table below lists the operating frequency bands of the module and complies with the 3GPP TS 05.05 technical specification.

Table 6.9: Module Operating Band

Frequency band	Receive	Transmission	Physical channel
GSM850	869～894MHz	824～849MHz	128~251
EGSM900	925～960MHz	880～915MHz	0~124，975~1023
DCS1800	1805 ～ 1880MHz	1710 ～ 1785MHz	512~885
WCDMA B1	2110 ～2170 MHz	1920～ 1980 MHz	TX: 9612~9888
			RX: 10562~10838
WCDMA B2	1930 ～1990 MHz	1850 ～1910 MHz	TX: 9262~9538
			RX:9662~9938
WCDMA B4	2110 ～2155 MHz	1710～ 1755 MHz	TX:1312~1513
			RX: 1537~1738
WCDMA B5	869～894MHz	824～849MHz	TX: 4132~4233
			RX: 4357~4458
WCDMA B8	925～960MHz	880～915MHz	TX: 2712~2863

			RX: 2937~3088
WCDMA B9	1850 ~ 1890MHz	1750 ~ 1785MHz	TX: 8762~8912
			RX: 9237~9387
WCDMA B19	875 ~ 890MHz	830 ~ 845MHz	TX: 312~363
			RX: 712~763
CDMA BC0	869 ~ 894MHz	824 ~ 849MHz	1 ~ 799； 991 ~ 1023
TDSCDMA 1.9G	1880 ~ 1920 MHz	1880 ~ 1920MHz	9400 ~ 9600
TDSCDMA 2G	2010 ~ 2025 MHz	2010 ~ 2025MHz	10054 ~ 10121
LTE B1	2110 ~ 2170 MHz	1920 ~ 1980 MHz	TX: 18000 ~ 18599
			RX: 0~599
LTE B3	1805 ~ 1880 MHz	1710 ~ 1785 MHz	TX: 19200~19949
			RX: 1200~1949
LTE B5	869 ~ 894 MHz	824 ~ 849 MHz	TX: 20400~20649
			RX: 2400~2649
LTE B7	2620 ~ 2690 MHz	2500 ~ 2570 MHz	TX: 20750~21449
			RX:2750~3449
LTE B8	925 ~ 960 MHz	880 ~ 915 MHz	TX: 21450~21799
			RX:3450~3799
LTE B9	1805 ~ 1880 MHz	1750 ~ 1785 MHz	TX: 21800~22149
			RX: 3800~4149
LTE B12	729 ~ 746MHz	699 ~ 716MHz	TX: 23010~23179
			RX: 5010~5179
LTE B13	746 ~ 756 MHz	777 ~ 787 MHz	TX: 23180~23279
			RX: 5180~5279
LTE B17	734 ~ 746 MHz	704 ~ 716 MHz	TX: 23730~23849
			RX:5730~5849
LTE B19	875 ~ 890 MHz	830 ~ 845 MHz	TX: 24000~24149
			RX: 6000~6149
LTE B20	791 ~ 821 MHz	832 ~ 862 MHz	TX: 24150~24449
			RX: 6150~6449
LTE B26	859 ~ 894 MHz	814 ~ 849 MHz	TX: 26690~27039
			RX: 8690~9039
LTE B28b	773 ~ 803 MHz	718 ~ 748 MHz	TX: 27360~27659
			RX:9360~9659
LTE B38	2570 ~ 2620 MHz	2570 ~ 2620 MHz	37750 ~ 38249
LTE B39	1880 ~ 1920 MHz	1880 ~ 1920 MHz	38250 ~ 38649
LTE B40	2300 ~ 2400 MHz	2300 ~ 2400 MHz	38650 ~ 39649
LTE B41	2496 ~ 2690 MHz	2496 ~ 2690 MHz	39650 ~ 41589

Note: The SLM758's LTE TDD B41 band bandwidth is 100MHz (2555 ~ 2655 MHz), the

channel is 40240 ~ 41240.

6.11 RF Characteristics

The following table lists the conducted RF output power of the module, in accordance with 3GPP TS 05.05 technical specification, 3GPP TS 134121-1 standard.

Table 6.10: Conducted Output Power

Frequency band	Standard output power (dBm)	Output power tolerance (dBm)
GSM850、EGSM900	33dBm	±2
DCS1800	30dBm	±2
WCDMA	24 dBm	+1/-3
CDMABC0	25 dBm	±2
TDSCDMA	24 dBm	+1/-3
LTE	23 dBm	±2.7

6.12 Module Conduction Receiving Sensitivity

The table below lists the conducted receive sensitivity of the module and is tested under static conditions.

Table 6.11: Conducted Receive Sensitivity

Frequency band	Receive sensitivity (typical)	Receive sensitivity (maximum)
GSM850、EGSM900	<-108dBm	3GPPrequirements
DCS1800	<-108dBm	3GPPrequirements
WCDMAB1	<-109 dBm	3GPPrequirements
WCDMAB5	<-109 dBm	3GPPrequirements
CDMABC0	<-110 dBm	3GPPrequirements
TDSCDMA1.9G	<-110 dBm	3GPPrequirements
TDSCDMA2G	<-110 dBm	3GPPrequirements
LTEFDD/TDD	See Table 6.12	3GPPrequirements

Table 6.12: LTE Reference Sensitivity 3GPP Dual Antenna Requirements (QPSK)

E-UTRA Frequency band number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD

6	-	-	-100	-97			FDD
7	-	-	-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
9	-	-	-99	-96	-94.2	-93	FDD
10	-	-	-100	-97	-95.2	-94	FDD
11	-	-	-100	-97			FDD
12	-101.7	-98.7	-97	-94			FDD
13			-97	-94			FDD
14		-	-97	-94			FDD
...							
17	-	-	-97	-94			FDD
18	-	-	-100[7]	-97[7]	-95.2[7]	-	FDD
19	-	-	-100	-97	-95.2	-	FDD
20			-97	-94	-91.2	-90	FDD
21			-100	-97	-95.2		FDD
22			-97	-94	-92.2	-91	FDD
23	-104.7	-101.7	-100	-97	-95.2	-94	FDD
24			-100	-97			FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
26	-102.7	-99.7	-97.5[6]	-94.5[6]	-92.7[6]		FDD
27	-103.2	-100.2	-98	-95			FDD
28		-100.2	-98.5	-95.5	-93.7	-91	FDD
31	-99.0	-95.7	-93.5				FDD
...							
33	-	-	-100	-97	-95.2	-94	TDD
34	-	-	-100	-97	-95.2	-	TDD
35	-106.2	-102.2	-100	-97	-95.2	-94	TDD
36	-106.2	-102.2	-100	-97	-95.2	-94	TDD
37	-	-	-100	-97	-95.2	-94	TDD
38	-	-	-100	-97	-95.2	-94	TDD
39	-	-	-100	-97	-95.2	-94	TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-98	-95	-93.2	-92	TDD

6.13 WIFI Main RF Performance

The table below lists the main RF performance under WIFI conduction.

Table 6.13: Main RF performance parameters under WIFI conduction

Transmission performance(2.4G)				
	802.11B	802.11G	802.11N	
Transmit power (minimum rate)	19	16.5	15	dBm
Transmit power (maximum rate)	18	14.5	13	dBm
EVM (maximum rate)	20%	-27	-30	dB
Receiving performance(2.4G)				

Receiving sensitivity	802.11B	802.11G	802.11N	
Minimum rate	-96	-91	-90	dBm
Maximum rate	-89	-74	-72	dBm
Transmission performance(5G)				
	802.11A	802.11N	802.11AC	
Transmit power (minimum rate)	16	15	14	dBm
Transmit power (maximum rate)	13	12	10	dBm
EVM (maximum rate)	-25	-27	-32	dB
Receiving performance(5G)				
Receiving sensitivity	802.11A	802.11N	802.11AC (20M)	
Minimum rate	-89	-88.5	-88.5	dBm
Maximum rate	-74.5	-73	-67.5	dBm

Note: At the time of 5G plus FEM, the power under various standard modes was increased by 3DB, and the Receiving sensitivityn was increased by 1.5db.

6.14 BT Main RF Prformance

The table below lists the main RF performance under BT conduction.

Table 6.14: Main RF performance parameters under BT conduction

Transmission performance				
Transmit power	DH5	2DH5	3DH5	
	10	6	6	dBm
Receiving performance				
Receiving sensitivity	DH5	2DH5	3DH5	
	-94.5	-94.5	-86	dBm

6.15 GNSS Main RF Performance

The table below lists the main RF performance under GNSS conduction.

Table 6.15: Main RF performance parameters under GNSS conduction

GNSS working frequency band: 1575.42MHZ				
GNSS carrier-to-noise ratio CN0: 39dB/Hz				
GNSS sensitivity:	Capture (cold start)	Capture (hot start)	Track	
	-148	-156	-160	dBm
GNSS startup time	Hot start	Warm start	Cold start	
	2s	5s	40s	

7. Production

7.1. Top And Bottom Views Of The Module

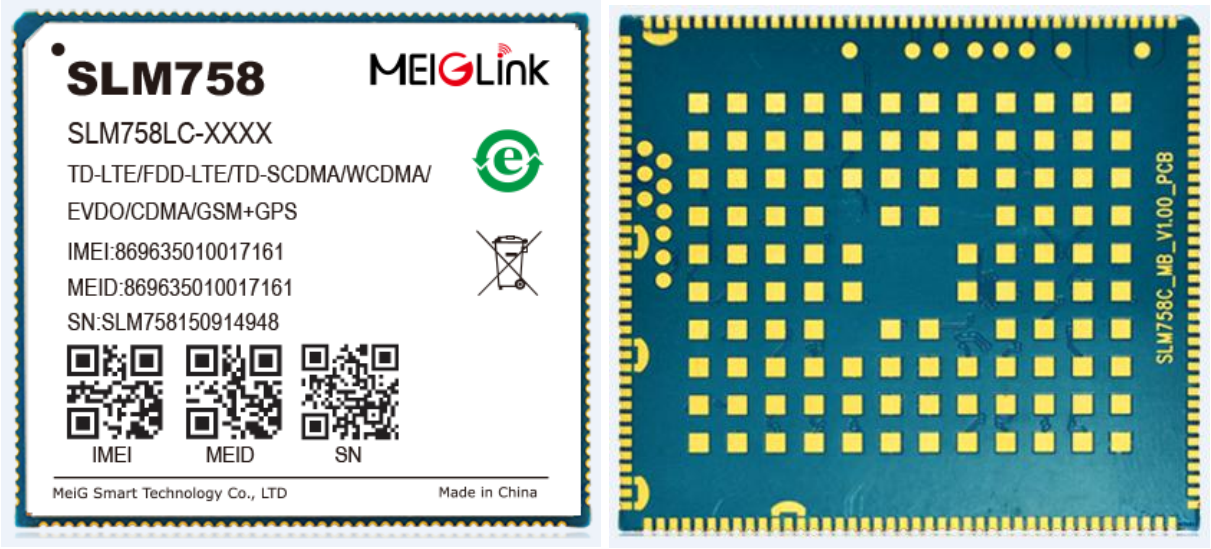


Figure 48: Module top and bottom views

7.2. Recommended Soldering Furnace Temperature Curve

Figure 49: Module recommended soldering furnace temperature curve

7.3. Humidity Sensitivity (MSL)

The SLM758 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of temperature <30 degrees and relative humidity <60%. Under ambient

conditions of temperature <40 degrees and relative humidity <90%, the shelf life is at least 6 months without unpacking. After unpacking, Table 22 lists the shelf life of the modules for different moisture sensitivity levels.

Table 7.1: Humidity sensitivity level distinction

Grade	Factory environment≦+30℃/60%RH
1	Indefinite quality in the environment≦+30℃/85% RH Under conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the time limit specified on the label.

After unpacking, the SMT patch should be taken within 168 hours under ambient conditions of <30 degrees and relative humidity <60%. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solderability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solderability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90 ℃ and as high as 125 ℃

7.4. Baking Requirements

Due to the humidity sensitivity of the module, the SLM758 should be thoroughly baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SLM758 should be baked for 192 hours in a cryogenic vessel at 40 ℃ +5 ℃/-0 ℃ and a relative humidity of less than 5%, or in a high temperature vessel at 80 ℃±5 ℃.Bake for 72 hours. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 7.2: Baking requirements:

Baking temperature	Humidity	Baking time
40 ℃±5 ℃	<5%	192 hours
120 ℃±5 ℃	<5%	4 hours

8. Support Peripheral Device List

Peripheral devices can support the devices included in the platform QVL. The following are the software default adapters.

Table 8.1: List of supported display models

Vendor	Drive IC	Specification
Zoneway	HX8394F	1280x720
Zoneway	OMT1287	1280x720

Table 8.2: Support for Camera Model List

Vendor	Drive IC	Specification
JinshengXin Vision	GC8024	8M
JinshengXin Vision	OV5670	5M
Sunny optical	S5K3L8	8M
Sunny optical	S5K5E8	5M

Table 8.3: Support for touch screen model list

Vendor	Drive IC	Specification
Zoneway	GT9147	5"
Zoneway	GT970	5"

Table 8.4: Support for G Sensor Model List

Vendor	Model	Specification
Bosch	BMA223	3-Axis,8-bit
Kionix	KXTJ2-1009	3-Axis,8-bit
SILAN	SC7A20TR	3-Axis,8-bit

Table 8.5: Support for Ecompass Model List

Vendor	Model	Specification
AKM	AK09918	3-Axis,14-bit

GMEMS	GMC303	3-Axis,14-bit

Table 8.6: Support PS/ALS Sensor Model List

Vendor	Model	Specification
LITEON	LTR-553ALS-01	ALS+PS

Table 8.7: Support for Gyro Sensor Model List

Vendor	Model	Specification
Bosch	BMI120	9-axis,16bit/16bit

Table 8.8: Peripheral Support List

Peripheral	Vendor	Model
Pressture sensor	Bosch	BMP280

9. Appendix

9.1. Related Documents

Table 9.1: Related documents

Serial number	File name	Comment
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)； Mobile Station (MS) conformance specification； Part 1： Conformance specification
[8]	AN_Serial Port	AN_Serial Port

9.2. Terms And Explanations

Table 9.2: Terms and explanations

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity

Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Phone book abbreviation	Explanations
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

9.3. Multiplexing function

Table 9.3: Multiplexing Functions

GPIO	Module pin	Reuse function		
		SPI	UART	I2C
1	261	MOSI		
2	260	MISO		
3	259	CS_N		SDA
4	258	CLK		SCL
4	11	MOSI	TX	
5	12	MISO	RX	
6	13	CS_N	CTS	SDA
7	14	CLK	RTS	SCL
8	232	MOSI		
9	231	MISO		
10	234	CS_N		SDA
11	233	CLK		SCL
12	15	MOSI	TX	
13	16	MISO	RX	
14	17	CS_N	CTS	SDA
15	18	CLK	RTS	SCL
16	256	MOSI	TX	
17	255	MISO	RX	
18	254	CS_N	CTS	SDA
19	253	CLK	RTS	SCL
20	176	MOSI	TX	
21	177	MISO	RX	
22	184	CS_N	CTS	SDA
23	185	CLK	RTS	SCL
137	267	MOSI		
138	266	MISO		
136	268	CS_N		SDA
135	269	CLK		SCL
96	197	MOSI		
97	198	MISO		
98	164	CS_N		SDA
99	165	CLK		SCL

Note: Blue is the default function

9.4. Safety Warning

Pay attention to the following safety precautions when using or repairing any terminal or mobile phone that contains modules. The user should be informed of the following safety information on the terminal device. Otherwise, Meig will not be responsible for any consequences caused by the user not following these warning actions.

Table 9.4: Security Warnings

Identification	Claim
	When you are at a hospital or medical facility, observe the restrictions on using your phone. If necessary, please turn off the terminal or mobile phone, otherwise the medical device may malfunction due to radio frequency interference.
	Turn off the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the aircraft. Ignoring the above will violate local laws and may result in a flight accident.
	Do not use mobile terminals or mobile phones in front of flammable gases. Turn off the mobile terminal when you are near an explosion, chemical factory, fuel depot, or gas station. It is dangerous to operate a mobile terminal next to any potentially explosive electrical equipment.
	The mobile terminal receives or transmits radio frequency energy when it is turned on. It can interfere with TV, radio, computer or other electrical equipment.
	Road safety first! Do not use a handheld terminal or mobile phone while driving, please use a hands-free device. Stop before using your handheld terminal or mobile phone.
	GSM mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

10. OEM/Integrators Installation Manual

10.1.Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part

15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

10.2.End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2APJ4-SLM758”
“Contains IC: 23860- SLM758“
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type Fixed External Antenna	2.4GHz band Peak Gain 0(dBi)	5.2GHz band Peak Gain 1(dBi)	5.3GHz band Peak Gain 1(dBi)	5.5GHz band Peak Gain 1(dBi)	5.8GHz band Peak Gain 1(dBi)
Antenna type Fixed External Antenna	BT Peak Gain 0(dBi)	WCDMA band 2 Peak Gain 7(dBi)	WCDMA band 4 Peak Gain -5.5(dBi)	WCDMA band 5 Peak Gain -6.5(dBi)	LTE band 2 Peak Gain 7(dBi)
Antenna type Fixed External Antenna	LTE band 4 Peak Gain 5.5(dBi)	LTE band 5 Peak Gain -6.5(dBi)	LTE band 7 Peak Gain -7(dBi)	LTE band 12 Peak Gain -6(dBi)	LTE band 13 Peak Gain -6(dBi)
Antenna type Fixed External Antenna	LTE band 17 Peak Gain -6(dBi)	LTE band 28 Peak Gain -5.5(dBi)			

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

10.3.Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

10.4.Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
List of applicable FCC rules
This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.

10.5.Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and
The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et
Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

10.6.Radiation Exposure Statement

This equipment complies with FCC/IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

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