# Circuit Description

## 1. Frequency Configuration

The receiver utilizes double conversion superheterodyne. The first IF is 73.05MHz and the second is 450KHz. The first local oscillator signal is supplied by PLL circuit. The second local oscillator signal (73.5MHz) is generated from TCXO (73.5MHz); The PLL circuit also generates the frequencies needed in the transmitter (See Fig.1).

Frequency Range: U1: 400 MHz—470MHz
U2: 450 MHz—512MHz
U3: 480 MHz—526MHz
U4: 440 MHz—490MHz
U5: 350 MHz—400MHz;

## 2. Receiver Circuit

The receiver section configuration is shown as Fig. 1.

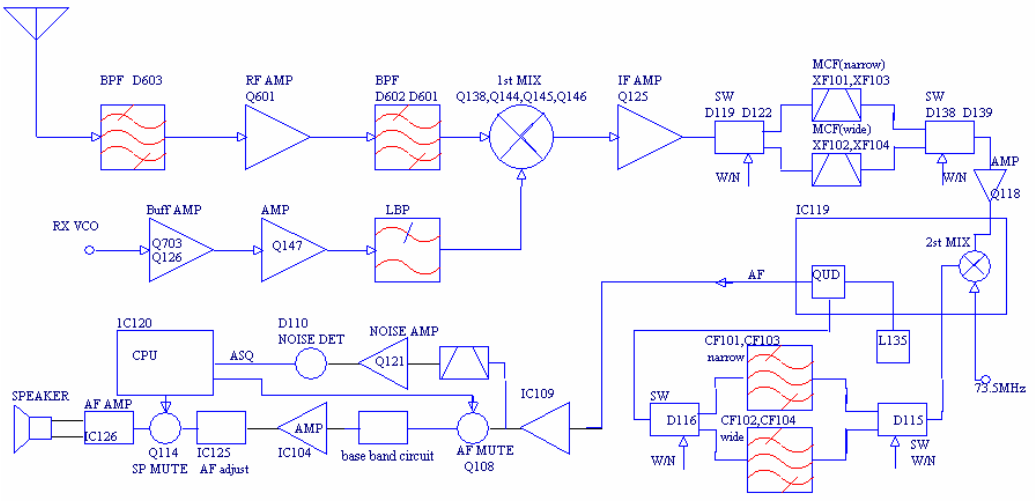


Figure 1 Receiver Section Configuration

### 2.1 RF AMP BPF

It consists of BPF (D603, D602, D601) and RF amplifier (Q601). The range of bandpass frequency (U1: 400 MHz—470MHz；U2: 450 MHz—512MHz U3: 480 MHz—526MHz；U4: 440 MHz—490MHz；U5: 350 MHz—400MHz). The signal is filtered by the RF Amp BPF to eliminate unwanted signals before going to the first mixer.

### 2.2 The First Mixer

The signal from RF AMP BPF is mixed with the first local oscillator signal from PLL circuit in the double-balance mixer (Q138, Q144, Q145, Q146) to generate a 73.05MHz first IF signal. The first IF signal is then fed through two crystal filters (N: XF101, XF103; W: XF102, XF104) to further remove spurious signals.

### 2.3 IF Amplifier

The first IF signal is amplified by Q125, Q118 and then enters IC119（TA31136FN）. The signal is mixed with the second local oscillator signal (73.05MHz) to create a 450KHz second IF signal. The second IF signal is then fed to a ceramic filter (N: CF101, CF103; W: CF102, CF104) to eliminate unwanted signals. The resulting signal is detected by IC119 and output from Pin9 as an AF signal.

### 2.4 AF Amplifier

The AF signal from IC119 is amplified by IC109 before being filtered. The resulting AF signal passes through Q108（AF MUTE）and IC121(electronic switch) , then is amplified by IC106 ( the received signalling is inputted into CPU for decoding) and IC104. The amplified signal is fed to IC125 (volume control) and Q114 (SP MUTE) before entering AF AMP (IC126). The outputted AF signal is then delivered to the speaker through control panel.

### 2.5 Squelch

The AF signal from IC119 is amplified by IC109 again, and then filtered to remove noise signals. The noise signal is amplified by Q121 and rectified by D110 to produce an ASQ level. The ASQ level is then compared in CPU (IC120) to generate a level which controls AF MUTE and SP MUTE. IC120 determines whether to output sounds from the speaker by controlling Q108, Q114.

# 3. Transmitter Circuit

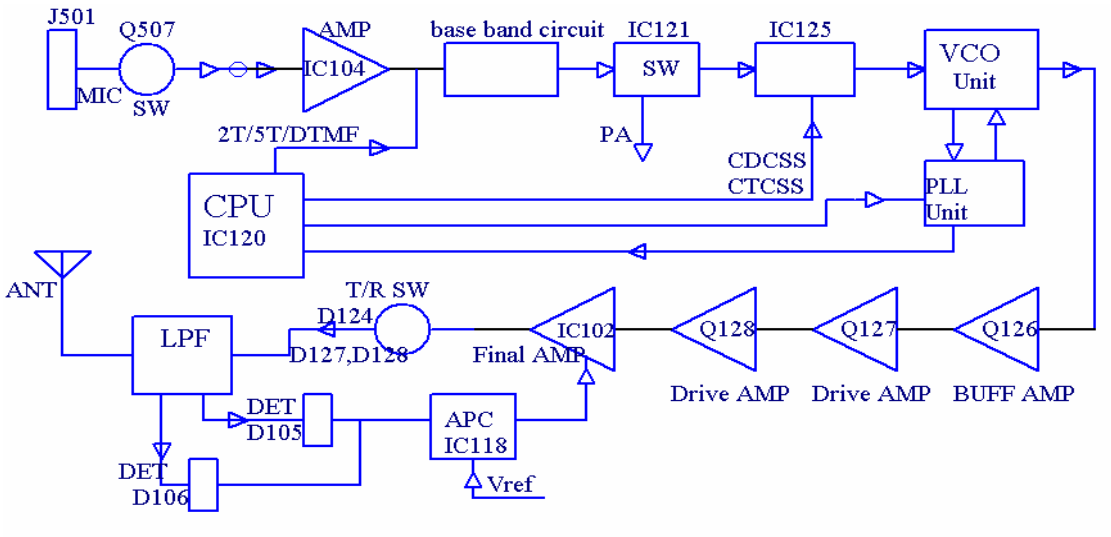


Figure 2 Transmitter Section Configuration

### 3.1 MIC Circuit and Modulation Circuit

The AF signal from MIC is amplified by IC104 after passing through the MIC control switch (Q507). The resulting signal is then amplified by IC106 and pre-emphasized, encoded. It is passed to IC121 (electronic switch) before reaching IC125. The signalling is inputted into IC125 and enters VCO for modulation.

### 3.2 Driver and Final Power Amplifier Circuit

TX-RF signal is outputted from Q703 in VCO circuit and amplified by Q126, Q127 and Q128. The amplified signal is then fed to IC102 (Power Module) and passes through LPF before reaching the antenna terminal.

### 3.3 APC

The APC is used to keep the power output at a constant preset value. D105 and D106 transform the signal from detector into DC voltage which is then compared with the reference voltage from CPU in IC118 and outputted as DC control voltage. The DC control voltage controls the output power by controlling the grid of IC102.

# 4. PLL Circuit

PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission. PLL circuit consists of TX frequency oscillator (Q701), RX frequency oscillator (Q702), buffer amplifier (Q703), RF amplifier (Q124), PLL IC (IC801), LPF (Q804, Q805) and TX/RX VCO control switch (Q704, Q706).

In transmit mode, IC120 transmits the frequency data to PLL IC. Q704 is turned on to activate TX VCO. The outputted signal is amplified by Q703, Q124, and then divided by PLL IC into 2.5KHz, 5KHz or 6.25KHz signal. The divided signal is compared with 2.5KHz, 5KHz or 6.25KHz reference signal from 16.8MHz crystal oscillator (2.5 PPM frequency stability) in the phase comparator. The frequency control voltage outputted from the phase comparator is sent to TX VCO after passing through LPF (Q804, Q805). In the meantime, modulation signal (TX) is passed to TX VCO for frequency modulation.

The working principle in receive mode is similar to that in transmit mode.

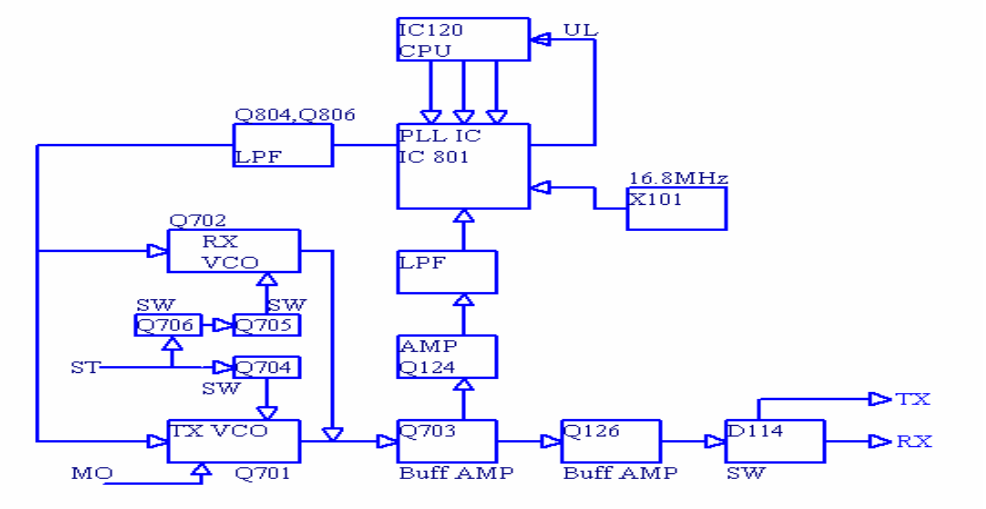


Figure 3 PLL Circuit

# 5. Control Circuit

Circuit in this section is comprised of CPU, reset IC, power supply controller and flash ROM.

## 5.1 CPU

IC120 (CPU) operates at 9.8304MHz. It controls the data transmission between receive circuit, transmit circuit, control circuit, display circuit and peripheral circuit.

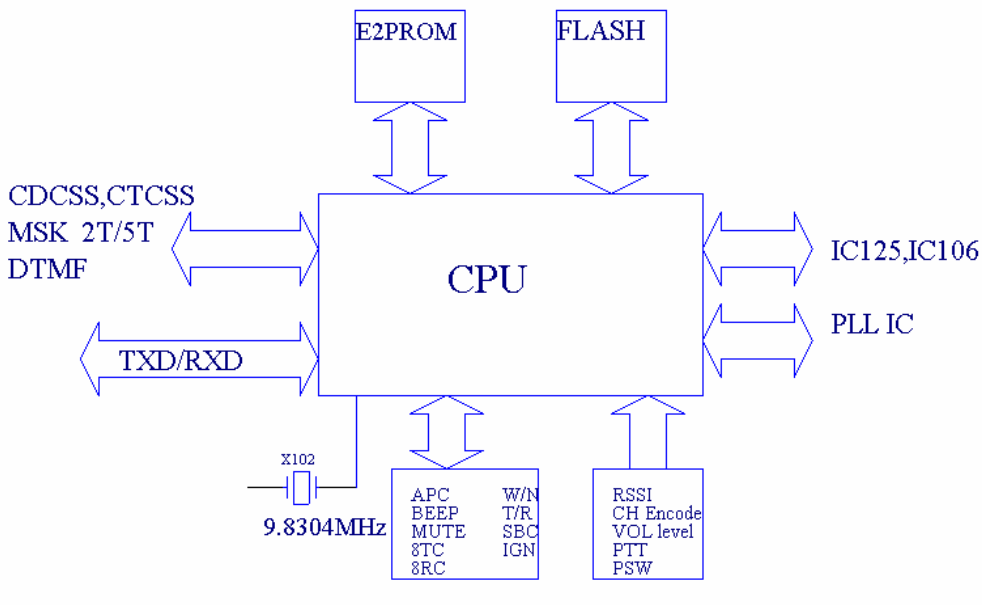


Figure 4 Control Circuit

## 5.2 Power Supply

Power supply of the radio is derived from the battery which supplies battery B+. D135 and D137 are over-voltage protection Diodes. Power-on/off can be controlled by software.

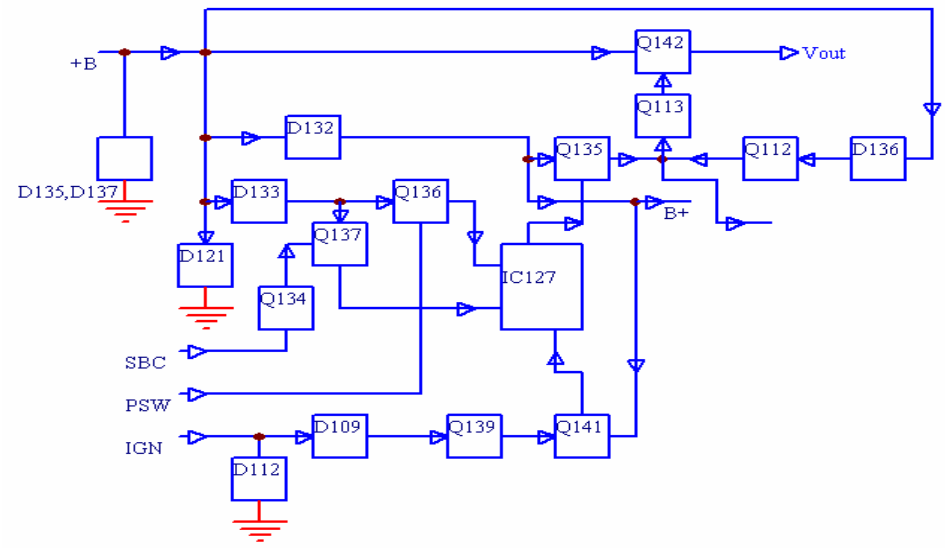


Figure 5 Power Switch Circuit

Vout provides power supply to IC115, IC114, IC113, and IC111, which produces 8V, 9V, 5V, and 3.3V voltage to the circuit.

## 6. Display Circuit

Display circuit is comprised of CPU (IC503), LCD module, LED and other components. Radio features are programmable by PF1-PF6. Data is displayed on the 12-digit and 4-digit dot matrix LCD in alphanumeric form.

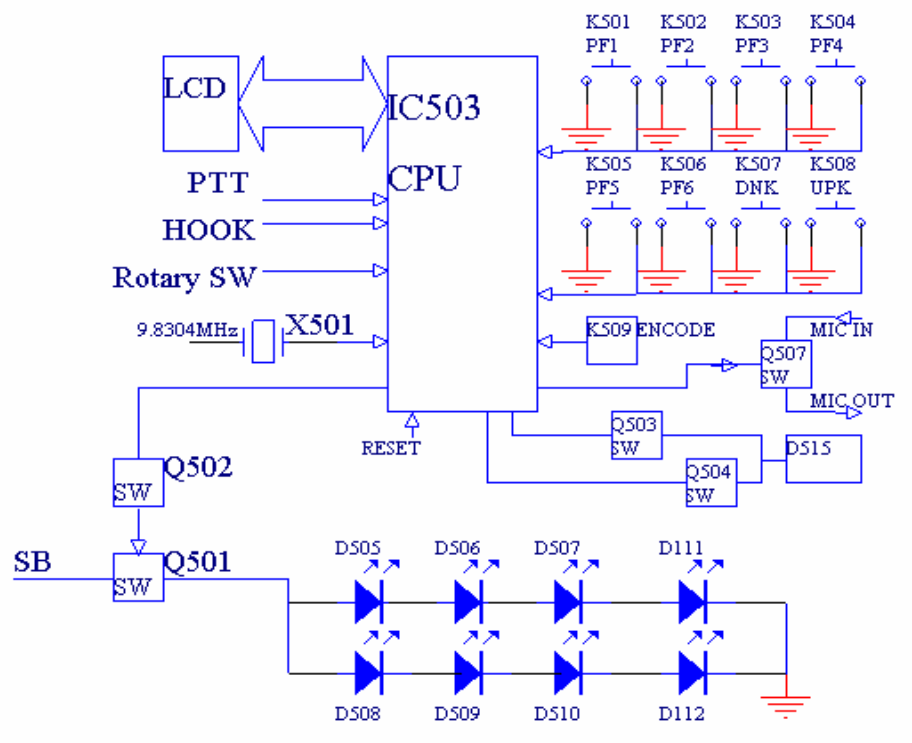


Figure 6 Display Circuit