Fibocom

Perfect Wireless Experience
完美无线体验

Applicability type

No.	Product model	Description
1	SS808-NA	16+2 eMCP,4G version

Copyright

Notice

The document is subject to update from time to time owing to the product version upgrade or other reasons. Unless otherwise specified, the document only serves as the user guide. All the statements, information and suggestions contained in the document do not constitute any explicit or implicit guarantee.

Trademark

The trademark is registered and owned by Fibocom Wireless Inc.

Versions

Version	Author	Assessor	Approver	Update Date	Description
V1.0.0	Gaoying	Tumin	Chenguojiang	07-12-2019	Initial version
V1.0.1	Gaoying	Tumin	Chenguojiang	07-12-2019	1、add VBAT line width no narrow than 3mm

Contents

Figure Index

Table Index

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: （1）This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

1 Reorient or relocate the receiving antenna.
2 Increase the separation between the equipment and receiver.
3 Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
4 Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:

1 Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
2 This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device is intended only for OEM integrators under the following conditions:
1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed for use with this device is 3 dBi.
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: ZMOSS808NA”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

1 Introduction

1.1 Instruction

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SS808 series module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the SS808 series module and develop products.

1.2 Reference Standards

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: U(U)SIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment ((U)SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (U(U)SIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (U(U)SIM) Application Toolkit (USAT)
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

1.3 Related Document

NA

2 Product Overview

2.1 Product Specification

SS808 series smart module integrates core components such as Baseband, eMCP, PMU, Transceiver, PA; it supports long distance multi-mode communication such as FDD/TDD-LTE,WCDMA and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. SS808 series module is embedded with Android operating system and support various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 1 Support Bands

Mode	Band
WCDMA	Band 2/4/5
FDD-LTE	Band 2/4/5/7/12/13/25/26/66
TDD-LTE	Band41(2496MHz ~ 2690MHz)
WIFI 802.11a/b/g/n/ac	2402-2482 MHz;5180-5825MHz
BT4.2 LE	2402-2480 MHz
GNSS	GPS/GLONASS /BeiDou

2.2 Product Specification

The SS808 module is available in 232 LCC+LGA package that includes 148 LCC pins and 84 LGA pins. The dimension is 41mm×41mm×2.80mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring and multimedia terminals.

Table 2 Main Performance

Performance	Description
Power	DC 3.5~4.2V, typical voltage: 3.8V
Application CPU	ARM Cortex-A53 microprocessor cores at 1.8 GHz, 64-bit processor, one quad with 512 KB L2 cache + one quad with 512 KB L2 cache
Memory	2GB LPDDR3+ 16 GB eMMC Flash

Performance	Description
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation 3GPP R6 CAT6 HSUPA: Maximum uplink rate 5.76Mbps 3GPP R8 CAT24 DC-HSPA+: Maximum downlink rate 42Mbps
LTE features	Support FDD/TDD CAT4 Support 1.4-20M RF bandwidth Downlink support multi-user MIMO Maximum uplink rate 50Mbps, maximum downlink rate 150Mbps
WLAN features	Support 2.4G and 5G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, the maximum rate up to 433Mbps
Bluetooth features	BT4.2 (BR/EDR+BLE)
Satellite positioning	GPS/GLONASS/BeiDou
SMS	Text and PDU modes Point-to-Point MO and MT SMS cell broadcast SMS storage: stored in the module by default
LCD interface	Two 4-Lane MIPI_DSI interfaces Support maximum 1920*1200 60fps
Camera interface	Two 4-Lane MIPI_CSI interface, up to 2.1Gbps per lane, support 2 or 3 cameras 4-Lane interface supports up to 21MP pixels
Audio interface	Audio Input: 2 analog MIC inputs Internal integrated bias Audio output: Class AB stereo headphone output Class AB differential handset output Class D differential speaker amplifier output
USB interface	USB2.0 HS interface, with data transfer rate up to 480 Mbps USB3.0 SS interface, with data transfer rate up to 5Gbps Support USB OTG

Performance	Description
(U)SIM interface	Two (U)SIM card interfaces supporting (U)SIM card: 1.8/3V adaptive Support dual (U)SIM dual standby (default dual) Support hot plug (close by default)，support hot plug (close by default)
UART interface	Three UART serial interfaces, with the maximum rate up to 4Mbps One 4-line serial interface supporting RTS and CTS hardware flow control One 2-line serial interface One 2-line debug serial interface
SDIO interface	Support SD3.0, 4bit SDIO; SD card supports hot plug
I2C interface	Multiple I2C interfaces, with a maximum speed up to 3.4 Mbps, and can be used for peripherals such as TP, Camera, and Sensor
ADC interface	Universal ADC, resolution 15 bits
RTC	Support
Antenna interface	MAIN antenna, DRX antenna, GNSS antenna, WIFI/BT antenna interface
Physical characteristics	Dimension: 41mm×41mm×2.80mm Encapsulation: 148 LCC + 84 LGA Weight: TBD
Temperature range	Operating temperature: -30°C~75°C [1)] Storage temperature: -40°C ~ 85°C
Software update	USB/OTA/SD
RoHS	RoHS Compliant

Note:

1）When the module is operating in this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Pin definitions

2.3.1 Pin assignment

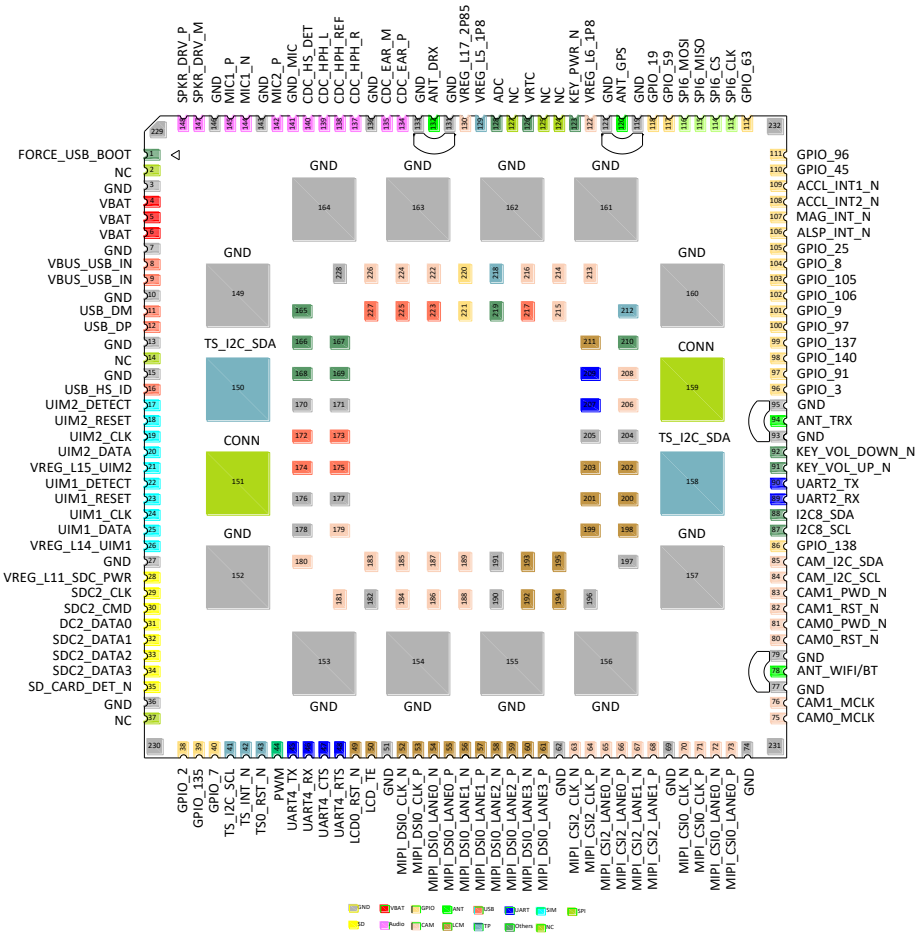

Figure 1 Pin Assignment

Note:

"NC" represent No Connect，the pin for this position is reserved and does not need to be connected.

2.3.2 Pin description

Table 3 I/O Description Parameters

Symbol	Description
I/O	Input/Output
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input

Symbol	Description
AO	Analog Output
OD	Open Drain

Descriptions of SS808 module pins are presented in the following table:

Pin Name	Pin #	I/O	Pin Description	Note
Power				
VBAT	4,5,6	PI	Main power input	Voltage range: 3.5~4.2V, recommend 3.8V
VRTC	126	PI/PO	RTC clock power supply	Voltage range: 2.0~3.25V, recommend 3.0V
VREG_L2_1P1	226	PO	1.1V voltage output	Drive current TBD
VREG_L5_1P8	129	PO	1.8V voltage output	Drive current TBD
VREG_L6_1P8	122	PO	1.8V voltage output	Drive current TBD
VREG_L10_2P8	224	PO	2.8V voltage output	Drive current TBD
VREG_L11_SDC_PWR	28	PO	SD card power supply, 2.95V	Drive current TBD
VREG_L14_UIM1	26	PO	(U)SIM card 1 power supply	1.8/3V adaptive, TBD
VREG_L15_UIM2	21	PO	(U)SIM card 2 power supply	1.8/3V adaptive, TBD
VREG_L17_2P85	130	PO	2.85V voltage output	Drive current TBD
VREG_L22_2P8	222	PO	2.8V voltage output	Drive current TBD
GND	3,7,10,13,15,27,36,51,62,69,74,77,79,93,95,119,121,131,133,136,143,146,149,152,153,154,155,156,157,160,161,162,163,164,170,171,176,177,178,182,190,191,196,197,204,205,228,229,230,231,232		GND	51 Pins
External PMI Interface				
PON_1	165	DI	PMI trigger power on signal	

Pin Name	Pin #	I/O	Pin Description	Note
PM8953_GPIO_8	168	DO	PMIC GPIO	
SPMI_DATA	167	I/O	SPMI data signal	
SPMI_CLK	169	DO	SPMI clock signal	
PM_PON_RESET_N	166	DO	Power_on reset signal	
Key				
KEY_PWR_N	123	DI	Power key	Active low, don't add pull-up circuit
KEY_VOL_UP_N	91	DI	Volume +	Active low
KEY_VOL_DOWN_N	92	DI	Volume -	Volume- key by default, active low. Can be Configured as reboot, don't add pull-up circuit
(U)SIM card interface				
UIM1_DATA	25	I/O	(U)SIM card 1 data	
UIM1_CLK	24	DO	(U)SIM card 1 clock	
UIM1_RESET	23	DO	(U)SIM card 1 reset	
UIM1_DETECT	22	DI	(U)SIM card 1 plug detection	Default disabled
UIM2_DATA	20	I/O	(U)SIM card 2 data	
UIM2_CLK	19	DO	(U)SIM card 2 clock	
UIM2_RESET	18	DO	(U)SIM card 2 reset signal	
UIM2_DETECT	17	DI	(U)SIM card 2 plug detection	Default disabled
VREG_L14_UIM1	26	PO	(U)SIM card 1 power supply	1.8/3V adaptive
VREG_L15_UIM2	21	PO	(U)SIM card 2 power supply	1.8/3V adaptive

Pin Name	Pin #	I/O	Pin Description	Note
SD card interface				
SDC2_DATA3	34	I/O	SD card data interface	
SDC2_DATA2	33	I/O	SD card data interface	
SDC2_DATA1	32	I/O	SD card data interface	
SDC2_DATA0	31	I/O	SD card data interface	
SDC2_CLK	29	DO	SD card clock	
SDC2_CMD	30	I/O	SD card command interface	
SD_CARD_DET_N	35	DI	SD card detection	Active low by default
VREG_L11_SDC_PWR	28	PO	SD card power supply, 2.95V	
I2C interface				
I2C8_SCL	87	OD	I2C clock	For sensor default
I2C8_SDA	88	OD	I2C data	For sensor default
TS_I2C_SCL	41	OD	I2C clock	For touch panel default
TS_I2C_SDA	150,158	OD	I2C data	For touch panel default
CAM_I2C_SCL	84	OD	I2C clock	For camera default
CAM_I2C_SDA	85	OD	I2C data	For camera default
CAM2_SCL	206	OD	I2C clock	For camera default
CAM2_SDA	208	OD	I2C data	For camera default
USB interface				
VBUS_USB_IN	8,9	PI	5V input	Only have detect function
USB_DP	12	I/O	USB 2.0 differential data +	

Pin Name	Pin #	I/O	Pin Description	Note
USB_ DM	11	I/O	USB 2.0 differential data -	
USB_HS_ID	16	DI	USB OTG detection	
USB1_SS_RX_P	173	DI	USB 3.0 differential data receive +	
USB1_SS_RX_M	175	DI	USB 3.0 differential data receive -	
USB1_SS_TX_P	172	DO	USB 3.0 differential data transmit +	
USB1_SS_TX_M	174	DO	USB 3.0 differential data transmit -	
USB_SS_SWITCH_SEL	217	DO	USB Type-C switch control input	
USB_CC2	223	AI/AO	USB Type-C connector configuration channel	
USB_CC1	227	AI/AO		
USB_VCONN	225	AI	Power input (5 V, 210 mA from VBUS) to drive active cables	
UART interface				
UART2_TX	90	DO	UART2 data transmit	Debug serial port default
UART2_RX	89	DI	UART2 data receive	
UART4_TX	45	DO	UART4 data transmit	
UART4_RX	46	DI	UART4 data receive	
UART4_CTS	47	DI	UART4 clear to send	
UART4_RTS	48	DO	UART4 request to send	
UART5_TX	209	DO	UART5 data transmit	
UART5_RX	207	DI	UART5 data receive	
SPI interface				

Pin Name	Pin #	I/O	Pin Description	Note
SPI6_CLK	113	DO	SPI clock	
SPI6_CS	114	DO	SPI chip select	
SPI6_MISO	115	DI	SPI Master input slave output	
SPI6_MOSI	116	DO	SPI Master output slave input	
LCD interface				
MIPI_DSI0_CLK_P	53	AO	Main LCD MIPI clock +	
MIPI_DSI0_CLK_N	52	AO	Main LCD MIPI clock -	
MIPI_DSI0_LANE0_P	55	AI/AO	Main LCD MIPI Lane 0+	
MIPI_DSI0_LANE0_N	54	AI/AO	Main LCD MIPI Lane 0-	
MIPI_DSI0_LANE1_P	57	AI/AO	Main LCD MIPI Lane 1+	
MIPI_DSI0_LANE1_N	56	AI/AO	Main LCD MIPI Lane 1-	
MIPI_DSI0_LANE2_P	59	AI/AO	Main LCD MIPI Lane 2+	
MIPI_DSI0_LANE2_N	58	AI/AO	Main LCD MIPI Lane 2-	
MIPI_DSI0_LANE3_P	61	AI/AO	Main LCD MIPI Lane 3+	
MIPI_DSI0_LANE3_N	60	AI/AO	Main LCD MIPI Lane 3-	
LCD0_RST_N	49	DO	Main LCD reset	
MIPI_DSI1_CLK_P	192	AO	Sub-LCD MIPI clock+	
MIPI_DSI1_CLK_N	193	AO	Sub-LCD MIPI clock-	
MIPI_DSI1_LANE0_P	194	AI/AO	Sub-LCD MIPI Lane 0+	
MIPI_DSI1_LANE0_N	195	AI/AO	Sub-LCD MIPI Lane 0+	
MIPI_DSI1_LANE1_P	198	AI/AO	Sub-LCD MIPI Lane 1+	
MIPI_DSI1_LANE1_N	199	AI/AO	Sub-LCD MIPI Lane 1-	

Pin Name	Pin #	I/O	Pin Description	Note
MIPI_DSI1_LANE2_P	200	AI/AO	Sub-LCD MIPI Lane 2+	
MIPI_DSI1_LANE2_N	201	AI/AO	Sub-LCD MIPI Lane 2-	
MIPI_DSI1_LANE3_P	202	AI/AO	Sub-LCD MIPI Lane 3+	
MIPI_DSI1_LANE3_N	203	AI/AO	Sub-LCD MIPI Lane 3-	
LCD1_RST_N	216	DO	Sub-LCD reset signal	
PWM	44	DO	LCD backlight PWM control	
LCD1_BL_EN	211	DO	Sub-LCD backlight enable control	
LCD_TE	50	DI	LCD synchronization signal	Keep floating if unused
Touch panel interface				
TS0_INT_N	42	DI	Main LCD TP interrupt	
TS0_RST_N	43	DO	Main LCD TP reset	
TS1_INT	212	DI	Sub-LCD TP interrupt	
TS1_RST_N	218	DO	Sub-LCD TP reset	
Camera interface				
MIPI_CSI2_CLK_P	64	AO	Rear camera MIPI clock +	
MIPI_CSI2_CLK_N	63	AO	Rear camera MIPI clock -	
MIPI_CSI2_LANE0_P	66	AI/AO	Rear camera MIPI Lane0 +	
MIPI_CSI2_LANE0_N	65	AI/AO	Rear camera MIPI Lane0 -	
MIPI_CSI2_LANE1_P	68	AI/AO	Rear camera MIPI Lane1 +	
MIPI_CSI2_LANE1_N	67	AI/AO	Rear camera MIPI Lane1 -	
MIPI_CSI2_LANE2_P	181	AI/AO	Rear camera MIPI Lane2 +	
MIPI_CSI2_LANE2_N	183	AI/AO	Rear camera MIPI Lane2 -	

Pin Name	Pin #	I/O	Pin Description	Note
MIPI_CSI2_LANE3_P	180	AI/AO	Rear camera MIPI Lane3 +	
MIPI_CSI2_LANE3_N	179	AI/AO	Rear camera MIPI Lane3 -	
CAM0_MCLK	75	DO	Rear camera master clock	
CAM0_RST_N	80	DO	Rear camera reset	
CAM0_PWD_N	81	DO	Rear camera power down	
MIPI_CSI0_CLK_P	71	AO	Front camera MIPI clock +	
MIPI_CSI0_CLK_N	70	AO	Front camera MIPI clock -	
MIPI_CSI0_LANE0_P	73	AI/AO	Front camera MIPI Lane0 +	
MIPI_CSI0_LANE0_N	72	AI/AO	Front camera MIPI Lane0 -	
MIPI_CSI0_LANE1_P	184	AI/AO	Front camera MIPI Lane1 +	
MIPI_CSI0_LANE1_N	185	AI/AO	Front camera MIPI Lane1 -	
MIPI_CSI0_LANE2_P	186	AI/AO	Front camera MIPI Lane2 +	
MIPI_CSI0_LANE2_N	187	AI/AO	Front camera MIPI Lane2 -	
MIPI_CSI0_LANE3_P	188	AI/AO	Front camera MIPI Lane3 +	
MIPI_CSI0_LANE3_N	189	AI/AO	Front camera MIPI Lane3 -	
CAM1_MCLK	76	DO	Front camera master clock	
CAM1_RST_N	82	DO	Front camera reset	
CAM1_PWD_N	83	DO	Front camera power down	must not pull up before power on the module
CAM2_MCLK	213	DO	Depth camera master clock	
CAM2_RST_N	214	DO	Depth camera reset	
CAM2_PWD_N	215	DO	Depth camera power down	
IOVDD_1.8V_EN	210	DO	IOVDD Power enable	

Pin Name	Pin #	I/O	Pin Description	Note
AFVDD_2.8V_EN	219	DO	AFVDD Power enable	
Audio interface				
SPKR_DRV_P	148	AO	Louder speaker driver output+	
SPKR_DRV_N	147	AO	Louder speaker driver output-	
CDC_EAR_P	134	AO	Earpiece output+	
CDC_EAR_N	135	AO	Earpiece output-	
CDC_HPH_L	139	AO	Headphone output, left channel	
CDC_HPH_REF	138	-	Headphone ground reference	
CDC_HPH_R	137	AO	Headphone output, right channel	
CDC_HS_DET	140	AI	Headphone plug detection	
MIC2_P	142	AI	Headphone microphone input	
GND_MIC	141	/	Microphone bias filter ground	
MIC1_N	144	AI	Main microphone input -	
MIC1_P	145	AI	Main microphone input +	
Antenna interface				
ANT_TRX	94	I/O	2G/3G/4G main antenna	
ANT_DRX	132	AI	Diversity reception antenna	
ANT-WIFI/BT	78	I/O	WIFI/BT antenna	
ANT_GPS	120	AI	GNSS antenna	
INT interface				

Pin Name	Pin #	I/O	Pin Description	Note
ALSP_INT_N	106	DI	Ambient light sensor interrupt	
MAG_INT_N	107	DI	Magnetic sensor interrupt	
ACCL_INT2_N	108	DI	Accelerometer sensor interrupt	
ACCL_INT1_N	109	DI	Accelerometer sensor interrupt	
ADC interface				
ADC	128	AI	ADC detect	Can configure to 0.3V~VBAT
Force Download interface				
FORCE_USB_BOOT	1	DI	Force download	Active high 1.8V, must not pull up before power on the module
GPIO interface				
GPIO_2	38	I/O	General Purpose Input and Output.1.8V power domain	B-PD:nppukp
GPIO_3	96	I/O		B-PD:nppukp
GPIO_7	40	I/O		B-PD:nppukp
GPIO_8	104	I/O		B-PD:nppukp
GPIO_9	101	I/O		B-PD:nppukp
GPIO_19	118	I/O		B-PD:nppukp
GPIO_25	105	I/O		B-PD:nppukp
GPIO_45	110	I/O		B-PD:nppukp
GPIO_59	117	I/O		B-PD:nppukp
GPIO_63	112	I/O		B-PD:nppukp
GPIO_91	97	I/O		B-PD:nppukp

Pin Name	Pin #	I/O	Pin Description	Note
GPIO_96	111	I/O		B-PD:nppukp
GPIO_97	100	I/O		B-PD:nppukp
GPIO_105	103	I/O		B-PD:nppukp, must not pull up before power on the module
GPIO_106	102	I/O		B-PD:nppukp,must not pull up before power on the module
GPIO_113	220	I/O		Tuner control must not pull up before power on the module
GPIO_114	221	I/O		Tuner control, must not pull up before power on the module
GPIO_135	39	I/O		Tuner control
GPIO_137	99	I/O		Tuner control
GPIO_138	86	I/O		B-PD:nppukp
GPIO_140	98	I/O		B-PD:nppukp
Other Interfaces				
CONN	151	-	NC	
CONN	159	-	NC	
NC Interface				
NC	2,14,37,124,125,127		NC	Keep floating

备注：

标有 “Boot configuration”的管脚不允许硬件上拉。

3 Application Interface

3.1 Power supply

The SS808 provides three VBAT pins for connecting to external power supply source. The input range of power is 3.5V~4.2V and the recommended value is 3.8V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. In extreme cases, the peak current of the module can reach 3A and if the power supply capacity is insufficient that VBAT voltage drop below 3V, the module may be powered off or restarted. The VBAT voltage drop is shown as follow figure:

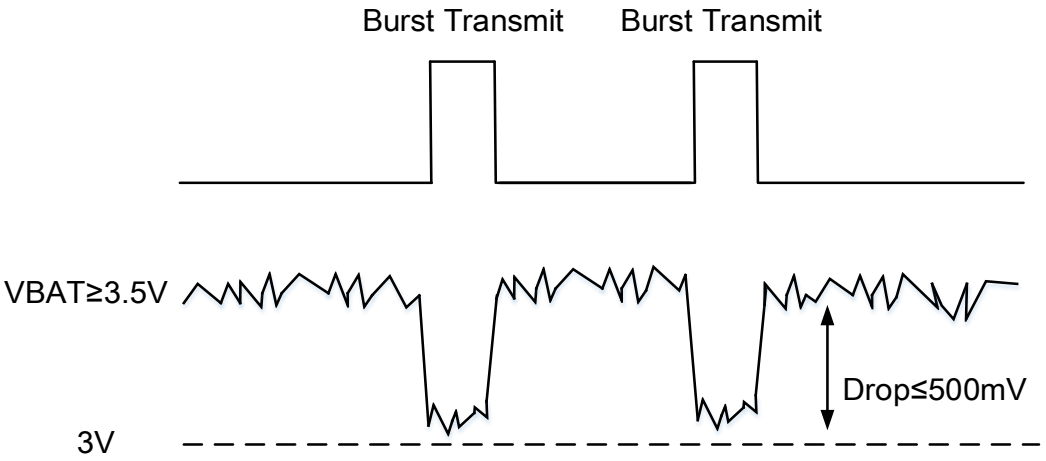

Figure 2 VBAT Voltage Drop

3.1.1 Power input

External power source supply the module by VBAT pins. To ensure the power voltage is no less than 3V, it is recommended to connect two 220μF tantalum capacitors with low ESR and decoupling capacitors of 1uF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides the PCB trace of VBAT should as short and wide as possible (no narrow than 3mm) and the ground plane of the power section should be flat. That can reduce the equivalent impedance of the VBAT trace and ensure at maximum transmit power, significant voltage drop will not occur at high currents.

Table 4 Power Supply

Parameters	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.2	V

The reference design of power supply is shown as follow figure:

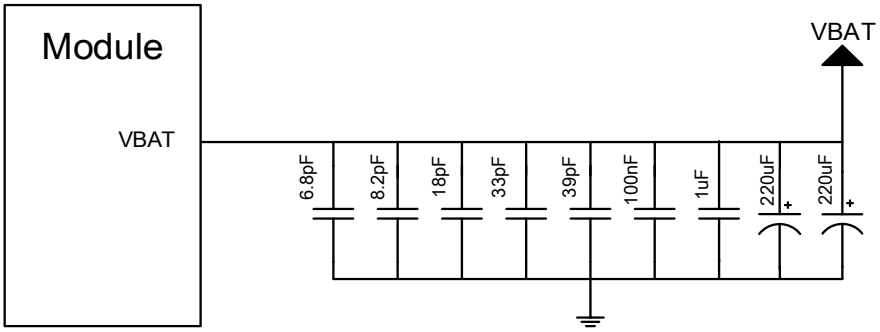

Figure 3 Power Supply Reference Design

Table 5 Power Supply Decoupling Capacitor Design

Recommended capacitor	Application	Description
220uF x 2	Voltage stabilizing capacitor	To reduce power fluctuations during module operation, it is required to adopt low ESR capacitor LDO or DCDC power requires not less than 440uF capacitor Battery power can be properly reduced to 100 ~ 220uF capacitor
1uF,100nF	Digital signal noise	Filter clock and digital signal interference
39pF,33pF,18pF,8.2pF,6.8pF		Filter high frequency interference

3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When powered on VBAT pin, the VRTC pin will output voltage. When cut off power supply of VBAT and want keep real time clock it needs to be powered by the external power (coin cell for example). The VRTC parameters are as follows:

Table 6 VRTC Parameters

Parameters	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.5	3.1	3.2	V
VRTC input voltage (clock works well)	2.0	3.0	3.25	V
VRTC input current (clock works well)		TBD	TBD	uA

The reference design of VRTC pin powered by external power source is shown as follow figure:

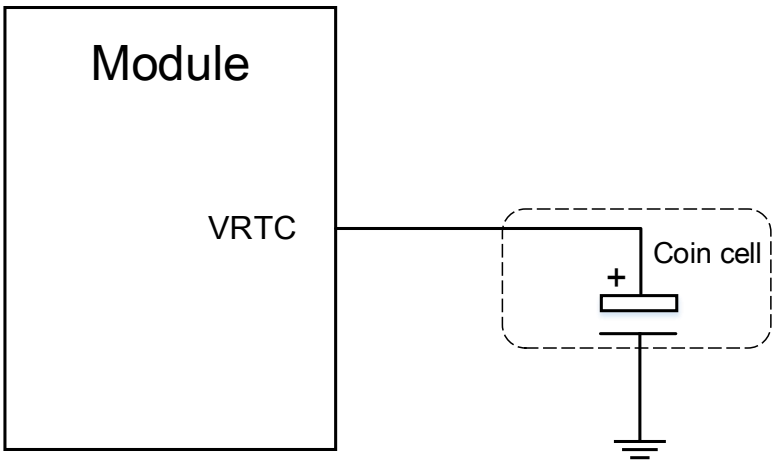

Figure 4 VRTC Reference Design

3.1.3 Power Output

The SS808 module provide multiple power outputs for peripheral circuits. It is recommended to connect 33pF and 10pF capacitors in parallel with every power to avoid high frequency interference effectively.

Table 7 Power Output

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
VREG_L2_1P1	0.375~1.5375	1.1	TBD
VREG_L5_1P8	-	1.8	TBD
VREG_L6_1P8	-	1.8	TBD
VREG_L10_2P8	1.75~3.3375	2.8	TBD
VREG_L11_SDC_PWR	1.75~3.3375	2.95	TBD
VREG_L14_UIM1	1.75~3.3375	1.8/3	TBD
VREG_L15_UIM2	1.75~3.3375	1.8/3	TBD
VREG_L17_2P85	1.75~3.3375	2.85	TBD
VREG_L22_2P8	1.75~3.3375	2.8	TBD

3.2 Control signal

3.2.1 Power on/off

SS808 series module provides one-way power on/off control signal to module's power on/off, restart and sleep/wake up. Its pin definition is shown as follow table：

Table 8 Power on/off Signal

Pin Name	Pin #	I/O	Description	Note

KEY_PWR_N	123	DI	Active low, can be used to power on/off, restart, sleep/wakeup the module	

3.2.1.1 Power on

After module's VBAT pin is powered, pull down KEY_PWR_N pin for more than 2 seconds can trigger module power on. The button control and OC drive power on reference design is shown as follows:

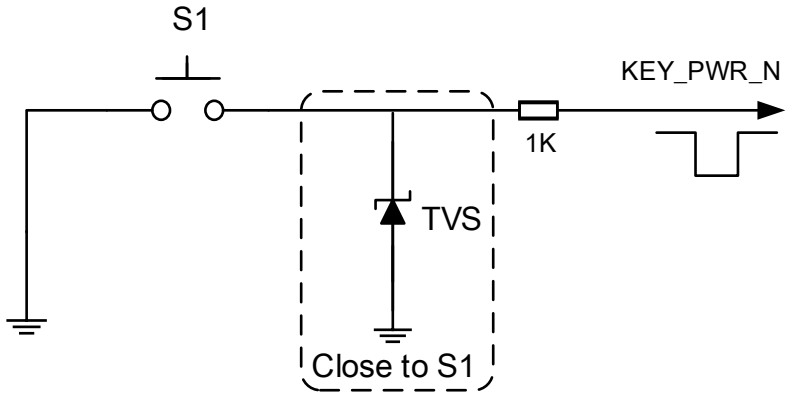

Figure 5 Button Power on Reference Design

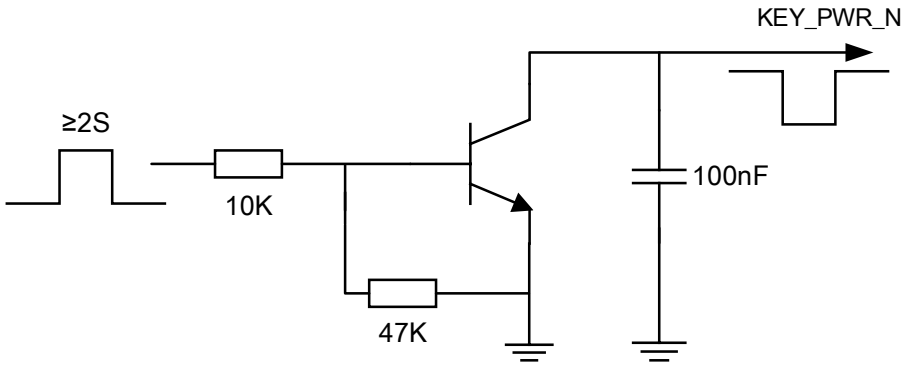

Figure 6 OC Drive Power on Reference Design

The power on timing is shown as follows:

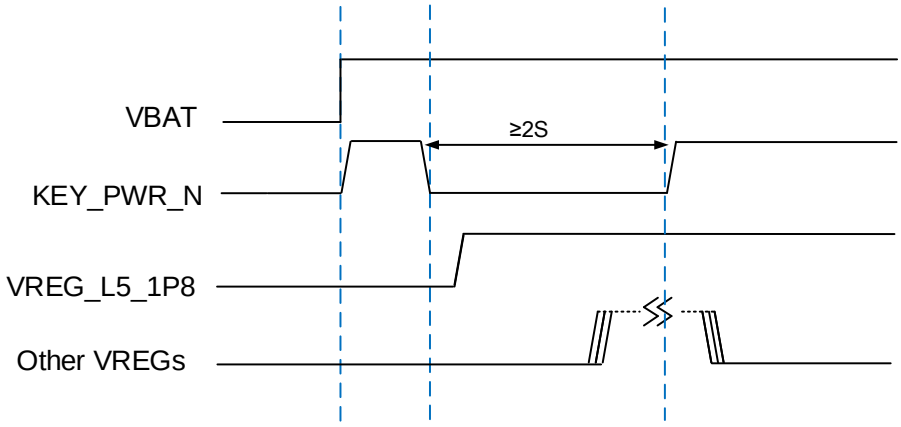

Figure 7 Power on Timing

3.2.1.2 Power off

Normal power off: when module in operating mode, pull down KEY_PWR_N 500mS and then release it, user interface will display selection box (select power off or restart).

Force power off: pull down KEY_PWR_N pin more than 10S module will be forced power off. The power off timing is shown as follows:

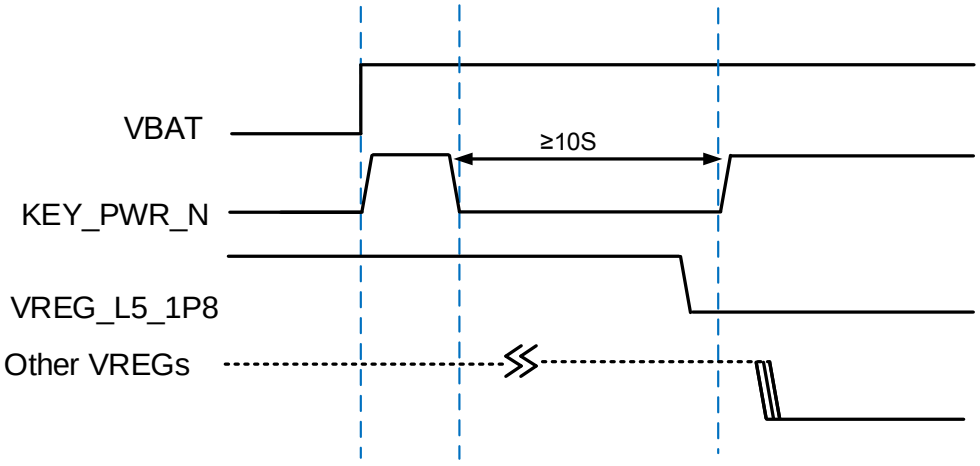

Figure 8 Power off Timing

Note：

When the system is abnormal or shutdown, can use force power off method to power off the module, please use normal method generally, otherwise may cause data loss and other anomalies.

3.2.1.3 Sleep/Wake up

When module in standby mode, pull down KEY_PWR_N 100mS and then release it, module will enter sleep mode. When module in sleep mode, pull down KEY_PWR_N 100mS and then release it, module can be waked up.

3.2.2 Volume control

KEY_VOL_DOWN_N and KEY_VOL_UP_N are the volume down and volume up keypads; its circuit design can refer to the power on keypad circuit.

Note：

The parallel capacitance of volume key shall not exceed 100pF.

3.3 SPMI

SS808 series module provide external SPMI that used for connect external PMI chip. The reference diagram is shown as follow figure:

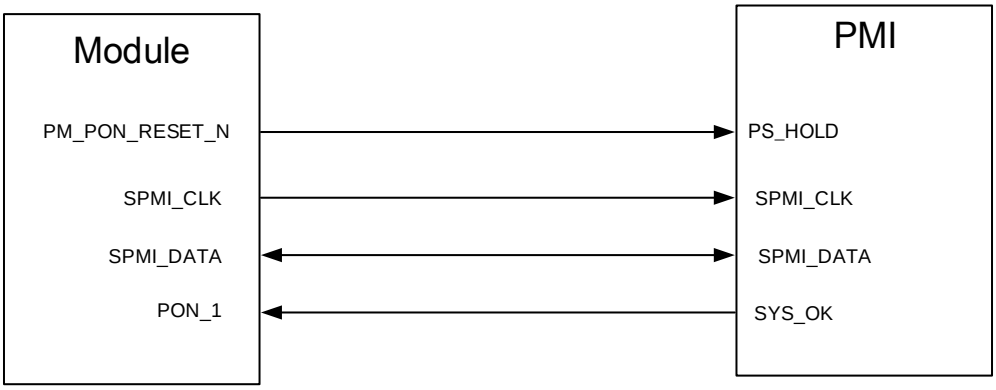

Figure 9 External SPMI Diagram

Design notice:

1）SPMI_CLK, SPMI_DATA, and PMI_RESIN_N are susceptible to glitches, please ensure these signals routed away from EMI aggressors like RF antenna and switchers (SMPS).

2）SPMI_CLK and SPMI_DATA are high speed signal and need three dimensional ground.

3.4 USB

The SS808 series module supports one USB 2.0 and one USB3.0 interface; USB2.0 supports HS (480Mbps) modes and compatible USB1.1 FS (12Mbps). USB3.0 supports SS (5Gbps) mode. USB supports OTG function, HUB expansion interface and Type-C interface; USB2.0 and USB3.0 cannot work at the same, and USB 2.0 support software download while USB 3.0 unsupported. Its pin definition is shown in the following table:

Table 9 USB2.0 Pin Definition

Pin Name	Pin #	I/O	Description	Note
VBUS_USB_IN	8,9	PI	5V input	
USB_DP	12	I/O	USB differential signal	
USB_ DM	11	I/O		

Table 10 USB3.0 Pin Definition

Pin Name	Pin #	I/O	Description	Note
USB_VCONN	225	AI	Power input (5V, 210mA) for driving Active data cable	
USB1_SS_RX_P	173	DI	USB 3.0 differential data receiving signal	
USB1_SS_RX_M	175	DI		
USB1_SS_TX_P	172	DI	USB 3.0 differential data transmission signal	
USB1_SS_TX_M	174	DO		

Pin Name	Pin #	I/O	Description	Note
USB_SS_SWITCH_SEL	217	DO	USB Type-C data switch control	
USB_CC2	223	AI/AO	USB Type-C connector configuration pin	
USB_CC1	227	AI/AO		
USB_HS_ID	16	DI	USB OTG detection	

The reference design of USB2.0 is show as follow figure:

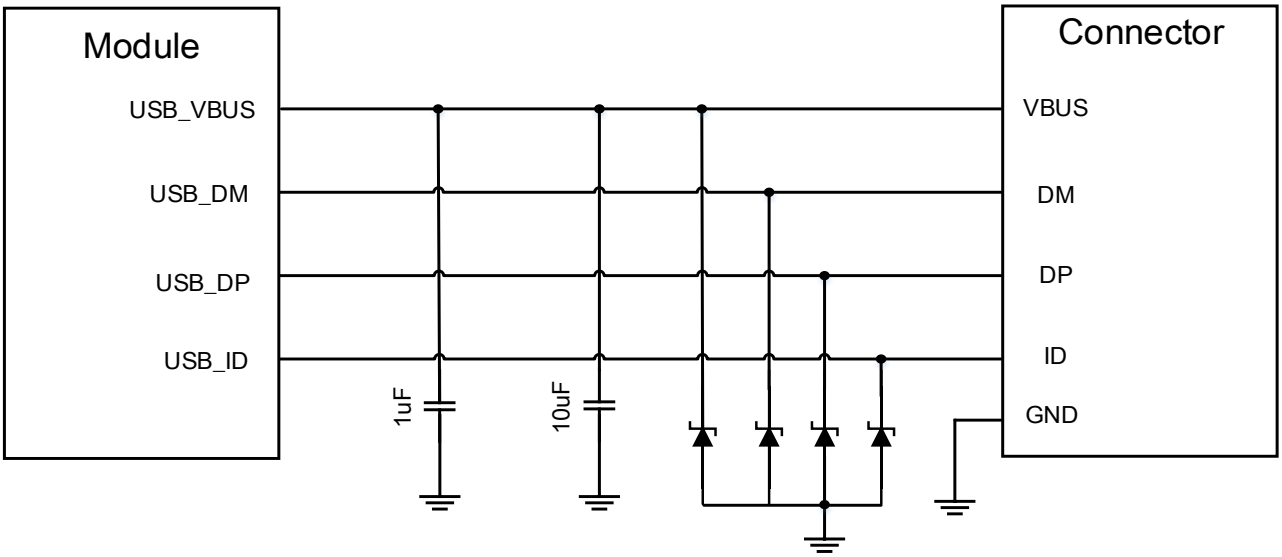

Figure 10 USB2.0 Reference Design

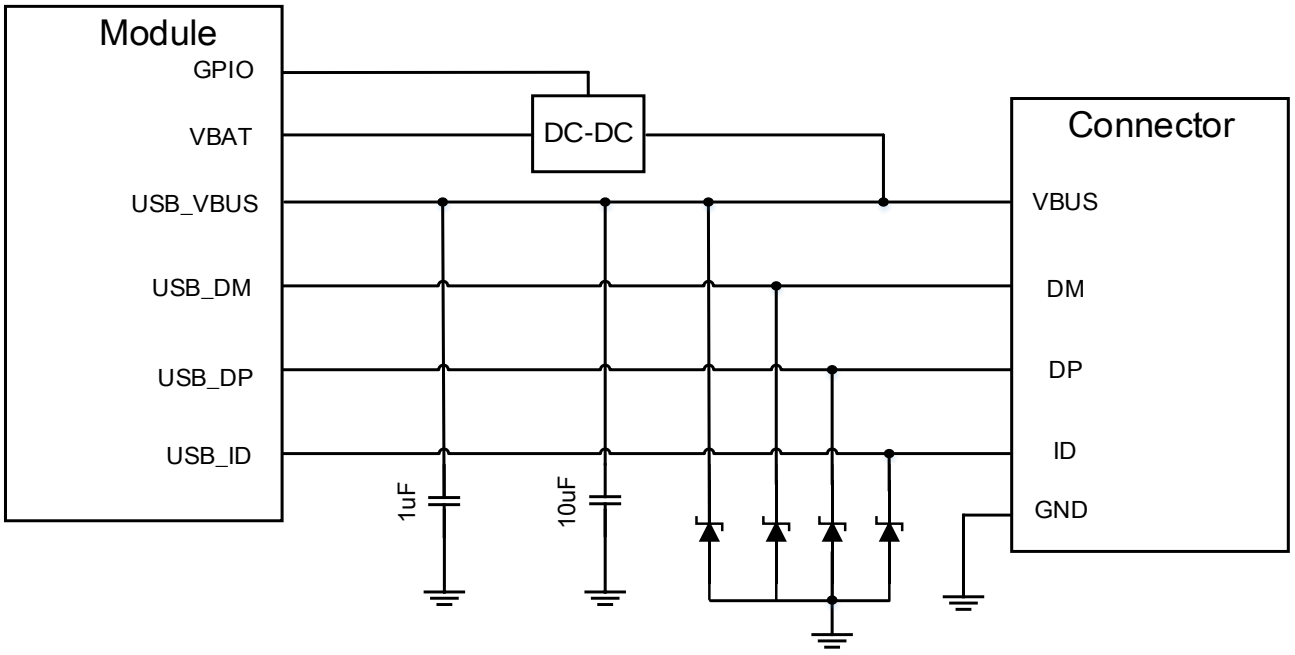

Figure 11 USB2.0 Reference Design(with OTG function)

The reference design of USB3.0 is show as follow figure:

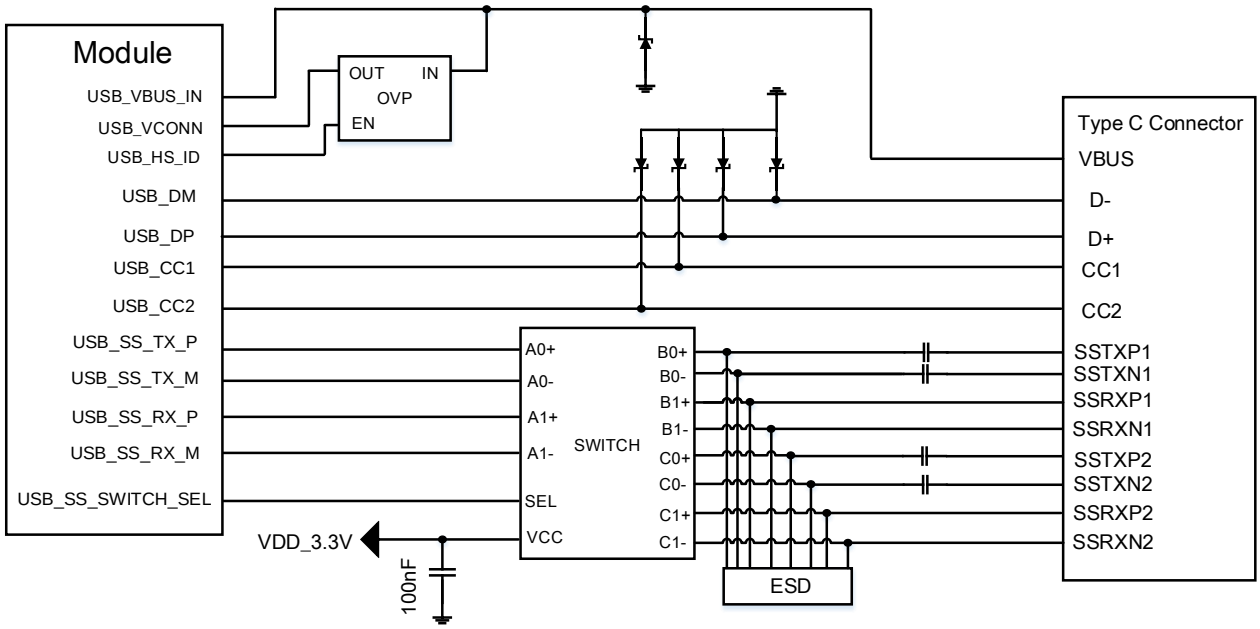

Figure 12 USB3.0 Reference Design

Note:

1) please chose junction capacitor less than 2pF for ESD protection device of USB_DP/DM

2) USB_DP and USB_DM are high-speed differential signal. The highest transmission rate is 480Mbps. Please pay attention to the following requirements in PCB layout:

- USB_DP and USB_DM signal cables are required to be parallel and equal in length (differential cable length controlled within 2mm), while the right-angle route shall be avoided, and differential 90Ω impedance shall be controlled.
- USB2.0 differential signal cable is laid on the signal layer nearest to the ground, with well grounded

3) USB_ID can be simulated by using GPIO, GPIO_18 by default.

4) Pease choose DC-DC that satisfy output is 5V when support OTG function.

USB3.0 (Type-C) interface circuit design:

1) USB3.0 is a high-speed signal cable and needs to be well-shielded (differential cable ground wrap), and follows the principle of high-speed differential routing

2) Do differential impedance control, 90 ohms ±10% and control differential cable length within 0.7mm

3) ESD device parasitic capacitor must be less than 0.5pF

3.5 UART

SS808 series module defines three UART ports，all are 1.8V voltage domain. Its pin definition is shown as follow table:

Table 11 UART Interface Pin Definition

Pin Name	Pin #	I/O	Description	Note
UART2_TX	90	DO	UART2 data transmit	Debug serial port
UART2_RX	89	DI	UART2 data receive	
UART4_TX	45	DO	UART4 data transmit	
UART4_RX	46	DI	UART4 data receive	
UART4_CTS	47	DI	UART4 clear to send	
UART4_RTS	48	DO	UART4 request to send	
UART5_TX	209	DO	UART5 data transmit	
UART5_RX	207	DI	UART5 data receive	

All series ports are 1.8V voltage domain, if the peripheral is other voltage domain, please add level shift.

level shift reference design is shown as follow figure:

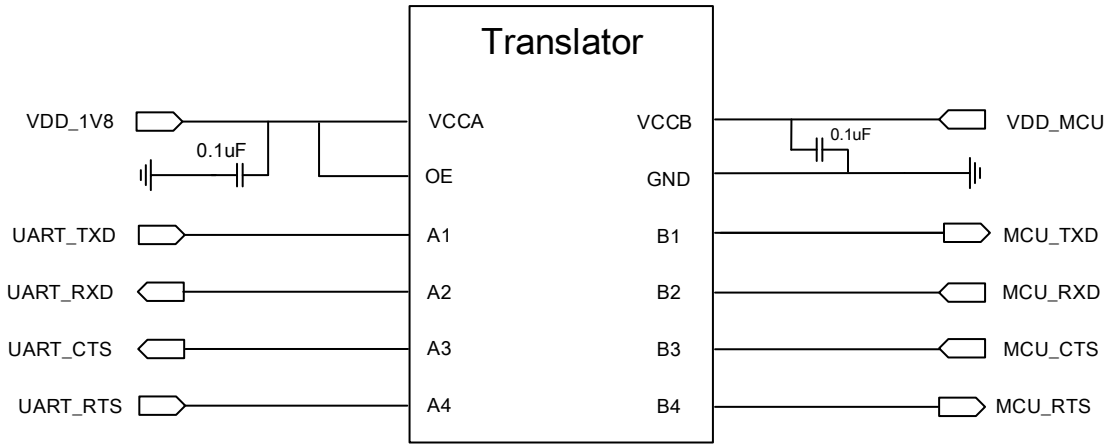

Figure 13 Level Shift Reference Design

3.6 SPI

SS808 series module provide one master only SPI interface, the pin definition is as follows:

Table 12 SPI Pin Definition

Pin Name	Pin #	I/O	Description	Note
SPI6_CLK	113	DO	SPI clock	DMA mode not supported
SPI6_CS	114	DO	SPI chip select	DMA mode not supported
SPI6_MISO	115	DI	SPI Master input slave output	DMA mode not supported
SPI6_MOSI	116	DO	SPI Master output slave input	DMA mode

				not supported

Note:

SPI6 don't support DMA mode.

3.7 (U)SIM

The SS808 supports two (U)SIM cards, dual-SIM dual-standby single-active (default dual) and both support hot plug (default off).

Table 13 (U)SIM Pin Definition

Pin Name	Pin #	I/O	Description	Note
UIM1_DATA	25	I/O	(U)SIM 1 data signal	
UIM1_CLK	24	DO	(U)SIM 1 clock signal	
UIM1_RESET	23	DO	(U)SIM 1 reset signal	
UIM1_DETECT	22	DI	(U)SIM 1 plug detect	Off by default
UIM2_DATA	20	I/O	(U)SIM 2 data	
UIM2_CLK	19	DO	(U)SIM 2 clock	
UIM2_RESET	18	DO	(U)SIM 2 reset	
UIM2_DETECT	17	DI	(U)SIM 2 plug detect	Off by default
VREG_L14_UIM1	26	PO	(U)SIM 1 power supply	
VREG_L15_UIM2	21	PO	(U)SIM 2 power supply	

(U)SIM reference design is shown as follow figure:

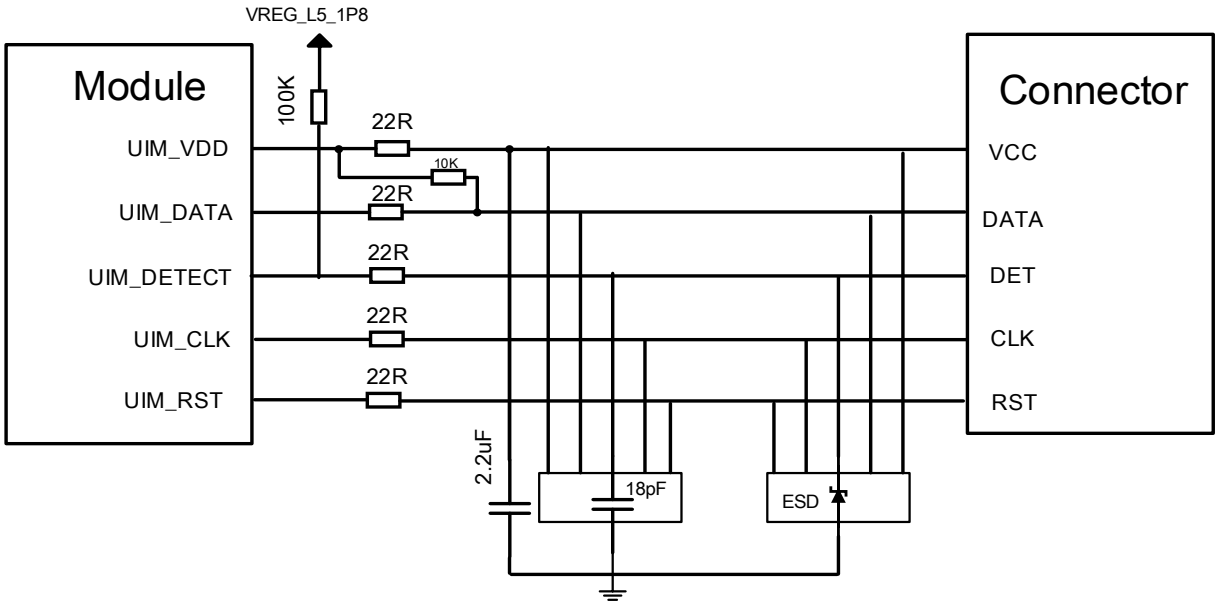

Figure 14 (U)SIM Reference Design

(U)SIM card design notice:

1) The length from the (U)SIM card holder to module should less than 100mm.

2) The layout and routing of the (U)SIM card must be kept away from EMI interference sources such as RF antenna and digital switch power.

3) The decoupling capacitors of the (U)SIM card signal and the ESD device should be placed close to the card holder.

3.8 SDIO

SS808 series module support one SDIO interface. The pin definition is as follows:

Table 14 SDIO Pin Definition

Pin Name	Pin #	I/O	Description	Note
SDC2_DATA3	34	I/O	SD card data interface	
SDC2_DATA2	33	I/O	SD card data interface	
SDC2_DATA1	32	I/O	SD card data interface	
SDC2_DATA0	31	I/O	SD card data interface	
SDC2_CLK	29	DO	SD card clock	
SDC2_CMD	30	I/O	SD card command	
SD_CARD_DET_N	35	DI	SD card detection	
VREG_L11_SDC_PWR	28	PO	SD power supply	

SDIO interface reference design is shown as follow figure:

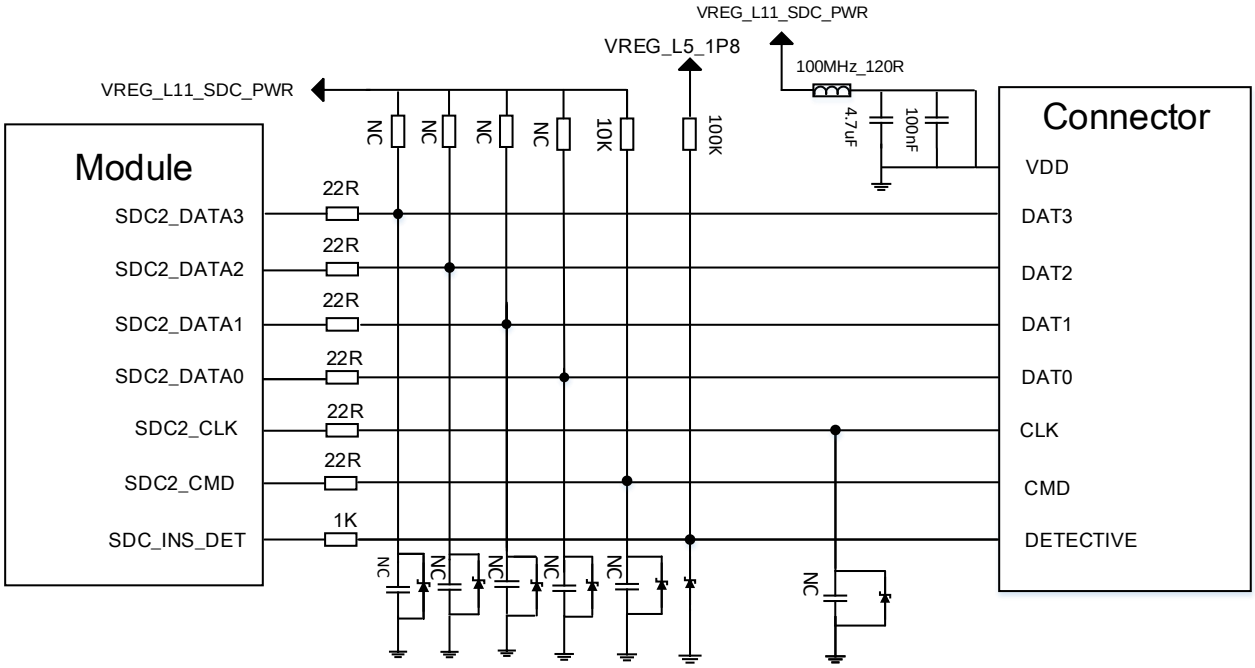

Figure 15 SDIO Reference Design

SDIO design notice:

1) VREG_L11_SDC_PWR is the SD card peripheral driving power and can provide about 800mA current. Pay attention to controlling the width of trace.

2) Pull up SD_DET with VREG_L5_1P8

3) SDIO is a high-speed digital signal cable, needs to be shielded.

3.9 GPIO

SS808 series module have rich GPIOs and the interface level is 1.8V. The pin definition is as follows:

Table 15 GPIO List

Pin Name	Pin #	I/O	Description
GPIO_2	38	B-PD:nppukp	NO
GPIO_3	96	B-PD:nppukp	NO
GPIO_7	40	B-PD:nppukp	NO
GPIO_8	104	B-PD:nppukp	NO
GPIO_9	101	B-PD:nppukp	YES
GPIO_19	118	B-PD:nppukp	NO
GPIO_25	105	B-PD:nppukp	YES
GPIO_45	110	B-PD:nppukp	YES
GPIO_59	117	B-PD:nppukp	YES

Pin Name	Pin #	I/O	Description
GPIO_63	112	B-PD:nppukp	YES
GPIO_91	97	B-PD:nppukp	YES
GPIO_96	111	B-PD:nppukp	NO
GPIO_97	100	B-PD:nppukp	YES
GPIO_105	103	B-PD:nppukp	NO
GPIO_106	102	B-PD:nppukp	NO
GPIO_113	220	B-PD:nppukp	NO
GPIO_114	221	B-PD:nppukp	NO
GPIO_135	39	B-PD:nppukp	NO
GPIO_137	99	B-PD:nppukp	YES
GPIO_138	86	B-PD:nppukp	NO
GPIO_140	98	B-PD:nppukp	YES

Note：

B: Bidirectional digital with CMOS input

H: High-voltage tolerant

NP: pdpukp = default no-pull with programmable options following the colon (:)

PD: nppukp = default pulldown with programmable options following the colon (:)

PU: nppdkp = default pullup with programmable options following the colon (:)

KP: nppdpu = default keeper with programmable options following the colon (:)

3.10 I²C

SS808 series module provides four I2C interfaces for TP, camera, sensor, etc. And four I2C interfaces are all open-drain outputs, when in use, please pull up to 1.8V power domain through pull-up resistors. The pin definition is shown as follow table:

Pin Name	Pin #	I/O	Description	Note
I2C8_SCL	87	OD	Sensor I2C clock	
I2C8_SDA	88	OD	Sensor I2C data	
TS_I2C_SCL	41	OD	Main touch panel I2C clock	
TS_I2C_SDA	150,158	OD	Main touch panel I2C data	
CAM_I2C_SCL	84	OD	Camera I2C clock	
CAM_I2C_SDA	85	OD	Camera I2C data	

Pin Name	Pin #	I/O	Description	Note
CAM2_I2C_SCL	206	OD	Camera I2C clock	
CAM2_I2C_SDA	208	OD	Camera I2C data	

Note: When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address.

3.11 ADC

SS808 series module provides one ADC interfaces and its maximum Resolution is 15 bits, its pin definition is shown as follow table:

Table 16 ADC Pin Definition

Pin Name	Pin #	I/O	Description	Note
ADC	128	AI	ADC detection pin	0.3V~VBAT Configurable

3.12 LCM

The video output of SS808 series module can support dual-screen display; its screen interface is based on MIPI_DSI standard and supports 4 sets of high-speed differential data transmit. Each set support 2.1Gbps speed maximum and supports 1080P maximally.

Table 17 LCM Pin Definition

Pin Name	Pin #	I/O	Description	Note
VREG_L6_1P8	122	PO	LCD IO voltage	
VREG_L17_2P85	130	PO	LCD analog power VDD	
MIPI_DSI0_CLK_P	53	AO	Main-LCD MIPI clock +	
MIPI_DSI0_CLK_N	52	AO	Main-LCD MIPI clock +	
MIPI_DSI0_LANE0_P	55	AI/AO	Main LCD MIPI Lane0 +	
MIPI_DSI0_LANE0_N	54	AI/AO	Main LCD MIPI Lane0 -	
MIPI_DSI0_LANE1_P	57	AI/AO	Main LCD MIPI Lane1 +	
MIPI_DSI0_LANE1_N	56	AI/AO	Main LCD MIPI Lane1 -	
MIPI_DSI0_LANE2_P	59	AI/AO	Main LCD MIPI Lane2 +	
MIPI_DSI0_LANE2_N	58	AI/AO	Main LCD MIPI Lane2 -	
MIPI_DSI0_LANE3_P	61	AI/AO	Main LCD MIPI Lane3 +	
MIPI_DSI0_LANE3_N	60	AI/AO	Main LCD MIPI Lane3 -	

Pin Name	Pin #	I/O	Description	Note
LCD0_RST_N	49	DO	Main LCD reset	
MIPI_DSI1_CLK_P	192	AO	Sub-LCD MIPI clock +	
MIPI_DSI1_CLK_N	193	AO	Sub-LCD MIPI clock -	
MIPI_DSI1_LANE0_P	194	AI/AO	Sub-LCD MIPI Lane0 +	
MIPI_DSI1_LANE0_N	195	AI/AO	Sub-LCD MIPI Lane0 -	
MIPI_DSI1_LANE1_P	198	AI/AO	Sub-LCD MIPI Lane1 +	
MIPI_DSI1_LANE1_N	199	AI/AO	Sub-LCD MIPI Lane1 -	
MIPI_DSI1_LANE2_P	200	AI/AO	Sub-LCD MIPI Lane2 +	
MIPI_DSI1_LANE2_N	201	AI/AO	Sub-LCD MIPI Lane2 -	
MIPI_DSI1_LANE3_P	202	AI/AO	Sub-LCD MIPI Lane3 +	
MIPI_DSI1_LANE3_N	203	AI/AO	Sub-LCD MIPI Lane3 -	
LCD1_RST_N	216	DO	Sub-LCD reset	
PWM	44	DO	LCD backlight PWM control	
LCD1_BL_EN	211	DO	Sub-LCD backlight enable control	
LCD_TE	50	DI	LCD tearing effect	

The reference design of LCD interface circuit is shown as follow:

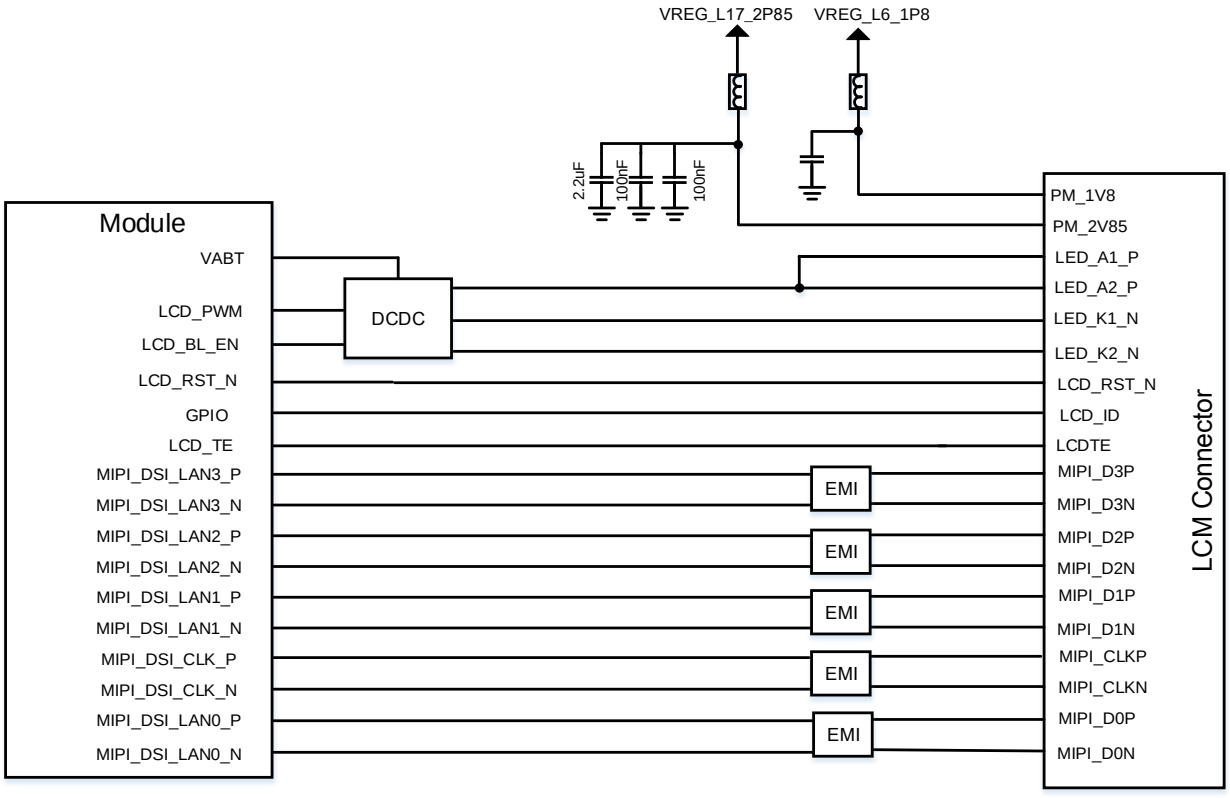

Figure 16 LCM Reference Design

LCM design notice:

1) MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the electromagnetic interference of the circuit.

2) MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;

3) The MIPI signal needs to be controlled with a differential impedance of 100-ohm tolerance ±10%;

4) The total length of the trace must not exceed 300mm;

5) The intra lane match of MIPI signal must be controlled within 0.67mm;

6) The inter lane match of MIPI signal must be controlled within 1.3mm;

7) It is recommended that the space of intra lane should be 1.5 times trace width and the differential cable should keep 3 times trace width from other cable.

3.13 TP

SS808 series module provides one I2C interface can be used to connect the touch panel and it provides power, interrupt, reset pins. The pin definition of the module is shown in the follow table:

Table 18 TP Pin Definition

Pin Name	Pin #	I/O	Description	Note
TS0_INT_N	42	DI	Main LCD TP interrupt signal	
TS0_RST_N	43	DO	Main LCD TP reset signal	
VREG_L5_1P8	129	PO	Main LCD TP IO voltage output	
VREG_L10_2P8	224	PO	Main LCD TP VDD voltage output	
TS_I2C_SCL	41	OD	Main LCD TP I2C clock	
TS_I2C_SDA	150,158	OD	Main LCD TP I2C data	
TS1_INT	212	DI	Sub-LCD TP interrupt signal	
TS1_RST_N	218	DO	Sub-LCD TP reset signal	

TP reference design circuit is shown as follows:

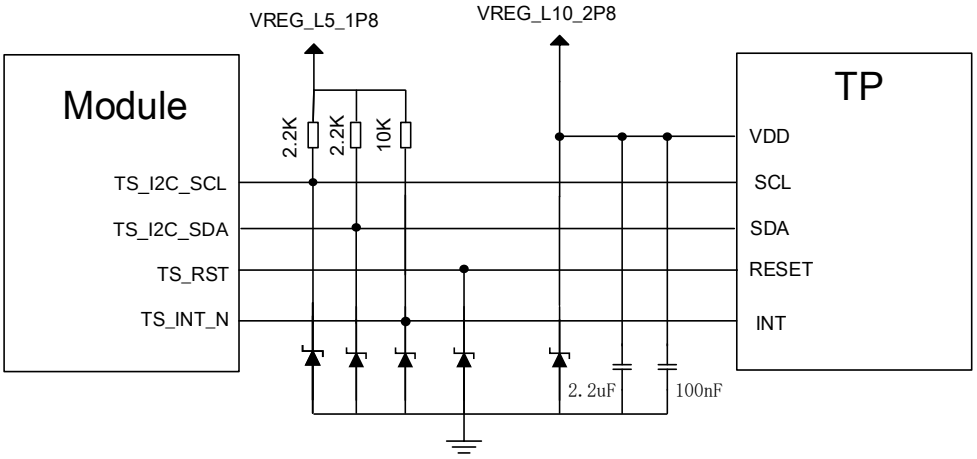

Figure 17 TP Reference Design

3.14 Camera

The camera interface is based on the MIPI_CSI standard and can support two(4-Lane+4-Lane) or three(4-Lane+2-Lane+1-Lane) cameras (three cameras by default), maximum 21MP pixel. The pin definition of camera interface is shown as follow figure:

Table 19 Camera Interface Pin Definition

Pin Name	Pin #	I/O	4-Lane+4-Lane	4-Lane+2-Lane+1-Lane
VREG_L6_1P8	122	PO	DOVDD power supply	DOVDD power supply
VREG_L22_2P8	222	PO	AVDD supply	AVDD power supply
VREG_L2_1P1	226	PO	DVDD supply	DVDD power supply
VREG_L17_2P85	130	PO	Camera focus motor drive AFVDD power supply	Camera focus motor drive AFVDD power supply
MIPI_CSI2_CLK_P	64	AO	Rear camera MIPI Clock+	Rear camera MIPI Clock+
MIPI_CSI2_CLK_N	63	AO	Rear camera MIPI Clock-	Rear camera MIPI Clock-
MIPI_CSI2_LANE0_P	66	AI/AO	Rear camera MIPI Lane0 +	Rear camera MIPI Lane0 +
MIPI_CSI2_LANE0_N	65	AI/AO	Rear camera MIPI Lane0 -	Rear camera MIPI Lane0 -
MIPI_CSI2_LANE1_P	68	AI/AO	Rear camera MIPI Lane1 +	Rear camera MIPI Lane1 +
MIPI_CSI2_LANE1_N	67	AI/AO	Rear camera MIPI Lane1 -	Rear camera MIPI Lane1 -
MIPI_CSI2_LANE2_P	181	AI/AO	Rear camera MIPI Lane2 +	Rear camera MIPI Lane2 +
MIPI_CSI2_LANE2_N	183	AI/AO	Rear camera MIPI Lane2 -	Rear camera MIPI Lane2 -
MIPI_CSI2_LANE3_P	180	AI/AO	Rear camera MIPI Lane3 +	Rear camera MIPI Lane3 +
MIPI_CSI2_LANE3_N	179	AI/AO	Rear camera MIPI Lane3 -	Rear camera MIPI Lane3 -
CAM0_MCLK	75	DO	Rear camera master clock	Rear camera master clock

Pin Name	Pin #	I/O	4-Lane+4-Lane	4-Lane+2-Lane+1-Lane
CAM0_RST_N	80	DO	Rear camera reset	Rear camera reset
CAM0_PWD_N	81	DO	Rear camera power down	Rear camera power down
CAM_I2C_SCL	84	OD	Camera I2C clock	Camera I2C clock
CAM_I2C_SDA	85	OD	Camera I2C data	Camera I2C data
MIPI_CSI0_CLK_P	71	AO	Front camera MIPI Clock+	Front camera MIPI Clock+
MIPI_CSI0_CLK_N	70	AO	Front camera MIPI Clock -	Front camera MIPI Clock -
MIPI_CSI0_LANE0_P	73	AI/AO	Front camera MIPI Lane 0	Front camera MIPI Lane 0 +
MIPI_CSI0_LANE0_N	72	AI/AO	Front camera MIPI Lane 0 -	Front camera MIPI Lane 0 -
MIPI_CSI0_LANE1_P	184	AI/AO	Front camera MIPI Lane 1+	Front camera MIPI Lane 1+
MIPI_CSI0_LANE1_N	185	AI/AO	Front camera MIPI Lane1 -	Front camera MIPI Lane 1 -
MIPI_CSI0_LANE2_P	186	AI/AO	Front camera MIPI Lane 2	Depth camera MIPI Lane 0 +
MIPI_CSI0_LANE2_N	187	AI/AO	Front camera MIPI Lane 2 -	Depth camera MIPI Lane 0 -
MIPI_CSI0_LANE3_P	188	AI/AO	Front camera MIPI Lane 3+	Depth camera MIPI Clock+
MIPI_CSI0_LANE3_N	189	AI/AO	Front camera MIPI Lane 3 -	Depth camera MIPI Clock-
CAM1_MCLK	76	DO	Front camera master clock	Front camera master clock
CAM1_RST_N	82	DO	Front camera reset	Front camera reset
CAM1_PWD_N	83	DO	Front camera power down	Front camera power down
CAM2_SCL	206	OD	NC	Depth camera I2C clock
CAM2_SDA	208	OD	NC	Depth camera I2C data
CAM2_MCLK	213	DO	NC	Depth camera master clock
CAM2_RST_N	214	DO	NC	Depth camera reset
CAM2_PWD_N	215	DO	NC	Depth camera power down

3.14.1 Rear camera

Reference design of rear camera is shown as follows:

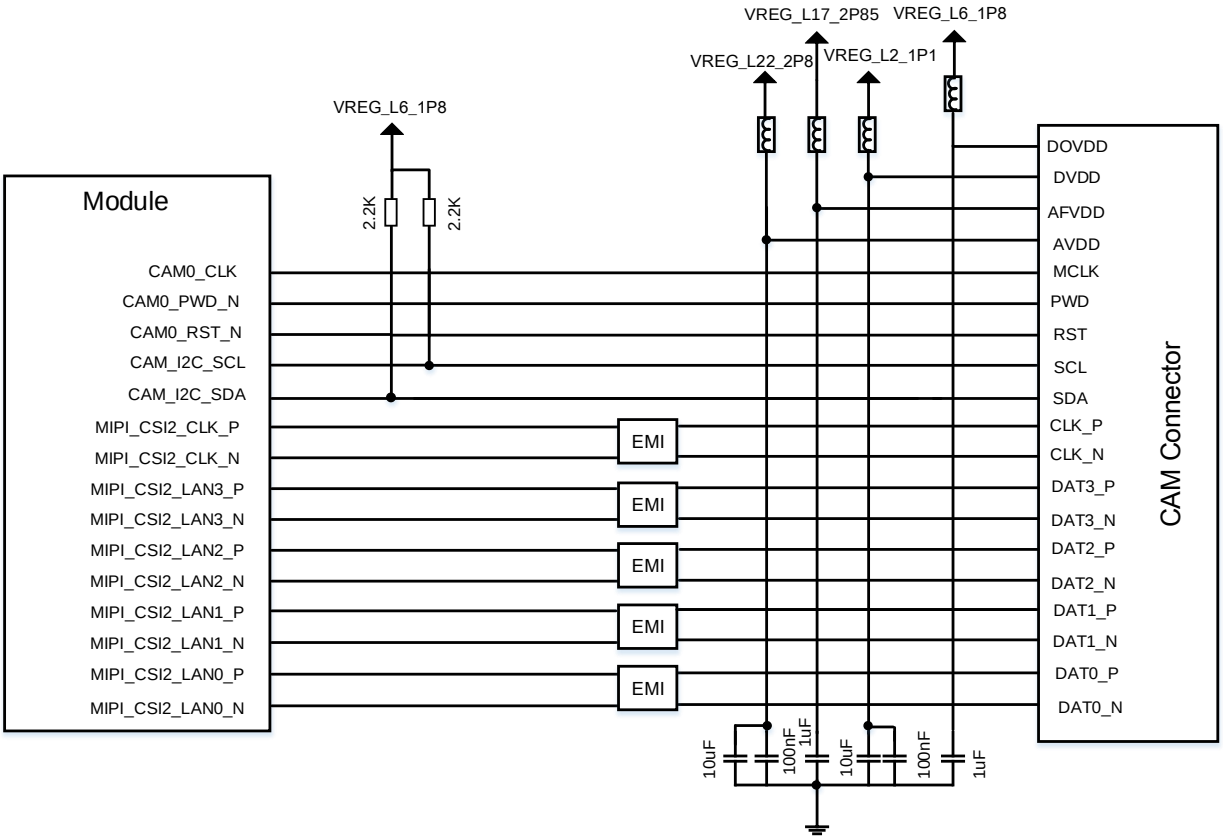

Figure 18 Rear Camera Reference Design

3.14.2 Front camera

Reference design of 4-Lane front camera is shown as follows:

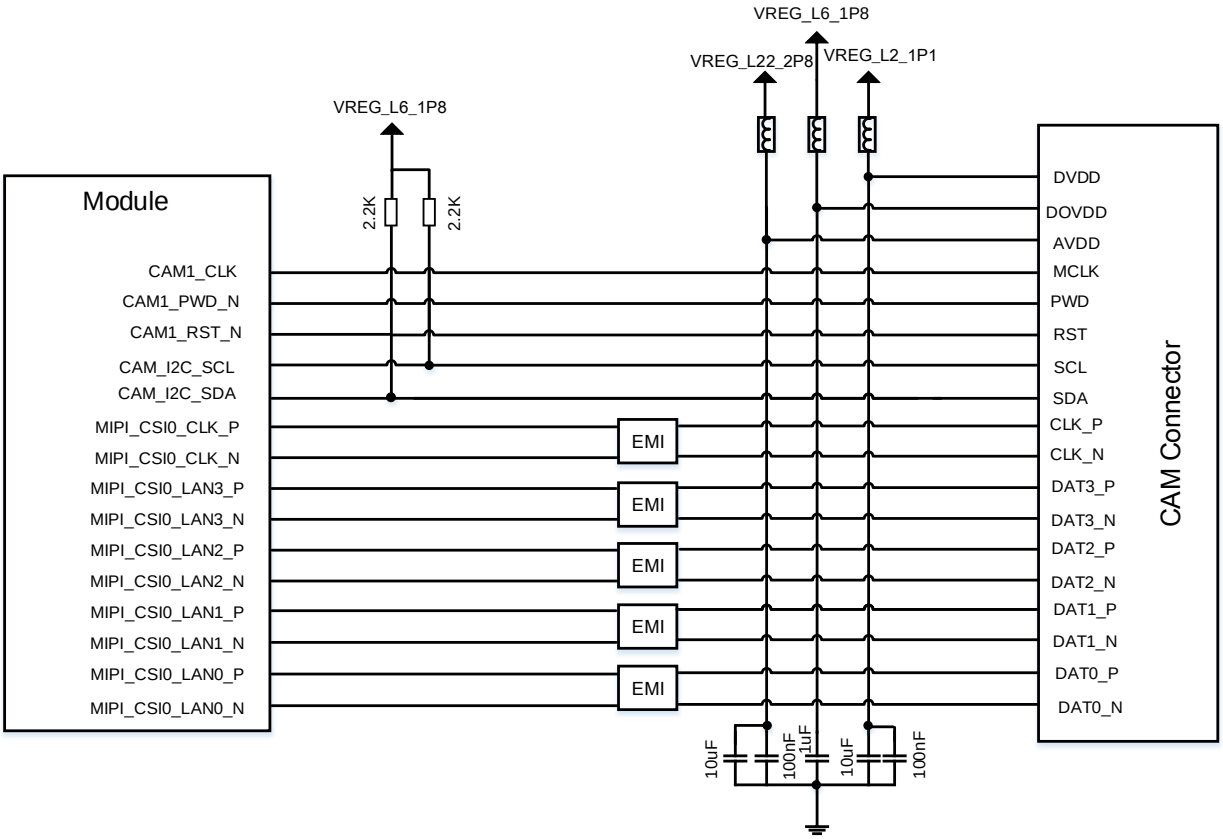

Figure 19 Lane Front Camera Reference Design

Reference design of 2-Lane front camera is shown as follows:

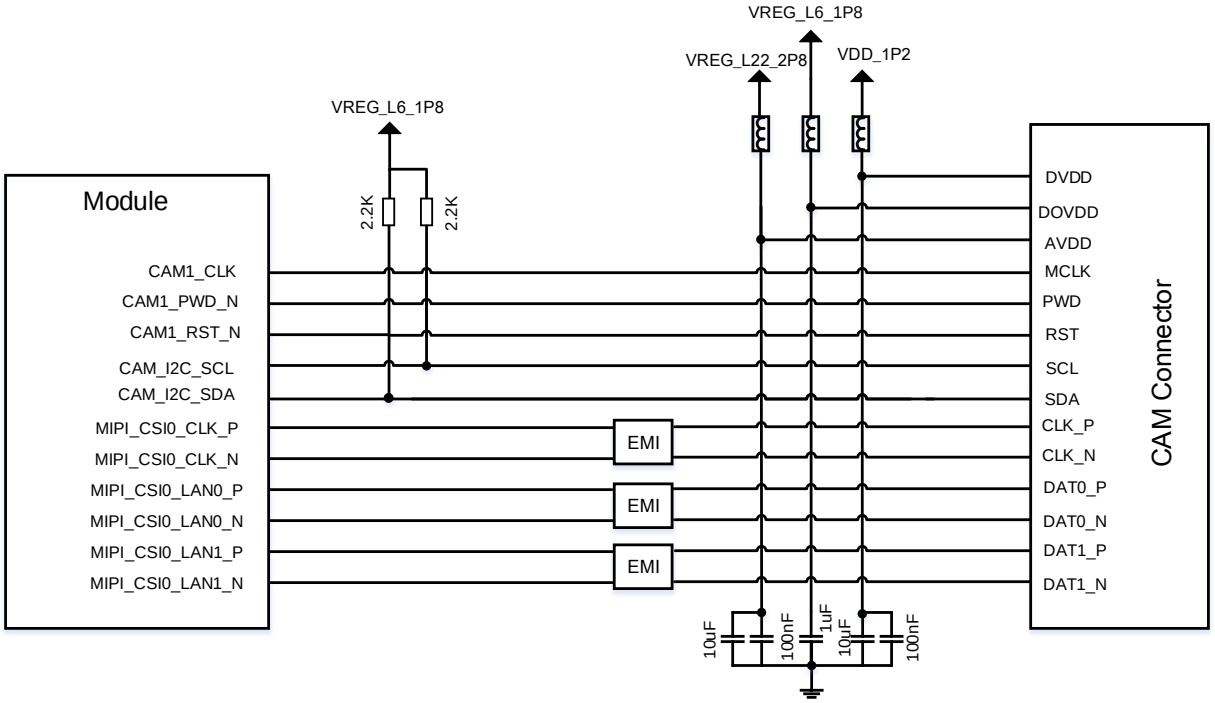

Figure 20 Lane Front Camera Reference Design

3.14.3 Depth camera

Reference design of depth camera is shown as follows:

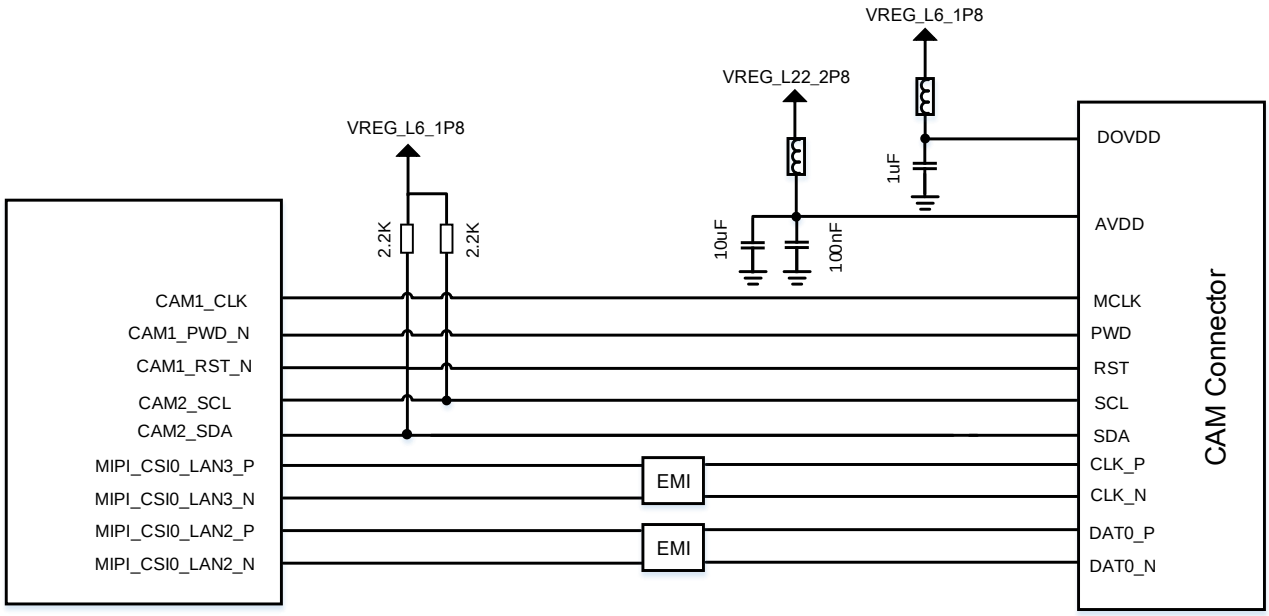

Figure 21 Depth Camera Reference Design

3.14.4 Design notice

MIPI_CSI is a high-speed signal which has relatively high requirement for routing and must be prioritized when PCB layout.

1) MIPI is a high-speed signal. It is recommended to connect the common mode inductor in series near the camera connector to reduce the electromagnetic interference of the circuit.

2) MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;

3) The MIPI signal need to be controlled with a differential impedance of 100 ohm and an error of ±10%;

4) The total length of the trace does not exceed 300mm;

5) The intra lane match of MIPI signal must be controlled within 0.67mm;

6) The inter lane match of MIPI signal must be controlled within 1.3mm;

7) It is recommended that the space of intra lane should be 1.5 times trace width and the differential cable should keep 3 times trace width from other cable;

8) CAM_CLK is a high-speed clock signal and requires three-dimensional grounding

9) The analog voltage AVDD routing should be away from interference sources, otherwise it is easy to bring interference of power noise

10) If the front and rear cameras share the I2C, you need to confirm that the I2C addresses of the two cameras do not conflict.

11) Camera analog power supply suggest to add LDO with high PSRR ability

3.15 Sensor

SS808 series module use I2C to communicate with sensors and support various types of sensors, such as accelerometer sensor, ambient light sensor, magnetic sensor and gyroscopes etc.

Table 20 Sensor Interface Pin Definition

Pin Name	Pin #	I/O	Description	Note
I2C8_SCL	87	OD	I2C clock	
I2C8_SDA	88	OD	I2C data	
ALSP_INT_N	106	DI	Ambient light sensor interrupt	
MAG_INT_N	107	DI	Magnetic sensor interrupt	
ACCL_INT2_N	108	DI	Accelerometer sensor interrupt	
ACCL_INT1_N	109	DI	Accelerometer sensor interrupt	

3.16 Audio

SS808 series module support analog audio, and have 2 input 3 output. Pin definition is shown as follows:

Table 21 Audio Interface Pin Definition

Pin Name	Pin #	I/O	Description	Note
SPKR_DRV_P	148	AO	Louder speaker driver output+	
SPKR_DRV_N	147	AO	Louder speaker driver output-	
CDC_EAR_P	134	AO	Earpiece output+	
CDC_EAR_N	135	AO	Earpiece output-	
CDC_HPH_L	139	AO	Headphone output, left channel	
CDC_HPH_REF	138	/	Headphone ground reference	
CDC_HPH_R	137	AO	Headphone output, right channel	
CDC_HS_DET	140	AI	Headphone plug detection	
MIC2_P	142	AI	Headphone microphone input	
GND_MIC	141	AI	Headphone microphone input	
MIC1_N	144	AI	Main microphone input -	
MIC1_P	145	AI	Main microphone input +	

Design notice:

1) SS808 series module has MIC bias circuit internally, and no external addition is required.

2) The SPK is configured class D amplifier and cannot be connected to an external amplifier. It is

recommended to connect 8-ohm speakers. Note that the route width must meet the power rating requirements. If an external audio amplifier is required, dual input please choose dual channel and signal input channel can configurable by software.

3) The reference ground of the headphone has already grounded in the module. The external circuit is recommended not to be grounded and resistor can be reserved.

4) Reduce noise and improve audio quality, the following approaches are recommended:

- Keep audio PCB routing away from the antenna and high-frequency digital signal
- Reserve LC filter circuit in audio circuit to prevent EMC
- Audio routing needs to be masked

3.16.1 Microphone Circuit Design

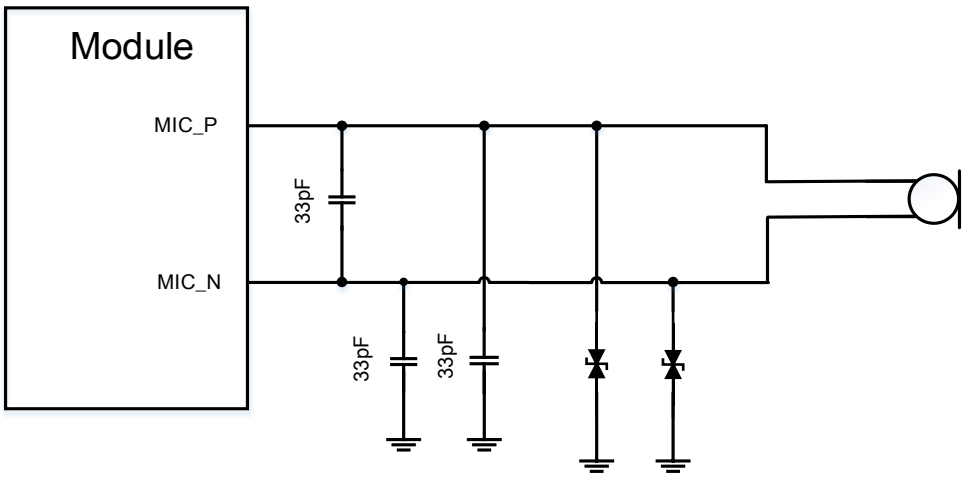

Figure 22 Microphone Reference Design

Note：

Recommendation TVS for headphone to prevent system level issue, please choose bidirectional device.

3.16.2 Earpiece Circuit Design

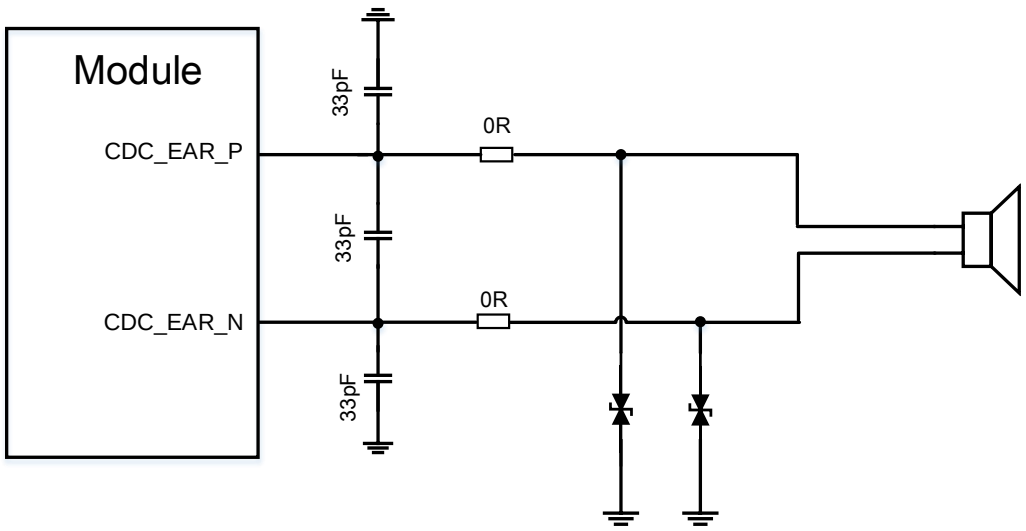

Figure 23 Earpiece Reference Design

3.16.3 Headphone Circuit Design

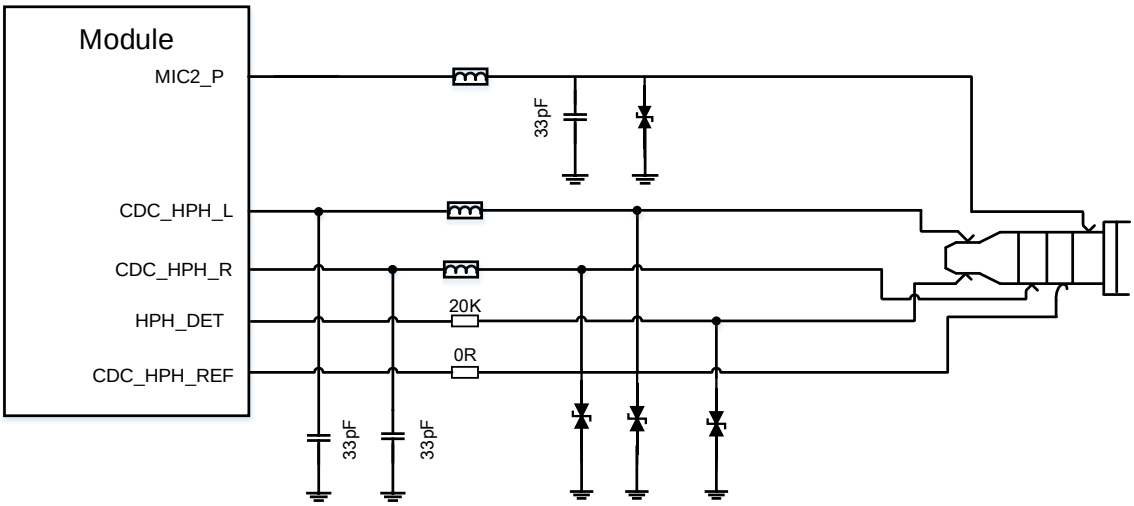

Figure 24 Headphone Circuit Design

3.16.4 Speaker Circuit Design

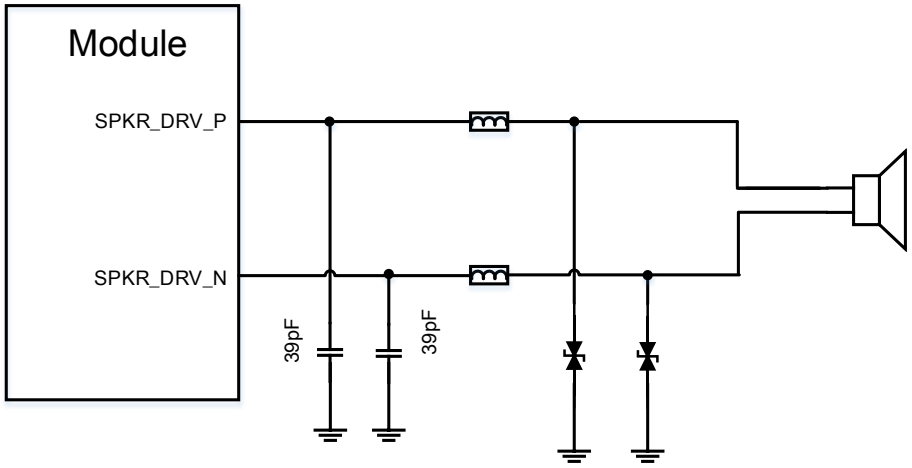

Figure 25 Speaker Circuit Design

3.17 Force Download Interface

SS808 series module provides USB_FORCE_BOOT pin as an emergency download interface. Connect the USB_FORCE_BOOT with VREG_L5_1P8 pin when power on, the module can enter the emergency download mode which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin. Reference design is shown as follow figure:

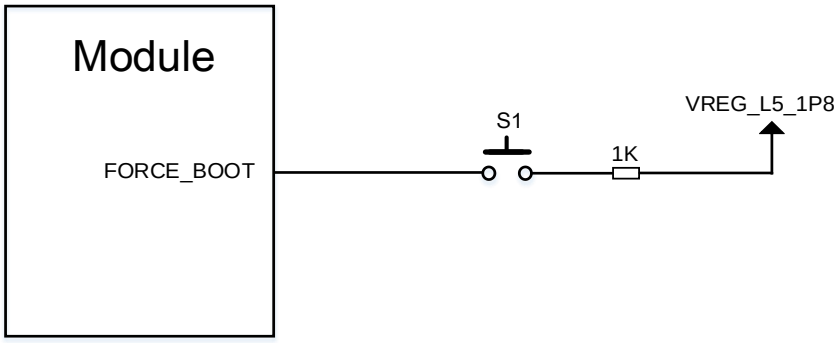

Figure 26 Force Download Reference Design

4 Antenna Interface

SS808 series module support 2/3/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 MAIN/DRX Antenna

SS808 series module provides two 2G/3G/4G antenna interfaces. The ANT_MAIN is used to receive and transmit RF signal, the ANT_DRX is used for diversity reception.

Table 22 MAIN/DRX Antenna Interface Definition

Pin Name	Pin #	I/O	Description	Note
ANT_TRX	94	I/O	2G/3G/4G antenna interface	
ANT_DRX	132	AI	Diversity reception antenna	

4.1.1 Operating Band

Table 23 Module Operating Band

Mode	Band	Tx (MHz)	Rx (MHz)
WCDMA	Band 2	1850 - 1910	1930 - 1990
	Band 4	1710 - 1755	2110 - 2155
	Band 5	824 - 849	869 - 894
LTE FDD	Band 2	1850 - 1910	1930 - 1990
	Band 4	1710 - 1755	2110 - 2155
	Band 5	824 - 849	869 - 894
	Band 7	2500 - 2570	2620-2690
	Band 12	698 - 716	728 - 746
	Band 13	777-787	746-756
	Band 25	1850-1915	1930-1995
	Band 26	814-849	859-894
	Band 66	1710-1780	2110-2180
LTE TDD	Band 41	2496 –2690	2496 –2690

4.1.2 Circuit Reference Design

When use the SS808 series module, it is necessary to connect the antenna pin with the RF connector or antenna feed point on the main board via an RF trace. Microstrip trace is recommended for RF trace, with insertion loss within 0.2dB and impedance at 50ohm.A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel components are directly connected across the RF trace and should not pull out a branch, as the figure shows:

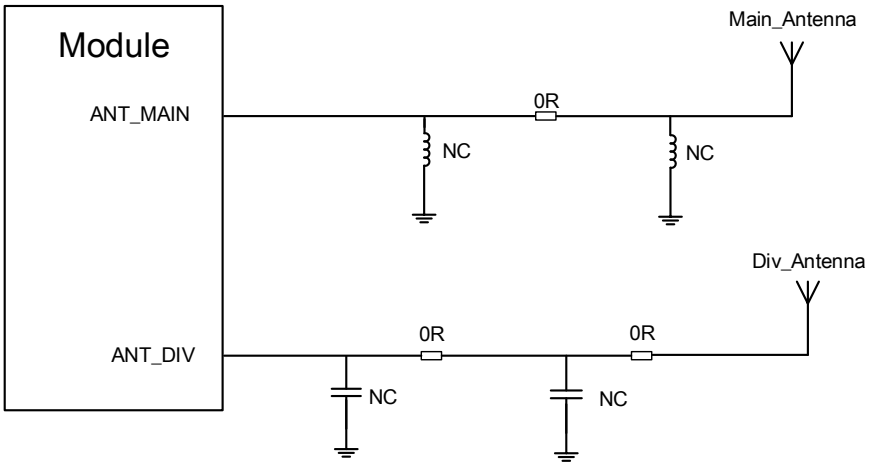

Figure 27 MAIN/DRX Antenna Reference Design

4.2 WIFI/BT Antenna

Microstrip trace is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50 ohm.

Table 24 WIFI/BT Antenna Interface Definition

Pin Name	Pin #	I/O	Description	Note
ANT-WIFI/BT	78	I/O	WIFI/BT antenna interface	

4.2.1 Operating Frequency

Table 25 WIFI/BT Operating Frequency

Mode	Frequency	Unit
WIFI	2402~2482	MHz
	5180~5825	MHz
BT4.2	2402~2480	MHz

4.2.2 WIFI/BT Antenna Reference Design

WIFI/BT antenna reference design is shown as follows：

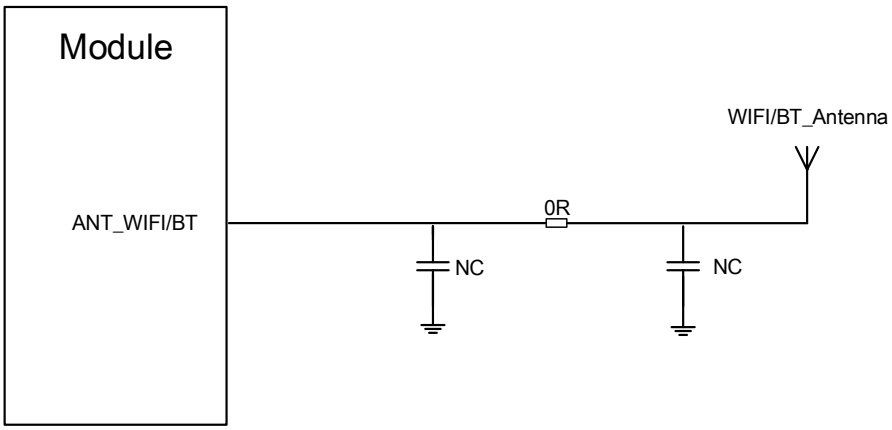

Figure 28 WIFI/BT Antenna Reference Design

4.3 GNSS Antenna

GNSS supports GPS GLONASS BeiDou

Table 26 GNSS Antenna Interface Definition

Pin Name	Pin #	I/O	Description	Note
ANT_GPS	120	AI	GNSS antenna interface	

4.3.1 Operating Frequency

Table 27 GNSS Operating Frequency

Mode	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.42-1605.8	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 GNSS Antenna Reference Design

SS808 series module have a built-in LNA. The passive antenna is used in the design of the device. Microstrip trace is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50 ohm.

The GNSS antenna reference design is shown as follows:

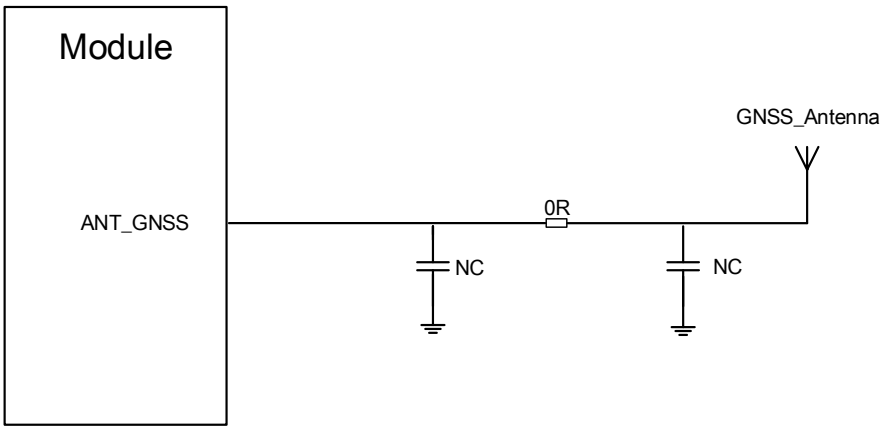

Figure 29-1 GNSS Antenna Reference Design

The active antenna reference circuit is shown in the following figure:

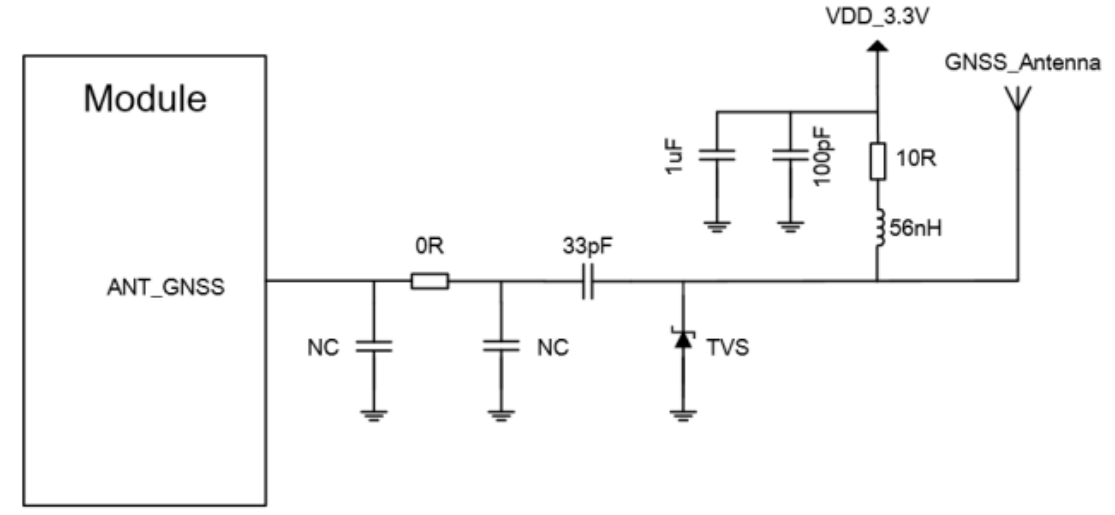

Figure 29-2 GNSS active antenna connection diagram

The power of the active antenna is fed from the antenna's signal line through a 56nH inductor. Common active antennas supply power from 3.3V to 5.0V.The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-performance LDO be used to power the antenna. The active antenna gain requirement is <17db. If the gain is> 17db, the reserved π-type matching needs to be used to increase the attenuation network.

4.4 Antenna Requirement

SS808 series module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 28 Antenna Requirements

SS808 Module Antenna Requirements	
Standard	**Antenna requirements**
WCDMA/LTE	VSWR: ≤ 2 Gain (dBi): 3 Max input power (W): 50 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB (0.7-1GHZ) Insertion loss: < 1.5dB(1.4-2.2GHZ) Insertion loss: < 2dB(2.3-2.7GHZ)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 3 Max input power (W): 50 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB
GNSS	Frequency range: 1559MHz~1607MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) Passive antenna gain: > 0dBi Active antenna noise figure: <1.5dB (typical) Active antenna gain:> -2dBi Built-in LNA gain of active antenna: <17dB (typical)

5 Antenna PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal traces should be within 50Ω. In general, the impedance of the RF signal trace is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually in two ways: microstrip trace and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip trace and coplanar waveguide when the impedance cable is at 50Ω.

- Microstrip trace entirety structure

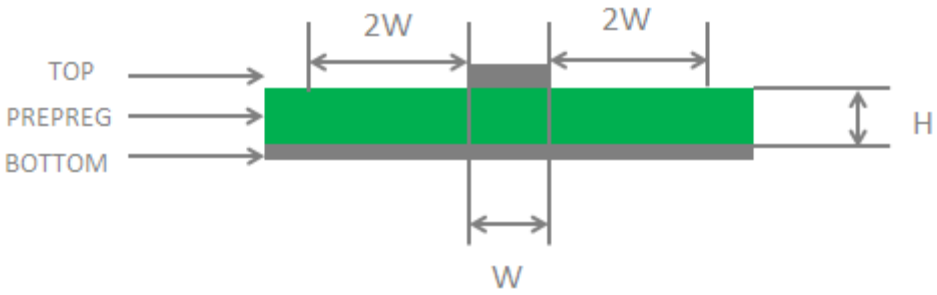

Figure 29 Two-layer PCB Microstrip Cable Structure

- Coplanar waveguide entirety structure

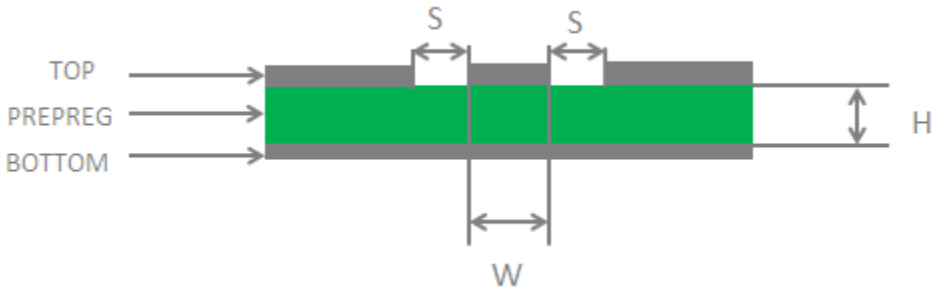

Figure 30 Two-layer PCB Coplanar Waveguide Structure

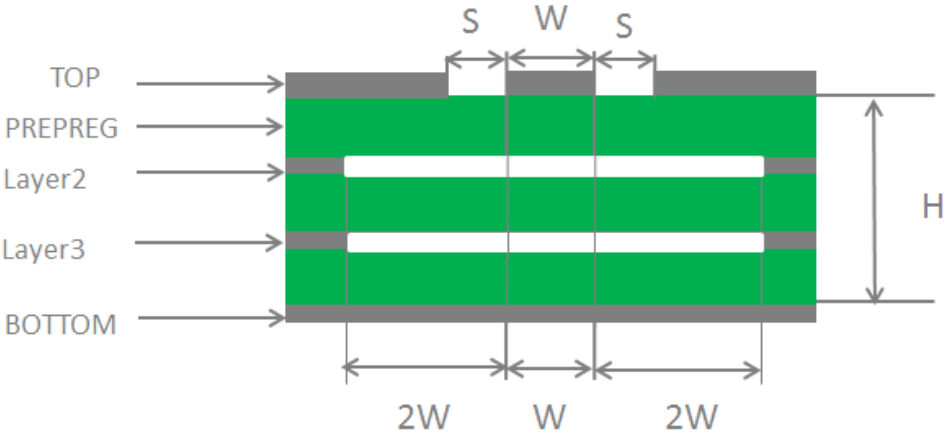

Figure 31 Four-layer PCB Coplanar Waveguide Structure (Reference Ground layer3)

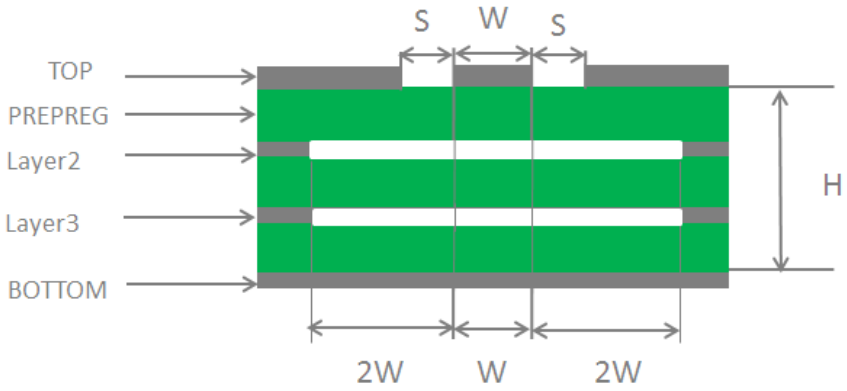

Figure 32 Four-layer PCB Coplanar Waveguide Structure (Reference Ground layer4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degree.
- Attention should be paid to the establishment of the component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal trace should be entirety; adding a certain amount of ground holes around the signal and the reference ground can help improve the RF performance; the distance between the ground hole and the signal trace should be at least 2 times the trace width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

SS808 series module supports 2.4G and 5G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum speed up to 433Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance

Table 29 WIFI Transmit Power

Frequency	Mode	Date Rate	Bandwidth (Mhz)	Mask Margin(dB)
2.4G	802.11b	1Mbps	20	17.0±3
		11Mbps	20	17.0±3
	802.11g	6Mbps	20	16.0±3
		54Mbps	20	13.0±3
	802.11n	MCS0	20	15.0±3
		MCS7	20	12.0±3
		MCS0	40	15.0±3
		MCS7	40	12.0±3
5G	802.11a	6Mbs	20M	19.0±2
		54Mbps	20M	16.0±2
	802.11n	MCS0	20M	18.0±2
		MCS7	20M	15.0±2
		MCS0	40M	17.0±2

Frequency	Mode	Date Rate	Bandwidth (Mhz)	Mask Margin(dB)
		MCS7	40M	14.0±2
	802.11ac	MCS0	20M	18.0±2
		MCS8	20M	16.0±2
		MCS0	40M	180±2
		MCS9	40M	14.0±2
		MCS0	80M	18.0±2
		MCS9	80M	12.0±2

Table 30 WIFI RX Sensitivity

Frequency	Mode	Date Rate	Bandwidth (Mhz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-92.0
		11Mbps	20	-88.0
	802.11g	6Mbps	20	-89.0
		54Mbps	20	-72.0
	802.11n	MCS0	20	-85.0
		MCS7	20	-70.0
5G	802.11a	6Mbps	20M	-89.0
		54Mbps	20M	-72.0
	802.11n	MCS0	20M	-86.0
		MCS7	20M	-70.0
	802.11n	MCS0	40M	-83.0
		MCS7	40M	-67.0
	802.11ac	MCS0	20M	-88.0
		MCS8	20M	-66.0
		MCS0	40M	-85.0
		MCS9	40M	-61.0
		MCS0	80M	-82.0
		MCS9	80M	-55.0

The reference standards are as follows:

IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY,June 2007

IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

6.3 Bluetooth Overview

SS808 series module supports BT4.2 (BR/EDR+BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1MHz and can accommodate 79 channels. The BLE channel bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 31 BT Rate and Version Information

Version	Date Rate	Throughput	Note
BT1.2	1Mb/s	> 80Kbit/s	
BT2.0+EDR	2Mb/s	> 80Kbit/s	
BT3.0+HS	24Mbps	Refer 3.0+HS	
BT4.2 LE	24Mbps	Refer 4.2 LE	

The reference standards are as follows:

Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009

Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009

6.4 Bluetooth Performance

Table 32 BT Performance Index

Type	DH-5	2-DH5	3-DH5	Unit
Transmitter	9±2.5	8±2.5	8±2.5	dBm
Sensitivity	-89	-88	-84	dBm

7 GNSS

7.1 Overview

SS808 series smart module supports multiple positioning systems including GPS, GLONASS and Beidou. The module is embedded with LNA which can effectively improve the sensitivity of GNSS.

7.2 GNSS performance

Table 33 GNSS Positioning Performance

Parameter	Description	Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-157	dBm
C/No	-130dBm	39	dB-Hz
TTFF	Cold Start	44	S
	Warm Start	40	S
	Hot Start	2.5	S
CEP	Static accuracy	5	m

8 Electrical, Reliability and RF Performance

8.1 Recommended Parameters

Table 34 Recommended Parameters

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.2	V
USB_VBUS	4.75	5	5.25	V
VRTC	2.0	3.0	3.25	V
Operating Temperature	-30	25	75	℃
Storage Temperature	-40	25	85	℃

8.2 Power Consumption

Table 35 Power Consumption

Parameter	Description	Condition	Result	Unit
I_{off}	Power Off	Power Off	50	uA
I_{sleep}	WCDMA	DRX=8	3.83	mA
	TDD LTE	DPC (Default Paging Cycle) =#256	3.96	
	FDD LTE	DPC (Default Paging Cycle) =#256	4.72	
	Radio Off	AT+CFUN=4 Flight Mode	3.24	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band2@ max power	504	mA
		Band4@ max power	559	
$I_{LTE-RMS}$	FDD data RMS Current	Band2@max power(10MHz,1RB)	591	mA
		Band4@max power(10MHz,1RB)	575	
		Band5@max power(10MHz,1RB)	600	
		Band7@max power(10MHz,1RB)	616	
		Band12@max power(10MHz,1RB)	612	
		Band13@max power(10MHz,1RB)	580	
		Band25@max power(10MHz,1RB)	590	
		Band26@max power(10MHz,1RB)	600	

Parameter	Description	Condition	Result	Unit
		Band66@max power(10MHz,1RB)	633	
		Band41@max power(10MHz,1RB)	321	

8.3 RF Transmit Power

The transmit power of each band of the SS808 module is shown in the following table:

Table 36 RF Transmit Power

Mode	Band	Max Power(dBm)	Min Power(dBm)
	Band II	24dBm+1/-3dbm	<-49dBm
	Band IV	24dBm+1/-3dbm	<-49dBm
	Band V	24dBm+1/-3dbm	<-49dBm
	Band VIII	24dBm+1/-3dbm	<-49dBm
LTE FDD	Band 2	23dBm±2dbm	<-39dBm
	Band 4	23dBm±2dbm	<-39dBm
	Band 5	23dBm±2dbm	<-39dBm
	Band 7	23dBm±2dbm	<-39dBm
	Band 12	23dBm±2dbm	<-39dBm
	Band 13	23dBm±2dbm	<-39dBm
	Band 25	23dBm±2dbm	<-39dBm
	Band 26	23dBm±2dbm	<-39dBm
	Band 66	23dBm±2dbm	<-39dBm
	Band 41	23dBm±2dbm	<-39dBm

8.4 RF Receiver Sensitivity

The sensitivity of each frequency band of the SS808 series module is shown in the following table:

Table 37 RF Receiver Sensitivity

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
	Band II	-111.2	-111.1	-114.2	-104.7	dBm
	Band IV	-109.6	-110.2	-113.1	-106.7	dBm
	Band V	-111.1	-111.4	-114.4	-104.7	dBm
LTE FDD (10M)	Band 2	-99.8	-100	-102.7	-94.3	dBm
	Band 4	-97.8	-99	-101.5	-96.3	dBm
	Band 5	-99.1	-100	-102	-94.3	dBm
	Band 7	-97.5	-97	-100.5	-94.3	dBm
	Band 12	-98.5	-99.4	-102	-93.3	dBm
	Band 13	-98.7	-98.9	-101.1	-93.3	dBm
	Band 25	-99.8	-98.5	-102.5	-92.8	dBm
	Band 26	-99	-100.2	-102	-93.8	dBm
	Band 66	-98	-99.5	-101.5	-96.3	dBm
LTE TDD (10M)	Band 41	-96	-95.5	-99	-94.3	dBm

8.5 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, so ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

ESD performance parameters table 1-6 (Temperature: 25°C, Humidity: 45%)

Table 38 ESD Performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±4	±8	kV

Other interface	±0.5	±1	kV

9 Structural Specification

9.1 Structural Dimension

The structural dimension of SS808 series module is shown in the follow figure:

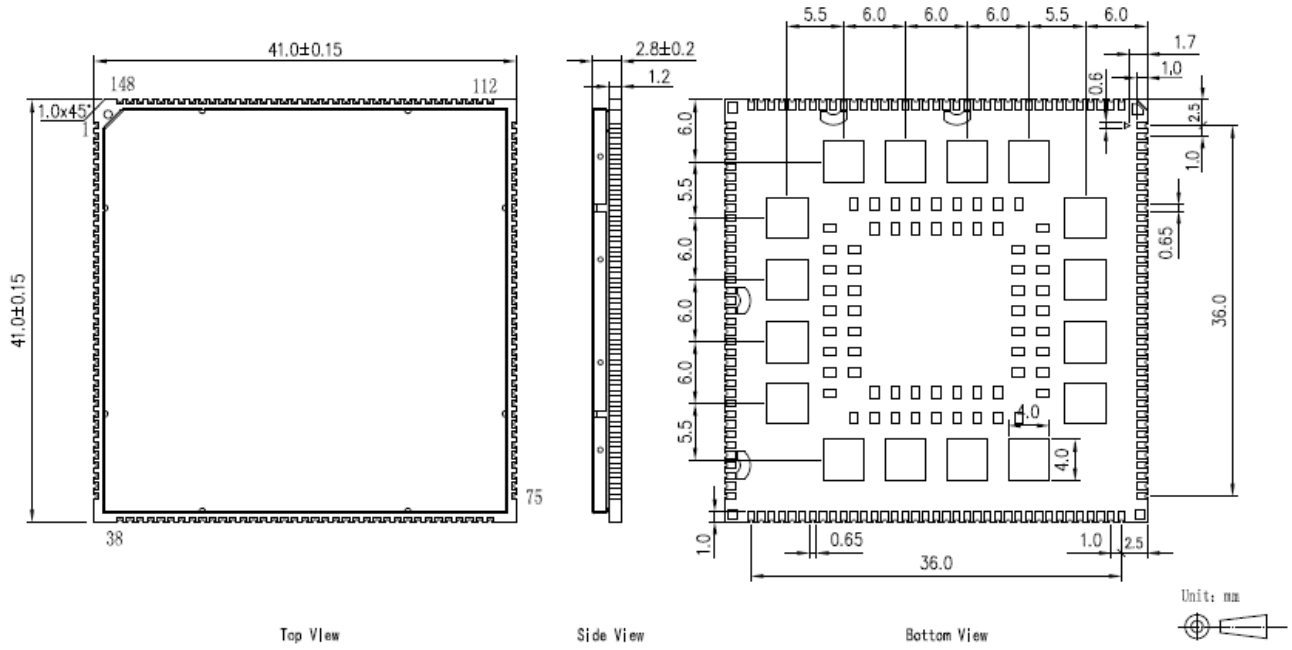

Figure 33 Structural Dimension

9.2 PCB Soldering Pad and Stencil Design

PCB soldering pad and stencil design please refer to《FIBOCOM SS808 SMT Design Description》.

10 Production and Storage

10.1 SMT

SMT production process parameters and related requirements please refer to《FIBOCOM SS808 SMT Design Description》.

10.2 Carrier and storage

Carrier and storage please refer to《FIBOCOM SS808 SMT Design Description》.

11 Terms and acronyms

Table 39 Terms and Acronyms

Term	Definition
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly PolarizedRMS
RMS	Root Mean Square

RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

12 WARING

changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End user must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Host manufacturer is responsible for ensuring that the host continues to be compliant with the Part 15 subpart B unintentional radiator requirements after the module is installed and operational.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID: ZMOSS808NA".The grantee's FCC ID can be used only when all FCC compliance

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the Max allowed antenna gain is as following table showed: ≤3dBi
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed