Fibocom
PERFECT WIRELESS EXPERIENCE

FG101-NA(FCC ID：ZMOFG101NA)

Hardware Guide

V1.1

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Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

Contents

Change History

V1.1 (2022-09-15)	Added band information and NON-PRO notes corresponding to CA band.
V1.0 (2022-05-24)	Initial version.

1 Foreword

1.1 Document Description

This document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of the FG101-NA wireless module. With the assistance of this document and other related documents, application developers can quickly understand the hardware functions of the FG101-NA module and develop product hardware.

1.2 Safety Instructions

By following the safety guidelines below, you can ensure your personal safety and help protect the product and work environment from potential damage. Product manufacturers need to communicate the following safety instructions to end users. Fibocom Wireless does not assume any responsibility for the consequences caused by users' misuse because they do not comply with these safety rules.

Road safety first! When you are driving, do not use any handheld mobile device even if it has a hand-free feature. Stop the car before making a call.

Please turn off the mobile device before boarding. The wireless feature of the mobile device is not allowed on the aircraft to prevent interference with the aircraft communication system. Ignoring this note may result in flight safety issue or even violate the law.

When in a hospital or health care facility, please be aware of restrictions on the use of mobile devices. Radio frequency interference may cause medical equipment to malfunction, so it may be necessary to turn off the mobile device.

The mobile device does not guarantee that an effective connection can be made under any circumstances, for example, when there is no prepayment for the mobile device or (U)SIM is invalid. When you encounter the above situation in an emergency, please remember to use emergency calls, and ensure that your device is turned on and in an area with strong signal.

Your mobile device receives and transmits RF signals when it is poweredon. Your mobile device will receive and transmit RF signals when it is turned on. RF interference occurs when it is near a TV, radio, computer, or other electronic device.

Keep mobile device away from flammable gases. Turn off the mobile device when you are near to gas stations, oil depots, chemical plants orexplosive workplaces. There are potential safety hazards when operating electronic equipment in any potentially explosive area.

1.3 Waring

1.3.1 Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart

B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the
instructions, require that the host product manufacturer must notify to Fibocom Wireless Inc. that they wish to change
the antenna trace design. In this case, a Class II permissive change application is required to be filed
by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOFG101NA”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

(4)The max allowed antenna gain is 4.07dBi for external monopole antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

1.3.2 FCC Statement

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide

reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the
OEM integrator is still responsible for testing their end-product for any additional compliance
requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

2 Product Overview

2.1 Product Introduction

Fibocom FG101-NA series modules support Cat 6, Cat 12, and Cat 13 three network levels, and support CA network architecture. FG101-NA integrates Baseband, Memory, PMIC, Transceiver, PA and other core devices, supporting long-distance communicationmodes of FDD-LTE, TDD-LTE and WCDMA. The maximum downlink rate supported in CAmode is 600 Mbps, and the maximum uplink rate is 150 Mbps.
FG101-NA is designedwith LGA package and is applicable to various scenarios such as CPE, VR/AR, gateway,Internet TV set-top box, and intelligent monitoring.

2.2 Product Specifications

2.2.1 Radio Frequency Features

Table 1. Operating Band

System	FG101-NA(CAT12)
WCDMA	Band 2/4/5
FDD-LTE	Band2/4/5/7/12/13/14/17/25/26/29/30/66/71
TDD-LTE	Band 41 (194M) /46/48

Table 2. Transmission Capacity

System	FG101-NA
WCDMA	Downlink peak rate is 42Mbps Uplink peak rate is 5.76Mbps
LTE	Downlink peak rate is 600Mbps Uplink peak rate is 150Mbps Downlink 4 × 4 MIMO

Table 3. Modulation Features

System	FG101-NA
WCDMA	WCDMA modulation characteristics: Support 3GPP R9/DC-HSDPA/HSPA+/HSDPA/HSUPA/WCDMA Support QPSK modulation
LTE	LTE modulation characteristics: Support 3GPP R12 Support Maximu 3DLCA 、2DLCA Support downlink 256QAM, 64QAM, 16QAM and QPSK modulation Support uplink 64QAM、16QAM、QPSK modulation Support RFbandwidth 1.4 MHz to 20 MHz

2.2.2 Other Key Features

Table 4. Other Key Features

Item	Description
Power supply	DC: 3.4 V–4.3 V Typical voltage: 3.8 V
Storage	2Gb LPDDR2 + 2Gb NAND Flash
Supported systems	Linux/Android/Windows
Power class	Class 3 (23.5dBm ± 2dBm) for WCDMA bands Class 3 (23dBm ± 2dBm) for LTE bands Class 2 (26dBm ± 2dBm) for LTE band41 HPUE
Satellite	GPS/GLONASS/Galileo/BDS

positioning	
SMS	Support
Audio interface	Support PCM digital audio interface
USB interface	A set of USB 3.0 superspeed (SS) interfaces with data transmission rate up to 5 Gbps Compatible with USB 2.0 highspeed (HS) interfaces, with data transmission rate up to 480 Mbps Used for AT command transmission, data transmission, software debugging, software upgrading, etc.
PCIe interface	PCIe Gen2 × 1Lane, the maximum transmission rate is 5GT/s, and RC mode is supported
SIM interface	2 sets of SIM card interfaces, supporting dual SIM single standby Support USIM: 1.8 V and 3 V
I2C interface	A set of I2C with a maximum speed of 3.4 Mbps
Physical characteristic	Dimensions: 39.5 mm x 37 mm x 2.8 mm Packaging: 299-pin LGA Weight: 8.54g ± 0.5g
Temperature range	Operating temperature: –30°C to 75°C The module works normally within this temperature range, and the related performance meets the requirements of 3GPP standards. Extended temperature: –40°C to 85°C The module works normally within this temperature range, and the baseband and RF functions are normal. However, some indicators may exceed the range of 3GPP standards. When the temperature returns to the normal working range of the module, all the indicators

	of the module meet the requirements of 3GPP standards. Storage temperature: –40°C to 90°C The storage temperature range of the module when the module is powered off.
Software upgrade	Through USB interface/FOTA
Environmental standards	RoHS and halogen-free

2.3 Supported CA Combinations

Table 5. CA combinations supported by FG101-NA

Combi nation	CA Configuration	ULCA	4x4 MIMO	Notes
CAT12_2DLCA	CA_2A-4A	- -	2A,4A	- -
	CA_2A-5A	- -	2A	- -
	CA_2A-12A	- -	2A	- -
	CA_2A-13A	- -	2A	- -
	CA_2A-14A	- -	2A	- -
	CA_2A-29A	- -	2A	- -
	CA_2A-30A	- -	30A,2A	- -
	CA_2A-66A	- -	2A,66A	- -
	CA_4A-5A	- -	4A	- -
	CA_4A-12A	- -	4A	- -
	CA_4A-13A	- -	4A	- -
	CA_4A-29A	- -	4A	- -
	CA_4A-30A	- -	4A,30A	- -

CA_5A-30A	- -	30A	- -
CA_5A-66A	- -	66A	- -
CA_12A-30A	- -	30A	- -
CA_13A-66A	- -	66A	- -
CA_14A-30A	- -	30A	- -
CA_14A-66A	- -	66A	- -
CA_29A-30A	- -	30A	- -
CA_2A-2A	- -	- -	- -
CA_4A-4A	- -	4A	- -
CA_25A-25A	- -	- -	- -
CA_25A-26A	- -	25A	- -
CA_25A-41A	- -	25A,41A	- -
CA_26A-41A	- -	41A	- -
CA_41A-41A	- -	- -	- -
CA_66A-66A	- -	66A	- -
CA_2C	- -	- -	- -
CA_5B	5B	- -	- -
CA_41C	41C	- -	- -
CA_66C	- -	- -	- -
CA_2A-46A	- -	2A	- -
CA_4A-46A	- -	4A	- -
CA_13A-46A	- -	- -	- -
CA_25A-46A	- -	25A	- -
CA_46A-66A	- -	66A	- -
CA_5A-46A	- -	- -	- -
CA_12A-66A	- -	66A	- -
CA_29A-66A	- -	66A	- -

	CA_30A-66A	- -	30A,66A	- -
	CA_66B	- -	- -	- -
	CA_4A-71A	- -	4A	- -
	CA_2A-71A	- -	2A	- -
	CA_66A-71A	- -	66A	- -
	CA_48C	- -	- -	- -
	CA_2A-48A	- -	2A	- -
	CA_5A-48A	- -	- -	- -
	CA_13A-48A	- -	- -	- -
	CA_48A-66A	- -	66A	- -
	CA_2A-7A	- -	2A,7A	- -
	CA_4A-7A	- -	4A,7A	- -
	CA_7A-7A	- -	- -	- -
	CA_7A-12A	- -	7A	- -
	CA_7A-66A	- -	66A,7A	- -
	CA_5A-5A	- -	- -	- -
	CA_12A-12A	- -	- -	- -
	CA_12A-25A	- -	25A	- -
	CA_12A-46A	- -	- -	- -
	CA_12B	- -	- -	- -
	CA_26A-46A	- -	- -	- -
	CA_5A-25A	- -	25A	- -
	CA_5A-41A	- -	41A	- -
	CA_5A-7A	- -	7A	- -
	CA_7A-46A	- -	7A	- -
	CA_7B	- -	- -	- -
	CA_7C	7C	- -	- -

	CA_2A-4A-4A	- -	- -	- -
	CA_2A-4A-5A	- -	- -	- -
	CA_2A-4A-12A	- -	- -	- -
	CA_2A-4A-13A	- -	- -	- -
	CA_2A-5A-30A	- -	- -	- -
	CA_2A-12A-30A	- -	- -	- -
	CA_2A-29A-30A	- -	- -	- -
	CA_2A-5A-66A	- -	- -	- -
	CA_2A-13A-66A	- -	- -	- -
	CA_2A-14A-30A	- -	- -	- -
	CA_2A-14A-66A	- -	- -	- -
	CA_2A-30A-66A	- -	- -	- -
	CA_2A-66A-66A	- -	- -	- -
CAT12-3DLCA	CA_4A-5A-30A	- -	- -	- -
	CA_4A-12A-30A	- -	- -	- -
	CA_4A-29A-30A	- -	- -	- -
	CA_2A-2A-5A	- -	- -	- -
	CA_2A-2A-12A	- -	- -	- -
	CA_2A-2A-13A	- -	- -	- -
	CA_2A-2A-30A	- -	- -	- -
	CA_2A-2A-66A	- -	- -	- -
	CA_4A-4A-5A	- -	- -	- -
	CA_4A-4A-12A	- -	- -	- -
	CA_4A-4A-13A	- -	- -	- -
	CA_13A-66A-66A	- -	- -	- -
	CA_14A-30A-66A	- -	- -	- -
	CA_2A-5B	- -	- -	- -

	CA_2A-66C	- -	- -	- -
	CA_5A-66A-66A	- -	- -	- -
	CA_5B-30A	- -	- -	- -
	CA_5B-66A	- -	- -	- -
	CA_25A-41C	- -	- -	- -
	CA_26A-41C	- -	- -	- -
	CA_41A-41C	- -	- -	- -
	CA_66A-66C	- -	- -	- -
	CA_41D	- -	- -	- -
	CA_2A-5A-46A	- -	- -	- -
	CA_2A-13A-46A	- -	- -	- -
	CA_2A-46A-66A	- -	- -	- -
	CA_2A-46C	- -	- -	- -
	CA_4A-46C	- -	- -	- -
	CA_5A-46A-66A	- -	- -	- -
	CA_13A-46A-66A	- -	- -	- -
	CA_13A-46C	- -	- -	- -
	CA_5A-46C	- -	- -	- -
	CA_2A-12A-66A	- -	- -	- -
	CA_2A-66B	- -	- -	- -
	CA_5A-30A-66A	- -	- -	- -
	CA_5A-66B	- -	- -	- -
	CA_12A-30A-66A	- -	- -	- -
	CA_12A-66A-66A	- -	- -	- -
	CA_13A-66B	- -	- -	- -
	CA_29A-30A-66A	- -	- -	- -
	CA_29A-66A-66A	- -	- -	- -

	CA_30A-66A-66A	- -	- -	- -
	CA_46C-66A	- -	- -	- -
	CA_2A-2A-46A	- -	- -	- -
	CA_46A-66A-66A	- -	- -	(NON-PRO)
	CA_2A-4A-71A	- -	- -	- -
	CA_4A-4A-71A	- -	- -	- -
	CA_2A-2A-71A	- -	- -	- -
	CA_13A-48C	- -	- -	- -
	CA_5A-48C	- -	- -	- -
	CA_48D	- -	- -	- -
	CA_48A-66C	- -	- -	(NON-PRO)
	CA_2A-48A-66A	- -	- -	- -
	CA_2A-48C	- -	- -	- -
	CA_48C-66A	- -	- -	(NON-PRO)
	CA_2A-5A-48A	- -	- -	- -
	CA_2A-13A-48A	- -	- -	- -
	CA_5A-48A-66A	- -	- -	- -
	CA_13A-48A-66A	- -	- -	- -
	CA_12A-66C	- -	- -	- -
	CA_66A-66A-71A	- -	- -	- -
	CA_2A-66A-71A	- -	- -	- -
	CA_2A-2A-4A	- -	- -	- -
	CA_4A-5B	- -	- -	- -
	CA_5A-5A-66A	- -	- -	- -
	CA_5A-66C	- -	- -	- -
	CA_13A-66C	- -	- -	- -
	CA_48A-66A-66A	- -	- -	(NON-PRO)

	CA_48A-66B	- -	- -	(NON-PRO)
	CA_4A-48C	- -	- -	- -
	CA_2A-2A-14A	- -	- -	- -
	CA_14A-66A-66A	- -	- -	- -
	CA_2C-66A	- -	- -	- -
	CA_66C-71A	- -	- -	- -
	CA_2A-4A-30A	- -	- -	- -
	CA_12A-46C	- -	- -	- -
	CA_12A-66B	- -	- -	- -
	CA_25A-25A-26A	- -	- -	- -
	CA_25A-25A-41A	- -	- -	- -
	CA_25A-25A-46A	- -	- -	(NON-PRO)
	CA_25A-26A-41A	- -	- -	- -
	CA_25A-41A-41A	- -	- -	- -
	CA_25A-46C	- -	- -	- -
	CA_26A-41A-41A	- -	- -	- -
	CA_2A-12A-12A	- -	- -	- -
	CA_2A-12A-46A	- -	- -	- -
	CA_2A-12B	- -	- -	- -
	CA_2A-29A-66A	- -	- -	- -
	CA_2A-2A-29A	- -	- -	- -
	CA_2A-4A-29A	- -	- -	- -
	CA_2A-4A-7A	- -	- -	- -
	CA_2A-7A-12A	- -	- -	- -
	CA_2A-7A-66A	- -	- -	- -
	CA_2A-7A-7A	- -	- -	- -
	CA_2A-7C	- -	- -	- -

	CA_2C-12A	- -	- -	- -
	CA_2C-29A	- -	- -	- -
	CA_2C-30A	- -	- -	- -
	CA_2C-5A	- -	- -	- -
	CA_4A-12A-12A	- -	- -	- -
	CA_4A-12B	- -	- -	- -
	CA_4A-4A-29A	- -	- -	- -
	CA_4A-4A-30A	- -	- -	- -
	CA_4A-4A-7A	- -	- -	- -
	CA_4A-7A-12A	- -	- -	- -
	CA_4A-7A-7A	- -	- -	- -
	CA_4A-7C	- -	- -	- -
	CA_5A-7A-46A	- -	- -	- -
	CA_5A-7A-7A	- -	- -	- -
	CA_5A-7C	- -	- -	- -
	CA_66A-66B	- -	- -	- -
	CA_66D	- -	- -	- -
	CA_7A-46C	- -	- -	- -
	CA_7A-66A-66A	- -	- -	- -

2.4 Functional Block Diagram

Functional block diagram shows the main hardware features of the FG101-NA series module, including the baseband and RF features.

Baseband section

- CPU
- PMIC

- LPDDR2
- NAND
- USB, PCIe, (U)SIM, PCM, I^2C, SPI, UART, SDIO, GPIOs, ADCs
- WCDMA/LTE TDD/LTE FDD controller

RF section

- RF Transceiver
- RF PA
- RF Switch
- RF filter
- Antenna

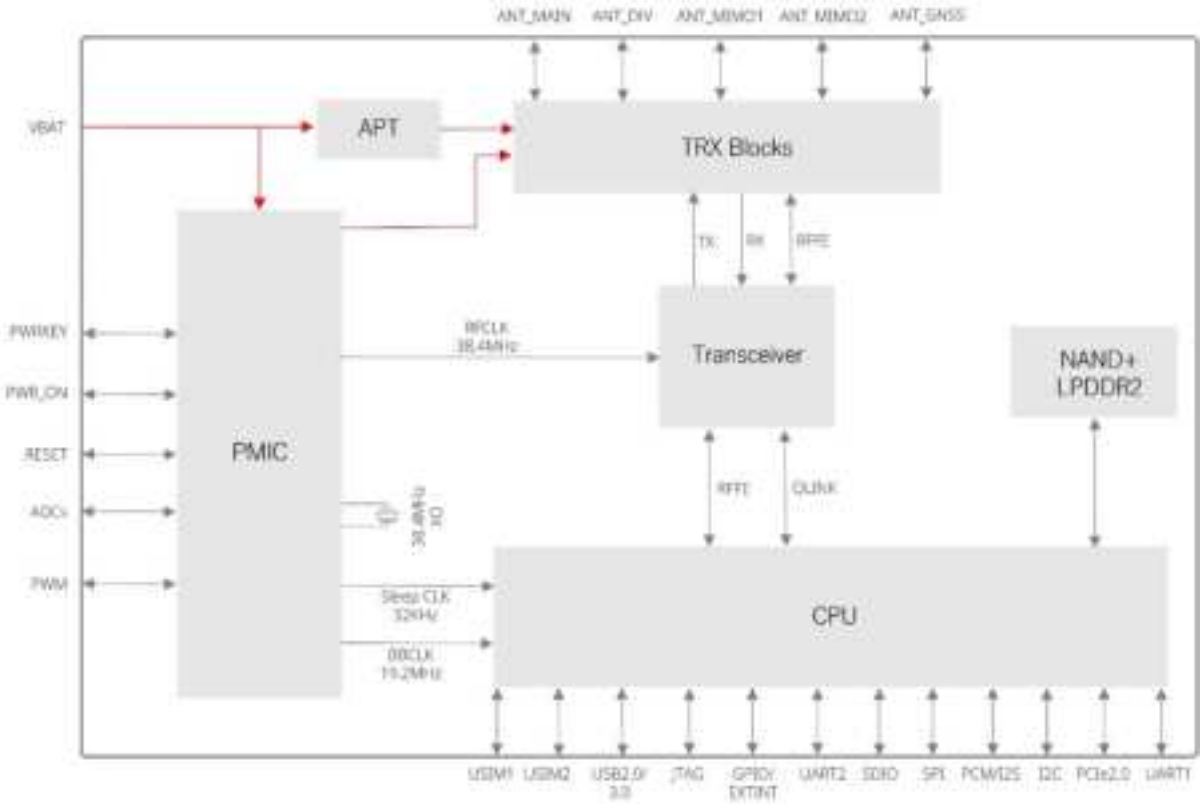


Figure 1. Functional Block Diagram

2.5 Evaluation Board

Fibocom provides EVB-LGA-F01 and ADP-FG101-NA evaluation boards to facilitate module debug and use. For details about usage, see *Fibocom_FG101_Hardware_Guide_EVB* and *Fibocom_ADP-FG101-NA_Hardware_Guide*.

3 Pin Definition

3.1 Pin Distribution

The FG101-NA series module uses LGA packaging and have 299 pins in total. The following figure shows a top perspective view of the pin distribution.

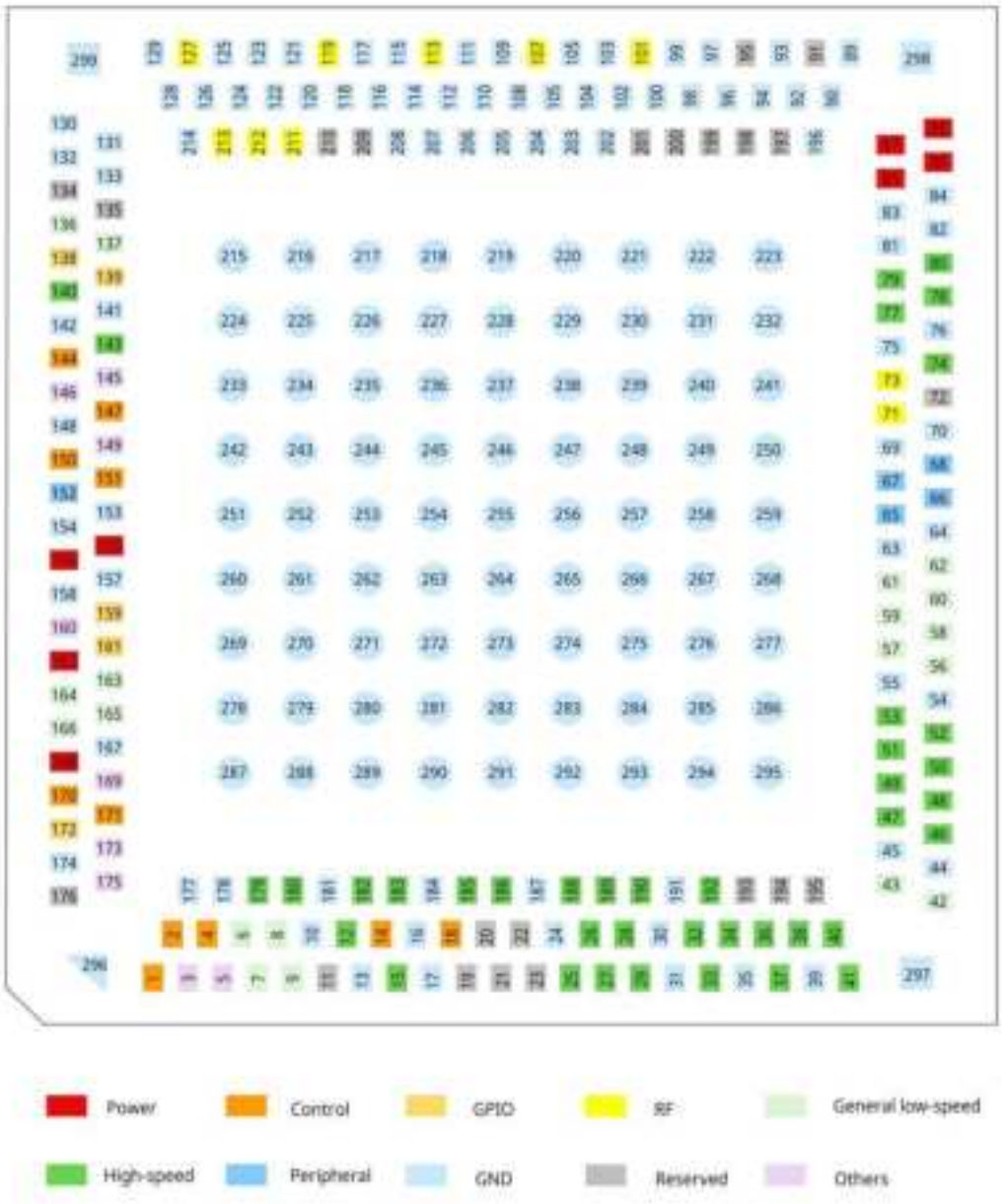


Figure 2. Pin Distribution

The pin details on the left and upper side of the module are shown in the following figure.

Figure 3. Pin Details (1)

The pin details on the right side and below the module are shown in the following figure.

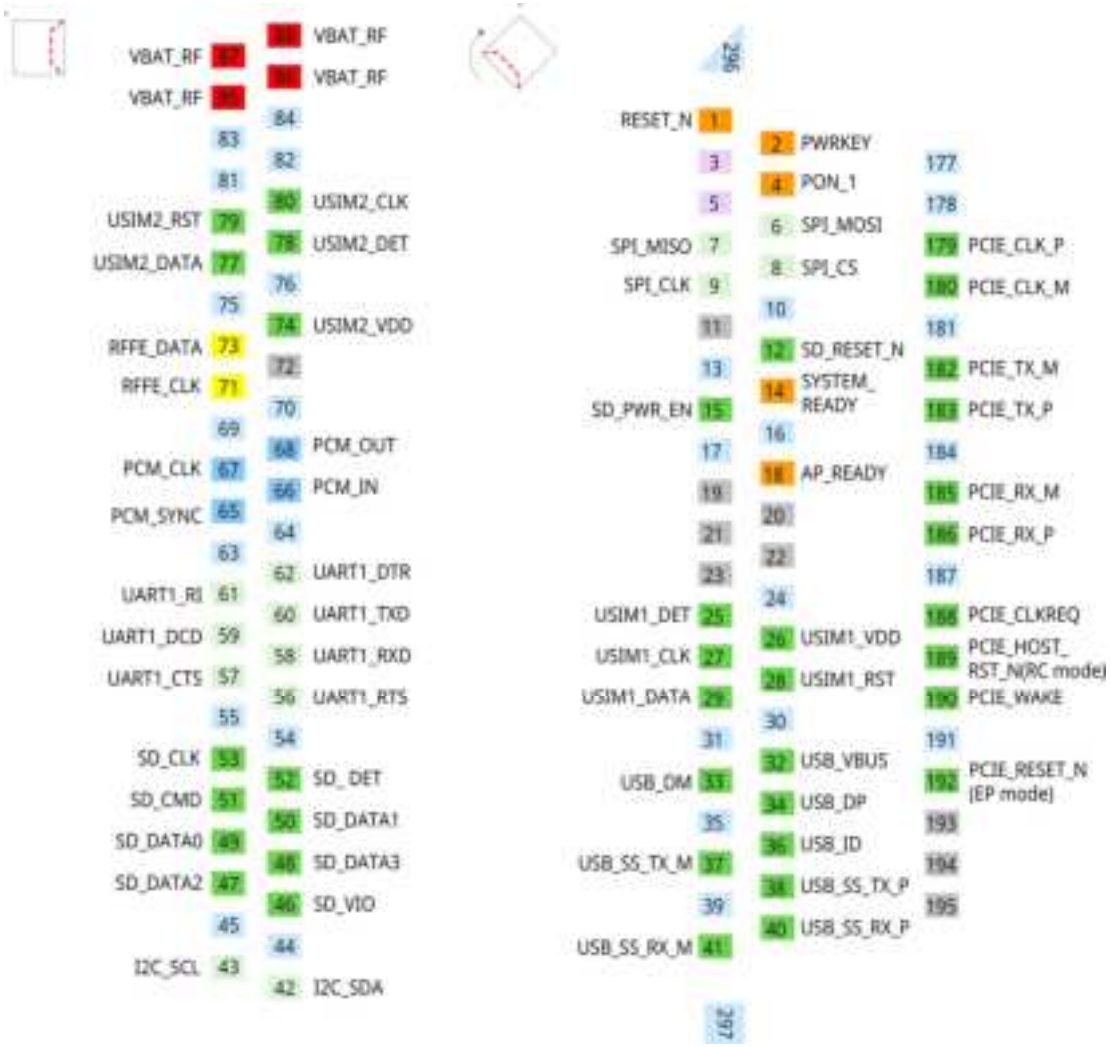


Figure 4. Pin Details (2)

3.2 Pin Function

The pin functions of FG101-NA series module are shown in the following table.

Table 6. LGA Pin Function Description

Pin Number	Pin Name	I/O	Power Domain	Reset Status	Pin Description
1	RESET_N	DI	1.8V	PU	Module reset signal, active low and no external pull-up is required

2	PWRKEY	DI	1.8V	PU	Module power on/off signal. Pull down it for more than 1.6s to power on. For details, refer to “Control Interface” section. No external pull-up is required
3	BT_EN*	DO	1.8V	PD	BT function enable pin, reserved
4	PON_1	DI	1.8V	PD	Module startup signal, high level startup, used for automatic startup function
5	WLAN_PWR_EN*	DO	1.8V	PD	WLAN power enable, reserved
6	SPI_MOSI	DIO	1.8V	- -	SPI data output
7	SPI_MISO	DIO	1.8V	- -	SPI data input
8	SPI_CS	DIO	1.8V	- -	SPI chip selection signal
9	SPI_CLK	DIO	1.8V	- -	SPI clock signal
12	SD_RESET_N*	DO	1.8V	- -	Reset output signal, which is connected to eMMC chip and reserved
14	SYSTEM_READY	DO	1.8V	- -	Module sleep status detection signal
15	SD_PWR_EN	DO	1.8V	PD	External SD card power switch control signal
18	AP_READY	DI	1.8V	- -	Host sleep status detection signal
25	USIM1_DET	DI	1.8V	- -	(U)SIM card hot plug detection

26	USIM1_VDD	PO	1.8V/3V	- -	(U)SIM power supply, the module automatically identifies 1.8 V or 3.0 V (U)SIM card
27	USIM1_CLK	DO	1.8V/3V	- -	(U)SIM clock signal line
28	USIM1_RST	DO	1.8V/3V	- -	(U)SIM reset signal line
29	USIM1_DATA	DIO	1.8V/3V	- -	(U)SIM data signal line
32	USB_VBUS	DI	- -	- -	USB insertion detection
33	USB_DM	AIO	- -	- -	USB 2.0 differential data signal (–)
34	USB_DP	AIO	- -	- -	USB 2.0 differential data signal (+)
36	USB_ID*	DI	1.8V	- -	OTG identification signal, which is reserved.
37	USB_SS_TX_M	AO	- -	- -	USB 3.0 differential transmitting signal (–)
38	USB_SS_TX_P	AO	- -	- -	USB 3.0 differential transmitting signal (+)
40	USB_SS_RX_P	AI	- -	- -	USB 3.0 differential receiving signal (+)
41	USB_SS_RX_M	AI	- -	- -	USB 3.0 differential receiving signal (–)
42	I2C_SDA	OD	1.8V	PU	I2C interface data signal, which is pulled up internally
43	I2C_SCL	OD	1.8V	PU	I2C interface clock signal, which is pulled up internally

46	SD_VIO*	PO	1.8V/3V	- -	SD card IO power supply, 3.0V or 1.8V adaptive, which is reserved for SDIO pull-up. SD card needs external power supply
47	SD_DATA2	DIO	1.8V/3V	- -	SD card data signal
48	SD_DATA3	DIO	1.8V/3V	- -	SD card data signal
49	SD_DATA0	DIO	1.8V/3V	- -	SD card data signal
50	SD_DATA1	DIO	1.8V/3V	- -	SD card data signal
51	SD_CMD	DIO	1.8V/3V	- -	SD card command signal
52	SD_ DET	DI	1.8V	- -	SD card hot plug detection signal
53	SD_CLK	DO	1.8V/3V	- -	SD card clock signal
56	UART1_RTS*	DO	1.8V	- -	Request to send data, reserved
57	UART1_CTS*	DI	1.8V	- -	Clear to send, reserved
58	UART1_RXD*	DI	1.8V	- -	Module receives data, reserved
59	UART1_DCD*	DO	1.8V	- -	Module outputs carrier detection, reserved
60	UART1_TXD*	DO	1.8V	- -	Module transmits data, reserved
61	UART1_RI	DO	1.8V	- -	Module outputs ring indicator
62	UART1_DTR*	DI	1.8V	- -	Ready, sleep mode control, reserved
65	PCM_SYNC	DIO	1.8V	- -	PCM data synchronization signal by default

66	PCM_IN	DI	1.8V	- -	PCM data input signal by default
67	PCM_CLK	DO	1.8V	- -	PCM clock signal by default
68	PCM_OUT	DO	1.8V	- -	PCM output signal by default
71	RFFE_CLK*	DO	1.8V	- -	RFFE clock signal, used to control external tuner, reserved
73	RFFE_DATA*	DIO	1.8V	- -	RFFE data signal, used to control external tuner, reserved
74	USIM2_VDD	PO	1.8V/3V	- -	(U)SIM2 power supply, the module automatically identifies 1.8 V or 3.0 V (U)SIM card
77	USIM2_DATA	DIO	1.8V/3V	- -	(U)SIM2 data signal line by default, SPI_MOSI (reserved)
78	USIM2_DET	DI	1.8V	- -	(U)SIM2 card hot plug detection, SPI_MISO (reserved)
79	USIM2_RST	DO	1.8V/3V	- -	(U)SIM reset signal line by default, SPI_CS (reserved)
80	USIM2_CLK	DO	1.8V/3V	- -	(U)SIM2 clock signal line by default, SPI_CLK (reserved)
85~88	VBAT_RF	PI	- -	- -	RF power input (3.4 V–4.3 V)
101	ANT_MIMO1	AI	- -	- -	MIMO1 antenna
107	ANT_DIV	AI	- -	- -	Diversity antenna
113	ANT_MIMO2	AI	- -	- -	MIMO2 antenna
119	ANT_GNSS	AI	- -	- -	GNSS antenna

127	ANT_MAIN	AIO	- -	- -	Main antenna
136	DBG_RXD	DI	1.8V	- -	DEBUG serial port receives data
137	DBG_TXD	DO	1.8V	- -	DEBUG serial port transmits data
138	GPIO_1	DIO	1.8V	- -	General GPIO
139	GPIO_2	DIO	1.8V	- -	General GPIO
140	USB_BOOT	DI	1.8V	PD	Emergency download, active high. It is recommended to reserve test points.
143	OTG_PWR_EN*	DO	1.8V	PD	OTG power enabling, reserved
144	SLEEP_IND	DO	1.8V	- -	Sleep status indicator
145	COEX_UART_TXD*	DO	1.8V	- -	LTE and WLAN share a serial port transmission signal line, reserved
146	COEX_UART_RXD*	DI	1.8V	- -	LTE and WLAN share a serial port receiving signal line, reserved
147	NET_MODE	DO	1.8V	- -	Indicator of registered network mode, reserved
149	WLAN_EN*	DO	1.8V	- -	Wake up WLAN module, reserved
150	WAKEUP_IN	DI	1.8V	- -	External device wake-up module, active low by default. The software can be configured
151	W_DISABLE_N	DI	1.8V	PU	Module flight mode control, pulled up by default. Low level enables the module to enter

					flight mode
152	I2S_MCLK	DO	1.8V	- -	Reserved, I2S function is not developed currently
155,156	VBAT_BB	PI	- -	- -	Baseband power input (3.4V–4.3V)
159	GPIO_3	DIO	1.8V	- -	General GPIO. Interrupt triggering is supported
160	WLAN_WAKE*	DI	1.8V	- -	WLAN chip wakes up module, reserved
161	GPIO_4	DIO	1.8V	- -	General GPIO. Interrupt triggering is supported
162	VDD_RF_2V8	PO	- -	- -	2.7 V voltage output, 100 nF capacitance to ground is required
163	UART2_TXD*	DO	1.8V	- -	Bluetooth serial port transmits data, reserved
164	UART2_RTS*	DO	1.8V	- -	Bluetooth serial port requests to send data, reserved
165	UART2_RXD*	DI	1.8V	- -	Bluetooth serial port receives data, reserved
166	UART2_CTS*	DI	1.8V	- -	Bluetooth serial port clear to send data, reserved
168	VDD_EXT_1V8	PO	- -	- -	1.8V power output
169	WLAN_SLP_CLK*	DO	1.8V	- -	WLAN sleep clock signal, reserved

170	NET_STATUS	DO	1.8V	PD	Network connection status indicator (default)
171	STATUS	DO	1.8V	PD	System operation status indicator, reserved
172	GPIO_5	DIO	1.8V	- -	General GPIO
173	ADC0	AI	1.8V	- -	Analog to digital input port 0
175	ADC1	AI	1.8V	- -	Analog to digital input port 1
179	PCIE_CLK_P	AO	- -	- -	PCIe reference clock signal positive
180	PCIE_CLK_M	AO	- -	- -	PCIe reference clock signal negative
182	PCIE_TX_M	AO	- -	- -	PCIe data transmitting signal negative
183	PCIE_TX_P	AO	- -	- -	PCIe data transmitting signal positive
185	PCIE_RX_M	AI	- -	- -	PCIe data receiving signal negative
186	PCIE_RX_P	AI	- -	- -	PCIe data receiving signal positive
188	PCIE_CLKREQ	DIO	1.8V	OD	PCIe clock request signal
189	PCIE_HOST_RST_N	DO	1.8V	PD	PCIe reset signal
190	PCIE_WAKE	DI	1.8V	OD	PCIe wake-up signal

192	PCIE_RESET_N*	DI	1.8V	PD	EP mode PCIe reset signal, reserved
211	TUNER_1*	DO	1.8V	- -	General RF control signal, reserved
212	TUNER_2*	DO	1.8V	- -	General RF control signal, reserved
213	TUNER_3*	DO	1.8V	- -	General RF control signal, reserved

Table 7. LGA Pin Function Description

Pin Number	Pin Name	I/O	Pin Description
10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76,81~84, 89, 90, 92~94, 96~100, 102~106, 108~112, 114~118, 120~126, 128~133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202~208, 214~299	GND	G	GND
11, 19~23, 72, 91, 95, 134, 135, 176, 193~195, 197~201, 209, 210	NC	- -	- -

Pins marked with * are reserved functions or under development.Leave unused pins floating.

Table 8. I/O Parameter Description

Type	Description
PI	Power input

PO	Power output
DI	Digital input
DO	Digital output
DIO	Digital input/output
AI	Analog input
AO	Analog output
AIO	Analog input/output
OD	Open drain

4 Electrical Characteristics

4.1 Limit Voltage Range

The limit voltage includes the absolute limit voltage and the operating limit voltage. Theabsolute limit voltage is the maximum voltage that the module can bear, beyond whichthe module may be damaged. The operating limit voltage is the normal operating voltagerange of the module, beyond which the module will have an abnormal performance.

4.1.1 Absolute Limit Voltage

The following table describes the absolute limit voltage ranges of FG101-NA series module.

Table 9. Absolute Limit Voltage Range

Parameter	Description	Minimum Value (V)	Maximum Value (V)
VBAT	Power supply	–0.3	6
GPIO	Digital IO level supply voltage	–0.3	2.3

4.1.2 Operating Limit Voltage

Table 10. Operating Limit Voltage (Signal)

Signal	Logical low level		Logical high level	
	Minimum Value (V)	Maximum Value (V)	Minimum Value (V)	Maximum Value (V)
Digital input	-0.3	0.36	0.7 × VDD	VDD + 0.3
Digital output	0	0.45	VDD - 0.45	VDD
RESET_N	-0.3	0.5	1.25	1.89

PWRKEY	-0.3	0.5	1.25	1.89
PON_1	-0.3	0.5	1.25	1.89

Table 11. Operating Limit Voltage (Power Supply)

Parameter	I/O	Minimum Value (V)	Typical Value	Maximum Value (V)
VBAT	PI	3.4	3.8	4.3
USIM1_VDD	PO	1.75/2.8	1.8/2.85	1.85/2.928
USIM2_VDD	PO	1.75/2.8	1.8/2.85	1.85/2.928
SD_VIO	PO	1.75/2.8	1.8/2.85	1.85/2.928
USB_VBUS	PI	2.4	5.0	5.25

4.2 Power Consumption

The power consumption of FG101-NA series module measured under 3.8 V power supply is described in the following table. For AT commands used for USB sleep andwakeup, see *Fibocom_FG101_AT Commands User Manual*. The USB used in the power consumption test is USB3.0.

Table 12. Power Consumption

Parameter	Mode	Status	Average Current TypicalValue (mA)
I_{off}	Power off	Module power-off	TBD
I_{sleep}	WCDMA	DRX8 (USB sleep)	TBD
	FDD-LTE	Paging Cycle #64 (USB sleep)	TBD
	FDD-LTE	Paging Cycle #256 (USB sleep)	TBD

	TDD-LTE	Paging Cycle #64 (USB sleep)	TBD
	TDD-LTE	Paging Cycle #256 (USB sleep)	TBD
	Radio Off	AT+CFUN=4 (USB sleep)	TBD
I_{idle}	WCDMA	DRX6 (USB sleep)	TBD
		DRX6 (USB wakeup)	TBD
	FDD-LTE	Paging Cycle #64 (USB sleep)	TBD
		Paging Cycle #64 (USB wakeup)	TBD
	TDD-LTE	Paging Cycle #64 (USB sleep)	TBD
		Paging Cycle #64 (USB wakeup)	TBD
$I_{WCDMA-RMS}$	WCDMA	Band2 @+23.5dBm	700
		Band4 @+23.5dBm	700
		Band5 @+23.5dBm	650
$I_{LTE-RMS(10MHz\ 1RB)}$	FDD-LTE	Band2 @+23dBm	700
		Band4 @+23dBm	700
		Band5 @+23dBm	650
		Band7 @+23dBm	850
		Band12 @+23dBm	650
		Band13 @+23dBm	650

		Band14 @+23dBm	650
		Band17 @+23dBm	650
		Band25 @+23dBm	700
		Band26 @+23dBm	650
		Band30 @+23dBm	850
		Band66 @+23dBm	700
		Band71 @+23dBm	650
	TDD-LTE	Band41 @+26dBm	650
		Band48 @+23dBm	480

Table 13. 2CA Power Consumption

2CA Typical Combination	Transmitting Band@FRB@Data Transmission Status	Typical Current (mA)
2A-5A	B2+B5 @+21dBm	750
2A-12A	B2+B12 @+21dBm	750
2A-13A	B2+B13 @+21dBm	750
2A-14A	B2+B14 @+21dBm	750
71A-66A	B71+B66 @+21dBm	750
30A-4A	B30+B4 @+21dBm	900
66A-7A	B66+B7 @+21dBm	900

Table 14. 3CA Power Consumption

3CA Typical Combination	Transmitting Band@FRB@Data Transmission Status	Typical Current (mA)
2A-4A-5A	B2+B4+B5 @+21dBm	750
2A-4A-12A	B2+B4+B12 @+21dBm	750
2A-4A-13A	B2+B4+B13 @+21dBm	790
2A-14A-30A	B2+B14+B30 @+21dBm	900
2A-14A-66A	B2+B14+B66 @+21dBm	750
2A-66A-66A	B2+B66+B66 @+21dBm	750
4A-29A-30A	B4+B29+B30 @+21dBm	900
4A-5A-30A	B4+B5+B30 @+21dBm	900

5 Functional Interface

5.1 Power Supply

The following table describes the power interface of FG101-NA series module.

Table 15. Power Interface

Pin Name	I/O	Pin Number	Description
VBAT_RF	PI	85, 86, 87, 88	Module RF power supply, 3.4V–4.3V, 3.8V is recommended
VBAT_BB	PI	155, 156	Module baseband power supply, 3.4V–4.3V, 3.8V is recommended
VDD_EXT_1V8	PO	168	LDO power supply output, 1.8V/50mA is output
VDD_RF_2V8	PO	162	LDO power supply output, 2.7V/50mA is output
GND	G	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89, 90, 92~94, 96~100, 102~106, 108~112, 114~118, 120~126, 128~133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202~208, 214~299	Ground

In this document, VBAT includes VBAT_RF and VBAT_BB. The supply voltage of VBAT_RF and VBAT_BB must be consistent.

5.1.1 Power Input

The FG101-NA series module is powered on through the VBAT pin. The following figure shows the recommended power supply design.

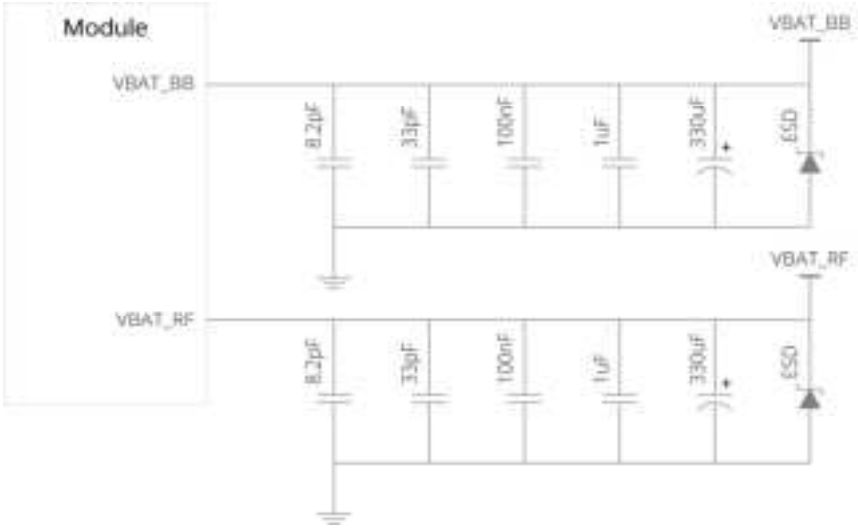


Figure 5. Recommended Power Supply Design

The filter capacitor design of power supply is shown in the following table.

Table 16. Power Supply Filter Capacitor Design

Recommended Capacitor	Application	Description
330uF x 2	Voltage stabilizing capacitor	To reduce the power supply fluctuation when the module works, it is required to adopt low ESR capacitor, which is not less than 440uF, and the

		driving capacity of VBAT power supply current is not less than 2.0 A.
1uF, 100nF	Digital signal noise	Filter out interference caused by clock and digital signals.
33pF	850 MHz/900 MHz band	Filter out low band RF interference
8.2pF	1800/1900/2100/2300/2500/2600MHz band	Filter out middle/high band RF interference.

Stable power supply ensures proper operating of the module. During design, ensure thatthe power supply ripple is less than 300 mV (circuit ESR < 100 mΩ). When the module isworking in maximum load, ensure that the power supply voltage is not lower than 3.4 V.Otherwise, the module may power off or restart. The position of that ESD device can beuse for placing ESD or surge protection device according to the requirements of thewhole machine test. When the module is working in Burst transmit state, the power limit is shown in the following figure.

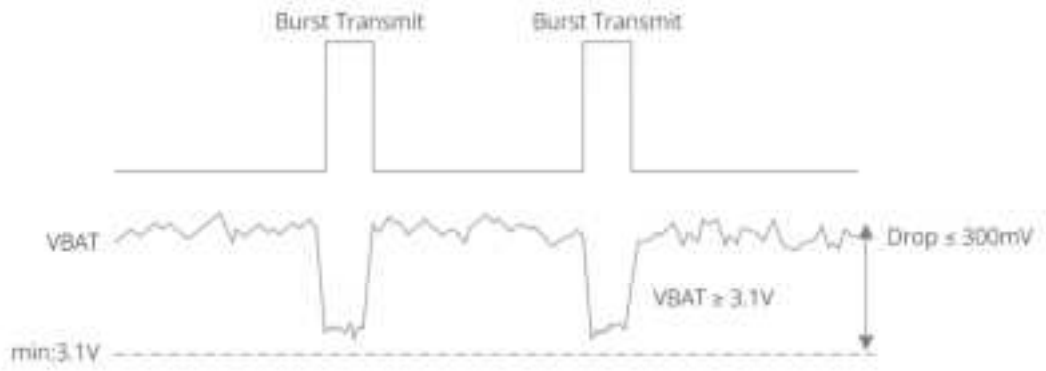


Figure 6. Power Supply Limit

5.1.2 Power Ouput

FG101-NA series module outputs a 1.8 V voltage through the VDD_EXT_1V8 for the

internal digital circuit of module to use. The voltage is the logic level of the module andcan be used to instruct module power-on/off, or used by external low current (< 50 mA)circuits. FG101-NA series module outputs a 2.7V level through the VDD_RF_2V8 for theexternal RF or other circuits to use, with an output current < 50 mA. Leave the signalfloating if not used. The logic level of VDD_EXT_1V8 and VDD_RF_2V8 is defined in the following table.

Table 17. Power Voltage of VDD_EXT_1V8 and VDD_RF_2V8

Parameter	Minimum Value (V)	Typical Value (V)	Maximum Value (V)
VDD_EXT_1V8	1.75	1.8	1.85
VDD_RF_2V8	2.65	2.7	2.85

5.2 Control Interface

The module has three control signals for power on/off and reset of the module. The pins are defined in the following table.

Table 18. Control Signal

Pin Name	I/O	Pin Number	Description
RESET_N	DI	1	In the power-on state, pull down RESET_N for 0.5s to 3s, and then release it. The module is reset. The chip is internally pulled up.
PWRKEY	DI	2	In the power-off state, pull down PWRKEY for 1.6s to 3s, and then release it. The module is started. In the power-on state, pull down the PWRKEY for 3s–7s, and then release it. The module is powered off. The chip is internally pulled up.

PON_1	DI	4	Module on/off signal, pull up to power on. In the power-off state, pull up the PON_1 for more than 1.2s. The module is powered on. There is a 64kΩ pull-down inside the chip and a high level of 1.8V, so external partial voltage needs to be considered.

5.2.1 Power on/off

5.2.1.1 Power-on

FG101-NA has the following power-on methods:

When the module is in power-off mode, pull down the PWRKEY for 1.6s to 3s to power on the module. It is recommended to use OC/OD drive circuit to control PWRKEY pin. The reference circuit is shown in the following figure.

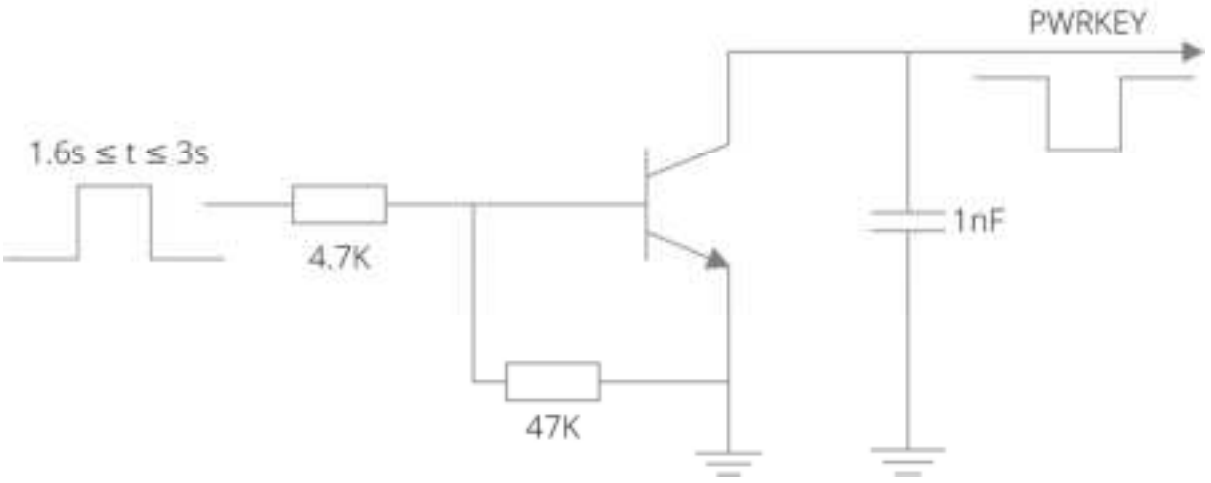


Figure 7. OC Drive Power-on Reference Circuit

- Use a button switch to control PWRKEY to power on/off the module and place a TVS (ESD9X5VL-2/TR is recommended) near the button for ESD protection. The reference circuit is shown in the following figure.

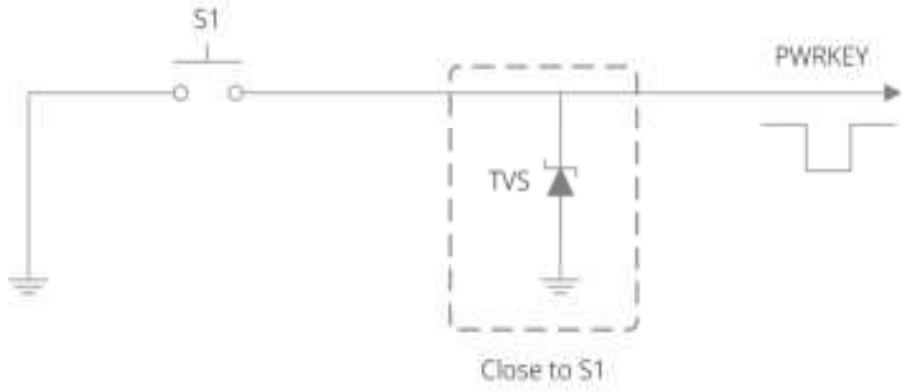


Figure 8. Button Power-on Reference Circuit

- When PWR_ON is normally pulled high, the module will be powered on automatically. The reference circuit is shown in the following figure.

Figure 9. Automatic Power-on Reference Circuit

5.2.1.2 Power-on Sequence

The following figure shows the power-on sequence.

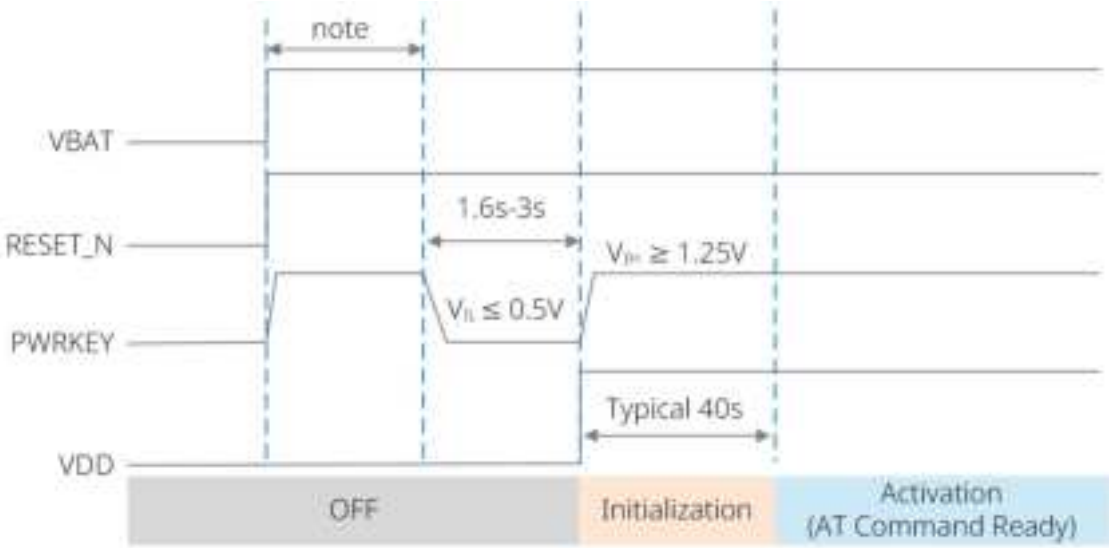


Figure 10. Power-on Sequence (PWRKEY)

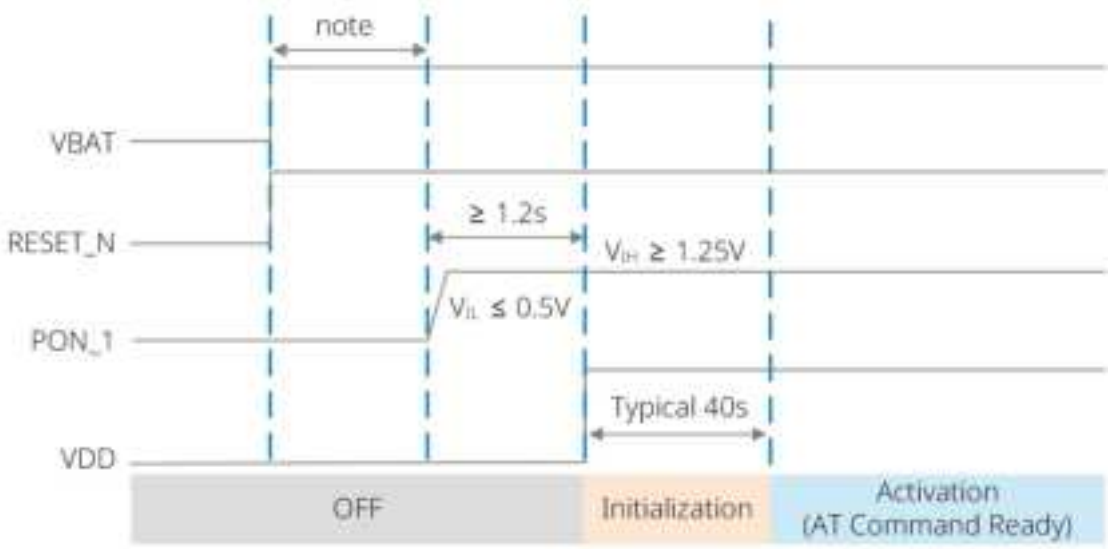


Figure 11. Power-on Sequence (PON_1)

Before pulling down PWRKEY pin, make sure the VBAT voltage is stable. It is recommended to control the interval from power-up by VBAT to PWRKEY pin pull-down no less than 30ms. It takes about 40s to power on the module. Other operations can be performed only after the power-on is completed.

5.2.1.3 Power-off

The module supports the following three power-off modes.

Table 19. Power-off Modes

Power-off Mode	Power-off Method	Applicable Scenario
Low voltage power off	The module will power off when the VBAT voltage is too low or power down occurs	The normal power-off process is not performed
Hardware power off	Pull down PWRKEY for 3s to 7s and then release	Hardware power off normally

AT command power off	AT+CPWROFF	Software power off normally

The power-off sequence is shown in the following figure.

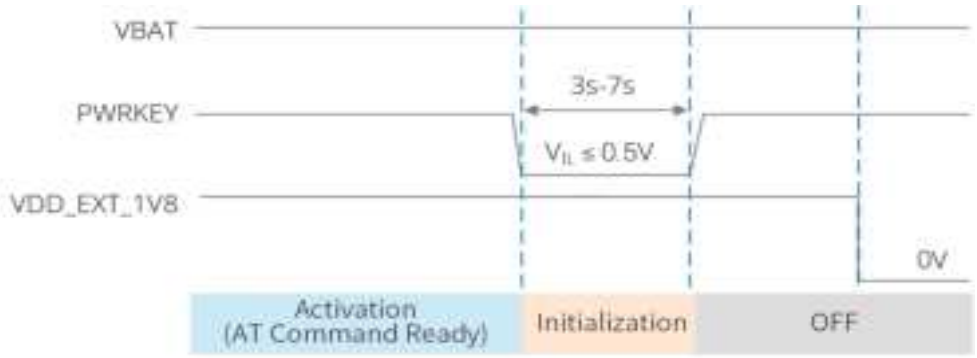


Figure 12. Power-off Sequence

When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal Flash. It is recommended to shut down the module by the PWRKEY pin or AT command before cutting off the power supply.

When using the AT command to power off the module, make sure that the PWRKEY pin is always at the high level after the shutdown command is executed, otherwise the module will automatically power on again.

During the power-off process, it takes about 6 seconds from the release of PWRKEY to the complete power-off of VDD_EXT. Other operations suchas power-on, reset, etc. can be performed only after the power-off is completed.

5.2.2 Reset

FG101-NA series module can be reset by hardware and software.

Table 20. Reset Methods

Reset Method	Action
Hardware reset	Pull down the RESET_N pin for 0.5s to 3s, and then release
Software reset	Send the AT+CFUN=15 command

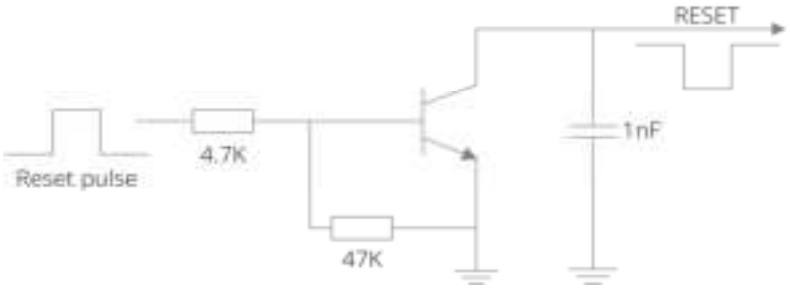


Figure 13. OC Drive Reset Reference Circuit

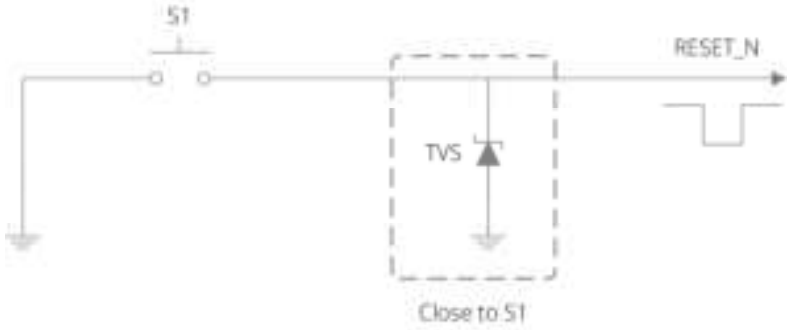


Figure 14. Button Reset Reference Circuit

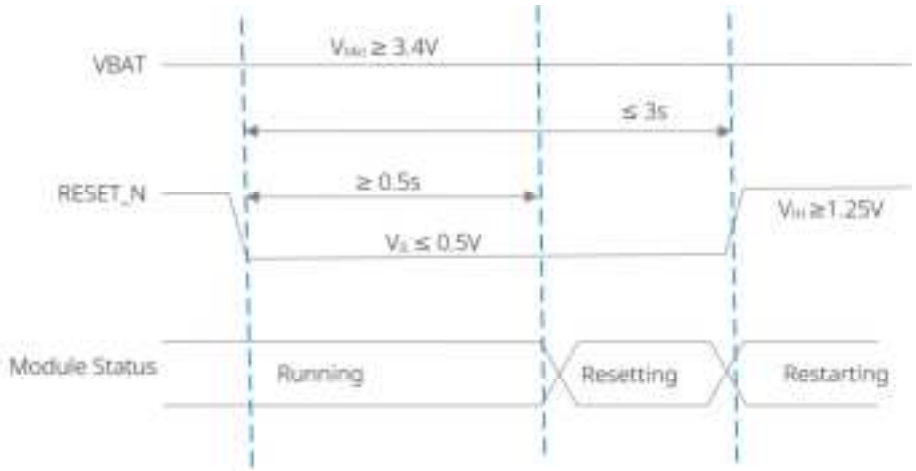


Figure 15. Reset Sequence

It is recommended to wait at least 20 seconds between two reset operations. The RESET pin can be internally pulled up, without external pull-up. Keep the pin floating when it is not used.

5.3 Network Status Indication Interface

FG101-NA series module provides three network status indication interfaces. The default pin 170 is the network status indicator pin. The pin definitions are shown in the following table.

Table 21. Network Status Indication

Pin Name	I/O	Pin Number	Description
NET_MODE	DO	147	Indicator of registered network mode, reserved
NET_STATUS	DO	170	Network connection status indicator (default)
STATUS	DO	171	System operation status indicator, reserved

Network status indication interface drives the network status indicators and is used to describe the network status of the module. The following table describes the working status of the network status indicator.

Table 22. Working Status of the Network Status Indicators

Mode	Level Status of Network Indication Pin	Indicator Status	Description

1	600 ms high/600 ms low	Quick flash 600 ms on/600 ms off	No SIM card SIM PIN Registering with the network (T < 15s) Registration failed
2	75 ms low/3000 ms high	75 ms off/3000 ms on	Standby
3	75 ms high/75 ms low	Speed flash 75 ms on/75 ms off	Data chaining establishment
4	Low	Off	Voice call
5	High	On	Sleep mode

The three status indicators of the module can be designed with reference to the circuit shown in the following figure.

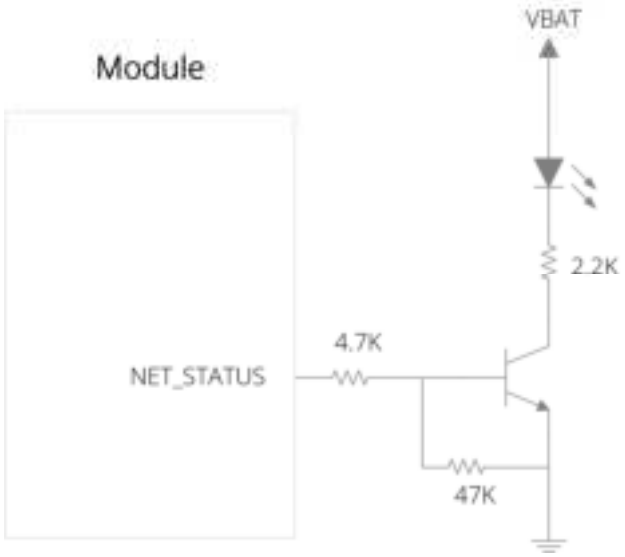


Figure 16. Reference Circuit of Network Status Indicators

5.4 (U)SIM Card Interface

FG101-NA series module has built-in (U)SIM card interface, and supports 1.8 V and 3.0 V

(U)SIM cards.

5.4.1 (U)SIM Pin Definition

(U)SIM pin definition is described in the following table.

Table 23. (U)SIM Pin Definition

Pin Name	I/O	Pin Number	Description
USIM1_DET	DI	25	(U)SIM1 hot plug detection
USIM1_VDD	PO	26	(U)SIM1 power supply
USIM1_DATA	DIO	29	(U)SIM1 data signal
USIM1_CLK	DO	27	(U)SIM1 clock signal
USIM1_RST	DO	28	(U)SIM1 reset signal
USIM2_VDD	PO	74	(U)SIM2 power supply
USIM2_DATA	DIO	77	(U)SIM2 data signal
USIM2_DET	DI	78	(U)SIM2 hot plug detection
USIM2_RST	DO	79	(U)SIM2 reset signal
USIM2_CLK	DO	80	(U)SIM2 clock signal

5.4.2 (U)SIM Interface Circuit

(U)SIM Card Slot with Card Detection Signal.

(U)SIM card slot should be selected for (U)SIM design. It is recommended to use (U)SIM card slot with hot plug detection function.

The following figure shows the reference design circuit. When (U)SIM card is inserted, USIM_DET pin is at high level, when (U)SIM card is removed, USIM_DET pin is at

low level.

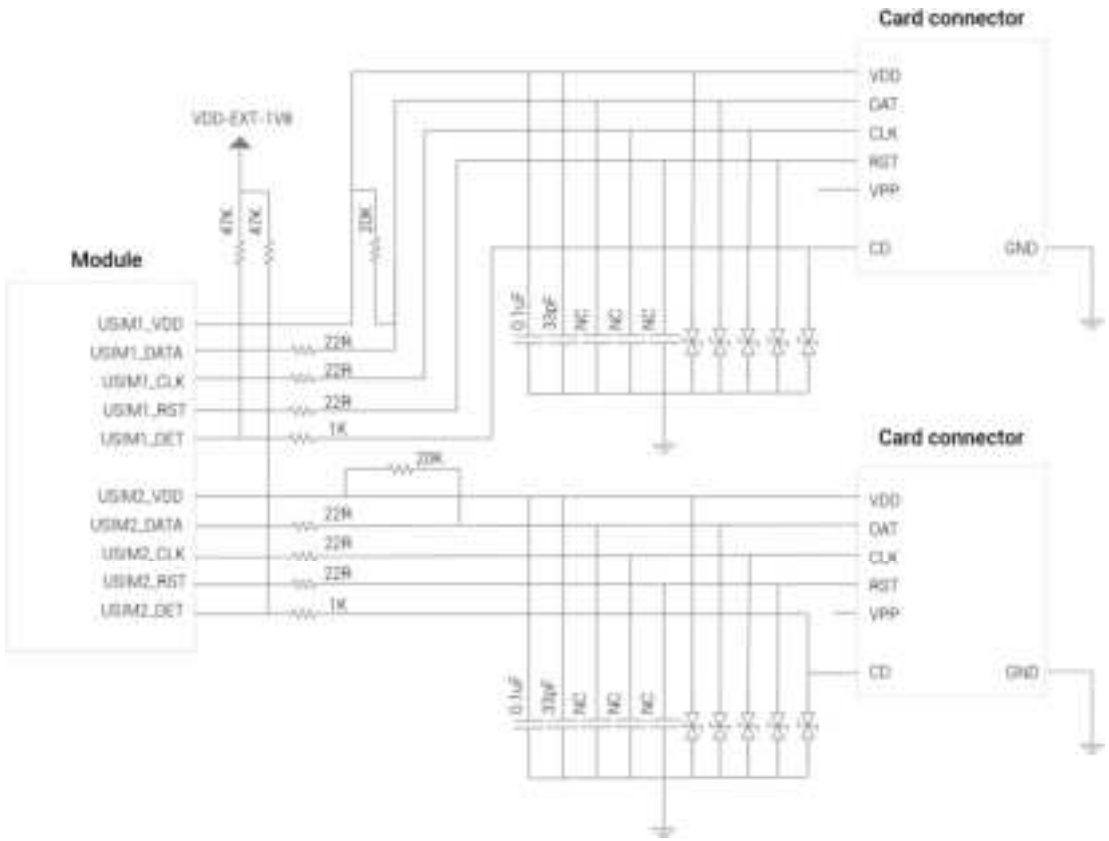


Figure 17. (U)SIM Card Slot with Card Detection Signal

5.4.3 (U)SIM Card Hot Plug

The FG101-NA series module supports the (U)SIM card hot plug function. The module detects the status of the USIM1_DET/USIM2_DET pin to determine whether a (U)SIM card is inserted or removed.

USIM1_DET/USIM2_DET is active high by default (if the card is at high level, the card is inserted; otherwise, the card is removed). The hot plug detection can be enabled/disabled by the AT command as follows.

Table 24. (U)SIM Card Hot Plug Function Configuration

AT Command	Function	Remark

AT+MSMPD=1	(U)SIM card hot plug detection is enabled	Default setting
AT+MSMPD=0	(U)SIM card hot plug detection is disabled	Effective after restart

5.4.4 (U)SIM Design Requirements

(U)SIM circuit design must meet EMC standards and ESD requirements, and at the sametime, EMS capability must be improved to ensure that the (U)SIM can work stably. Thefollowing points need to be strictly observed in the design:

- (U)SIM card slot should be located as close to the module as possible, and kept away from the RF antenna, DCDC power, clock signal lines and other strong interference sources.
- (U)SIM card slot is covered by metal shield shell to improve EMS.
- The routing length from the module to the (U)SIM card slot shall not exceed 100 mm. Longer cable will reduce signal quality.
- The USIM_CLK and USIM_DATA signal lines are grounded and isolated to avoid mutual interference. If conditions do not permit, at least the (U)SIM signal must be grounded as a set.
- The filter capacitor and ESD device of the (U)SIM card signal line are placed close to the (U)SIM card slot.
- The total capacitance of the equivalent capacitance and the parallel filter capacitance of the ESD device is less than 27pF.
- USIM_DATA requires a pull-up resistor of 20KΩ to USIM_VDD.
- Refer to the specification for PCB packaging design of (U)SIM card slot. The PCB surface layer under the 6 clips should be keepout to avoid short circuit caused by the clips scraping the green oil.

5.5 USB Interface

FG101-NA module supports USB 3.0 (5 Gb/s) ultra-high-speed data transmission, and is also compatible with USB high-speed (480 Mb/s) for download, debugging, data transmission and other functions. Only USB 2.0 interface can be used for download and debug, so the USB 2.0 interface signal must be led out.

USB pin definition is shown in the following table.

Table 25. USB Pin Definition

Pin Name	I/O	Pin Number	Description
USB_VBUS	PI	32	USB insertion detection signal
USB_DM	AIO	33	USB 2.0 differential data signal (–)
USB_DP	AIO	34	USB 2.0 differential data signal (+)
USB_ID*	DI	36	USB ID detection pin, reserved
USB_SS_TX_M	AO	37	USB 3.0 differential transmitting signal (–)
USB_SS_TX_P	AO	38	USB 3.0 differential transmitting signal (+)
USB_SS_RX_P	AI	40	USB 3.0 differential receiving signal (+)
USB_SS_RX_M	AI	41	USB 3.0 differential receiving signal (–)
USB_BOOT	DI	140	Force USB download control signal; pull this pin up to VDD_EXT_1V8, and then power on, and the module enters the download mode
OTG_PWR_EN	DO	143	OTG mode external power enable control, reserved

5.5.1 USB Interface Circuit

The USB interface reference circuit is shown in the following figure.

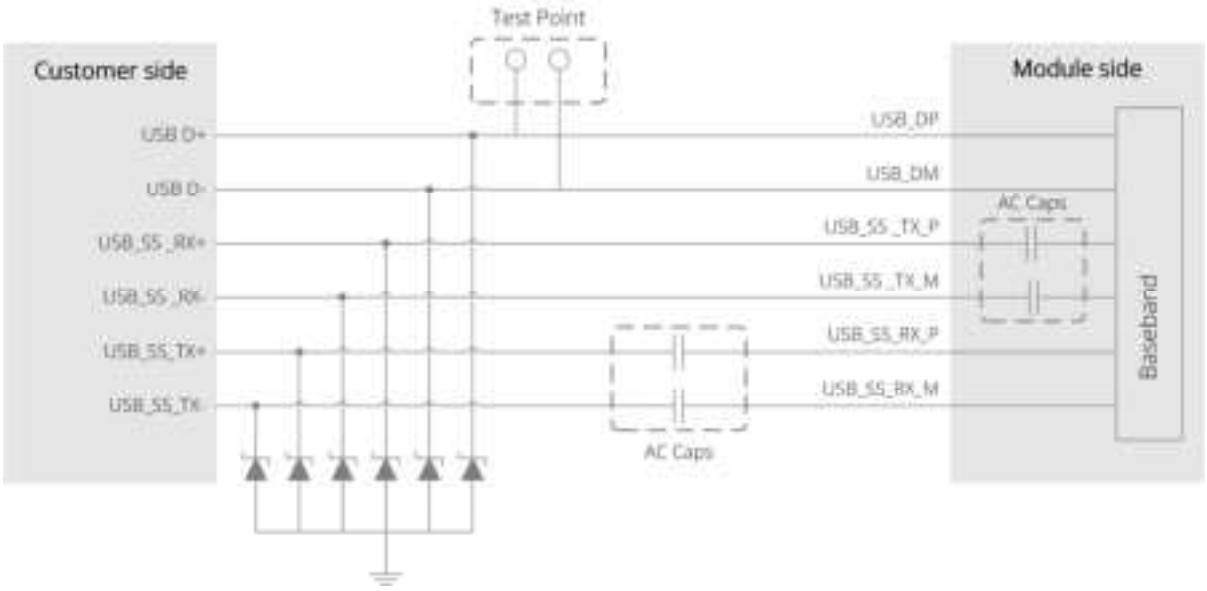


Figure 18. Reference Design of USB Interface Circuit

5.5.2 USB Routing Rules

5.5.2.1 USB 2.0 Routing Rules

Since the module supports USB 2.0 High-Speed, TVS tube equivalent capacitance on theUSB_D+/D– differential signal line must be less than 1 pF, and a 0.5 pF TVS is recommended.

USB_D– and USB_D+ are high speed differential signal lines with the maximum transmission rate of 480 Mbit/s. The following rules must be strictly followed in PCB layout:

- USB_D– and USB_D+ signal lines should have the differential impedance of 90Ω±10Ω.
- USB_D– and USB_D+ signal line difference must be less than 2mm in length and parallel, avoiding the right-angle routing.
- USB_D– and USB_D+ signal lines should be routed on the layer that is closest to the ground layer, and protected with GND all around.

5.5.2.2 USB 3.0 Routing Rules

USB_SS_RX_P/USB_SS_RX_M and USB_SS_TX_P/USB_SS_TX_M are two sets of differentialsignals, with differential impedance controlled at 90Ω±7Ω; the trace length differencewithin the differential pair is controlled to ≤ 0.15 mm, and the trace length difference between the differential sets is controlled to ≤ 10 mm. TVS tube equivalent capacitance on the differential signal line must be less than 0.5 pF.

Minimize passages during high-speed cabling to ensure continuous impedance.

USB 3.0 signals are super speed differential signal lines with the maximum theoreticaltransfer rate of 5Gbps. The following rules shall be followed carefully in PCB layout:

- USB_SS_TX_P/USB_SS_TX_M and USB_SS_RX_P/ USB_SS_RX_M are two pairs of differential signal lines, and their differential impedance should be controlled as 90Ω±7Ω.
- Traces in the differential pair must be parallel with equal length, and the length difference should be controlled less than 0.15 mm, avoiding right-angle traces.
- Traces between differential pairs must be parallel with equal length, and the length difference should be controlled less than 10 mm, avoiding right-angle traces.
- The two pairs differential signal lines should be routed on the layer that is closest to the ground layer, and protected with GND all around.

5.6 UART Interface and Application

FG101-NA series module supports 3-channel UART interface, with the maximum baudrate of 921600 bps and the default baud rate of 115200 bps. The following table describes pins of UART interface.

Table 26. UART Pin Definition

Pin Name	I/O	Pin Number	Description

UART1_RTS*	DO	56	Send data request, reserved
UART1_CTS*	DI	57	Clear to send, reserved
UART1_RXD*	DI	58	Module receiving data, reserved
UART1_DCD*	DO	59	Module output carrier detection, reserved
UART1_TXD*	DO	60	Module transmitting data, reserved
UART1_RI	DO	61	Module output ring indicator, which is host wakeup control signal
UART1_DTR*	DI	62	Ready, sleep mode control, reserved
DBG_RXD	DI	136	Debug UART receiving signal
DBG_TXD	DO	137	Debug UART transmitting signal
UART2_TXD*	DO	163	UART2 transmitting data signal, reserved
UART2_RTS*	DO	164	UART2 request to send data signal, reserved
UART2_RXD*	DI	165	UART2 receiving data signal, reserved
UART2_CTS*	DI	166	UART2 clear to send data signal, reserved

Pins marked with * are reserved functions or under development.

The UART interface level of FG101-NA series module is 1.8 V, if the customer hostsystem level is 3.3 V or other, a level conversion circuit needs to be added to the UARTsignal, and the UART level conversion reference circuit is shown in the following figure.

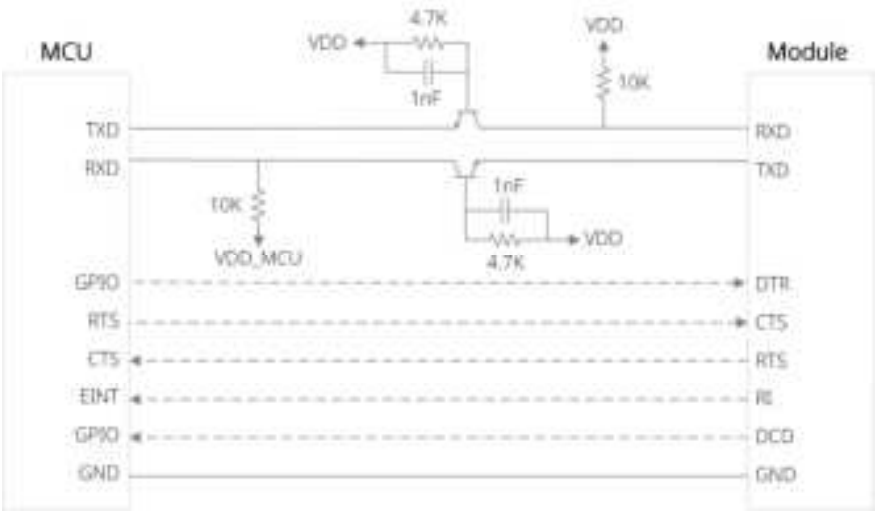


Figure 19. UART Level Conversion Reference Circuit

- Transistor level conversion circuits cannot be used for applications whose baud rate exceeds 460kbps.
- Pay attention to the definition and connection direction of input and output for each signal to avoid reverse connection of input and output.
- The VDD_EXT_1V8 voltage domain is used for VDDs on one side of all serial modules.

5.7 ADC Interface

FG101-NA series module supports two-channel ADC interface with minimum accuracy of ± 10mV. Run the AT+MMAD command to read the voltage value of ADC interface. The voltage range of ADC interface is 0V to 1.8V.

Table 27. ADC Pin Definition

Pin Name	I/O	Pin Number	Description
ADC0	AI	173	ADC interface 0
ADC1	AI	175	ADC interface 1

It is recommended to ground ADC signal lines to improve ADC voltage measurement accuracy.

5.8 I²C Interface

FG101-NA series module supports 1-way I²C interface, and the standard I²Cspecification, version 3.0 is applied.

The I²C signal module is internally pull-up and does not need an external pull-up resistor.

Table 28. I2C Pin Definition

Pin Name	Pin Number	Type	Description
I2C_SDA	42	OD	I2C data signal
I2C_SCL	43	OD	I2C clock signal

5.9 PCM Digital Audio Interface

The FG101-NA series module provides a digital audio interface for communication with external codec and other digital audio devices.

5.9.1 PCM Interface Definition

PCM interface signals include transmission clock PCM_CLK, frame synchronization signalPCM_SYNC, and input and output PCM_IN/PCM_OUT.

Table 29. PCM Pin Definition

Pin Name	I/O	Pin Number	Description
PCM_SYNC	IO	65	PCM sync signal
PCM_IN	DI	66	PCM input signal

PCM_CLK	IO	67	PCM clock signal
PCM_OUT	DO	68	PCM output signal

Default transmission clock frequency is 2.048 MHz, sampling rate is 8 KHz, and resolution is 16 bit.

5.9.2 PCM Application Circuit

The application reference circuit of the external codec chip of the PCM interface is shown in the following figure.

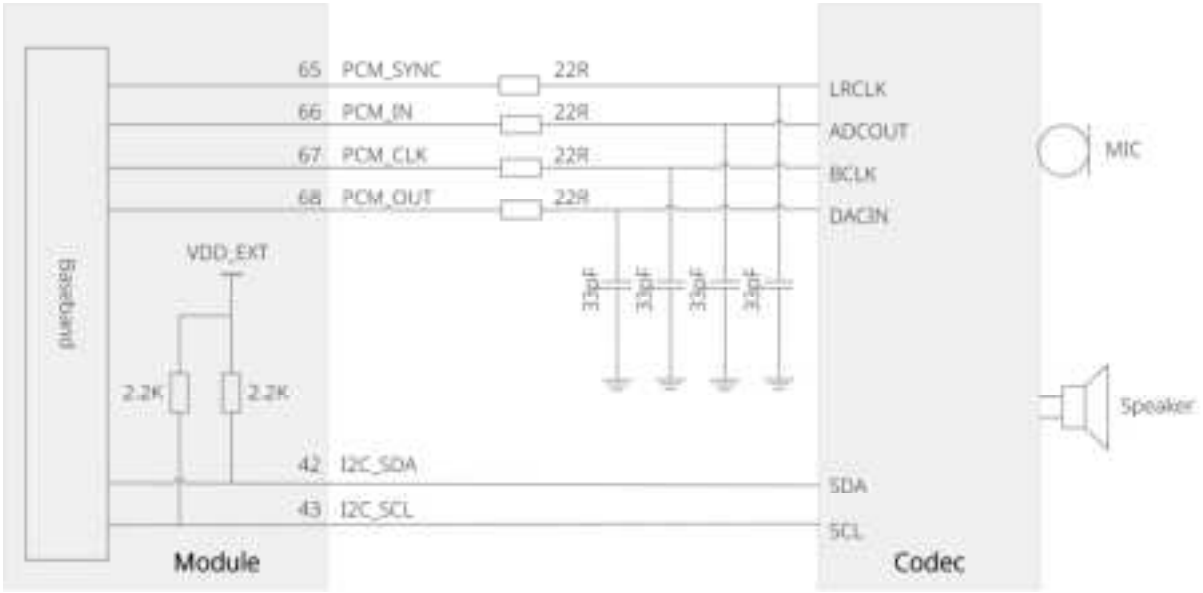


Figure 20. Reference Circuit of the PCM Interface External codec Chip

5.10 SDIO Interface

FG101-NA series module supports one SDIO interface. The standard is as follows: *Physical Layer Specification* version 3.0 and *SDIO Card Specification* version 3.0.

5.10.1 SDIO Pin Definition

SDIO pin definition is described in the following table.

Table 30. SDIO Pin Definition

Pin Name	I/O	Pin Number	Description
SD_RESET_N	DO	12	Reset output signal; connected to eMMC chip; keep floating when SD card function is used; reserved
SD_PWR_EN	DO	15	SD card external power switch control signal
SD_VIO	PO	46	SD card power supply, 3.0V or 1.8V adaptive, reserved for SDIO pull-up use, external power supply is required for SD card power supply.
SD_DATA0	DIO	49	SDIO data signal bit0
SD_DATA1	DIO	50	SDIO data signal bit1
SD_DATA2	DIO	47	SDIO data signal bit2
SD_DATA3	DIO	48	SDIO data signal bit3
SD_CMD	DIO	51	SDIO command signal
SD_CLK	DO	53	SDIO clock signal
SD_ DET	DI	52	SDIO hot plug detection signal

5.10.2 SDIO Interface Routing Rules

SD card circuit design must meet EMC standards and ESD requirements, and at the sametime, EMS capability must be improved to ensure that the SD card can work stably. The following principles must be strictly followed in the design:

- If the routing length of signal lines is equal to or less than 50 mm, it is recommended to place the SD card connector as close to the SD signal pin of the module as possible because the internal cabling length of the module is 20 mm. If the routing length is

equal to or less than 30 mm, the routing length difference of the clock signal line and data signal line should be controlled equal to or less than 1 mm.

- The SD signal line must be grounded all around and kept away from RF antenna, DCDC power supply, clock signal line and other strong interference sources.
- Reference ground must be installed for the SD signal line, and data line impedance must be controlled with 50 Ω (±10%).
- The total load capacitance on the SD signal lime must be smaller than 1 pF.

5.10.3 SDIO Interface Application Circuit

For SDIO application circuit, please refer to the following figure. SD card connector detectpin is floating when no card is inserted, and is short to ground when a card is inserted.The detect pin is at low level when the SD card is inserted. The SD card needs to bepowered by an external power supply. The voltage ranges from 2.7V to 3.6V, and the typical value is 2.95V. The output current must be greater than 800mA.

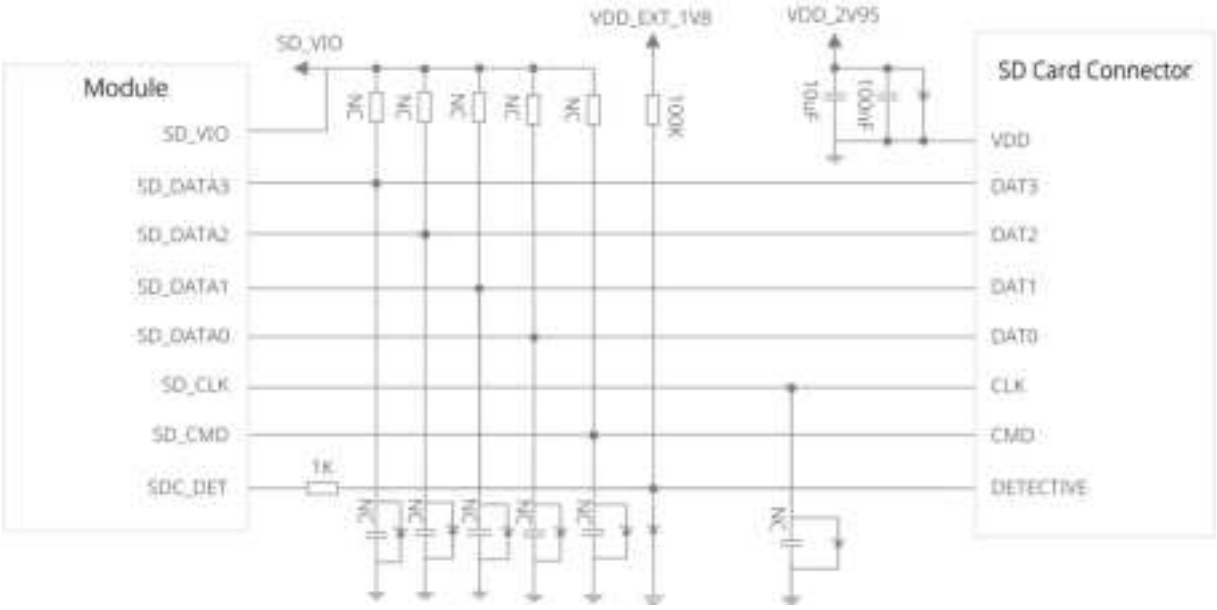


Figure 21. SD Card Reference Circuit

5.11 SPI Interface

The FG101-NA module supports one set SPI interface, and it works in Master mode by

default, and the clock supports 50 MHz at most.

Table 31. SPI Pin Definition

Pin Name	I/O	Pin Number	Description
SPI_MOSI	DO	6	SPI interface output signal
SPI_MISO	DI	7	SPI interface input signal
SPI_CS	DO	8	SPI interface chip selection signal
SPI_CLK	DO	9	SPI interface clock signal

5.12 PCIe Interface

FG101-NA module supports a set of PCIe GEN 2.0 × 1 lane.

Table 32. PCIe Pin Definition

Pin Name	I/O	Pin Number	Description
PCIE_CLK_P	AO	179	PCIe reference clock signal positive
PCIE_CLK_M	AO	180	PCIe reference clock signal negative
PCIE_TX_M	AO	182	PCIe data transmitting signal negative
PCIE_TX_P	AO	183	PCIe data transmitting signal positive
PCIE_RX_M	AI	185	PCIe Data receiving signal negative
PCIE_RX_P	AI	186	PCIe Data receiving signal positive
PCIE_CLKREQ	DIO	188	PCIe clock request signal
PCIE_HOST_RST_N	DO	189	PCIe reset signal

PCIE_WAKE	DI	190	PCIe wake-up signal
PCIE_RESET_N	DI	192	PCIe EP mode reset signal, reserved

5.12.1 PCIe Routing Rules

FG101-NA module supports PCIe 2.0 × 1, including three differential pairs: transmitting pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.

PCIe can achieve the maximum transmission rate of 5GT/s. The following rules must bestrictly followed in PCB layout:

- The differential signal pairs are required to be parallel wires with equal length, and the difference in length is less than 0.15 mm.
- The differential signal pair traces shall be as short as possible and be controlled within 15 inch (380 mm) for AP end.
- The impedance of differential signal pair traces is controlled to be 100Ω±10%.
- Avoid discontinuous reference ground, such as segment and space.
- When the differential signal traces go through different layers, the via hole of ground signal should be close to that of signal, and generally, each pair of signals require 1-3 ground signal via holes and the traces shall never cross the segment of plane.
- Try to avoid bended traces and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of differential pairs. As shown in the following Figure, the bending angle of all traces should be equal to or greater than 135°, the spacing between differential pair traces should be larger than 20mil, and the traces caused by bending should be greater than 1.5 times trace width at least. When a serpentine route is used for length match with another route, the bended length of each segment shall be at least 3 times the route width (≥ 3W). The largest spacing between the bended part of the serpentine trace and another one of the differential traces must be less than 2 times the spacing of normal differential traces (S1 < 2S).

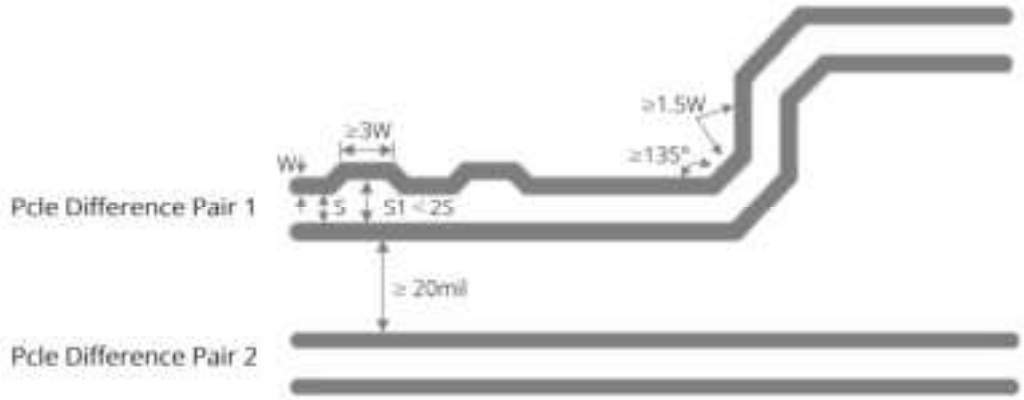


Figure 22. PCIe Routing Requirements

- The difference in length of two data lines in differential pair should be within 0.15 mm, and the length match must be met for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in the following figure. However, there is no specific requirements for the length match of transmitting pair and receiving pair, that is, the length match is only required in the internal differential lines rather than between different differential pairs. The length match should be close to the signal pin and pass the small-angle bending routing design.

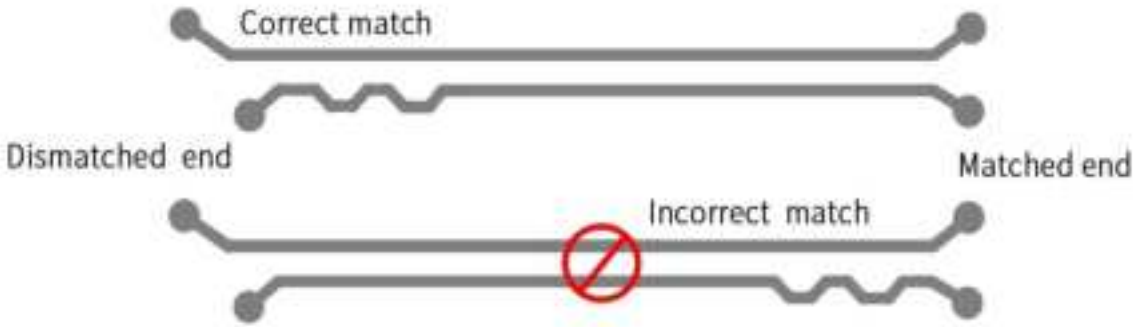


Figure 23. Length Match Design of PCIe Difference Pair

5.12.2 PCIe Application Circuit

Please refer to the following figure for PCIe application circuit, and *FIBOCOM FG101-NA Reference Design* for details.

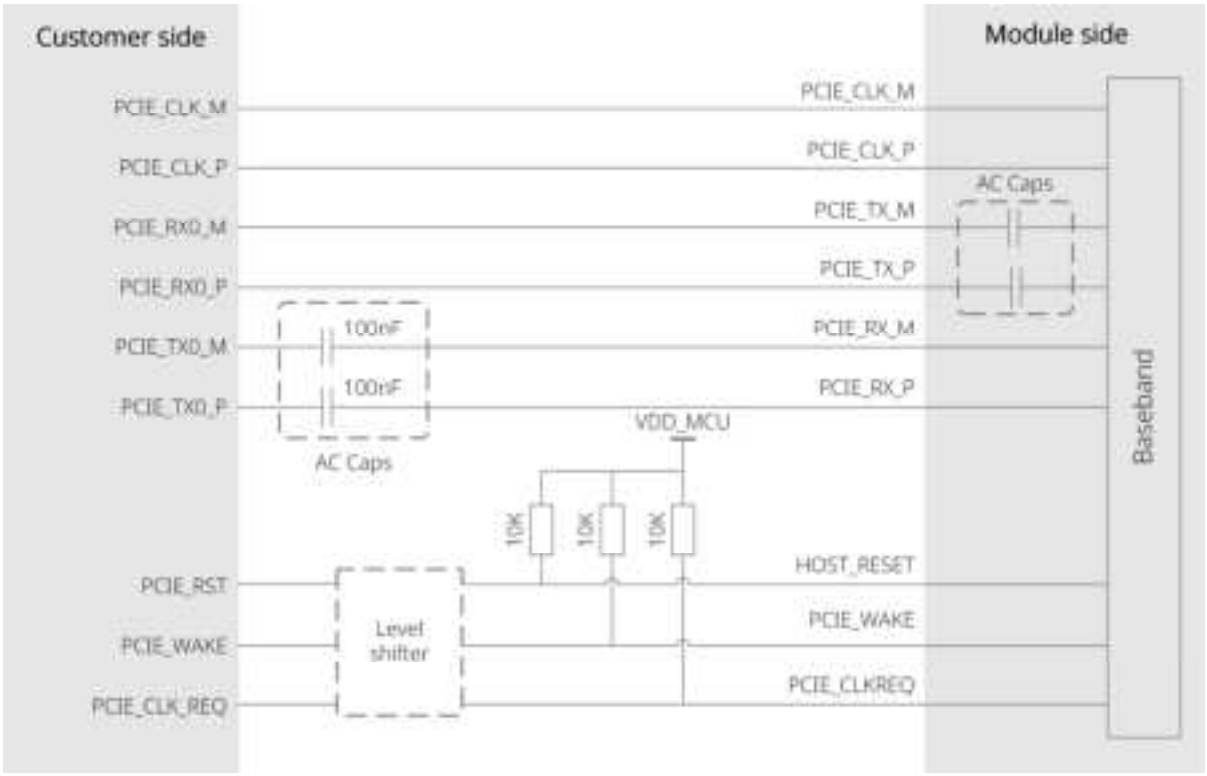


Figure 24. PCIe Application Circuit

5.13 GPIO Interface

FG101-NA module reserves five GPIO interfaces for clients, with a voltage domain of 1.8V. Clients can use the interfaces as required and simply leave them floating when not in use.

GPIO pin definition is described in the following table.

Table 33. GPIO Pin Definition

Pin Name	I/O	Pin Number	Description	Usage
GPIO_1	IO	138	General input/output interface 1	Pull down inside the chip by default.
GPIO_2	IO	139	General input/output	Pull down inside the chip by default.

			interface 2	
GPIO_3	IO	159	General input/output interface 3	Pull down inside the chip by default. Interrupt wake-up is supported.
GPIO_4	IO	161	General input/output interface 4	Pull down inside the chip by default. Interrupt wake-up is supported.
GPIO_5	IO	172	General input/output interface 5	Pull down inside the chip by default.

5.14 Flight Mode Control Interface

W_DISABLE_N pin is described in the following table.

Table 34. W_DISABLE_N pin Description

Pin Name	I/O	Pin Number	Description
W_DISABLE_N	DI	151	Module flight mode control (internal pulled up by default)

FG101-NA series module supports two ways as described in the following table to enter flight mode:

Table 35. Ways for Module to Enter Flight Mode

1	Hardware GPIO interface control	Send AT+GTFMODE=1 to turn on the hardware control flight mode function; pulled up or float the pin The module is in normal mode when W_DISABLE# pin is pulled up by default. When this pin is pulled down, the module enters flight mode.

2	AT command control	The module uses software to control the flight mode by default. When AT+GTFMODE=0: run the AT+CFUN=0 command to enter flight mode. run the AT+CFUN=1 command to enter normal mode.

5.15 Sleep/Wakeup Interface

When the module is in sleep mode, the module can be awakened by pulling down WAKEUP_IN pin.

When the module is in sleep mode and there is an incoming call or short message, thesignal output by the UART1_RI pin wakes up the host.

Table 36. Sleep/Wakeup Interface

Pin Name	I/O	Pin Number	Description
WAKEUP_IN	DI	150	External device wake-up module, active low by default.
UART1_RI	DO	61	Wake-up host control signal, which is pulled high by default, and pulled low to wake up module.

The module supports setting wake-up mode and waking up active level through AT commands. For details of configuration method, see *Fibocom_FG101_AT Commands User Manual*.

6 RF Interface

The FG101 series module has five antenna interfaces, and the pin definitions are described in the following table.

Table 37. Antenna Interface

Pin Name	I/O	Pin Number	Description
ANT_MIMO1	AI	101	MIMO1 antenna
ANT_DIV	AI	107	Diversity antenna
ANT_MIMO2	AI	113	MIMO2 antenna
ANT_GNSS	AI	119	GNSS antenna
ANT_MAIN	AIO	127	Main antenna

6.1 Operating Bands

Table 38. Operating Band

Band	Mode	Transmit (MHz)	Receive (MHz)
Band 2	LTE FDD/WCDMA	1850~1910	1930~1990
Band 4	LTE FDD/WCDMA	1710~1755	2110~2155
Band 5	LTE FDD/WCDMA	824~849	869~894
Band 7	LTE FDD	2500~2570	2620~2690
Band12	LTE FDD	699~716	729~746
Band 13	LTE FDD	777~787	746~756
Band 14	LTE FDD	788~798	758~768
Band 17	LTE FDD	704~716	734~746
Band 25	LTE FDD	1850~1915	1930~1995

Band 26	LTE FDD	814~849	859~894
Band 29	LTE FDD	- -	717~728
Band 30	LTE FDD	2305~2315	2350~2360
Band 41	LTE TDD	2496~2690	2496~2690
Band 46	LTE TDD	5150~5925	5150~5925
Band 48	LTE TDD	3550~3700	3550~3700
Band 66	LTE FDD	1710~1780	2110~2180
Band 71	LTE FDD	663~698	617~652
GPS L1	- -	- -	1575.42 ± 1.023
GLONASS L1	- -	- -	1602.5625 ± 4
BDS	- -	- -	1561.098 ± 2.046
Galileo	- -	- -	1559–1592

6.2 Transmitting Power

The following table describes the RF output power of FG101-NA series module.

Table 39. Output Power

Band	Minimum Value	Maximum Value
WCDMA	< -50dBm	23.5dBm ± 2dB
LTE FDD	< -40dBm	23dBm ± 2dB
LTE TDD	< -40dBm	23dBm ± 2dB

6.3 Receiving Sensitivity

Table 40. FG101-NA Dual Antenna Receiving Sensitivity

Mode	Band	3GPP Requirement	Rx Sensitivity Typ	Note

		(dBm)	(dBm)	
WCDMA	Band 2	-104.7	-113	- -
	Band 4	-106.7	-112.5	- -
	Band 5	-104.7	-113	- -
LTE FDD	Band 2	-94.3	-100	10MHz BW
	Band 4	-96.3	-100	10MHz BW
	Band 5	-94.3	-101	10MHz BW
	Band 7	-94.3	-100	10MHz BW
	Band 12	-93.3	-101	10MHz BW
	Band 13	-93.3	-101	10MHz BW
	Band 14	-93.3	-101	10MHz BW
	Band 17	-93.3	-101	10MHz BW
	Band 25	-92.8	-101	10MHz BW
	Band 26	-93.8	-101	10MHz BW
	Band 30	-95.3	-100	10MHz BW
	Band 66	-95.8	-100	10MHz BW
	Band 71	-93.5	-101	10MHz BW
LTE TDD	Band 41	-94.3	-98.5	10MHz BW
	Band 48	-95	-98.5	10MHz BW

Table 41. FG101-NA Four Antenna Receiving Sensitivity

Mode	Band	3GPP Requirement (dBm)	Rx Sensitivity Typ (dBm)	Note
LTE FDD	Band 2	-97	-103	10MHz BW

	Band 4	-97	-102	10MHz BW
	Band7	-97	-102	10MHz BW
	Band 25	-97	-103	10MHz BW
	Band 30	-97	-102	10MHz BW
	Band66	-97	-102	10MHz BW
LTE TDD	Band 41	-97	-100	10MHz BW
	Band 48	-97	-100	10MHz BW

6.4 GNSS Receiving Performance

The GNSS of FG101-NA module supports GPS/GLONASS/BDS/GALILEO, and the performance parameters of GNSS are shown in the following table.

Table 42. GNSS Performance Parameters

Indicator Performance	Description	Result	Unit
Current	Fixing,-130dBm/-122dBm	85	mA
	Tracking,-144dBm	80	mA
Sensitivity	Cold start	39	dB-Hz
	Acquisition	-145	dBm
	Tracking	-156	dBm
TTFF	Cold Start	40	s
	Warm Start	35	s
	Hot Start	3	s

Static Accuracy	Nominal accuracy	3	m

The above data is an average value obtained by testing some samples at 25°C.

6.5 Antenna indicators

The antenna requirements for FG101-NA module are described in the following table.

Table 43. Module Antenna Requirements

FG101-NA series module main antenna requirements	
WCDMA/LTE	VSWR: ≤ 2 Input power: > 28 dBm Input impedance: 50Ω Antenna gain: < 3.6dBi Antenna isolation: > 25dB Antenna correlation coefficient: < 0.5
GNSS	Frequency range: 1559 MHz–1609 MHz Polarization direction: right-circular or linear polarization VSWR: < 2:1 Passive antenna gain: > 0dBi

6.6 PCB Routing Design

6.6.1 Routing Rules

For modules that don't have a RF connector, customers need to route a RF trace to

connect to the antenna feeding point or connector. It is recommended to use a microstrip line. The shorter the better. The insertion loss should be controlled less than 0.2dB; and impedance should be controlled within 50Ω.

Add a π-type circuit (two parallel-component- grounded pins are connected directly tothe main GND) between the module and antenna connector (or feeding point) for antenna debugging.

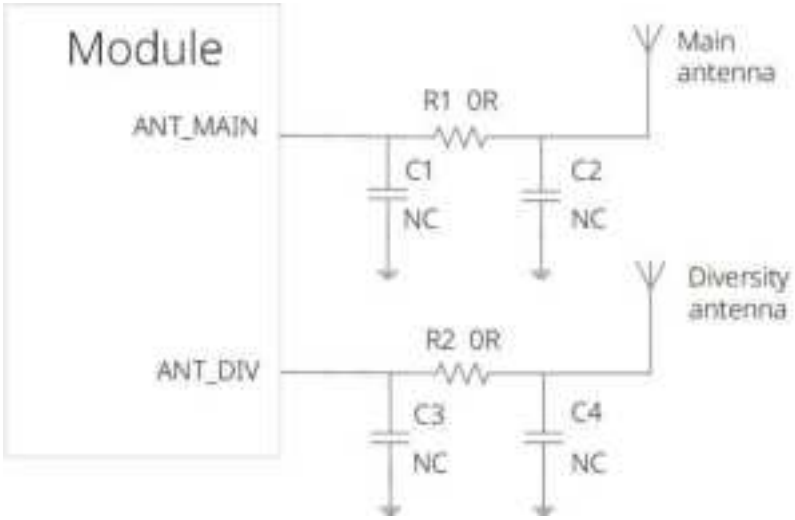


Figure 25.π Type Circuit

This signal line impedance is controlled within 50Ω during PCB cabling, and the RF performance is closely related to this cabling. PCB parameters that will affect the cabling impedance include:

- Trace width and thickness
- Dielectric constant and thickness of material
- Thickness of pad
- Distance from ground line
- Nearby traces

6.6.2 Impedance Design

The RF impedance of the two antennas' interface should to be controlled at 50Ω.

In practical application, RF routing mode is designed according to other parameters ofPCB, such as reference layer thickness, number of layers and stacking. Different reference GND layer will lead to different routing design.

6.6.3 3W Principle

During antenna RF signal cabling design on PCB, the first thing you need to consider is to follow "3W principle".

In order to reduce crosstalk between the lines, please ensure that line spacing is largeenough. If the line spacing is at least 3 times of the line width, 70% of the electric fieldbetween the lines will not interfere with each other, and this is called "3W principle".

Figure 26. 3W Principle

6.6.4 Impedance Design for Four-layer Board

The thickness of four-layer board is 1.0 mm. RF line is routed on Lay 1, and reference layer is on Lay 2 (GND layer).

The stacking varies with PCB vendor; the following figure is taken as an example.

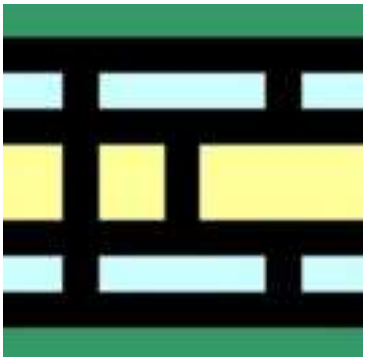


Figure 27. Four Layers (1+2+1) Thickness

Table 44. Four-layer Board Stacking Thickness

Layer	Material	Thickness (um)
- -	Solder Mask	- -
Lay1	0.33OZ + Plating	25
- -	PP 1080	65
Lay2	0.5OZ + Plating	25
- -	0.510mm(H/H OZ)	508
Lay3	0.510mm + Plating	25
- -	PP 1080	65
Lay4	0.33OZ + Plating	25
- -	Solder Mask	- -

The thickness from Lay 1 to Lay 2 is 65 ums, RF trace is 4 mils, and the distance from RF to GND is greater than 3 times of RF line width.

The blue area is Lay 1 and the red area is Lay 2, the highlighted part is RF line.

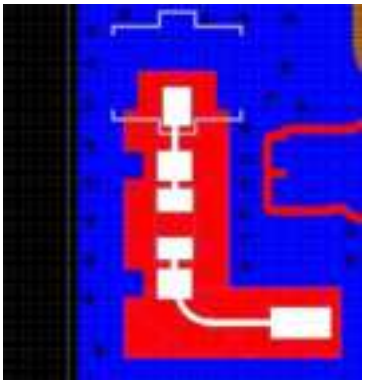


Figure 28. RF Traces

50Ω impedance calculation:

If the value of D1 exceeds 3 times of W1, it has weak effect on impedance.

Figure 29. Impedance Calculation for Four-layer Board Top Layer Trace

6.7 Main Antenna Design

6.7.1 External Antenna

The external antenna has good performance. The antenna is placed outside the completemachine, the antenna space is large, and the antenna performance is not easy to beaffected by the internal environment of the complete machine, so that the antenna doesnot need to be independently designed for each project. The compatibility is good. Most of the interfaces of such antennas are SMA interfaces.

Figure 30. External Antenna

6.7.2 Internal Antenna

6.7.2.1 Design Principle of Internal Antenna

Placement

- The antenna shall be arranged in the corners of the module.
- Avoid placing metal elements near the antenna.
- The shielding parts shall be as neat as possible. Do not use long strip shaped hole slots.
- Components with metal structure, such as horn, vibrator, and camera base plate shall be grounded.
- Avoid using long FPC. If a long FPC is required, add grounding shields on both sides.

Routing

- When connecting RF routing, apply circular arc treatment at the turning, take grounding and pay attention to characteristic impedance.
- RF ground shall be designed properly, PCB board and edge of ground shall be provided with "ground wall", and antenna led from RF module shall be made into microstrip line.
- The antenna RF feeding point pad is a round rectangular pad with the size of 2 mm × 3

mm. All layers of PCB that include the pad and surrounding and that are equal to and greater than 0.8 mm are not covered with copper.

- The center distance between RF and ground pad shall be between 4 mm and 5 mm.

6.7.2.2 Internal Antenna Classification

Internal Antenna Types There are three kinds of internal antennas: PIFA, IFA and monopole. Internal antennas may form interference and other potential problems in the product, so there are more requirements in the design.

The following table describes the differences of these three types of antennas.

Table 45. Antenna Differences

Antenna Type	Below Antenna Projection	Antenna Feed	Antenna Volume	Electrical Property	SAR
PIFA	Ground	2	Large	Very good	Low
MONOPOLE	No ground	1	Small	Good	Slightly high
IFA	Ground	2	Medium	About good	Medium

PIFA antenna

- Antenna structure

  There are two feeding points between the antenna and main board, one is module output, and the other is RF ground. It is recommended to design the antenna on the top of the device. The distance between the signal point and GND point should be at least 4 mm to 5 mm. The signal point and GND point can be put in different places, and more GND points mean more choices during antenna design.

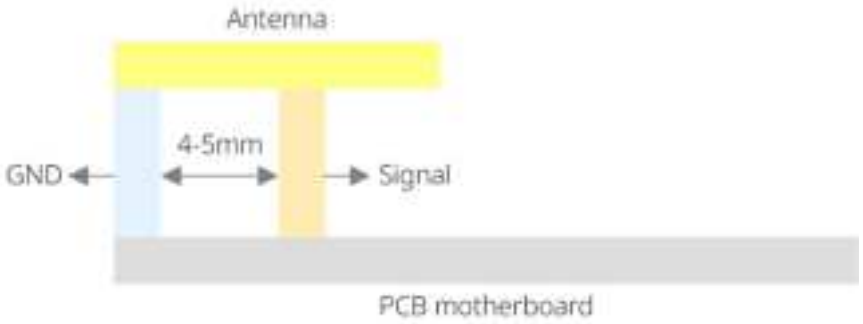


Figure 31. Location of the Signal Point and GND Point of PIFA Main board

There is complete paving in the antenna projection area. Do not place any component in the antenna area. The recommended length of PCB board should be 90 mm to 110 mm. The antenna performance is better if the board length is 105 mm.

- Structure of PIFA antenna

  Bracket

  The antenna consists of plastic bracket and metal sheet (radiator). Plastic bracket and metal sheet are fixed by hot melt method. The plastic is made of BS or PC material, the metal sheet is beryllium copper, phosphor copper, or stainless steel. If you want to use FPC, add two pins in the main board, which boasts a higher cost.

  Attached

  Attach the metal sheet (radiator) to the back cover of the module.

- Feed point of PIFA antenna

  The feeding point must be greater than 2mm × 3mm. Try to place it at the edge of the PCB board, and adopt round shape. Square with rounded corners is also preferred. The distance between feeding point pad and ground should be equal to or greater than 1mm.

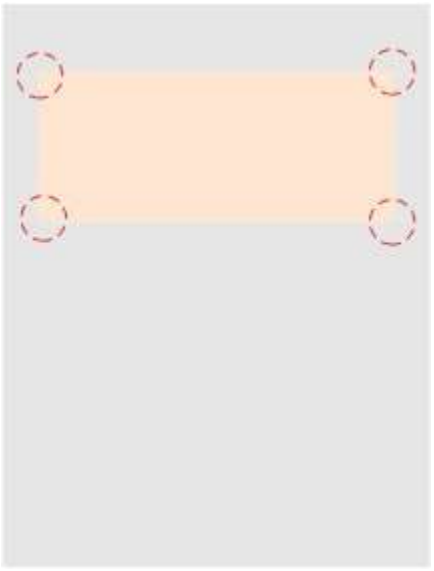


Figure 32. Pad Design Requirement

- Requirements on height and area

Operating Band	Height	Area
LTE TDD/FDD	> 6mm	> 15mm × 40mm
LTE TDD/FDD	> 6.5mm	> 17mm × 40mm
LTE TDD/FDD	> 8mm	> 20mm × 45mm

For details about WCDMA/LTE antenna design, refer to the area requirement of GSM antenna.

Monopole antenna

- Antenna structure

There is one feeding point between the antenna and main board, which is module output. It is recommended to design the antenna on the top of the device. The following figure shows the monopole antenna design.

Figure 33. Antenna Location

- Main board

  There should be no paving or PCB in the antenna projection area. Do not place any component in the antenna area. The recommended length of PCB board should be 80 mm to 100 mm. The antenna performance is improved if the board length is 95mm.

Figure 34. Requirements for Antenna Projection Area

- Structure of monopole antenna

  For details, see Structure of PIFA antenna.

- Feed point of monopole antenna

  For details, see Feed point of PIFA antenna.

- The height and area requirements for monopole antenna are described in the following table.

Operating Band	Height	Area
GSM/DCS	> 5mm	> 35mm × 7mm

GSM/DCS/PCS	> 6mm	> 35mm × 8mm
GSM850/GSM900/DCS1800/PCS1900	> 6mm	> 40mm × 10mm

For details about WCDMA/LTE antenna design, refer to the area requirement of GSM antenna.

IFA antenna

IFA antenna shares similarity with Monopole antenna and PIFA antenna. IFA antenna hastwo feeding branches, and allows ground under the antenna. The antenna has betterstability than Monopole antenna, and the antenna space requirement is between Monopole antenna and PIFA antenna.

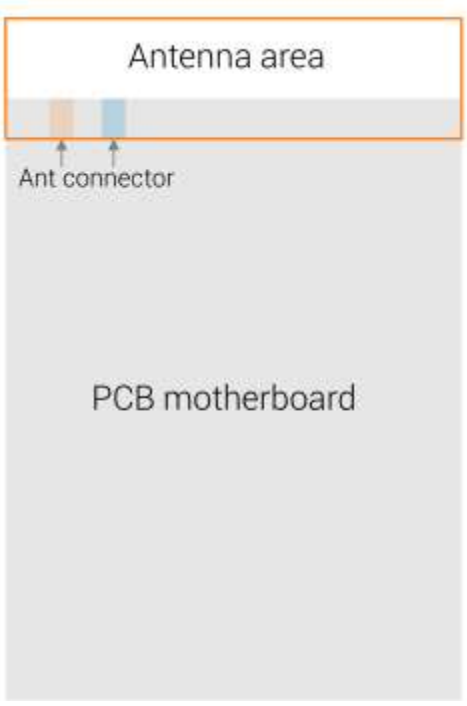


Figure 35. Location of Signal Point and GND Point

Antenna space requirement: monopole < IFA < PIFA. For other requirements, refer to the PIFA and monopole requirements.

6.7.3 Surrounding Environment Design of Internal Antenna

6.7.3.1 Handling of Speaker

Connecting beads or inductors on speaker can reduce the impact on RF.

6.7.3.2 Handling of Metal Structural Parts

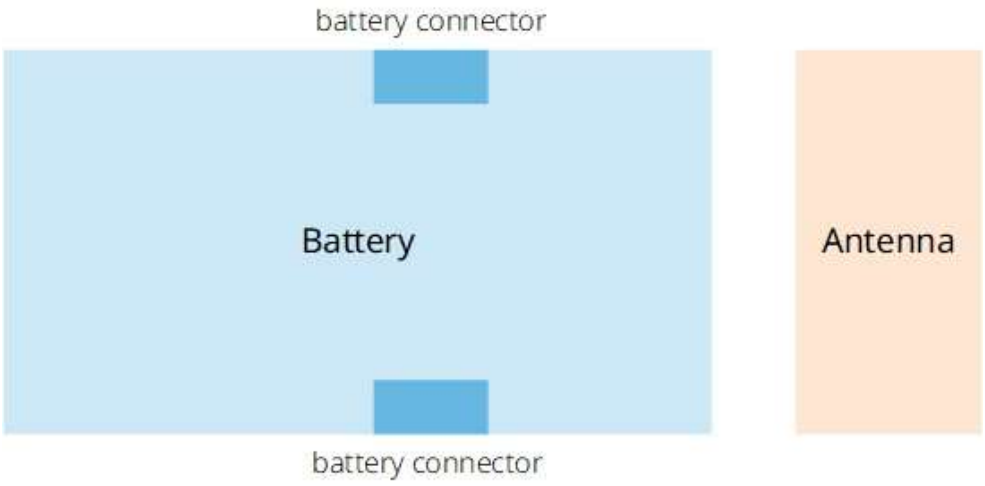
All the metal structural parts must be grounded correctly and reliably, and the circuit part must be shielded.

6.7.3.3 Handling of Battery

- The battery should be far away from antenna.

  - Monopole antenna: The distance between battery and antenna is equal to or greater than 5 mm.
  - PIFA antenna: The distance between battery and antenna is equal to or greater than 3 mm.

- Do not put the battery connector right beside the antenna.



6.7.3.4 Location of Large Components in Antenna Area

Do not place large metal components such as oscillator, speaker, and receiver aroundthe antenna; they may greatly affect the electrical performance of antenna. Do not spraythe cover of the antenna with conductive paint; be cautious when you use plating.

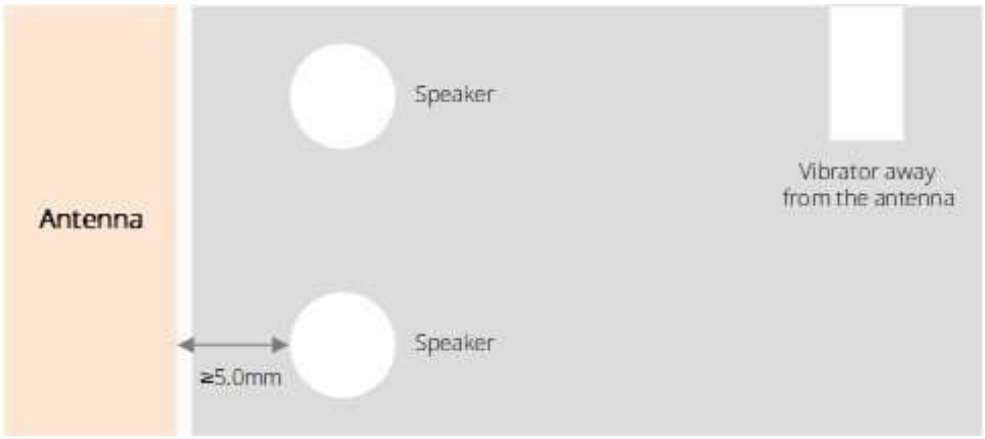


Figure 36. Location of Large Components

6.7.4 Common Problems of Internal Antenna Overall Design

Factors that would affect transmitting performance

- As the internal antenna is sensitive to the nearby medium, so the design of shell is closely related to antenna performance.

- Poor speaker layout will affect antenna performance.
- Poor battery layout will affect antenna performance.

Factors that would affect receiving performance

- If both the conductive performance of module and the radiated power of antenna meet requirement, then low sensitivity may be caused by main board design issue.
- Poor coupling sensitivity is caused by poor circuit design of LCD, LDO, and DC/DC.
- Device receiving performance is affected by VCXO or TXVCO harmonic of 19.2MHZ, 26MHZ, and 38.4MHZ systems.
- Poor coupling sensitivity is caused by SIM card clock.
- Poor FPC layout affects the receiving performance of the device.

Factors that would affect electromagnetic compatibility (EMC)

- Poor FPC layout affects EMC performance of the device.
- The metal element may absorb the antenna radiated power and produce a certain amount of secondary radiation, and coupling frequency is associated with the size of metal parts. Therefore, this kind of component should have a good grounding to eliminate or reduce secondary radiation.

6.8 Diversity and MIMO Antenna Design

- Diversity receiving technology is a main anti fading technology, which can greatly improve the transmission reliability in multipath fading channels. Its essence is to use two or more different methods to receive the same signal to overcome the fading and improve the receiving performance of the system.
- Diversity antenna can also multiplex different transmission paths in space using division multiplexing technology and receive data from the multiple different paths in parallel to improve the receiving throughput.

- The function of MIMO antenna is similar to that of diversity antenna, and they both can resist against fading and improve throughput.
- The customer is recommended to design the corresponding antenna according to the antenna requirements of each module antenna port.
- The design method of diversity antenna and MIMO antenna is consistent with that of main antenna. It is recommended to control the difference of the efficiency of diversity antenna and MIMO antenna from that of main antenna by no more than 3dB.
- The isolation of each antenna shall be greater than 25dB, and the antenna correlation coefficient shall be less than 0.5. High isolation does not mean good correlation coefficient. Customers need to evaluate two indexes separately. The isolation and correlation coefficient of antenna generally depend on:
  - Antenna isolation
  - Antenna type
  - Antenna directivity

6.9 GNSS Antenna Design

GNSS supports passive antenna. For antenna design requirements, refer to *Table30 Module Antenna Requirements*.

6.10 Other Interfaces

For the application of other interfaces, please refer to the recommended design. If theapplication scenario and the recommended design are not consistent, please contactFIBOCOM technicians for confirmation.

7 Thermal Design

FG101-NA module is designed to be workable on an extended temperature range, tomake sure the module can work properly for a long time and achieve a better performance under extreme temperatures or extreme working conditions, such as hightemperatures and high speed data transfer, refer to the following thermal design guidelines:

- Heat devices and other heat sources on the motherboard are as far away from the module as possible.
- The ground plane of the motherboard under the module is as complete as possible, and as many ground holes are drilled as possible to increase heat dissipation capability.
- The motherboard should have sufficient size or sufficient heat dissipation capacity, otherwise it is recommended to add heat sinks.

8 Electrostatic Protection

Although the ESD problem has been considered and ESD protection has been completed in the FG101-NA module design, the ESD problem may also occur in transportation and secondary development. Developers should consider ESD protection in the final product. In addition to ESD in packaging, customers should consider the recommended circuit of the interface design in the document during module application.

The following table describes the ESD discharge range allowed by the FG101-NA series module.

Table 46. Allowed ESD Discharge Range

Location	Air Discharge	Contact Discharge
VBAT, GND	±15KV	±8KV
Antenna interface	±15KV	±8KV
Other interfaces	±2KV	±1KV

9 Structural Specifications

9.1 Product Appearance

The appearance of the FG101-NA series module is shown in the following figure.

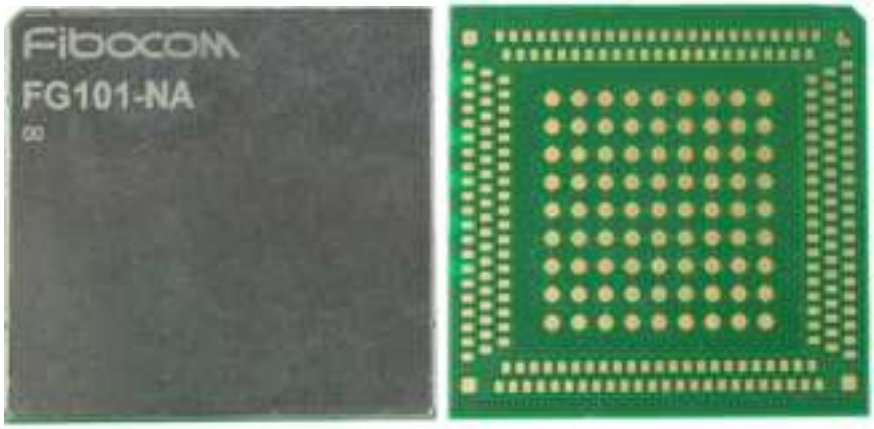


Figure 37. Product Appearance

9.2 Structural Dimensions

The structural dimension of the FG101-NA series module is shown in the following figure. The unit is mm.

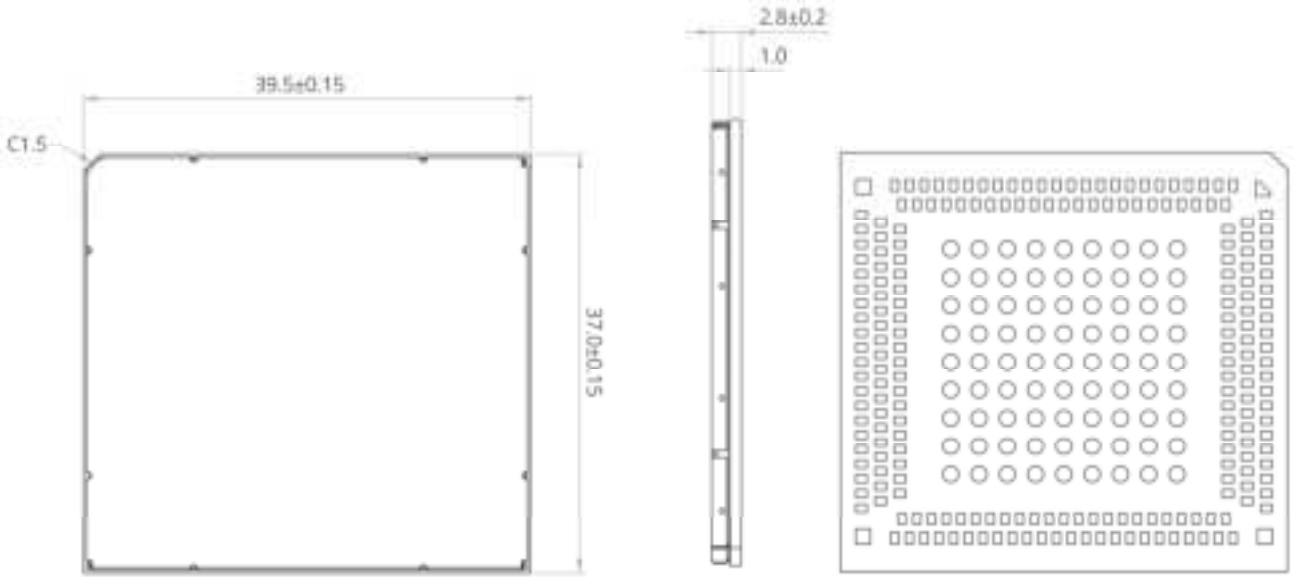


Figure 38. Structural Dimensions

9.3 PCB Pad and Stencil Design

For PCB pad and stencil design, please refer to *FIBOCOM FG101 Series SMT Design Guide*.

9.4 SMT

For SMT production process parameters and related requirements, please refer to *FIBOCOM FG101 Series SMT Design Guide*.

9.5 Packaging and Storage

For package and storage requirements, please refer to *FIBOCOM FG101 Series SMT Design Guide*.

Appendix A: Acronyms and Abbreviations

bps	Bits Per Second
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
HSDPA	High Speed Down Link Packet Access
Imax	Maximum Load Current
LED	Light Emitting Diode
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
RF	Radio Frequency
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TE	Terminal Equipment

TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access