TK-390 Circuit Description

The KENWOOD model TK-390is a UHF/FM hand-held transceiver designed to operate in the frequency range of 403 to 430MHz (FCC ID: ALH21903130),The unit consists of a receiver, a transmitter, a phase-locked loop (PLL) frequency synthesizer, a digital control unit, power supply circuits and a signaling unit.

1. RECEIVER CIRCUIT

The receiver is double conversion superheterodyne, designed to operate in the frequency range of 403 to 430MHz (FCC ID: ALH21903130).

1.1 FRONT-END RF AMPLIFIER

An incoming signal from the antenna is applied to on RF amplifier (Q200 and Q201) after passing through a transmit/receive switch circuit (D10 and D11 are off) and a 2-pole helical filter (L205). After the signal is amplified, the signal is filtered by a 2-poles helical filter (L210) to eliminate unwanted signals before it is passed to the first mixer.

1.2 FIRST MIXER

The signal from the RF amplifier is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (IC200) to become a 44.85MHz first intermediate frequency (lst IF) signal. The first IF signal is fed through two monolithic crystal filters (MCFs: XF300 for the Wide, and XF301 for the Narrow,) to further remove spurious signals.

1.3 IF AMPLIFIER

The first IF signal is amplified by Q302, and then enters IC300 (FM processing IC). The signal is heterodyned again with a second local oscillator signal with in IC300 to become a 455kHz second IF signal. The second IF signal is fed through a 455kHz ceramic filter, CF300 and CF301 (for Wide), CF302 and CF303 (for Narrow) to further eliminate unwanted signals before it is amplified and FM detected in IC300. In order to keep FM detection signal level constant, loads on FM detection signal line is switched by Q305 according to Wide/Narrow mode signal.

1.4 AUDIO AMPLIFIER

The recovered audio signal obtained from IC300, is amplified by IC607 (control board), low-pass filtered by IC607, high-pass filtered by IC607 and band-eliminate filtered by IC607. The audio signals then passed through an audio frequency switch (Q8) and de-emphasized by IC607. The processed audio signal passes through an audio volume control and is amplified to a sufficient level to drive a loud speaker by an audio power amplifier BTL (IC1).

1.5 SQUELCH AND MUTE CIRCUIT

The output signal from the squelch circuit, which consists of IC605 and Q600, is applied to the microprocessor. The microprocessor passes information to the shift register (IC404) and it controls the mute control lines (AMP SW, INT, AFC and EXT AFC) according to the input signal (noise pulse) and the microprocessor task condition.

2. TRANSMITTER

2.1 MICROPHONE CIRCUIT

The signal from the microphone is high-pass filtered by IC607 , passed through microphone mute circuit (Q403), limited and pre-emphasized by IC607, D601.

2.2 MODULATOR CIRCUIT

The output of the Audio-processor (IC607) is passed to the D/A converter (IC603) for maximum deviation adjustment and the summing amplifier (IC604) before being applied to a varactor diode in the voltage controlled oscillator (VCO) located in the frequency synthesizer section.

2.3 DRIVER AND FINAL POWER AMPLIFIER CIRCUITS

The transmit signal obtained from the VCO buffer amplifier Q5, is amplified to approximately 13dBm by Q6 and Q8. This amplified signal is passed to the power module (IC501). The power module consists of a 2-stages amplifier and is capable of producing up to 4.0W of RF power.

2.4 TRANSMIT/RECEIVE SWITCHING CIRCUIT

The power module output signal is passed through a transmit/receive switching circuit before it is passed to the antenna terminal. The transmit/receive switching circuit is comprised of D10 and D11. D10 and D11 are turned on (conductive) in transmit mode and turned off (isolated) in receive mode.

2.5 AUTOMATIC POWER CONTROL CIRCUIT AND TRANSMITTER

OUTPUT LEVEL SWITCH
The automatic power control (APC) circuit stabilizes the transmitter output power at a pre-determined level by sensing the collector current of the final amplifier transistor in the power module. The voltage comparator (IC7) compares the voltage obtained by the above collector current with a reference voltage, set using the microprocessor and Q7. An APC voltage proportional to the difference between the sensed voltage and the reference voltage appears at the output of IC7. This output voltage controls Q9, which in turn controls the voltage at pin 2 of the power module, which keeps the transmitter output power constant. The transmitter output power can be varied to 1W output power by the microprocessor, which in turn changes the reference voltage and hence the output power.

3. PLL FREQUENCY SYNTHESIZER

3.1 PLL

The frequency step of the PLL circuit is 5 or 6.25 or 7.5kHz. A 16.8MHz reference oscillator signal is divided at IC5 by a fixed counter to produce the 5 or 6.25 or 7.5kHz reference frequency. The VCO output signal is buffer amplified by Q3, then divided in IC5, by a dual-modules programmable counter in this case. The divided signal is compared in phase with the 5 or 6.25 or 7.5kHz reference signal in the phase comparator also in IC5. The output signal from the phase comparator is low pass filtered and passed to the VCO to control the oscillator frequency.

3.2 VOLTAGE CONTROLLED OSCILLATOR (VCO)

The operating frequency is generated by Hybrid Integrated Circuit (HIC) in transmit mode and HIC in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes. The T/R pin is set high in receive mode causing IC400,and turn on.

3.3 UNLOCK DETECTOR CIRCUIT

If a pulse signal appears at the LD pin of IC5, an unlock condition occurs,
The voltage applied to the UL pin of the microprocessor to go low. When the microprocessor detects this condition, the transmitter is disabled by ignoring the push-to-talk switch input signal.

4. DIGITAL CONTROL CIRCUIT

4.1 KEY SWITCHES CIRCUIT

The key switches channel switches (channel selector) information are entered directly into the display microprocessor (IC406).

4.2 RESET CIRCUIT

When the power is initially turned on, the reset circuit (IC409).

4.3 LAMP CIRCUIT

An LED is provided to illuminate the LCD and its operation is controlled by the display microprocessor.

4.4 SHIFT REGISTER CIRCUIT

Serial data is sent to the shift register (IC400,IC403,IC404,IC405) from the microprocessor to control various functions in the unit.

5. POWER SUPPLY CIRCUIT

5.1 POWER SWITCHING CIRCUIT

A 5V reference voltage is derived from an external power supply or internal battery by IC402. This reference is used to provide a 5V supply in transmit mode [5T], and a 5V supply in receive mode [5R] and a 5V supply common in both modes [5C] and [5CM] based on the control signal sent from the microprocessor or shift register. IC400 in the control unit provide a 5V supply for the control and display circuits.

6. ADDITIONAL CIRCUIT

6.1 QT, DQT ENCODE

The QT, DQT encoder tone is set by the data from the microprocessor. QT, DQT tone is generated by the microprocessor (IC406). The output is applied to the VCO(IC10) and TCXO (XI) after passing through the D/A converter (IC603) for tone deviation adjustment and the summing amplifier (IC605).

6.2 QT, DQT DECODE

A part of the recovered audio signal obtained at the amplifier IC601(2/2) are the QT and DQT tones and are low pass filtered by IC602 and passed to the microprocessor for decoding.

6.3 DTMF ENCODE

Once a signal is passed from the DTMF key pad to the microprocessor. The microprocessor passes this information to the DTMF encoder. The encoded signal is then passed to IC603 (D/A converter) for DTMF deviation adjustment. This signal provides a TX DTMF tone and a RX DTMF tone. The TX DTMF tone is passed to the pre-emphasis circuit (mic. amplifier) and then to the VCO. The RX DTMF tone is passed to the de-emphasis circuit, audio power amplifier and then to the speaker.

6.4 DTMF DECODE

The DTMF input signal from the IF IC is amplified by IC601(2/2) and goes to IC600 DTMF decoder. The decoded information is then processed by the microprocessor.