

BLOCK DIAGRAM

REVISION HISTORY			
NO.	REV.	DESCRIPTION	DATE

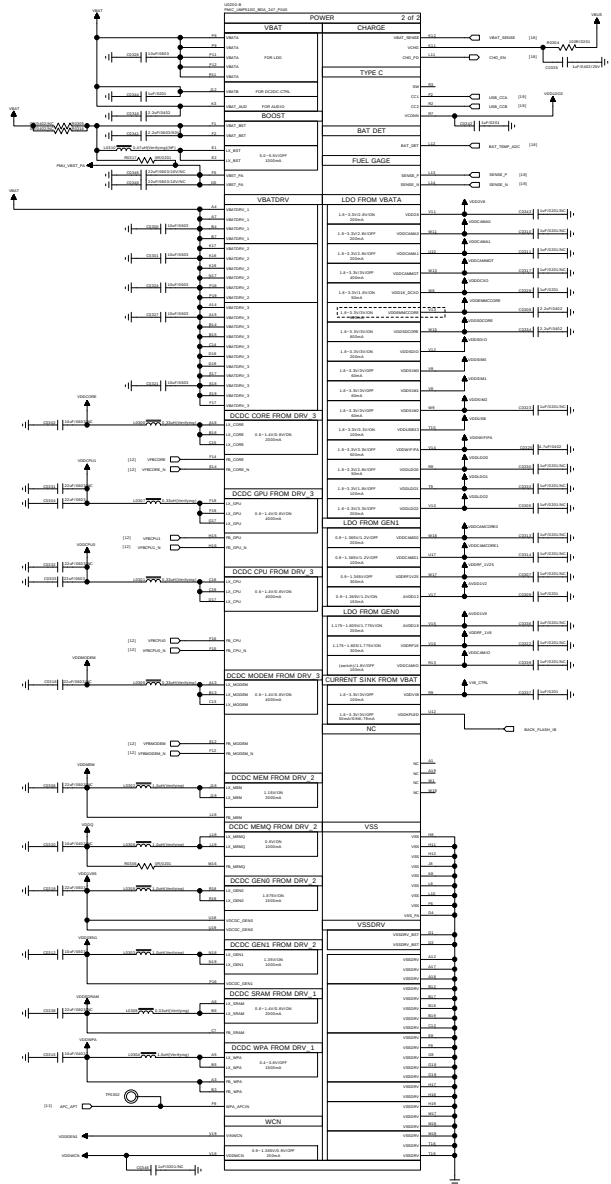
Title & Ref			
UMS9230 A CS A SCH V0.1.0			
Revision 0.1			
Author	Date	Submitted	
Hongyu Yang	2021-05-18	HWE	
Doc	Date	Reviewed	
Leiwen Ma	2021-05-18	UNISOC	
Approved	Date	CONFIDENTIAL AND PROPRIETARY	
Hongying Li	2021-05-18		

RF BLOCK DIAGRAM

REVISION HISTORY			
REV.	REV. NO.	DESCRIPTION	DATE

TITLE & REV.	
SECURITY INFO.	
DESIGNER	DATE
CHKD	DATE
APPROVED	DATE
APPROVED BY: HW	
UNISOC	
CONFIDENTIAL AND PROPRIETARY	

PMU_POWER



PMIC PN	PMIC VDDMMCCORE
UMP510G	3.0VDDHVA

Memory	UFS ICC	UFS VCCQ	UFS VCCQ2
UFS2.1 Device	PMIC VDDMMCCORE 3.0VDDHVA (up external LDO or DCDC)	Not Used	PMIC VDDCORE

Notes: If UFS ICC is greater than 600mA, please use external LDO or DCDC.

UMP510G DCDC output

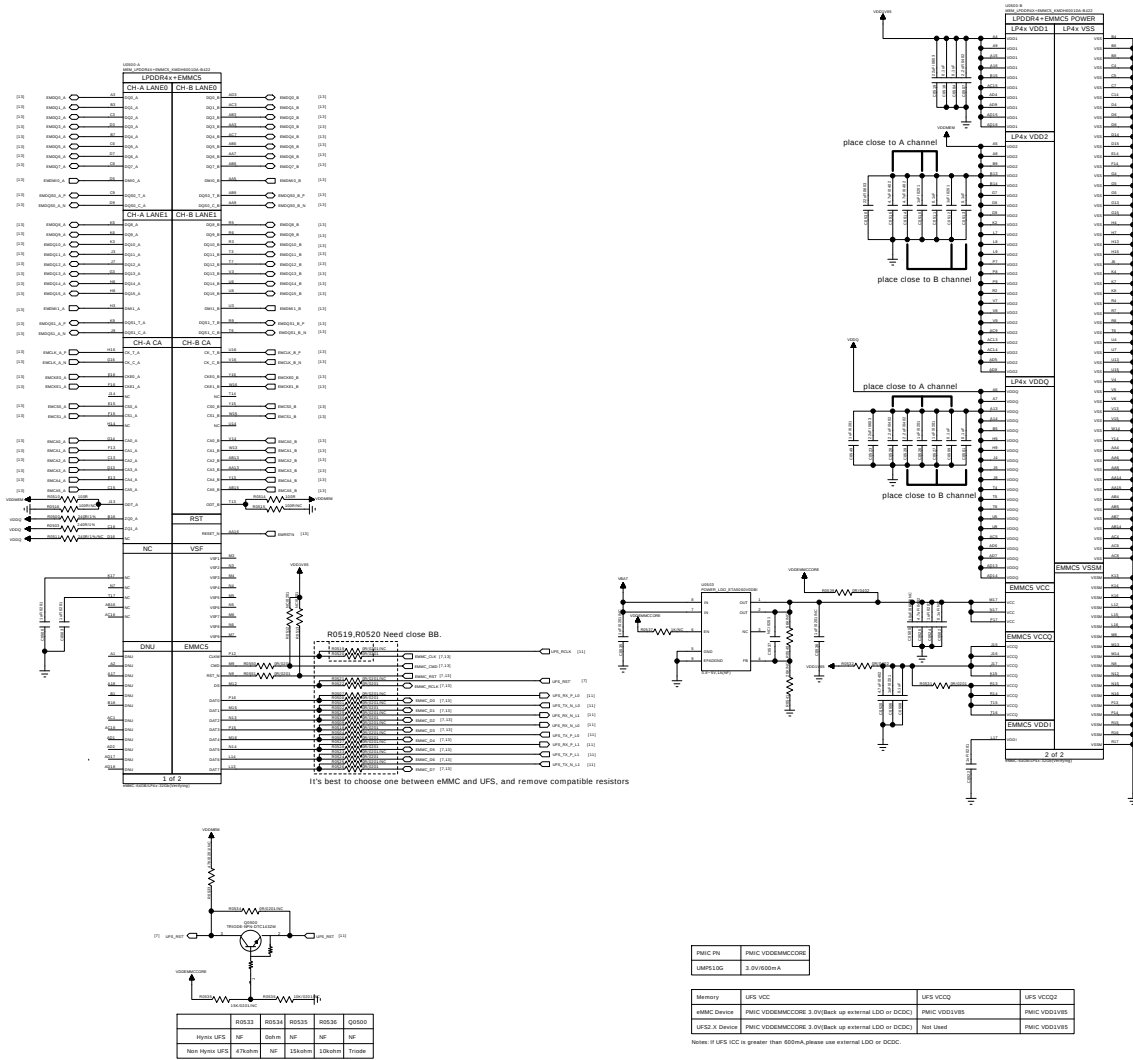
Input Power	Power Name	Output Voltage (V)	Output Current (mA)	Default Voltage (V)	Default
VBAT	DCDC CORE	0.3-1.3	2000	0.8	ON
	DCDC GPU	0.3-1.3	4000	0.8	ON
	DCDC CPU	0.3-1.3	4000	0.8	ON
	DCDC MODEM	0.3-1.3	4000	0.8	ON
	DCDC MEM	0.25-1.25	2000	1.15	ON
	DCDC MEMQ	0.25-1.25	1000	0.6	ON
	DCDC GEN0	1.8-2.5	1500	1.85	ON
	DCDC GEN1	0.6-1.5	1000	1.3	ON
	DCDC SRAM	0.3-1.3	2000	0.8	ON
VBAT	DCDC WPA	0.6-3.3	1500	/	OFF

UMP510G LDO output

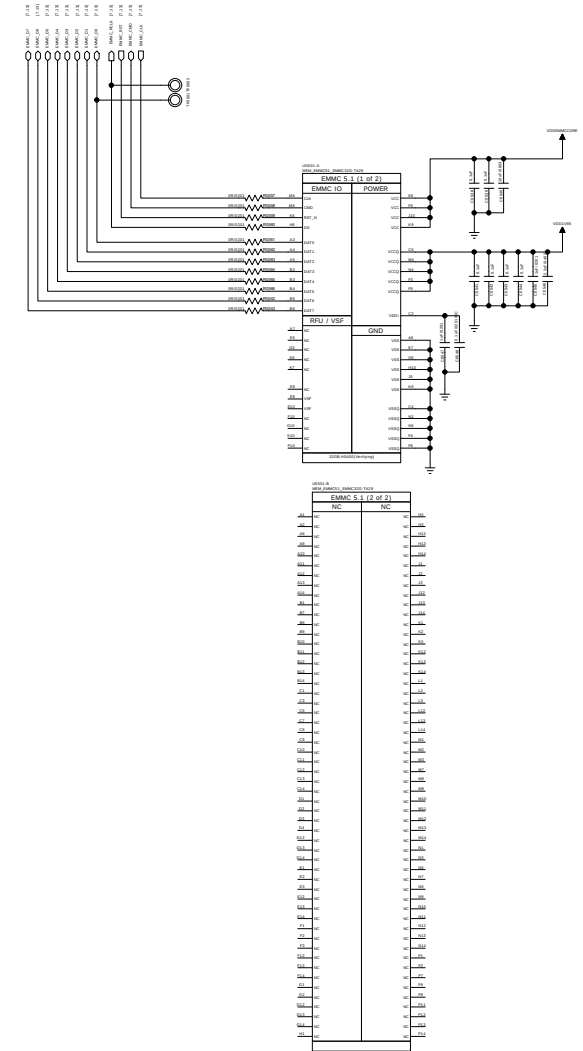
Input Power	Power Name	Output Voltage (V)	Output Current (mA)	Default Voltage (V)	Default
VBAT	VDD28	1.8-3.3	200	2.8	ON
	VDDCAMA0	1.8-3.3	200	2.8	OFF
	VDDCAMA1	1.8-3.3	200	2.8	OFF
	VDDCAMMOT	1.8-3.3	400	3	OFF
	VDD18_DCXO	1.8-3.3	50	1.8	ON
	VDDMMCCORE	1.8-3.3	600	3	ON
	VDDSDCORE	1.8-3.3	800	3	ON
	VDDSDIO	1.8-3.3	200	3	ON
	VDDSIM0	1.8-3.3	60	3	OFF
	VDDSIM1	1.8-3.3	60	3	OFF
	VDDSIM2	1.8-3.3	60	3	OFF
	VDDUSB33	1.8-3.3	100	3.3	ON
	VDDWIFIPA	1.8-3.3	500	3.3	OFF
	VDDLDO0	1.8-3.3	50	2.8	OFF
	VDDLDO1	1.8-3.3	100	3.3	OFF
	VDDLDO2	1.8-3.3	200	3.3	OFF
GEN1	VDDCAMD0	1.0-1.25	400	1.1	OFF
	VDDCAMD1	1.0-1.25	200	1.1	OFF
	VDDRF1V25	1.0-1.25	300	1.25	OFF
GEN1	AVDD12	1.0-1.25	150	1.2	ON
	AVDD18	1.2-1.8	200	1.8	ON
GEN0	VDDRF18	1.2-1.8	300	1.8	ON
	VDDCAMIO	1.2-1.8	100	1.8	OFF
GEN1	WCN	1.0-1.6	200	1	OFF

Title & Rev		
Revision History		
Rev	Date	Description
1.0	2024-01-10	Hardware DEPT.
1.0	2024-01-10	Spreadtrum communications, Inc.
1.0	2024-01-10	CONFIDENTIAL AND PROPRIETARY

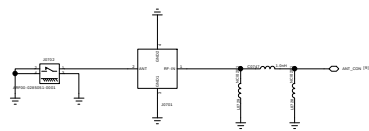
eMMC+LPDDR4/eMMC+LPDDR4X/UFS+LPDDR4X(Only support UFS2.X)



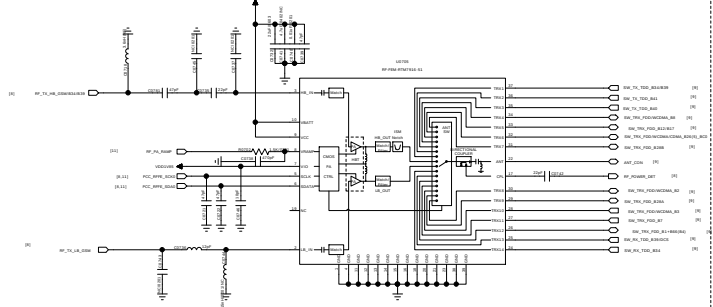
Discrete EMMC



Primary Antenna

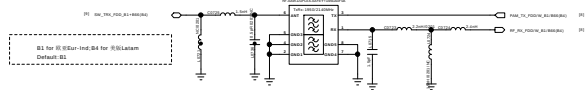


TDS/TDD B34_B39/GSM PA + Switch

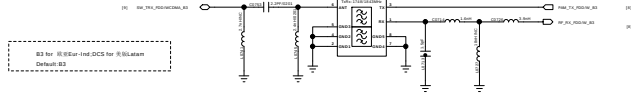


FDD LTE Parts

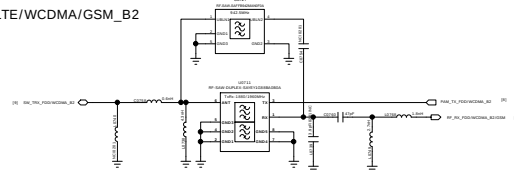
FDDLTE/WCDMA_B1



FDDLTE/WCDMA_B3

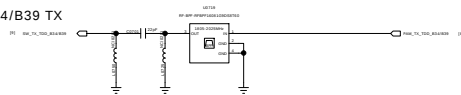


FDDLTE/WCDMA/GSM_B2

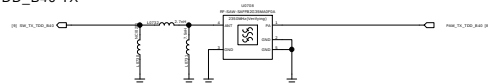


TDD LTE Parts

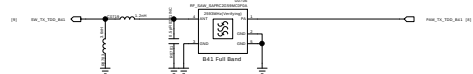
TDD_B34/B39 TX



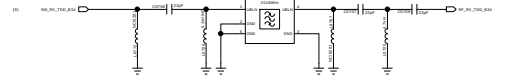
TDD_B40 TX



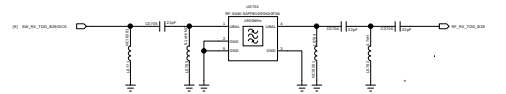
TDD_B41 TX



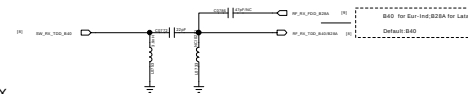
TDD_B34_RX



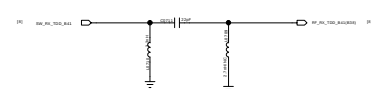
TDD_B39_RX



TDD_B40_RX

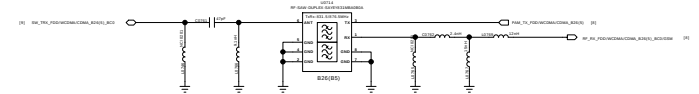


TDD_B41_RX

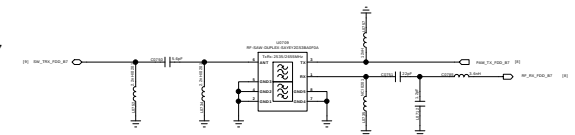


PRIMARY TRX Path FDD LTE Parts

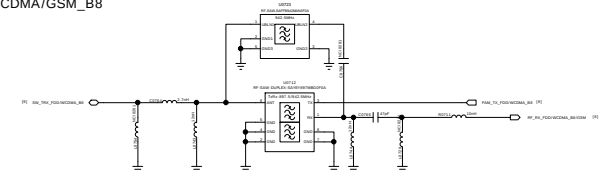
FDDLTE/WCDMA/CDMA/GSM_B5_B26



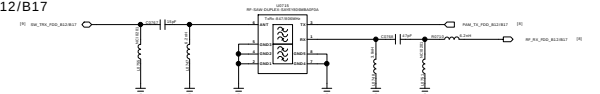
FDDLTE_B7



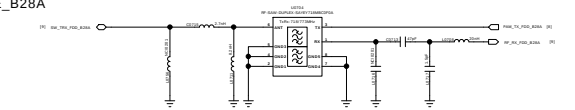
FDDLTE/WCDMA/GSM_B8



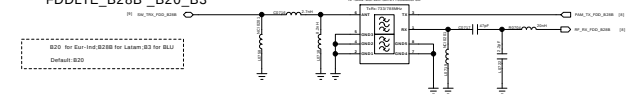
FDDLTE_B12/B17



FDDLTE_B28A



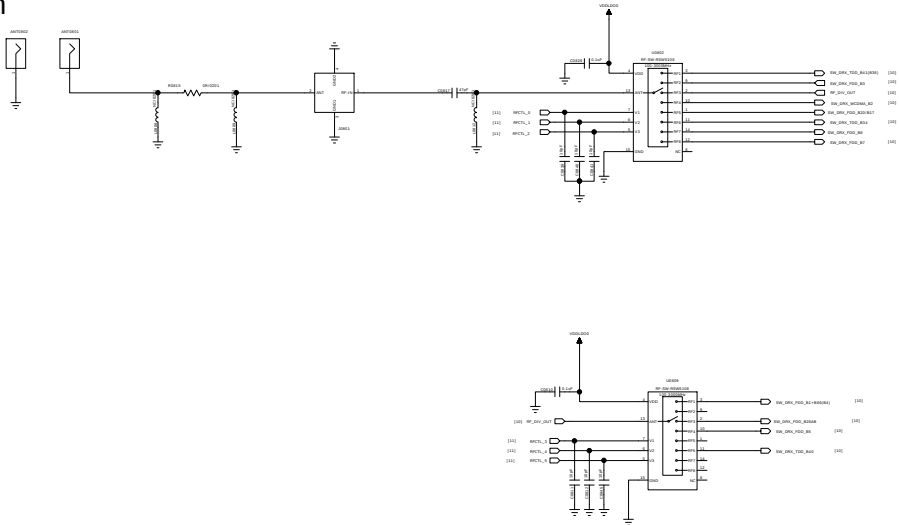
FDDLTE_B28B_B20_B3



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DESIGN:	DATE:	APPROVED:	Hardware DEPT.
FOR:	DATE:	DESIGNED:	Spreadtrum communications, Inc.
APPROVED:	DATE:	CONFIDENTIAL AND PROPRIETARY	

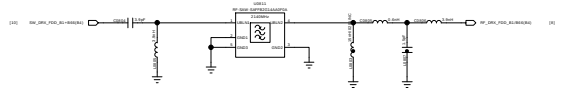
REVISION HISTORY			
REV.	REV. NO.	DESCRIPTION	DATE

Diversity LTE Path

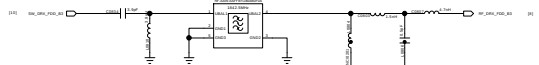


Diversity RX Path

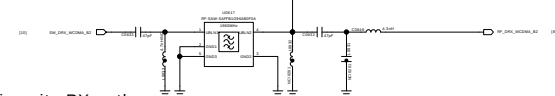
FDD_B1+B66(B4)_Diversity RX path



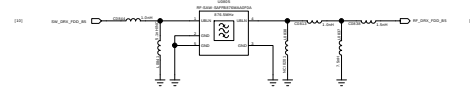
FDD_B3_Diversity RX path



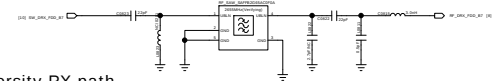
FDD_B2_Diversity RX path / B39_Diversity RX path



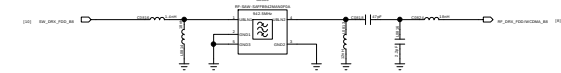
FDD_B5_Diversity RX path



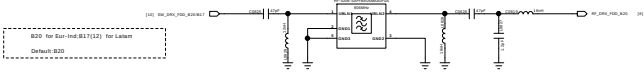
FDD_B7_Diversity Rx path



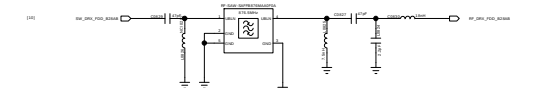
FDD_B8_Diversity RX path



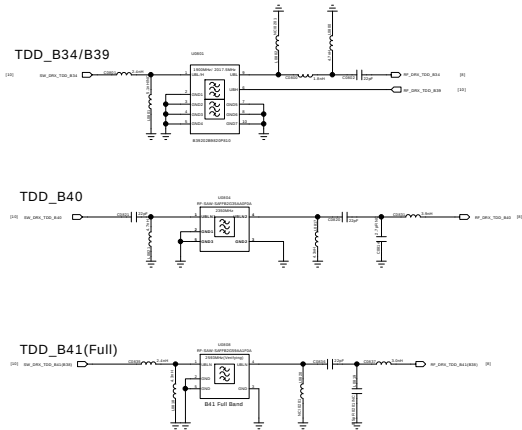
FDD_B12/B17_Diversity RX path



FDD_B28A/B_Diversity RX path



Diversity RX Path



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Revision No.:			
DESIGNER:	DATE:	APPROVED BY:	
FOR:	DATE:	Hardware DEPT.	
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		Spreadtrum communications, Inc.	
		CONFIDENTIAL AND PROPRIETARY	

close to 88

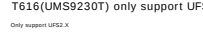
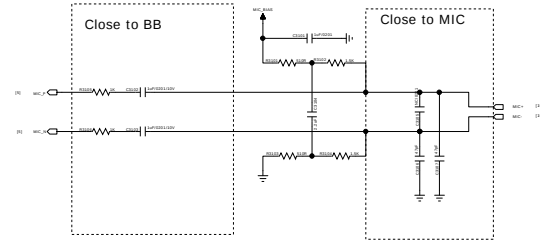


Figure 10: Memory architecture diagram showing the connection between the processor and memory. The diagram is divided into several sections: DATA LANE 0 A, DATA LANE 1 A, DATA LANE 0 B, DATA LANE 1 B, and EMAC. Each section shows the internal structure of the memory lanes, including data paths, control signals, and connections to the processor. The diagram is labeled "2 of 7".

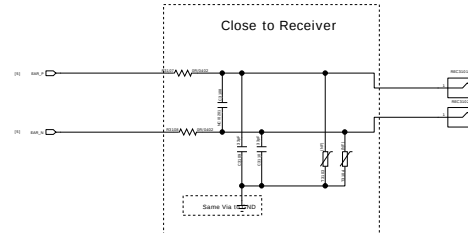
		TITLE & REV:	
		DOCUMENT NO.:	
DESIGNER:	DATE:	DESCRIPTION:	
		Hardware DEPT.	
FOR:	DATE:	COMPANY:	
		Spreadtrum communications, Inc.	
APPROVED:	DATE:	CONFIDENTIAL AND PROPRIETARY	

REVISION RECORD			
LTB	ECO NO.	APPROVED	DATE

MAIN MIC

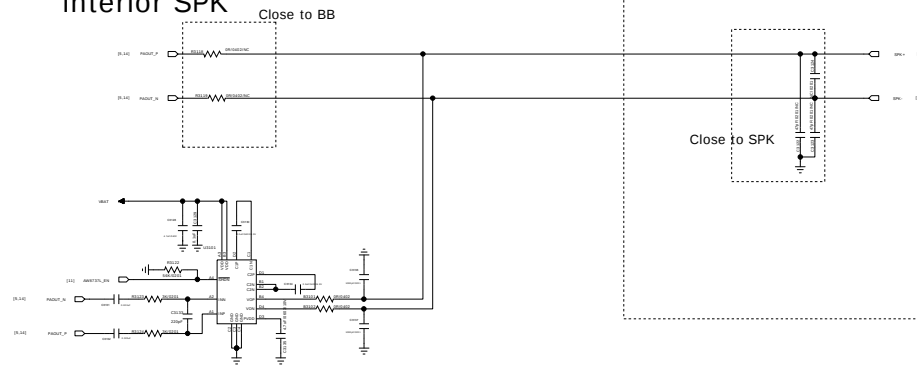


RECEIVER

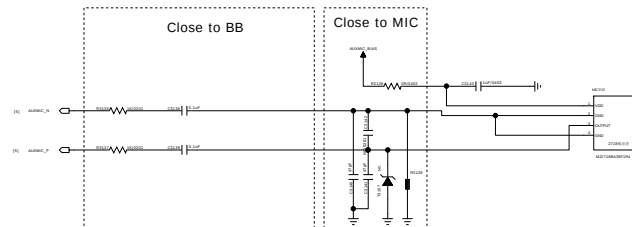


Audio PA

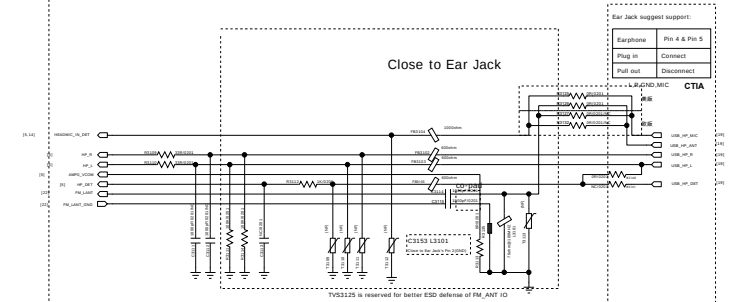
interior SPK



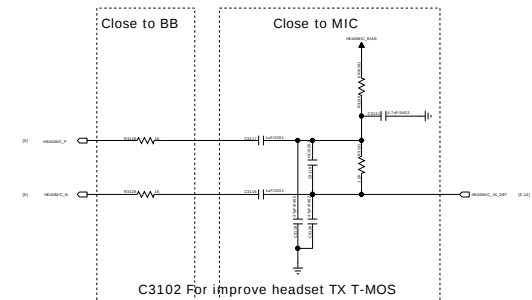
AUX MIC



3.5mm Ear Jack



HEAD MIC



		TITLE & REV:	
		REVISION NO.:	
ISSUED:	DATE:	DESCRIPTION:	
		Hardware DEPT.	
FOR:	DATE:	CARRIER:	
		Spectrum communications, Inc.	
APPROVED:	DATE:	CONTRACTUAL AND PROPRIETARY	

D



C

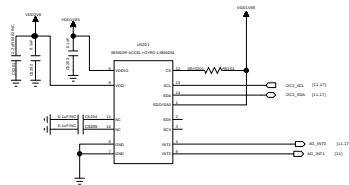


A

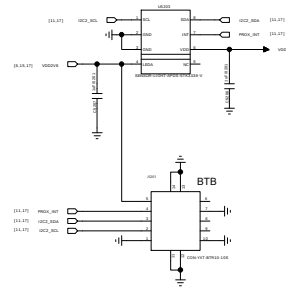


		TITLE & REV:	
		DOCUMENT NO:	
DESIGNER	DATE:	CONTRACTOR	
FOR	DATE:	COMPANY: Spreadtrum communications, Inc.	
APPROVED:	DATE:	CONFIDENTIAL AND PROPRIETARY	

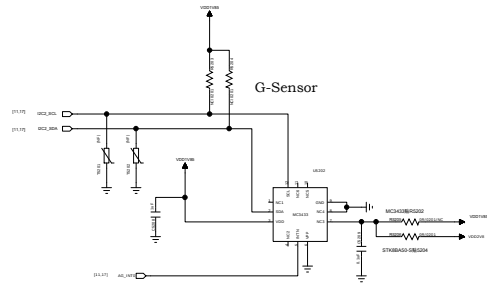
Accelerometer&GYRO: ICM-20600



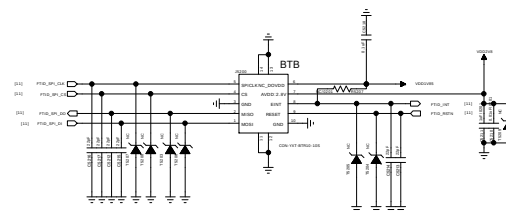
ALS & PROX



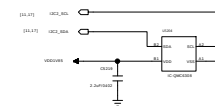
G Sensor



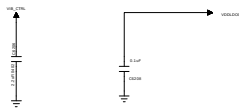
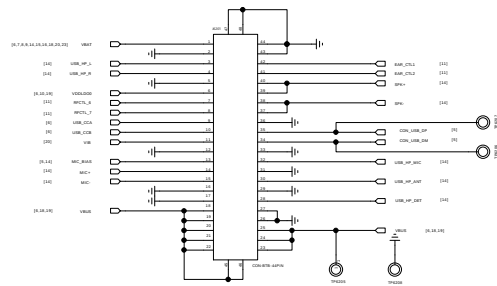
FingerPrint ID



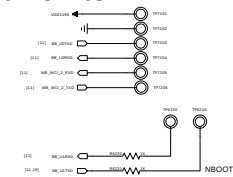
Magnetic Sensor



USB Connector



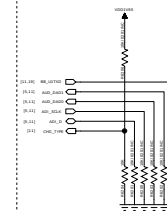
Test Points



MARK POINT



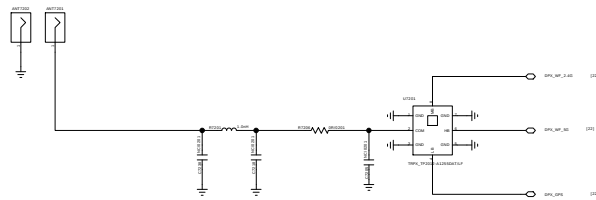
Strapping pin



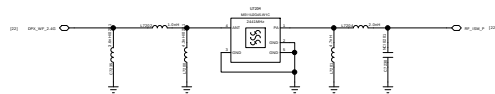
Ball name	Signal name in boot code	Value	Descriptions	Default vale
U1TXD	USB_DLOAD_EN	0	USB download(no time out)	1(ie=1,wpu)
		1	UART download	
		00	Reserved	
		01	UFS boot	
AUD_DAD1	ARM_BOOT_MD0	10	SD boot	1(ie=1,wpu) (MSB=MD1, LSB=MD0)
AUD_DAD0	ARM_BOOT_MD1	11	eMMC 6.5Mhz	
ADI_SCLK	ARM_BOOT_MD2	0	Reserved	1(ie=1,wpu)
		1	Reserved	
ADI_D	ARM_BOOT_MD3	0	NON-KEY Download(With timeout) mode	1(ie=1,wpu)
		1	Normal mode	
CHG_TYPE	ARM_BOOT_MD4	0	Other(DCP/other)	0(ie=1,wpd) 无按键下载 和INSProm有差别, 3s time
		1	USB insert(SDP/CDP)	

Title & Rev.			
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1.0	2019-01-10	Hardware DEPT.	
1.0	2019-01-10	Spreadtrum communications, Inc.	
APPROVED	DATE	CONFIDENTIAL AND PROPRIETARY	

WIFI&BT ANT



WIFI/BT SAW

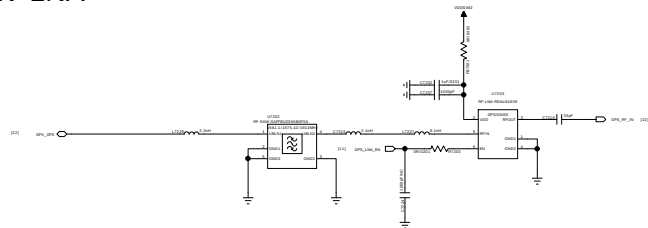


		C7205	R7230
Default	KCT8553C	0ohm	NF
Option	RFFM8516	10pF	3.9K

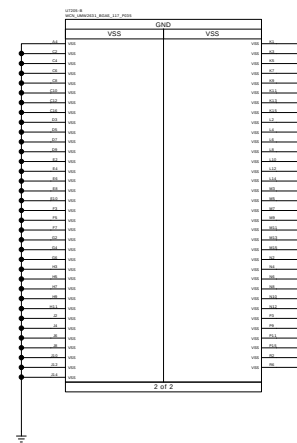
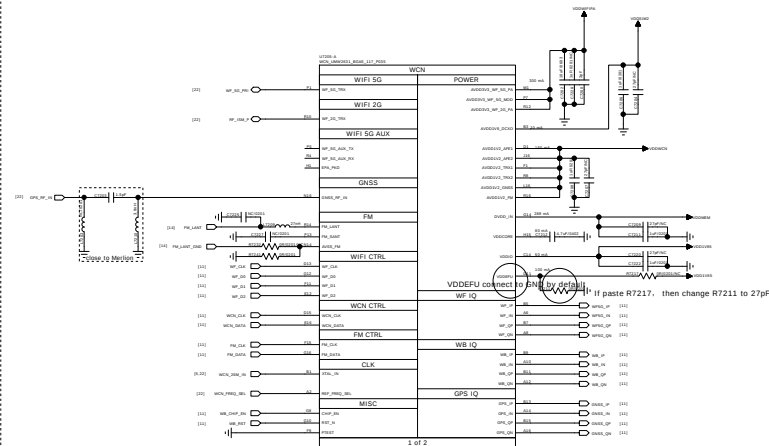
5G WIFI



GNSS SAW LNA



WCN



Bonding Option

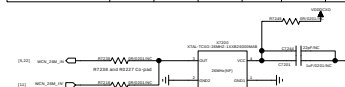
FREQ_SEL---Internal Pull-up	
0	52MHz
1	26MHz



REVISION RECORD			
LTB	ECO NO.	APPROVED:	DATE:

TSX (PMU) Only

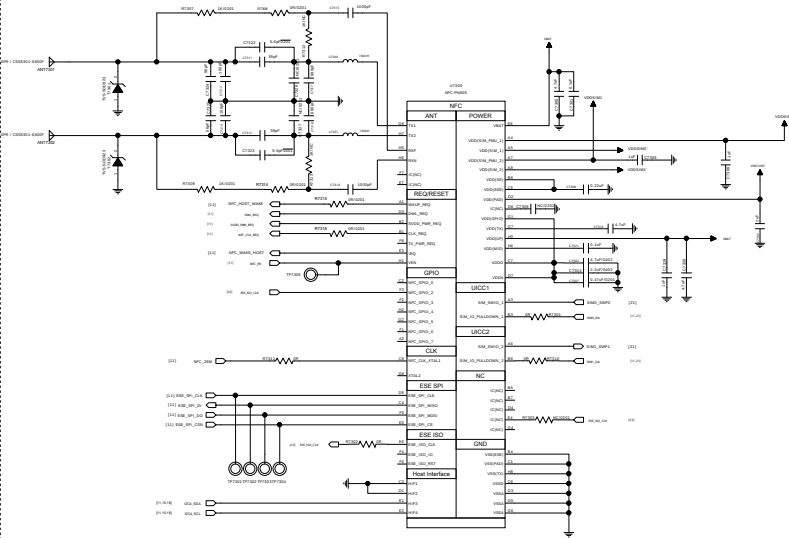
TSX (PMU) Only									
-->		X7200	R7220	R7238	R7218	C7244	C7201	R7245	R0227
	TSX (PMU) Only	NF	NF	NF	NF	NF	NF	NF	OR
	TCXO(WCN) + DCXO(PMU)	TCXO	NF	OR	OR	22pF	1uF	OR	NF
	TCXO(WCN) + 32K(PMU)	TCXO	OR	OR	NF	22pF	1uF	OR	NF



		TITLE & REV.	
		REVISION NO.	
ISSUED:	DATED:	CONTRACTOR	
		Hardware DEPT.	
FIG.	DATED:	CONTRACT	
		Spreadtrum communications, Inc.	
APPROVED:	DATED:	CONTRACTOR, AND PROJECT MANAGER	

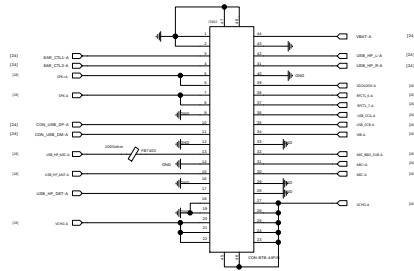
REVISION HISTORY			
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NFC

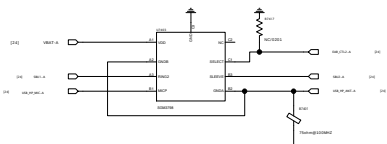


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REV.	REV. NO.	DESCRIPTION	DATE

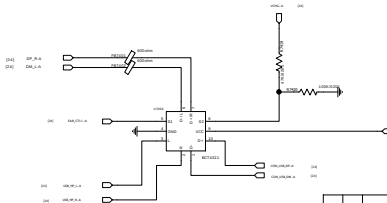
Main connector



TYPE-C Switch



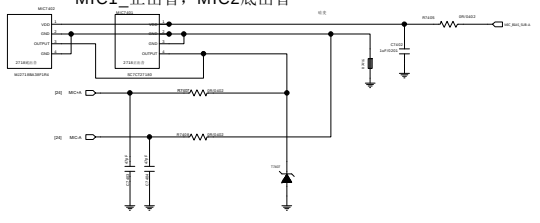
SELECT	FUNCTION
0	MICP-SLEEVE GND-RING2
1	MICP-RING2 GND-SLEEVE



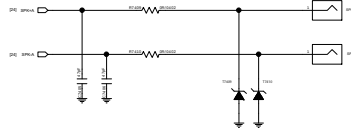
S1	S2	Audio Mode	USB Mode
0	1	OFF	ON
0	0	ON	OFF

MIC

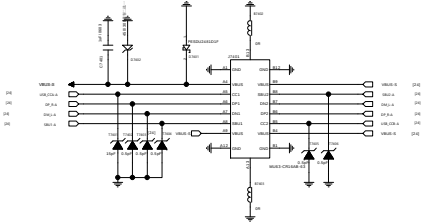
MIC1 正出音, MIC2底出音



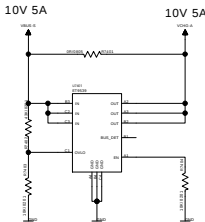
SPK



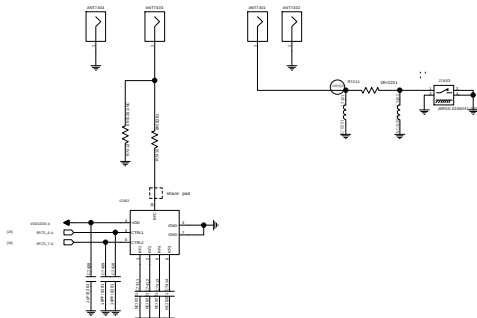
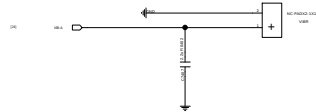
TYPE-C



OVP



VIBRATOR



REVISION HISTORY			
REV.	REV. NO.	DESCRIPTION	DATE