



## L620 Hardware Design

**NB-IoT Module Series** 

Version: V1.1

**Date**: 2018-06-05





### **Notice**

Some features of the product and its accessories described herein rely on the software installed, capacities and settings of local network, and therefore may not be activated or may be limited by local network operators or network service providers. Thus, the descriptions herein may not exactly match the product or its accessories which you purchase. Shanghai Mobiletek Communication Ltd reserves the right to change or modify any information or specifications contained in this manual without prior notice and without any liability.

## Copyright

This document contains proprietary technical information which is the property of Shanghai Mobiletek Communication Ltd. copying of this document and giving it to others and the using or communication of the contents thereof, are forbidden without express authority. Offenders are liable to the payment of damages. All rights reserved in the event of grant of patent or the registration of a utility model or design. All specification supplied herein are subject to change without notice at any time.

#### **DISCLAIMER**

ALL CONTENTS OF THIS MANUAL ARE PROVIDED "AS IS". EXCEPT AS REQUIRED BY APPLICABLE LAWS, NO WARRANTIES OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDINGBUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE MADE IN RELATION TO THE ACCURACY, RELIABILITY OR CONTENTS OF THIS MANUAL.TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, IN NO EVENT SHALL SHANGHAI MOBILETEKCOMMUNICATION LTD BE LIABLE FOR ANY SPECIAL, INCIDENTAL, INDIRECT, OR CONSEQUENTIAL DAMAGES, OR LOSS OF PROFITS, BUSINESS, REVENUE, DATA, GOODWILL SAVINGS OR ANTICIPATED SAVINGS REGARDLESS OF WHETHER SUCH LOSSES ARE FORSEEABLE OR NOT.



# **Version History**

| Date       | Version | Modify records   | Author  |
|------------|---------|--|---------|
| 2018-04-14 | V1.0    | First Release  | Rc.Dong |
| 2018-06-05 | V1.1    | Change PIN name of PIN16; modify peak current at different supply voltages | Rc.Dong |
|            |         |  |         |
|            |         |  |         |
|            |         |  |         |
|            |         |  |         |
|            |         |  |         |
|            |         |  |         |
|            |         |  |         |
|            |         |  |         |



## CONTENT

| 1. | Introduction                          | 5  |
|----|---------------------------------------|----|
|    | 1.1 Hardware Diagram                  | 5  |
|    | 1.2 Main features                     |    |
|    | 1.3 Specifications                    |    |
|    | 1.4 Interfaces                        |    |
|    |                                       |    |
| 2. | Package Information                   | 8  |
|    | 2.1 Pin Configuration                 | 8  |
|    | 2.2 Pin definition                    | 9  |
|    | 2.3 Package Information               | 11 |
|    | 2.3.1 Dimensions                      | 11 |
|    | 2.3.2 Module size                     | 12 |
|    | 2.3.3 Recommend Pad                   | 13 |
| 3. | Interface Circuit Design              | 14 |
| ٥. |                                       |    |
|    | 3.1 Power Section                     |    |
|    | 3.1.1 Power Supply                    |    |
|    | 3.1.2 Hardware Power On/Off           |    |
|    | 3.1.3 Hardware reset                  |    |
|    | 3.1.4 RTC_EINT Key                    |    |
|    | 3.2 SIM Interface                     |    |
|    | 3.2.1 Pin Description                 |    |
|    | 3.2.2 SIM application                 |    |
|    | 3.2.3 eSIM                            |    |
|    | 3.3 IIC Interface                     |    |
|    | 3.4 UART Interface                    |    |
|    | 3.4.1 Pin Description                 |    |
|    | 3.4.2 UART application                |    |
|    | 3.5 LED Interface                     |    |
|    | 3.5.1 LED Control circuit             |    |
|    | 3.5.2 LED Status description          |    |
|    | 3.6 ADC                               | 21 |
| 4. | Electrical characteristics            | 22 |
|    | 4.1 Electrical characteristic         | 22 |
|    | 4.2 Temperature characteristic        |    |
|    | 4.3 Absolute Maximum Power            |    |
|    | 4.4 Recommended operating conditions  |    |
|    | 4.5 Power consumption                 |    |
|    | 4.6 Power Sequence                    |    |
|    | 4.7 Digital Interface Characteristics |    |
|    | 4.8 ESD                               | 26 |



| 5. | RF Features  | 28 |
|----|--|----|
|    | 5.1 RF Main Features   | 28 |
|    | 5.2 Data link  | 30 |
|    | 5.3 Antenna Circuit Design                                     | 31 |
|    | 5.4 Antenna Design   | 32 |
| 6. | Storage and Production   | 34 |
|    | 6.1 Storage  |    |
|    | 6.2 Production   | 34 |
|    | 6.2.1 Module confirmation and moisture                         | 35 |
|    | 6.2.2 SMT reflow attentions                                    | 36 |
|    | 6.2.3 SMT stencil design and the problem of less tin soldering | 37 |
|    | 6.2.4 SMT attentions   | 37 |



## 1. Introduction

L620 is a small NB-IoT module for LCC package, with stable and reliable performance. It can be widely used for various products and equipment of IoT.

## 1.1 Main features

CPU

ARM Cortex-M4@78MHz





#### Flash

SYSRAM: 32KB

PSRAM: 32Mb

Flash: 32Mb

### Frequency bands

3GPP R13/R14

Band 2/5/12

### Output Power

22dBm±2dB

### Sensitivity

-139dBm±1dB

#### • Data transmission

DL: 25.5kbps

UL: 35.35kbps(single-tone)/58.3kbps(multi-tone)

### Ultra-low power consumption

PSM: 3.5uA @3.3V

## 1.2 Specifications

- Supply Voltage Range: 2.1∼3.6V (type3.3V)
- Dimensions: 17.6mm \* 15.8mm \* 2.3mm



- Package: 45-pin LCC
- Operation Temperature Range: -40 °C ~+85 °C
- Storage Temperature Range: -45°C~+90°C
- Support PSM and eDRX mode
- Weight : Approx 1g

## 1.3 Interfaces

- IIC
- GPIO
- EINT
- ADC
- SIM: Support 1.8V/3V or eSIM
- UART
- SPI
- IIS
- PWM



## 2. Package Information

## 2.1 Pin Configuration

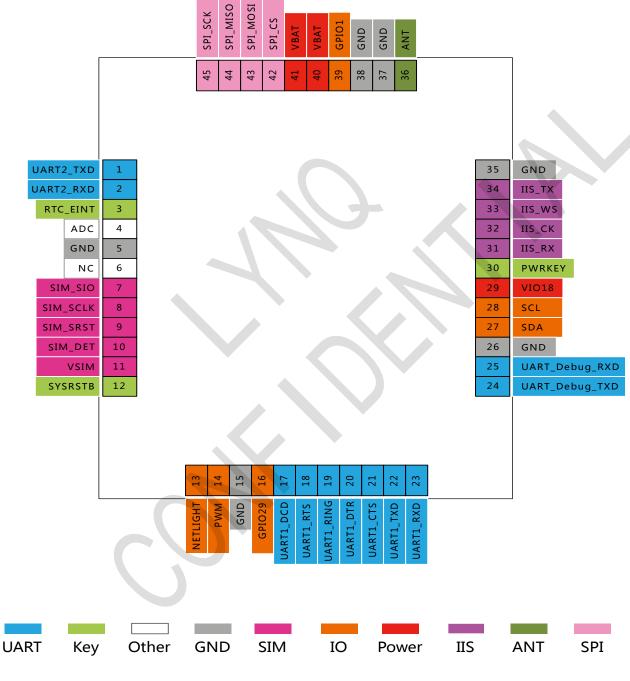


Figure 2-1 L620 Pin View



## 2.2 Pin definition

Table 2-1 L620 Pin description

| Pin<br>NO. | Pin name   | Туре | Function Description                         | Power domain | State (1) |
|------------|------------|------|--|--------------|-----------|
| 1.         | UART2_TXD  | 0    | UART2 transmit data output                   | VIO18        | Open      |
| 2.         | UART2_RXD  | - 1  | UART2 receive data input                     | VIO18        | Open      |
| 3.         | RTC_EINT   | - 1  | Wake up module for exiting PSM               | 0~3.6V       | Open      |
| 4.         | ADC        | 1    | ADC external input channel                   | 0~1.4V       | Open      |
| 5.         | GND        | G    | Ground                                       | -            | GND       |
| 6.         | NC         |      | NC   |              |           |
| 7.         | SIM_SIO    | I/O  | SIM data                                     | 1.8/3.0V     | Open      |
| 8.         | SIM_SCLK   | 0    | SIM clock                                    | 1.8/3.0V     | Open      |
| 9.         | SIM_RST    | 0    | SIM reset                                    | 1.8/3.0V     | Open      |
| 10.        | SIM_DET    |      | SIM detect pin                               | VIO18        | Open      |
| 11.        | VSIM       | Р    | SIM output voltage                           | 1.8/3.0V     | Open      |
| 12.        | SYSRSTB    | I    | System reset signal                          | 2.1~3.6V     | Open      |
| 13.        | NETLIGHT   | 0    | Output PIN as LED control for network status | VIO18        | Open      |
| 14.        | PWM        | 0    | PWM output                                   | VIO18        | Open      |
| 15.        | GND        | G    | Ground                                       |              | GND       |
| 16.        | GPIO29     | I/O  | General input/output PIN                     | VIO18        | Open      |
| 17.        | UART1_DCD  | DO   | UART1 data carrier detect                    | VIO18        | Open      |
| 18.        | UART1_RTS  | DI   | UART1 ready to receive                       | VIO18        | Open      |
| 19.        | UART1_RING | DO   | UART1 ring indicator                         | VIO18        | Open      |
| 20.        | UART1_DTR  | DI   | UART1 Data terminal ready                    | VIO18        | Open      |
| 21.        | UART1_CTS  | DO   | UART1 clear to send                          | VIO18        | Open      |



| 22. | UART1_TXD          | 0   | UART1 transmit data output      | VIO18      | Open |
|-----|--------------------|-----|---------------------------------|------------|------|
|     |                    |     |                                 |            |      |
| 23. | UART1_RXD          | - 1 | UART1 receive data input        | VIO18      | Open |
| 24. | UART_Debug_<br>TXD | 0   | UART_Debug transmit data output | VIO18      | Open |
| 25. | UART_Debug_<br>RXD | -1  | UART_Debug receive data input   | VIO18      | Open |
| 26. | GND                | G   | Ground                          |            | GND  |
| 27. | SDA                | I/O | IIC data                        | VIO18      | Open |
| 28. | SCL                | I/O | IIC clock                       | VIO18      | Open |
| 29. | VIO18              | Р   | 1.8V output voltage             | 1.8V       | Open |
| 30. | PWRKEY             | 1   | Powerkey                        | 0~3.6V     | Open |
| 31. | IIS_RX             | DI  | Digital audio input             | VIO18      | Open |
| 32. | IIS_CK             | 0   | The bit clock of the interface  | VIO18      | Open |
| 33. | IIS_WS             | 0   | The left/right word select      | VIO18      | Open |
| 34. | IIS_TX             | DO  | Digital audio output            | VIO18      | Open |
| 35. | GND                | G   | Ground                          |            | GND  |
| 36. | ANT                | ANT | Antenna                         |            | Open |
| 37. | GND                | G   | Ground                          |            | GND  |
| 38. | GND                | G   | Ground                          |            | GND  |
| 39. | GPIO1              | I/O | General input/output PIN        | VIO18      | Open |
| 40. | VBAT               |     | Davidania                       | 2.1- 2.6\/ | VBAT |
| 41. | VBAT               | Р   | Power supply                    | 2.1∼3.6V   | VBAT |
| 42. | SPI_CS             | 0   | SPI chip-select                 | VIO18      | Open |
| 43. | SPI_MOSI           | 1/0 | SPI master out slave in         | VIO18      | Open |
| 44. | SPI_MISO           | I/O | SPI master in slave out         | VIO18      | Open |
| 45. | SPI_SCK            | 0   | SPI clock                       | VIO18      | Open |

(1) Suggested status when not in use.



Table 2-2 Pin type description

| P:POWER     | G:GROUND          |
|-------------|-------------------|
| I:INPUT     | DI:DIGITAL INPUT  |
| O:OUTPUT    | DO:DIGITAL OUTPUT |
| ANT:ANTENNA | NC:NOT CONNECT    |

## 2.3 Package Information

### 2.3.1 Dimensions

The L620 mechanical dimensions are described as following figure (Top view, Back view, Side view).

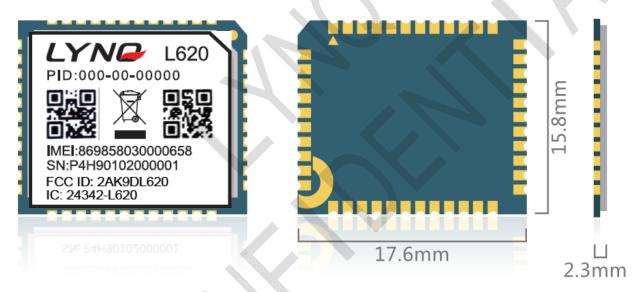


Figure 2-2 Mechanical Dimensions



## 2.3.2 Module size

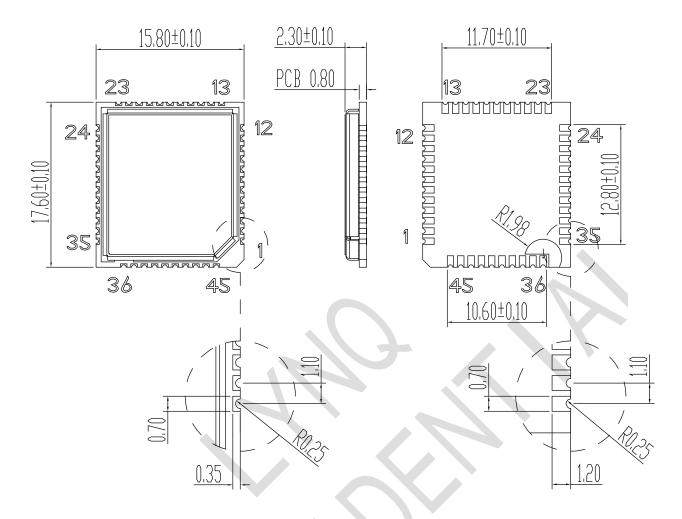


Figure 2-3 Module Size (Unit: mm)



## 2.3.3 Recommend Pad

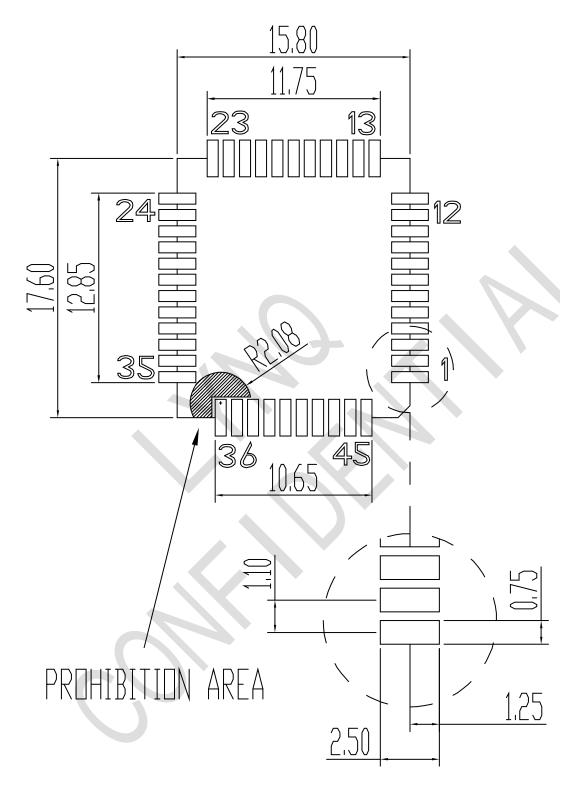


Figure 2-4 Recommend pad(Top view, Unit: mm)



## 3. Interface Circuit Design

#### 3.1 Power Section

## 3.1.1 Power Supply

VBAT is the main power supply of the module, and the input voltage range is 2.1V to 3.6V. The recommended voltage is 3.3V. Because the module transmit burst may cause voltage drops, it is recommended that the total bypass cap used in the VBAT be greater than 330uF. At this time, the module's transient peak current will reach 600mA. If the total bypass cap on the VBAT is less than 330uF, the module's transient peak current will reach 1A when the module's supply voltage is between 2.1V and 3.0V and the module's transient peak current will reach 600mA when the module's supply voltage is between 3.0V and 3.6V. During layout, the capacitors are close to the VBAT pins and VBAT trace width is about 1mm.

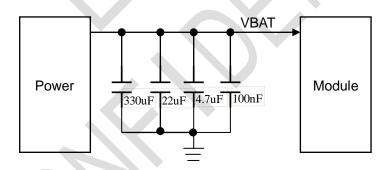


Figure 3-1 Power Supply circuit

Notes: According to the environment, please select capacitor as large value as possible; and add 100pF, 33pF capacitors if requiring.



#### 3.1.2 Hardware Power On/Off

Module 30-pin is the Power on/off key. Pulling down the PWRKEY at least 300ms∼1s and then releasing, the module will boot. There is internally pulled-up resistor.

Module 30-pin can also be used for hardware shutdown. When this pin has been pulled down over  $8\sim$ 11 seconds, the module will shutdown.

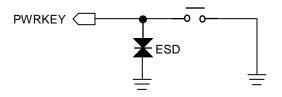


Figure 3-2 Turn on circuit

Note: In PSM mode, you can exit the PSM mode by pulling PWRKEY low.

#### 3.1.3 Hardware reset

Module 12-pin is the hardware reset input. The module will reset hardware when it receives a 48ms low level signal. It is internally pull-up to VBAT, and does not need to pull up externally.

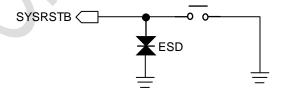


Figure 3-3 System Reset



## 3.1.4 RTC\_EINT Key

Module 3-pin is the RTC\_EINT input. The module will exit the PSM mode when it receives a 48ms low level signal. It is internally pull-up to VBAT, and do not need to pull up externally.

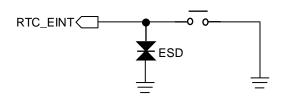


Figure 3-4 RTC\_EINT Key

## 3.2 SIM Interface

## 3.2.1 Pin Description

L620 supports and is able to automatically detect 3.0V and 1.8V SIM card. SIM card interface signal as shown in table 3-1.

Table 3-1 SIM Pin Description

| Pin NO. | Pin Name | Signal definition   | Function Description                         |
|---------|----------|---------------------|--|
| 7       | SIM_SIO  | SIM card data pin   | SIM card DATA signal, I/O signal             |
| 8       | SIM_SCLK | SIM card clock pin  | SIM card clock signal, output by the module  |
| 9       | SIM_SRST | SIM card reset pin  | SIM card reset signal, output by the module  |
| 10      | SIM_DET  | SIM detect pin      | SIM detect pin, input signal                 |
| 11      | VSIM     | VSIM output voltage | VSIM card power supply, output by the module |

## 3.2.2 SIM application

Please note to increase the ESD components on SIM card signal group (PIN number: 7, 8, 9, 11), near the SIM card seat.



In order to meet the requirements of 3GPP TS 27.005 protocol and EMC certification, the proposed SIM card is arranged near the module SIM card interface, and avoid to layout too long resulting in serious waveform distortion, affecting the signal integrity. SIM\_SCLK and SIM\_SIO signals are recommended to be protected. Paralleling a 1uF capacitor between GND and VSIM, that can filter out the interference of radio frequency signals.

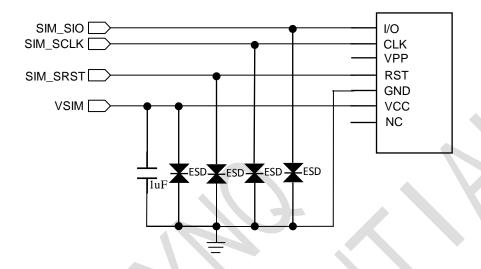


Figure 3-5 SIM Circuit

Note: The capacity value of ESD components should be under 22pF.

#### 3.2.3 eSIM

The eSIM card is reserved inside the module. The eSIM card and external SIM card can only be selected one by one.



Note: The module with the eSIM card is L620E; and the module with the external SIM card is L620.

### 3.3 IIC Interface

L620 module can support a group of IIC interface. When you need to use the IIC interface to communicate, which need external pull-up 4.7K resistor by VIO18.

### 3.4 UART Interface

## 3.4.1 Pin Description

The L620 provides three UART serial communication interfaces: the UART\_Debug can be used as the debug port on the AP of the L620 and can also be used to download software. It is a 2-wire UART interface. UART1 can be used as complete non-synchronous communication interface, supporting standard modem handshake signal control and in compliance with the RS-232 interface protocol, also supporting 4-wire serial bus interface or 2-wire serial bus interface mode. UART2 is used as a debug port on the modem of the L620.

The three groups of UART port support programmable data width, stop bits, and parity bits, with separate TX and RX FIFOs (512 bytes each). The max baud rate of normal application of UART (non-Bluetooth) is 921600bps. UART1 supports adaptive baud rate.

Table 3-2 UART Pin Description

| Pin NO. | Pin Name  | I/O | Function Description       |
|---------|-----------|-----|----------------------------|
| 1       | UART2_TXD | 0   | UART2 transmit data output |
| 2       | UART2_RXD | I   | UART2 receive data input   |



| 17 | UART1_DCD      | DO | UART1 data carrier detect   |
|----|----------------|----|---|
| 18 | UART1_RTS      | DI | UART1 ready to receive  |
| 19 | UART1_RING     | DO | UART1 ring indicator. It can be used as wake out signal to host from module |
| 20 | UART1_DTR      | DI | UART1 Data terminal ready(wake up module)                                   |
| 21 | UART1_CTS      | DO | UART1 clear to send   |
| 22 | UART1_TXD      | 0  | UART1 transmit data output  |
| 23 | UART1_RXD      | I  | UART1 receive data input  |
| 24 | UART_Debug_TXD | 0  | UART_Debug transmit data output   |
| 25 | UART_Debug_RXD | 1  | UART_Debug receive data input   |

## 3.4.2 UART application

If used UART in communication between the module and application processor, and the level is 1.8V, the connection mode is shown in Figure 3-6 and figure 3-7. You can use the complete RS232 mode, 4 wires or 2 wires mode connection. Module interface level is 1.8V. If the AP interface level does not match, you must increase the level conversion circuit.

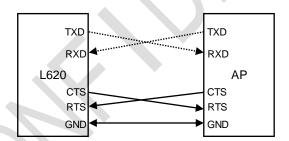


Figure 3-6 Connect to AP method(4lines)



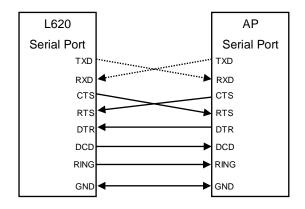


Figure 3-7 Connect to AP method

## 3.5 LED Interface

### 3.5.1 LED Control circuit

NETLIGHT (PIN13) can be used to control the LED status of the network.

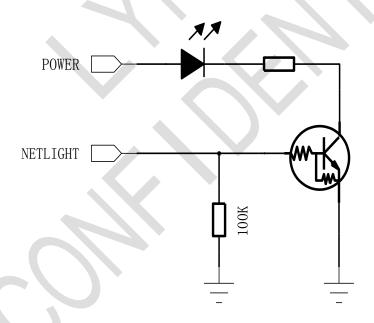


Figure 3-8 LED Circuit

## 3.5.2 LED Status description

NETLIGHT (PIN13) is used as the enable pin. Table 3-3 lists the LED status.



Table 3-3 LED Status

| LED Status                  | Module Status      |
|-----------------------------|--------------------|
| OFF                         | Power off          |
| Cycle 1Hz, duty ratio 50%   | Shut down network  |
| Cycle 0.3Hz, duty ratio 10% | Registered network |
| Cycle 10Hz, duty ratio 50%  | Data Transmit      |

## 3.6 ADC

The module provides an ADC for detecting light-sensitive resistors or other devices that require ADC detection. The Max voltage of ADC is 1.4V with 10-bit accuracy.

Table 3-4 ADC value

| Parameter   | Min. | Тур. | Max. | Unit |
|-------------|------|------|------|------|
| Input range | 0.05 |      | 1.4  | V    |



## 4. Electrical characteristics

## 4.1 Electrical characteristic

Table 4-1 Electrical characteristic

| Power        | Min. | Nom. | Max | Unit |
|--------------|------|------|-----|------|
| VBAT         | 2.1  | 3.3  | 3.6 | V    |
| Peak current | -0.3 |      | 1.0 | A    |

Notes: The over-low voltage can't power on the module; Over-high voltage may be danger to damage the module.

## 4.2 Temperature characteristic

Table 4-2 Temperature characteristic

| State   | Min. | Nom. | Max | Unit          |
|---------|------|------|-----|---------------|
| Working | -40  | 25   | 85  | ${\mathbb C}$ |
| Storage | -45  | 25   | 90  | ${\mathbb C}$ |



Note: When the temperature is over the range, the RF performance may be dropped. It also may cause power down or restart problem.

### 4.3 Absolute Maximum Power

Table 4-3 Absolute maximum power rating

| PIN Name | Description          | Min. | Тур. | Max. Unit |
|----------|----------------------|------|------|-----------|
| VIO18    | Digital power for IO | 1.62 | 1.8  | 1.98 V    |

## 4.4 Recommended operating conditions

Table 4-4 Recommended operating range

| PIN Name | Description          | Min. | Тур. | Max. | Unit |
|----------|----------------------|------|------|------|------|
| VIO18    | Digital power for IO | 1.62 | 1.8  | 1.98 | V    |

Note: All the GPIOs of module are 1.8V.

## 4.5 Power consumption

Table 4-5 Power Consumption

| Parameter      | Conditions | Min. | Average | Max. | Unit |
|----------------|------------|------|---------|------|------|
| Power off mode | VBAT=3.3V  | -    | 3.5     |      | uA   |



| PSM          | VBAT=3.3V   | -        | 3.5 |     | uA |
|--------------|---|----------|-----|-----|----|
| eDRX         | VBAT=3.3V, Value=81.92s, PTW=5.12s, Paging cycle: 1.28s | 150      |     | uA  |    |
| DRX          | VBAT=3.3V, Paging cycle: 1.28s                          | 0.9      |     | mA  |    |
| Wake mode    | VBAT=3.3V   |          | mA  |     |    |
| Band2        | VBAT=3.3V@TX: 22.69dBm                                  |          | mA  |     |    |
| Band5        | VBAT=3.3V@TX: 22.75dBm 144.6                            |          |     |     | mA |
| Band12       | VBAT=3.3V@TX: 22.9dBm                                   | 123.9    |     | mA  |    |
|              | 2.1V≤VBAT < 3.0V<br>VBAT(total bypass cap) < 330uF      | <b>3</b> |     | 1   | A  |
| Peak current | 3.0V≤VBAT≤3.6V<br>VBAT(total bypass cap) <330uF         |          |     | 600 | mA |
|              | 2.1V≤VBAT≤3.6V<br>VBAT(total bypass cap) ≥330uF         |          |     | 600 | mA |

Note: The test value of power consumption is the value tested in laboratory condition.

The power consumption of the L620 is explained as follows:

1. Wake mode (Normal working mode): The module is in normal working mode and all functions are normal. Data can be sent and received. In this mode, the module can switch to DRX/eDRX mode or



PSM mode.

- 2. DRX/eDRX mode: The module is in paging state. In this mode, the module can switch to normal working mode or PSM mode.
- 3. PSM mode: Only RTC of the module is working. In this mode, the module is in a network disconnected state and doesn't receive any network paging. Only when the TAU periodic request timer (T3412) is timeout, or the UE has the MO service to be processed and actively exits, the UE will exit the PSM mode and enter the connected state to process the uplink and downlink services.

## 4.6 Power Sequence

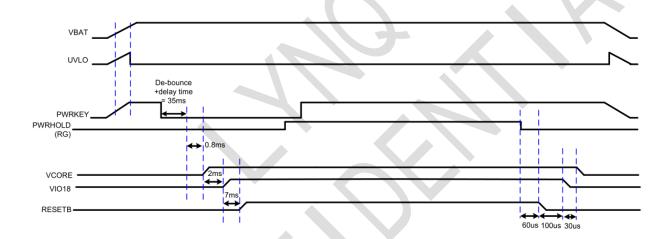


Figure 4-1 Power up time sequence diagram

## 4.7 Digital Interface Characteristics

Table 4-6 Digital IO Voltage

| Parameter | Description              | Min. | Typical | Max. | Unit |
|-----------|--------------------------|------|---------|------|------|
| VIH       | High level input voltage | 1.62 | 1.8     | 1.98 | V    |
| VIL       | Low level input voltage  | 0    | -       | 0.7  | V    |



| VOH | High level output voltage | 1.62 | 1.8 | 1.98 | V |
|-----|---------------------------|------|-----|------|---|
| VOL | Low level output voltage  | 0    | -   | 0.3  | V |

Note: Suit to all GPIOs, IIC, UART interfaces.

#### 4.8 **ESD**

Because there is no special protection against electrostatic discharge in the module, it is necessary to pay attention to the protection of electrostatic protection in the production, assembly and operation module. The performance parameters of the module test are as follows.

ESD parameter (Tem: 25°C, humidity: 45%)

Table 4-7 ESD Performance

| PIN Name | Contact discharge | Air discharge |
|----------|-------------------|---------------|
| VBAT     | ±4KV              | ±8KV          |
| GND      | ±4KV              | ±8KV          |
| RF_ANT   | ±4KV              | ±8KV          |

Enhanced ESD performance method:

- 1. If a converted board is added, it should have enough GND pins and be equally distributed. And the Layout of GND should be enough wide.
- 2 Key (Powerkey, RTC\_EINT key and Reset key) need to add ESD device. Reset key line can't be



near the edge of the board.

- 3. UART and other plug connector need to add ESD devices, and the other control lines from the outside of the machine also need to add ESD devices.
- 4. SIM card should be added ESD protect.
- 5. External antenna, please add ESD device, ESD C<sub>pf</sub><0.5pF.

Notes: For ESD protect, please add ESD methods according to upper ways.

ESD components include varistors and TVS. For better performance, please use

TVS.



## 5. RF Features

## 5.1 RF Main Features

- a) Support 3GPP R13/R14;
- b) Support Single-tone and Multi-tone;
- c) Support PSM and eDRX mode;
- d) Support bands include EUTRA 2/5/12;

The operating frequency range of the product is shown in table 5-1.

Table 5-1 Frequency Band

| Band   | Uplink                   | Downlink                | Note               |
|--------|--------------------------|-------------------------|--------------------|
| Band2  | 1850 MHz $\sim$ 1910 MHz | 1930 MHz $\sim$ 1990MHz |                    |
| Band5  | 824 MHz $\sim$ 849 MHz   | 869 MHz $\sim$ 894 MHz  | CTC/CMCC(optional) |
| Band12 | 699 MHz $\sim$ 716 MHz   | 729 MHz $\sim$ 746 MHz  |                    |



Table 5-2 Output power

| Band   | Max output power | Min output power |
|--------|------------------|------------------|
|        |                  |                  |
| Band2  | 22dBm±2dBm       | < -40dBm         |
| Band5  | 22dBm±2dBm       | < -40dBm         |
| Band12 | 22dBm±2dB        | < -40dBm         |
|        |                  |                  |

| Band   | 200 KHz (CAT NB1)<br>REF SENS<br>(Total) | 200 KHz(CAT<br>NB1)<br>REF SENS<br>(EPRE @15KHz) | 200 KHz(CAT<br>NB1)<br>NB-PDSCH<br>repetitions<br>(Total) | 200 KHz(CAT<br>NB1)<br>NB-PDSCH<br>repetitions<br>(EPRE @15KHz) |
|--------|--|--|---|---|
| Band2  | -117                                     | -126.4   | -129.4  | -139  |
| Band5  | -115                                     | -125.8   | -128.2  | -139  |
| Band12 | -115                                     | -126.1   | -128.6  | -139  |



## 5.2 Data link

Table 5-4 Data link

| Daniel | Single Tone |           | Multi Tone |          |  |
|--------|-------------|-----------|------------|----------|--|
| Band   | Downlink    | Uplink    | Downlink   | Uplink   |  |
| Band2  | 25.5kbps    | 35.35kbps | 25.5kbps   | 58.3kbps |  |
| Band5  | 25.5kbps    | 35.35kbps | 25.5kbps   | 58.3kbps |  |
| Band12 | 25.5kbps    | 35.35kbps | 25.5kbps   | 58.3kbps |  |





## 5.3 Antenna Circuit Design

The connecting part of the RF antenna supports the PAD form. The connection between the module and the main board antenna interface is required to be welded and connected through a microstrip line or a strip line. The microstrip line or strip line is designed according to the characteristic impedance of 50 ohm, and the length of the wire is less than 10mm. Reserved  $\Pi$  matching network.

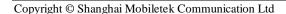




Figure R1, C1, C2 and R2 composition of the antenna matching network for antenna debugging, the default R1, R2 paste 0 ohm resistor and C2, C1 empty paste.

RF Connector in the figure is used for testing and conducting test (for example, CE, FCC, etc.), which need to be placed as close as possible by the module, the RF path from the module to the antenna feed point should be kept 50 ohm impedance control.

This product antenna peripheral circuit design, the proposed RF circuit Layout program: RF line trances top layer, a reference to the second layer. Users need to pay attention to the design of the PCB line: to ensure the RF has full reference GND layer.

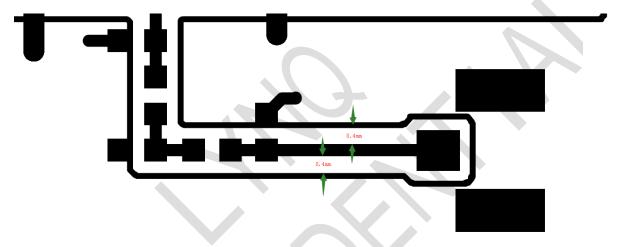


Figure 5-2 RF Trace Design

## 5.4 Antenna Design

PIFA or IFA antenna can be used for inner antenna; Whip antenna can be used for external antenna. The antenna gain must more than 3dBi. The recommend area of inner antenna: 100mm\*10mm\*6mm (L\*W\*H), the main board length no less than 90mm. The antenna should be as far as possible from the chip and memory, power interface, data cable interface, camera FPC, screen FPC, connector FPC, and other possible EMI modules and devices.



Table 5-5 Antenna Specifications

| Parameter    |             | Specification       |                             |
|--------------|-------------|---------------------|-----------------------------|
| Efficiency   |             | >40%                |                             |
| S11/VSWR     |             | <-10dB              |                             |
| Polarization |             | linear polarization |                             |
| TRP          | Low Band    | >18dBm              |                             |
|              | Middle Band | >18dBm              |                             |
| TIS          | Low Band    | <-107dBm            | (Total without repetitions) |
|              | Middle Band | <-107dBm            | (Total without repetitions) |
| Low Band     |             | Band 5/12           |                             |
| Middle Band  |             | Band 2              |                             |



## Storage and Production

## 6.1 Storage

The rank of moisture proof of the module is level 3. There is an obvious sign on the table of the internal and the external packaging.

In the vacuum sealed bag, the module can be stored for 180 days when the temperature is below 40°C and the humidity is below 90% under good air circulation.

Humidity level is descripted detail as follows:

Table 6-1 Humidity level

| Rank | Factory Environment ≤ +30°C /60%RH                   |  |
|------|--|--|
| 1    | No controll < 30°C /85%RH                            |  |
| 2    | One year   |  |
| 2a   | 4 weeks  |  |
| 3    | 168 hours  |  |
| 4    | 72 hours   |  |
| 5    | 48 hours   |  |
| 5a   | 24 hours   |  |
| 6    | Baking before using, SMT during the time table signs |  |

Notes: Moving, storage, production of module must meet the demand of IPC/JEDEC J-STD-033.

### 6.2 Production

The module is a humidity sensitive device. If the device needs reflow soldering, disassembly and



maintenance, we must strictly comply with the requirements of humidity sensitive device. If module is damp, a reflow soldering or using a hot-air gun maintenance will lead to internal damage, because the water vapor has the rapid expansion of the burst, causing physical injury to the device, like PCB foaming and BGA component fail. So customers should refer to the following recommendations.

#### 6.2.1 Module confirmation and moisture

The module in the production and packaging process should be strictly accordance with the humidity sensitive device operation. The factory packaging is vacuum bag, desiccant, and humidity indicator card. Please pay attention to the moisture control before SMT and the confirmation of the following aspects.

## **Demand of Baking confirmation**

Smart module uses vacuum sealed bag, which can make it stored for 6 months under the condition of temp 30°C and humidity < 60%. The module should be baked before reflowing soldering if any of the conditions below happen.

- 1. Storage exceeds the time limit.
- 2. Package damages and vacuum bags have air leakage.
- Humidity indicating card change the color at 10%.
- 4. Module is placed naked in the air over 168 hours.
- 5. Module is placed naked in the air under 168 hours but not temp 30°C and humidity < 60%.

#### **Baking condition confirmation**

The moisture proof level of the smart module is level 3. And the baking conditions are as follows.

Table 6-2 Baking conditions



| Baking conditions | 120°C / 5%RH              | 40°C / 5%RH               |
|-------------------|---------------------------|---------------------------|
| Baking time       | 4 hours                   | 30 days                   |
| Description       | not use the original tray | Can use the original tray |

(2

Notes: The original anti-ESD tray temperature does not exceed 50°C. Otherwise the tray will be deformed.

The anti-ESD tray of the original packaging is only used for packaging, and can't be used as a SMT tray.

During taking and placing, please take notes of ESD and cannot be placed as overlay.

## **Customer product maintenance**

If maintenance module after SMT, it is easy for damp module to damage when removing, so the module disassembly and other related maintenance operations should complete within 48 hours after SMT, or need to bake and then maintenance the module.

Because the module return from the field work can't ensure the dry state, it must be baked in accordance with the conditions of baking, then for disassembly and maintenance. If it has been exposed to the humid environment for a long time, please properly extend the baking time, such as 125°C /36 hours.

#### 6.2.2 SMT reflow attentions

The module has the BGA chips, chip resistances and capacitances internally, which will melt at high temperature. If module melt completely encountered a large shock, such as excessive vibration of reflux conveyor belt or hit the board, internal components will easily shift or be false welding. So, using intelligent modules over the furnace need to pay attention to:

Modules can't be vibrate larger, namely customer requirements as far as possible in orbit (chain)



furnace, furnace, avoid on the barbed wire furnace, in order to ensure smooth furnace.

 The highest temperature can't too high. In the condition that meet the welding quality of customer motherboard and module, the lower furnace temperature and the shorter maximum temperature time, the better.

Some customer's temperature curve in the line is not suitable, high temperature is too high, and customer motherboard melt good, but non-performing rate is on the high side. Through the analysis of the causes, it found that melt again of BGA components lead device offset and short circuit. After adjusting the temperature curve, it can ensure that the customer's motherboard the welding quality, and also improve the pass through rate. Non-performing rate is controlled below the 2/10000.

#### 6.2.3 SMT stencil design and the problem of less tin soldering

Part of customers found false welding or circuit short when reflowing. The main reason is module tin less, PCB distortion or tins too large. Suggestions are as follows:

- Suggest use ladder stencil, which means the depth of the region of module is thicker than other
  areas. Please adjust validation according to the measured thickness of solder paste, the actual
  company conditions and experience value. The products need to strictly test.
- Stencil: Reference module package, and the user can adjust according to their company experience; Outside of the module, the stencil extends outside. The GND pads use the net stencil.

#### 6.2.4 SMT attentions

If customer motherboard is thin and slender with a furnace deformation, warping risks, you will be suggested to create "a furnace vehicle" to ensure the welding quality. Other production proposals are as follows:

The solder pastes use brands like Alfa.



- The module must use the SMT machine mount (important), and do not recommend manually placed or manual welding.
- For SMT quality, Please ensure the necessary condition according to actual condition of factory before SMT, like SMT pressure, speed (very important), stencil ways.
- We must use the reflow oven more than 8 temperature zones, and strictly control the furnace temperature curve.

Recommended temperature:

- B. constant temperature zone: temperature 140-190°C, time: 60s-120s.
- E. recirculation zone: PEAK temperature 235-250°C, time over 220°C: 45s-75s.

Notes: customer's board deformation must be controlled well. By reducing the number of imposition or increasing patch clamp to reduce the deformation.

Module thickness of the stencil is recommended to be thickened, and the rest position can be maintained by 0.1mm.

#### FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment . This equipment should be installed and operated with minimum distance 20cm between the radiator your body.

#### ISED RF exposure statement:

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance 20cm between the radiator your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. Le rayonnement de la classe b repecte ISED fixaient un environnement non contrôlés. Installation et mise en œuvre de ce matériel devrait avec échangeur distance minimale entre 20 cm ton corps. Lanceurs ou ne peuvent pas coexister cette antenne ou capteurs avec d'autres.

#### End Product Labeling:

The outside of final products that contains this

module device must display a label referring to the enclosed module. This exterior label can use wording such as: "Contains Transmitter Module FCC ID:2AK9DL620/IC:24342-L620 or "Contains FCC ID:2AK9DLL620/IC:24342-L620 , Any similar wording that expresses the same meaning may be used.

Étiquetage du produit final

L'extérieur des produits finaux qui contient cette.Le module doit afficher une étiquette faisant référence au module ci-joint. Cette étiquette extérieure peut utiliser un libellé tel que: "Contient le module émetteur FCC ID:2AK9DL620/IC:24342-L620 ,Contient FCC ID:2AK9DL620/IC:24342-L620 RTout libellé similaire qui exprime la même signification peut être utilisé .

Single Modular Approval. Output power is conducted. This device is to be used in mobile or fixed applications only. Antenna gain including cable loss must not exceed 9.0 dBi @ Band 2 , 10.41 dBi @ Band 5 and 9.69 dBi @ Band 12 for the purpose of satisfying the requirements of CFR 47 2.1043 & 2.1091. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operated in conjunction with any antenna or transmitter, except in accordance with FCC multi-transmitter evaluation procedure. Compliance of this device in all final product configurations is the responsibility of the Grantee. Installation of this device into specific final products may require the submission of a Class II permissive change application containing data pertinent to RF Exposure, spurious emissions, ERP/EIRP, and Q • Q [ å | ^ authentication, or new application if appropriate.

For IC, to meet RF exposure & ERP/ERIP, the maximum net gain of antennas allowed are 9.5 dBi @ NB-IoT(Band 2), 9.08 dBi @ NB-IoT (Band 5) and 7.21 dBi @ NB-IoT (Band 12). The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.