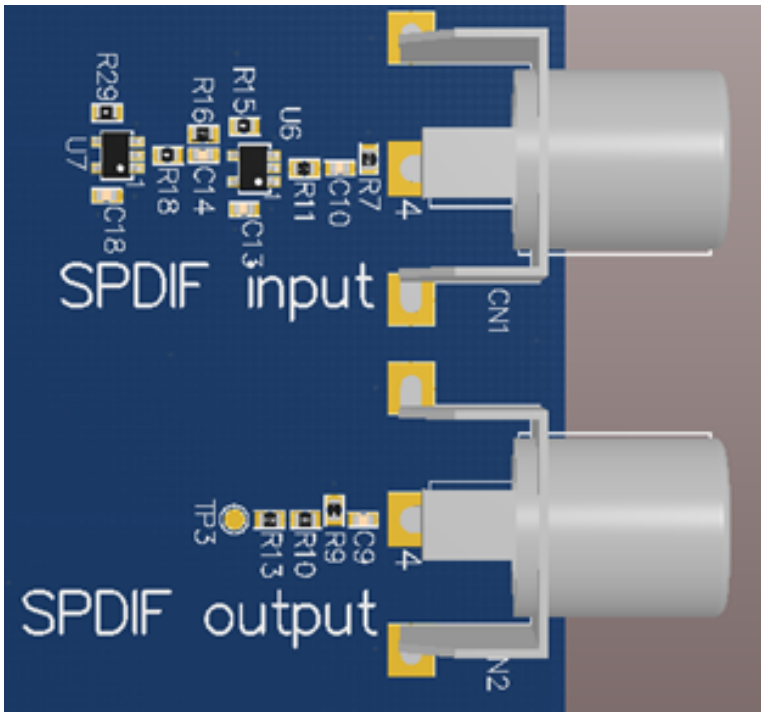
Figure 14. **SPDIF input MB1262/CN1 and output MB1262/CN2 connectors**



6.15.6 IO restriction to other features

Due to the share of some IO of STM32MP157xAA3 by multiple peripherals, the following limitations apply in using the audio features:

The SAI AUDIO CODEC must not be operated simultaneously with expansion connector MB1262/CN21.
The MEMS DFSDM must not be operated simultaneously with DFSDM of EXT MEMS module MB1262/CN8.

6.16 DSI LCD

Through the MB1262/CN19 connector, a DSI LCD mounted on a daughterboard MB1230 is provided. MB1230 is a 5.5" TFT 720*1280 pixels with LED backlight, MIPI® DSI interface and capacitive touch panel based on RK055AHD042-CT module embedding the LCD driver IC RM68200 and a touch screen controller GT9147.

3V3 and VIN supply MB1230:

- 3V3: for the LCD module (VDD_LCD and VIO_LCD) and Touch screen
- VIN: for the LED backlight of the LCD

6.16.1 DSI LCD interface

MB1230 is connected to the STM32MP157xAA3 through the DSI interface, I2C to control the GT9147, and LCD_BL_CTRL. LCD_INT signal is connected to MFX.

The I2C is I2C2 that is shared with all the peripherals: audio codec, MFX, RGB LTDC, camera, and USB hub. The GT9147 I^2C address is 0xBB.

Table 23 describes the IO configuration for the LCD interface.

Table 23. **IO configuration for the LCD interface**

IO	Configuration
PH4	I2C2_SCL
PH5	I2C2_SDA
DSI_D0P	DSI_D0_P is used as MIPI-DSI data Lane 0 positive
DSI_D0N	DSI_D0_N is used as MIPI-DSI data Lane 0 negative

IO	Configuration
DSI_D1P	DSI_D1_P is used as MIPI-DSI data Lane 1 positive
DSI_D1N	DSI_D1_N is used as MIPI-DSI data Lane 0 negative
DSI_CKP	DSI_CKP is used as clock Lane positive
DSI_DKN	DSI_DKN is used as clock Lane negative
PD13	LCD_BL_CTRL – Backlight Control
PF15	DSI_RESET
PC6	DSI_TE – Tearing Effect
MFX_IO14	LCD_INT - interruption

6.17 Camera

Through the MB1262/CN7 connector, a camera module mounted on a daughterboard MB1379 is provided. MB1379 is a 5 Mpixels, 8-bit color camera module based on OV5640 image sensor, clocked from a 24 MHz crystal (MB1379/X1). It is supplied by 2V8.

6.17.1 Camera interface

MB1379 is connected to the STM32MP157xAA3 through DCMI and I^2C interfaces. RSTI, XSDN, PLUG signals are connected to MFX.

The I2C is I2C2 that is shared with all the peripherals: audio codec, MFX, RGB LTDC, DSI LCD, and USB hub. The camera I²C address is 0x3C.

Table 24 describes the IO configuration for the camera interface.

Table 24. IO configuration for the camera interface

IO	Configuration
PH4	I2C2_SCL
PH5	I2C2_SDA
PH9	DCMI_D0
PH10	DCMI_D1
PH11	DCMI_D2
PH12	DCMI_D3
PH14	DCMI_D4
PI4	DCMI_D5
PB8	DCMI_D6
PE6	DCMI_D7
PI1	DCMI_D8(1)
PH7	DCMI_D9(1)
PI3	DCMI_D10(1)
PH15	DCMI_D11(1)
PB7	DCMI_VSYNC
PH8	DCMI_HSYNC
PA6	DCMI_PIXCLK
MFX_IO12	Camera PLUG detection
MFX_O3	RSTI - Camera RESETB, active low

IO	Configuration
MFX_O2	XSDN – Camera PWDN, active high

1. *Available on the MB1262/CN7 connector, but not used in the MB1379 module*

6.18 1 Gbps Ethernet

The STM32MP157x-EV1 board provides a 1 Gbps Ethernet feature thanks to an external physical interface device (PHY), RTL8211EG-VB-CG. This PHY is connected to the STM32MP157xAA3 Gigabit reduced medium-independent interface (RGMII), and is clocked from a 25 MHz Crystal (X1).

The Ethernet PHY is supplied by 3V3. It generates its own supply 1V05 and Digital/Analog 3V3.

LD1 LED is blinking to indicate the data transmission.

The Ethernet module connector MB1262/CN6 is for STMicroelectronics internal use only.

6.18.1 RGMII interface

Table 25 describes the IO configuration for the Ethernet interface.

Table 25. IO configuration for the Ethernet interface

IO	Configuration
PD10	PD10 (SUB_NRST) is used as PHY_NRST active Low
PA2	PA2 is used as ETH_MDIO
PG0	PG0 is used as ETH_MDINT
PC1	PB11 is used as ETH_MDC
PA7	PA7 is used as ETH_RX_DV(PHY_AD2)
PC4	PC4 is used as ETH_RXD0
PC5	PC5 is used as ETH_RXD1
PB0	PB0 is used as ETH_RXD2
PB1	PB1 is used as ETH_RXD3
PB11	PB11 is used as ETH_TX_EN
PG13	PG13 is used as ETH_TXD0
PG14	PG14 is used as ETH_TXD1
PC2	PB11 is used as ETH_TXD2
PE2	PE2 is used as ETH_TXD3
PA1	PA1 is used as ETH_RX_CLK
PG4	PG4 is used as ETH_GTX_CLK
PG5	PG5 is used as ETH_CLK125

Figure 15. **Ethernet connector MB1262/CN3**

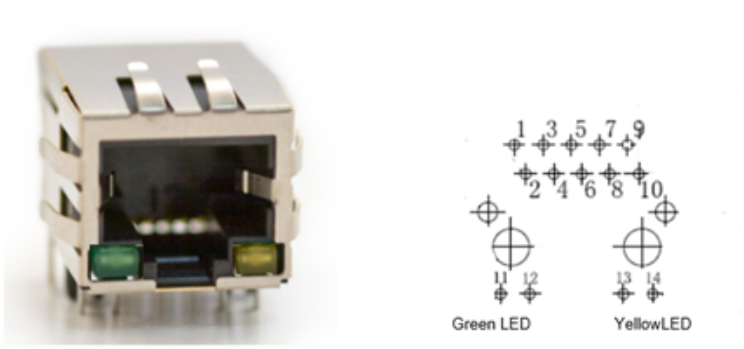


Table 26. **Ethernet connector pinout MB1262/CN3**

Pin number	Pin name	Function
1	TX1+	First Bidirectional pair to transmit and receive data
2	TX1-	
3	TX2+	Second Bidirectional pair to transmit and receive data
4	TX2-	
5	CT1	Common connected to GND
6	CT2	Common connected to GND
7	TX3+	Third Bidirectional pair to transmit and receive data
8	TX3-	
9	TX4+	Fourth Bidirectional pair to transmit and receive data
10	TX4-	
11	GA	Green Led anode
12	GC	Green Led cathode
13	YA	Yellow Led anode
14	YC	Yellow Led cathode
15	GND	GND
16	GND	GND

6.19 USB OTG HS

The STM32MP157x-EV1 board supports USB OTG high speed communication via a USB Micro-AB connector MB1262/CN16. OTG VBUS supply is managed by the STPMIC1. MB1262/LD2 turns green when USB OTG connection is established.

6.19.1 USB OTG interface

Table 27 describes the IO configuration for the USB OTG interface.

Table 27. **IO configuration for the USB OTG interface**

IO	Configuration
PA10	**OTG_ID line detection**
OTG_VBUS	**OTG_VBUS sensing**

IO	Configuration
USB_DP2	USB_DP2
USB_DM2	USB_DM2

Figure 16. USB OTG Type Micro-AB connector MB1262/CN16

Table 28. USB OTG Type Micro-AB connector pinout MB1262/CN16

Pin CN16	Pin name	Signal name	Function
1	**VBUS**	OTG VBUS	VBUS supply and sensing
2	**D-**	DM	USB_DM2
3	**D+**	DP	USB_DP2
4	**ID**	ID	ID
5	**GND**	VBUS	GND

6.20 USB host

The STM32MP157x-EV1 board provides 4 USB host port (2 dual USB Type A connectors MB1262/CN18 and CN20) thanks to a USB hub USB2514B-AEZC. The USB2514B have a full power management for each USB host port. The default configuration of USB2514B is done in HW, thus I2C is not needed by default. However, if required for a specification application, I2C may be accessed through MB1262/SB71 and SB68 to I2C2 as described in Table 29.

6.20.1 USB host interface

Table 29 describes the IO configuration for the USB host interface.

Table 29. IO configuration for the USB Host interface

IO	SB	Setting	Configuration(1)
PH5	MB1262/SB71	**OFF**	**PH5 is not used as I2C2_SDA**
PH4	MB1262/SB68	**OFF**	**PH4 is not used as I2C2_SCL**
PD10	-	-	SUB_NRST
USB_DP1	-	-	USB1_P
USB_DM1	-	-	USB1_N

1. *Default configuration in **bold***

Figure 17. **Dual USB TYPE A connector MB1262/CN18 and CN20**

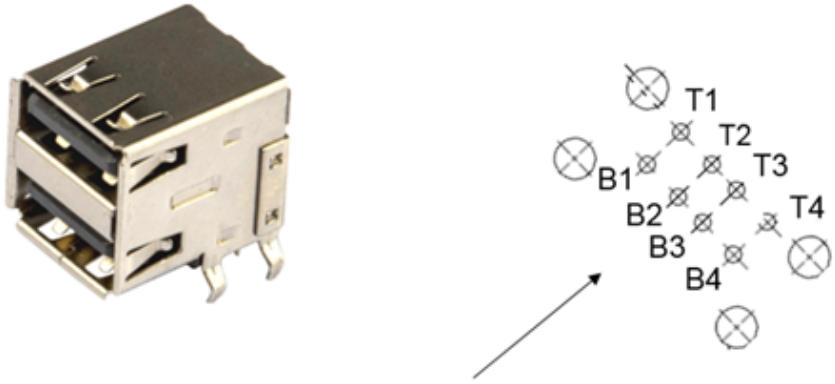


Table 30. **USB Host connector pinout MB1262/CN18**

Pin CN18	Pin name	Function
T1	**T1**	VBUS
T2	**T2**	DM
T3	**T3**	DP
T4	**T4**	GND
B1	**B1**	VBUS
B2	**B2**	DM
B3	**B3**	DP
B4	**B4**	GND

Table 31. **USB Host connector pinout MB1262/CN20**

Pin CN20	Pin name	Function
T1	**T1**	VBUS
T2	**T2**	DM
T3	**T3**	DP
T4	**T4**	GND
B1	**B1**	VBUS
B2	**B2**	DM
B3	**B3**	DP
B4	**B4**	GND

6.21 RS-232 port

The STM32MP157x-EV1 board offers one RS-232 communication port. The RS-232 communication port uses the DB9 male connector MB1262/CN12.

6.21.1 RS-232 interface

The RS-232 transceiver MB1262/U12 supply is 3V3. The RS-232 interface is connected to the STM32MP157xAA3 UART4 that is shared exclusively with the USB micro-B/ST-LINK v2-1 VCP as described in Table 32.

Table 32. HW configuration for the RS-232 interface

Jumpers	IO	Setting	Configuration(1)
MB1263/JP4	UART4_TX	**JP4[1-2]**	**connected to RS232 CN12**
		JP4[2-3]	Connected to ST-Link V2-1 VCP RX
MB1263/JP5	UART4_RX	**JP5[1-2]**	**connected to RS232 CN12**
		JP5[2-3]	Connected to ST-Link V2-1 VCP TX

1. *Default configuration in **bold***

Figure 18. HW configuration for the RS-232 interface

Figure 19. RS-232 connector pinout MB1262/CN12

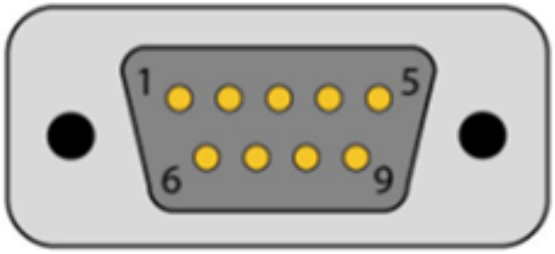


Table 33 RS-232 connector pinout MB1262/CN12

Table 33. RS-232 connector pinout MB1262/CN12

Board function	Pin	Pin	Board function
NC	**1**	**6**	DSR
RXD	**2**	**7**	NC
TXD	**3**	**8**	CTS

Board function	Pin	Pin	Board function
NC	**4**	**9**	NC
GND	**5**	-	

6.21.2 IO restriction to other features

The RS-232 must not be operated simultaneously with the STLINK-VCP.

6.22 FDCAN

The STM32MP157x-EV1 board supports one FDCAN compliant with ISO-11898-1 version 2.0 part A, B. The MB1262/CN15 DB9 male connector is available as FDCAN interface.

6.22.1 Operating voltage

A 5V/3v3 IO compliant high speed FDCAN transceiver is fitted between the MB1262/CN15 connector and the CAN controller port of STM32MP157xAA3.

6.22.2 FDCAN interface

Table 34 describes the IO for the CAN interface.

Table 34. IO configuration for the SDIO interface

IO	Signal
PG3	CAN_STBY
PH13	CAN_TX
PI9	CAN_RX

Figure 20 shows the FDCAN connector pinout MB1262/CN15.

Figure 20. FDCAN connector pinout CN15

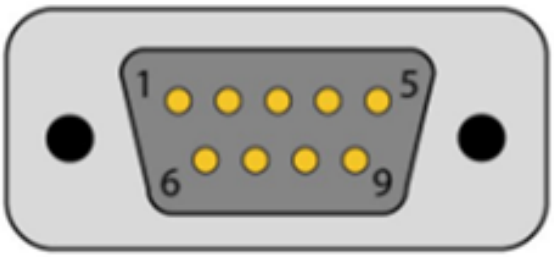


Table 35 describes the FDCAN interface and connector pinout CN17.

Table 35. FDCAN interface and connector pinout CN17

CAN transceiver	Board function	Pin	Pin	Board function	CAN transceiver
-	NC	**1**	**6**	GND	-
CANL	CANL	**2**	**7**	CANH	CANH
GND	GND	**3**	**8**	NC	-
-	NC	**4**	**9**	NC	-
-	GND	**5**	-		

6.23 Smartcard

The STM32MP157x-EV1 board supports one Smartcard interface. The MB1262/CN23 Smartcard connector is used as card reader.

6.23.1 Smartcard interface

A 3V3 Smartcard interface MB1262/U5 is used between the card reader connector MB1262/CN23 and the Smartcard controller port of STM32MP157xAA3.

The Smartcard interface is connected for some IO to the STM32MP157xAA3 and for other IO to the MFX IO expander.

Table 36. HW configuration for the Smartcard interface

IO	Configuration
PZ7	PZ7 is connected to Smartcard interface as SMARTCARD_IO
PZ6	PZ6 is connected to Smartcard interface as SMARTCARD_CLK
MFX_IO6	MFX_IO6 used as SMARTCARD_3/5V
MFX_IO7	MFX_IO7 used as SMARTCARD_OFF
MFX_IO8	MFX_IO8 used as SMARTCARD_RST
MFX_IO9	MFX_IO9 used as SMARTCARD_CMDVCC

Figure 21. Smartcard connector pinout MB1262/CN23

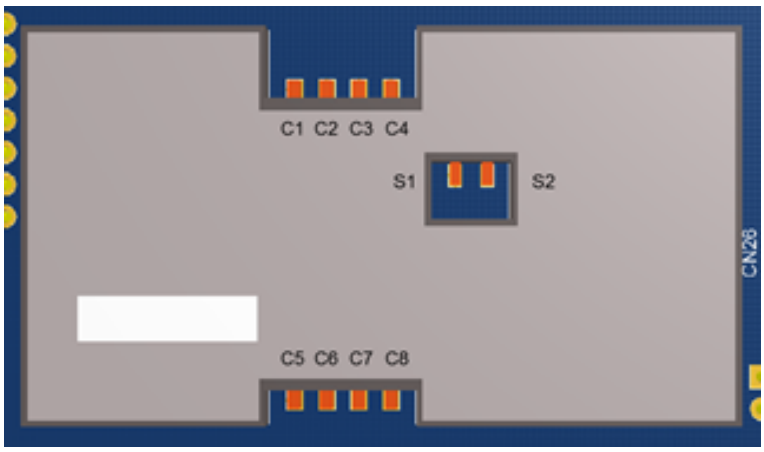


Table 37 describes the Smartcard interface MB1262/U5 and connector pinout MB1262/CN23.

Table 37. Smartcard interface MB1262/U5 and connector pinout MB1262/CN23

Pin	Board function	U5 Smartcard interface pin
C1	VCC: Card supply	U5-17
C2	RST: Card Reset	U5-16
C3	CLK: Card CLK	U5-15
C4	NC	U5-13
C5	GND: CARD GND	U5-14
C6	SWIO	-

Pin	Board function	U5 Smartcard interface pin
C7	I/O CARD DATA	U5-11
C8	NC	U5-12
S1	GND: CAR GND	GND
S2	DETECT: CARD-Detect (LOW)	U5-9

6.24 ADC/DAC

The STM32MP157x-EV1 provides some on-board analog-to-digital converters ADC and digital-to-analog converters DAC:

- 2x ADC/DAC
- 2x Fast ADC
- 1x Slow ADC

6.24.1 ADC/DAC IO interface

The STM32MP157xAA3 port PA4 may be configured to operate either as ADC input or as DAC output. PA4 is routed to two-way headers MB1263/JP11, to fetch signals to or from MB1263/JP11, or grounded it by fitting a jumper into MB1263/JP11. Same situation for PA5 and its related MB1263/JP10 header.

Parameters of the ADC/DAC low-pass filters formed with MB1263/R24, C31, R19 for PA4 and MB1263/R25, C32, R20 for PA5 may be modified by replacing these components according to application requirements (Default configuration is: R24/R19/R25/R20=0 Ohm, C31/C32 not fitted).

6.24.2 Fast ADC

ANA0 may be configured as a fast ADC channel routed to MB1263/JP8. MB1263/SB6, closed by default, should be opened.

ANA1 may be configured as a fast ADC channel routed to MB1263/JP9. MB1263/SB7, closed by default, must be opened.

Parameters of the low-pass filters formed with MB1263/R22, C29, and R17 for ANA0 and MB1263/R23, C30 and R18 for ANA1 may be modified by replacing these components according to application requirements (Default configuration is: R22/R17/R23/R18=0 Ohm, C29/C30 not fitted).

6.24.3 Slow ADC

The port PF12 may be configured as slow ADC channel, routed to MB1263/JP7. MB1263/SB5, closed by default, must be opened.

Parameters of the low-pass filters formed with MB1263/R21, C28, and R16 may be modified to application requirements (Default configuration is R21/R16=0 Ohm, C28 not fitted).

The VREF+ terminal of STM32MP157xAA3 is used as reference voltage for both ADC and DAC. By default, it is connected on board to VDDA through MB1263/R96, which may be removed to apply directly an external voltage to VREF+ for specific purposes.

Figure 22 ADC/DAC connectors MB1263/JP7, JP8, JP9, JP10, and JP11

Figure 22. ADC/DAC connectors MB1263/JP7, JP8, JP9, JP10, and JP11

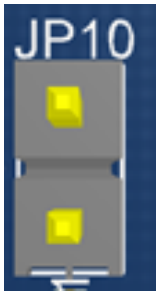


Table 38. **ADC/DAC connectors JP7/JP8/JP9/JP10/JP11 pinout**

Signal name	Pin	Pin	Signal name
ADC/DAC	**1**	**2**	GND

6.24.4 Limitations

Due to the share of some IO of STM32MP157xAA3 by multiple peripherals, the following limitations apply in using the PMOD Button features:

The fast ADC ANA0/ANA1 and slow ADC PF12 may not be operated simultaneously with motor control function.

6.25 I2C_EXT connector

I2C_EXT connector MB1262/CN13 may be connected to I²C bus daughterboard. CN13 connector pin 5 is connected to 3V3, so external module must be compliant with 3V3.

MFX_GPIO0 of MFX MCU provides EXT_RESET.

6.25.1 I2C_EXT IO interface

Table 39. **HW configuration for the I2C_EXT interface**

IO	Bridge	Setting[1]	Comment
PA11	MB1262/ SB51	**ON**	**PA11 ,used as I2C5_SCL, is connected to EXT_SCL**
		OFF	PA11 is not connected to EXT_SCL PA11 may be connected to the GPIO expansion connector through MB1262/ SB52
PA12	MB1262/ SB54	**ON**	**PA12 ,used as I2C5_SDA, is connected to EXT_SDA**
		OFF	PA12 is not connected to EXT_SDA PA12 may be connected to the GPIO expansion connector through MB1262/ SB55
MFX_GPIO0	-	-	**Connected to EXT_RESET**

1. *Default configuration is shown in **bold***

Figure 23 shows the I2C_EXT connector pinout MB1262/CN13.

Figure 23. **I2C_EXT connector pinout MB1262/CN13**

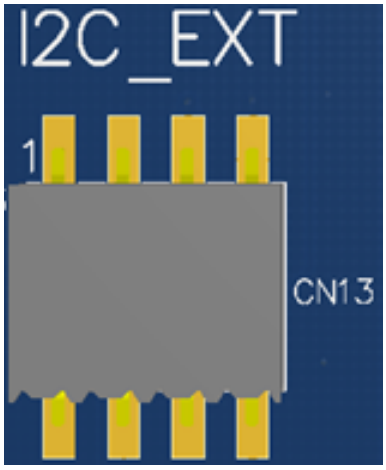


Table 40 describes the I2C_EXT connector pinout MB1262/CN13.

Table 40. **I2C_EXT connector pinout MB1262/CN13**

Signal name	Pin	Pin	Signal name
EXT_SDA	**1**	**2**	NC
EXT_SCL	**3**	**4**	EXT_RST
3V3	**5**	**6**	NC
GND	**7**	**8**	NC

6.26 MFX MCU

The MFX: Multi-Function eXpander MCU is used as a GPIO expander, in position MB1262/U20.

6.26.1 MFX IO expander

Supplied by 3V3.

The communication interface between MFX and STM32MP157xAA3 is I2C bus, and an IRQOUT pin.

The I2C is I2C2 that is shared with all the peripherals: Audio codec, DSI LCD, RGB LTDC, Camera, and USB Hub.

The MFX I²C address is 0x42h.

Table 41. **HW configuration for the MFX interface**

IO	SB	Setting	Configuration(1)
PI8	R127	**ON**	**MFX_IRQ_OUT is connected to PI8**
PH5	R124	**ON**	**PH5 is used as I2C2_SDA**
PH4	R125	**ON**	**PH4 is used as I2C2_SCL**
PD10	-	-	SUB_NRST

1. *Default configuration in **bold***

Table 42. **IO signals driven by the MFX**

Pin number	Pin name	Signal name	Function
18	GPIO0	JOY_CENTER	MB1262/B1 Joystick selection
19	GPIO1	JOY_DOWN	MB1262/B1 Joystick down direction
20	GPIO2	JOY_LEFT	MB1262/B1 Joystick left direction
39	GPIO3	JOY_RIGHT	MB1262/B1 Joystick right direction
40	GPIO4	JOY_UP	MB1262/B1 Joystick up direction
15	GPIO5	Audio_INT	MB1262/U8 audio codec interrupt
16	GPIO6	SMARTCARD_3V/5V	MB1262/U5 Smart card 3 V 5 V selection
17	GPIO7	SMARTCARD_OFF	MB1262/U5 Smart Card OFF
29	GPIO8	SMARTCARD_RST	MB1262/U5 Smart Card RESET
30	GPIO9	SMARTCARD_CMDVCC	MB1262/U5 smartcard VCC command
31	GPIO10	MIC_MEMS_LED	MB1262/CN8 pin12
32	GPIO11	-	-
33	GPIO12	CAMERA_PLUG	Camera plug detection
26	GPIO13	-	-
27	GPIO14	LCD_INT	DSI or LTDC interrupt

Pin number	Pin name	Signal name	Function
28	GPIO15	-	-

6.27 Motor control

The STM32MP157x-EV1 board supports both asynchronous and synchronous 3-phase brushless motor control via a 34-pin connector MB1262/CN22, which provides all required control and feedback signals, to and from motor power-driving board.

Available signals on this connector includes emergency stop, motor speed, 3-phase motor current, bus voltage, heatsink temperature coming from the motor driving board and 6 channels of PWM control signal (MC-xH/L) going to the motor driving circuit.

6.27.1 Motor control IO interface

Because of IO consuming limitation, the motor control IO interface is not enabled by default. As described below, some board modifications are needed to connect the motor control interface.

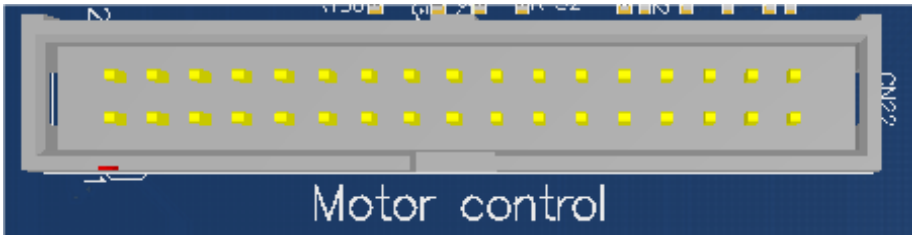
Table 43 describes the assignment of the MB1262/CN22 motor control interface and the IO function associated from the STM32MP157xAA3.

Table 43. Motor control terminal and IO function assignment

Motor Control connector CN22		STM32MP157xAA3 microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board configurations to enable Motor Control
1	Emergency Stop	PA6	TIM8_BKIN	DCMI_PIXCLK	Close MB1262/SB22
2	GND	-	-	-	-
3	MC_UH	PI5	TIM8_CH1	SAI_2_SCK_A	Close MB1262/SB67 Open MB1262/SB9 and SB66
4	GND	-	-	-	-
5	MC_UL	PH13	TIM8_CH1N	CAN_1_TX	Close MB1262/SB76
6	GND	-	-	-	-
7	MC_VH	PI6	TIM8_CH2	SAI_2_SD_A	Close MB1262/SB75 Open MB1262/SB10 and SB73
8	GND	-	-	-	-
9	MC_VL	PH14	TIM8_CH2N	DCMI_D4	Close MB1262/SB21
10	GND	-	-	-	-
11	MC_WH	PI7	TIM8_CH3	SAI_2_FS_A	Close MB1262/SB65 Open MB1262/SB11 and SB63
12	GND	-	-	-	-
13	MC_WL	PH15	TIM8_CH3N	DCMI_D11	Close MB1262/SB33
14	Bus Voltage	PA3	ADC_1_IN15	GPIO6_TIM2_CH4	Close MB1262/SB14
15	PhaseA current	PF12	ADC_1_IN6	-	Close MB1262/SB20
16	GND	-	-	-	-
17	PhaseB current	ANA0	ADC_1_IN0	ADC_2_IN0	Close MB1262/SB12
18	GND	-	-	-	-
19	PhaseC current	ANA1	ADC_2_IN1	-	Close MB1262/SB13
20	GND	-	-	-	-
21	NTC Bypass	PF3	GPIO	GPIO7	Close MB1262/SB19

Motor Control connector CN22		STM32MP157xAA3 microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board configurations to enable Motor Control
22	GND	-	-	-	-
23	Dissipative Brake	PH6	TIM12_CH1	GPIO12_TIM12_CH1	Close MB1262/SB29
24	GND	-	-	-	-
25	5V	-	-	-	-
26	Heatsink Temp.	PF11	ADC_1_IN2	SAI_2_SD_B	Close MB1262/SB70 Open MB1262/SB8 and SB69
27	PFC Sync	PE0	TIM4_ETR	SAI_2_MCLK_A	Close MB1262/SB53 Open MB1262/SB7
28	3V3	-	-	-	-
29	PFC PWM	PB8	TIM4_CH3	DCMI_D6	Close MB1262/SB24
30	GND	-	-	-	-
31	Encoder A	PH10	TIM5_CH1	DCMI_D1	Close MB1262/SB28
32	GND	-	-	-	-
33	Encoder B	PH11	TIM5_CH2	DCMI_D2	Close MB1262/SB30
34	Encoder Index	PH12	TIM5_CH3	DCMI_D3	Close MB1262/SB26

Figure 24. Motor control connector MB1262/CN22



6.27.2 Limitations

Due to the share of some IO of STM32MP157xAA3 by multiple peripherals, the following limitations apply in using the Motor control features:

The Motor control may not be operated simultaneously with the camera, audio Codec, CAN and GPIO expansion (GPIO6, 7 and 12).

6.28 GPIO 40-pin expansion connector

A 2x20-pin, 2.54 mm, GPIO connector is implemented on MB1262/CN21.

28 pins are GPIO, 8 are GND, 2x 5V DC and 2x 3V3 DC are provided on this connector.

This GPIO 40-pin expansion connector has a Raspberry Pi shields support capability.

Figure 25. MB1262/CN21 connector

Please note the pin1 position that is on the bottom right on MB1262/CN21.

Table 44 describes the MB1262/CN21 connector pinout.

Table 44. MB1262/CN21 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
-	3V3	**1**	**2**	5V	-
PA12	I2C5_SDA	**3**	**4**	5V	-
PA11	I2C5_SCL	**5**	**6**	GND	-
PI11	MCO1	**7**	**8**	USART3_TX	PB10
-	GND	**9**	**10**	USART3_RX	PB12
PG8	USART3_RTS	**11**	**12**	SAI2_SCKA	PI5
PD7	SDMMC3_D3	**13**	**14**	GND	GND
PG15	SDMMC3_CK	**15**	**16**	SDMMC3_CMD	PF1
-	3V3	**17**	**18**	SDMMC3_D0	PF0
PZ2	SPI1_MOSI	**19**	**20**	GND	GND
PZ1	SPI1_MISO	**21**	**22**	SDMMC3_D1	PF4
PZ0	SPI1_SCK	**23**	**24**	SPI1_NSS	PZ3
-	GND	**25**	**26**	GPIO	-
PH5	I2C2_SDA	**27**	**28**	I2C2_SCL	PH4
PG2	MCO2	**29**	**30**	GND	-
PA3	TIM2_CH4	**31**	**32**	TIM12_CH1	PH6
PI2	TIM8_CH4	**33**	**34**	GND	-
PI7	SAI2_FSA	**35**	**36**	USART3_CTS	PI10
PF5	SDMMC3_D2	**37**	**38**	SAI2_SDA	PI6
-	GND	**39**	**40**	SAI2_SDB	PF11

SAI2 on the GPIO connector supports PCM signals. SAI2 is shared between the audio codec and this GPIO expansion connector. By default, SAI2 is connected to the audio codec. I2C5 is connected by default to the I2C_EXT connector.

The following HW board modifications are needed to enable SAI2 and I2C5 on the GPIO expansion connector, as described in Table 45.

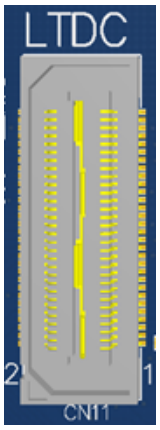
Table 45. HW configurations to enable SAI2 on the GPIO connector

STM32 pin	Board function	Board modifications to enable SAI2 on the GPIO connector
PI5	SAI2_SCKA	Open MB1262/SB9 and SB67. Close MB1262/SB66
PI7	SAI2_FSA	Open MB1262/SB11 and SB65. Close MB1262/SB63
PI6	SAI2_SDA	Open MB1262/SB10 and SB75. Close MB1262/SB73
PF11	SAI2_SDB	Open MB1262/SB8 and SB70. Close MB1262/SB69
PA12	I2C5_SDA	Open MB1262/SB54. Close MB1262/SB55
PA11	I2C5_SCL	Open MB1262/SB51. Close MB1262/SB52

6.29 RGB LTDC connector

A 2x30-pin RGB LTDC connector is implemented on MB1262/CN11.

Figure 26. MB1262/CN11 connector



A 24-bit RGB interface, LCD control signals (INT, Backlight BL_CTRL, LCD_RESET, I2C), HDMI_CEC and SPDIF_TX are available as described in the connector pinout Section 6.29 .

Table 46. MB1262/CN21 connector pinout

IO	Board function	Pin	Pin	Board function	IO
PK7	LTDC_DE	**1**	**2**	LTDC_R7	PJ6
-	-	**3**	**4**	LCD_INT	MFX_IO14
-	-	**5**	**6**	LTDC_B7	PK6
PJ4	LTDC_R5	**7**	**8**	-	-
PI12	LTDC_HSYNC	**9**	**10**	LTDC_VSYNC	PI13
-	-	**11**	**12**	-	-
MFX_O1	HDMI_PD	**13**	**14**	LTDC_R0	PI15
-	-	**15**	**16**	-	-
PJ0	LTDC_R1	**17**	**18**	LTDC_R2	PJ1
-	-	**19**	**20**	-	-
PJ2	LTDC_R3	**21**	**22**	LTDC_R4	PJ3
PK0	LTDC_G5	**23**	**24**	LTDC_G6	PK1
PJ4	LTDC_R5	**25**	**26**	LTDC_R6	PJ5
PK3	LTDC_B4	**27**	**28**	LTDC_B5	PK4
PJ6	LTDC_R7	**29**	**30**	LTDC_G0	PJ7
PK5	LTDC_B6	**31**	**32**	-	-
PJ8	LTDC_G1	**33**	**34**	LTDC_G2	PJ9
-	-	**35**	**36**	-	-
PJ10	LTDC_G3	**37**	**38**	LTDC_G4	PJ11
PJ12	LTDC_B0	**39**	**40**	LTDC_B1	PJ13
PJ14	LTDC_B2	**41**	**42**	LTDC_B3	PJ15
-	-	**43**	**44**	-	-

IO	Board function	Pin	Pin	Board function	IO
-	-	**45**	**46**	LCD_RESET (SUB_NRST)	PD10
-	3V3	**47**	**48**	5V	-
PK2	LTDC_G7	**49**	**50**	GND	-
PA15	HDMI_CEC	**51**	**52**	-	-
PH4	I2C2_SCL	**53**	**54**	SPDIF_TX	PB5
PH5	I2C2_SDA	**55**	**56**	GND	-
-	LCD_BL_CTRL	**57**	**58**	LTDC_CLK	PI14
-	-	**59**	**60**	GND	-

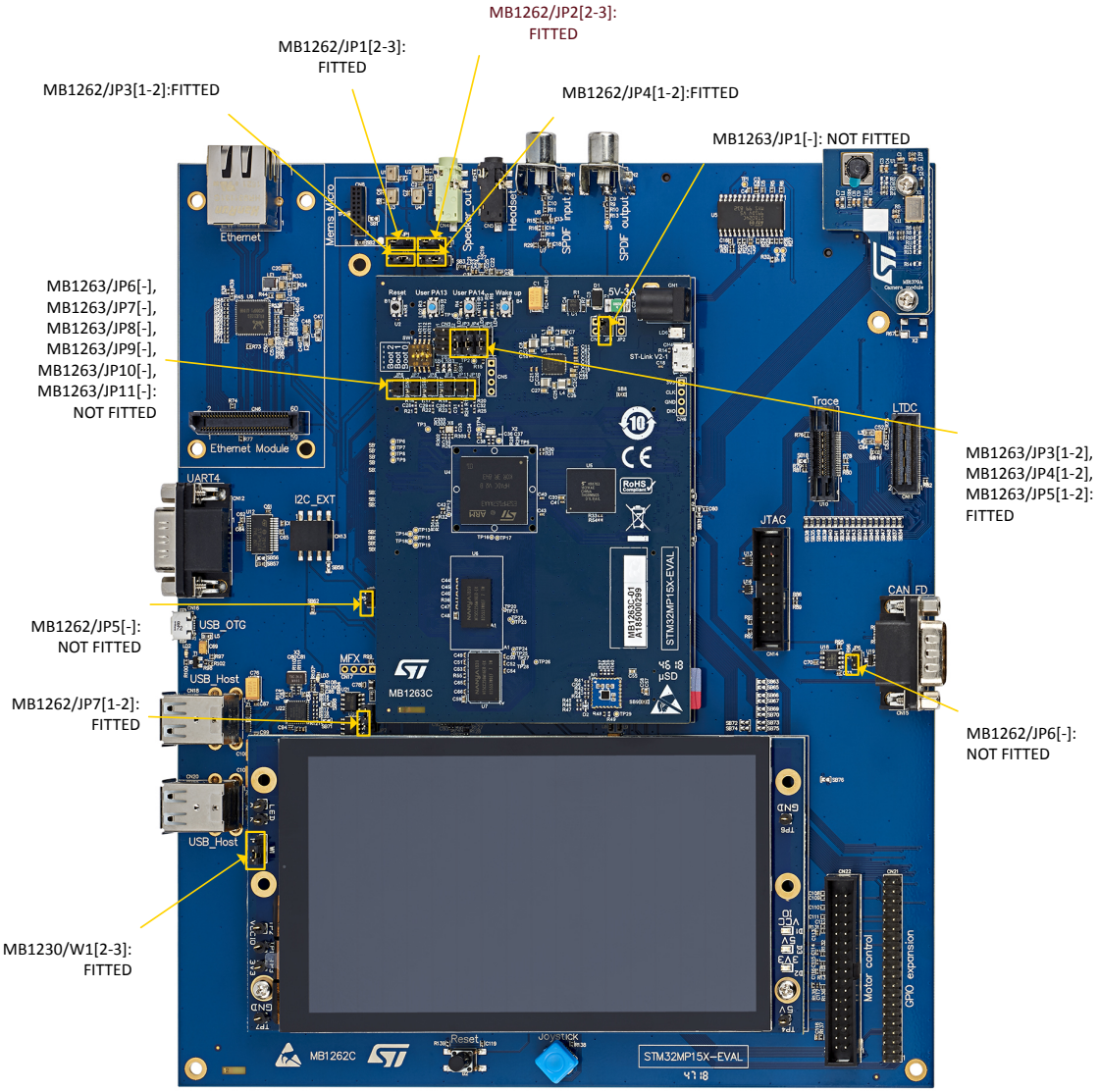
6.29.1 Limitations

LCD_INT, LCD_BL_CTRL are shared exclusively with the DSI.

Appendix A STM32MP157x-EV1 jumper summary

Figure 27 summarizes the jumper default setting of the STM32MP157x-EV1.

Figure 27. Jumper default setting of the STM32MP157x-EV1



Appendix B STM32MP157x-EV1 I/O Assignment

Table 47. **STM32MP157x-EV1 I/O Assignment**

LFBGA448 ball	IO Port	Main function	Motor Control connector
AA3	PA0	WAKE_UP	-
V4	PA1	ETH_RX_CLK	-
AB2	PA2	ETH_MDIO	-
T4	PA3	TIM2_CH4	Bus Voltage
V6	PA4	ADC1_IN18_DACOUT1	-
U5	PA5	ADC1_IN19_DACOUT2	-
W9	PA6	DCMI_PIXCLK	Emergency Stop
Y9	PA7	ETH_RX_DV	-
B13	PA8	SDMMC2_D4	-
A11	PA9	SDMMC2_D5	-
Y17	PA10	OTG_ID	-
Y16	PA11	I2C5_SCL	-
W16	PA12	I2C5_SDA	-
W3	PA13	PA13 GPIO	-
R3	PA14	PA14 GPIO	-
E11	PA15	HDMI_CEC	-
AB5	PB0	ETH_RXD2	-
AA5	PB1	ETH_RXD3	-
V13	PB2	UART4_RX	-
A12	PB3	SDMMC2_D2	-
C13	PB4	SDMMC2_D3	-
AA8	PB5	SPDIF_TX	-
W13	PB6	QSPI_BK1_NCS	-
F11	PB7	DCMI_VSYNC	-
AB8	PB8	DCMI_D6	PFC PWM
F12	PB9	SDMMC1_CDIR	-
V9	PB10	USART3_TX	-
Y5	PB11	ETH_TX_EN	-
AA7	PB12	USART3_RX	-
V10	PB13	DFSDM_CKOUT	-
A13	PB14	SDMMC2_D0	-
B12	PB15	SDMMC2_D1	-
U10	PC0	QSPI_BK2_NCS	-
AB3	PC1	ETH_MDC	-
Y1	PC2	ETH_TXD2	-
U3	PC3	DFSDM_DATA1	-
AB6	PC4	ETH_RXD0	-

LFBGA448 ball	IO Port	Main function	Motor Control connector
AA6	PC5	ETH_RXD1	-
E13	PC6	DSI_TE	-
D13	PC7	SDMMC1_D123DIR	-
E14	PC8	SDMMC1_D0	-
D14	PC9	SDMMC1_D1	-
F14	PC10	SDMMC1_D2	-
D15	PC11	SDMMC1_D3	-
E12	PC12	SDMMC1_CK	-
N2	PC13	PMIC_WAKEUP	-
P1	PC14	LSE_IN	-
P2	PC15	LSE_OUT	-
C10	PD0	NAND_D2	-
B10	PD1	NAND_D3	-
D12	PD2	SDMMC1_CMD	-
B11	PD3	SDMMC2_D123DIR	-
C9	PD4	NAND_NOE	-
A9	PD5	NAND_NWE	-
L3	PD6	NAND_NWAIT	-
F10	PD7	SDMMC3_D3	-
M1	PD8	NAND_D13	-
M2	PD9	NAND_D14	-
A8	PD10	NAND_D15	-
AB9	PD11	NAND_CLE	-
W12	PD12	NAND_ALE	-
V14	PD13	LCD_BL_CTRL	-
M3	PD14	NAND_D0	-
L1	PD15	NAND_D1	-
C5	PE0	SAI2_MCLKA	PFC Sync
D7	PE1	-	-
Y2	PE2	ETH_TXD3	-
A10	PE3	SDMMC2_CK	-
F15	PE4	SDMMC1_CKIN	-
C12	PE5	SDMMC2_D6	-
E9	PE6	DCMI_D7	-
W10	PE7	NAND_D4	-
Y12	PE8	NAND_D5	-
W11	PE9	NAND_D6	-
W14	PE10	NAND_D7	-
D5	PE11	uSD_LS_EN	-
E4	PE12	SAI2_SCKB	-

LFBGA448 ball	IO Port	Main function	Motor Control connector
A4	PE13	SAI2_FSB	-
B4	PE14	SAI2_MCLKB	-
C4	PE15	-	-
E10	PF0	SDMMC3_D0	-
B9	PF1	SDMMC3_CMD	-
F13	PF2	SDMMC1_D0DIR	-
V3	PF3	GPIO	NTC Bypass
F9	PF4	SDMMC3_D1	-
D9	PF5	SDMMC3_D2	-
AA11	PF6	QSPI_BK1_IO3	-
AA10	PF7	QSPI_BK1_IO2	-
AB10	PF8	QSPI_BK1_IO0	-
AB11	PF9	QSPI_BK1_IO1	-
V12	PF10	QSPI_CLK	-
W8	PF11	SAI_2_SDB	Heatsink Temp.
V8	PF12	SLOW ADC	PhaseA current
W7	PF13	DFSDM_DATA3	-
V7	PF14	uSD_LDO_SEL	-
W6	PF15	DSI_RESET	-
W5	PG0	ETH_MDINT	-
Y4	PG1	uSD_DETECT	-
W4	PG2	MCO2	-
U4	PG3	CAN_STBY	-
AB4	PG4	ETH_GTX_CLK	-
U8	PG5	ETH_CLK125	-
D11	PG6	SDMMC2_CMD	-
Y11	PG7	QSPI_BK2_IO3	-
Y8	PG8	USART3_RTS	-
W15	PG9	NAND_NCE	-
AA9	PG10	QSPI_BK2_IO2	-
U11	PG11	UART4_TX	-
J4	PG12	SPDIF_RX	-
AA1	PG13	ETH_TXD0	-
AA2	PG14	ETH_TXD1	-
D10	PG15	SDMMC3_CK	-
T1	PH0	HSE_IN	-
T2	PH1	HSE_OUT	-
AB7	PH2	QSPI_BK2_IO0	-
Y6	PH3	QSPI_BK2_IO1	-
A3	PH4	I2C2_SCL	-

LFBGA448 ball	IO Port	Main function	Motor Control connector
A2	PH5	I2C2_SDA	-
V11	PH6	TIM12_CH1	Dissipative Brake
W2	PH7	DCMI_D9	-
D6	PH8	DCMI_HSYNC	-
E6	PH9	DCMI_D0	-
B1	PH10	DCMI_D1	Encoder A
B3	PH11	DCMI_D2	Encoder B
F5	PH12	DCMI_D3	Encoder Index
D3	PH13	CAN_TX	MC_UL
C2	PH14	DCMI_D4	MC_VL
C1	PH15	DCMI_D11	MC_WL
D1	PI0	-	-
E2	PI1	DCMI_D8	-
E1	PI2	TIM8_CH4	-
E3	PI3	DCMI_D10	-
J6	PI4	DCMI_D5	-
F2	PI5	SAI2_SCKA	MC_UH
G5	PI6	SAI2_SDA	MC_VH
F1	PI7	SAI2_FSA	MC_WH
N1	PI8	MFX_IRQ_OUT	-
J5	PI9	CAN_RX	-
W1	PI10	USART3_CTS	-
T3	PI11	MCO1	-
H2	PI12	LTDC_HSYNC	TRACE_D0
H1	PI13	LTDC_VSYNC	TRACE_D1
D2	PI14	LTDC_CLK	TRACE_CLK
F3	PI15	LTDC_R0	-
J2	PJ0	LTDC_R1	TRACE_D8
L6	PJ1	LTDC_R2	TRACE_D9
K4	PJ2	LTDC_R3	TRACE_D10
J1	PJ3	LTDC_R4	TRACE_D11
K2	PJ4	LTDC_R5	TRACE_D12
K1	PJ5	LTDC_R6	TRACE_D2
L5	PJ6	LTDC_R7	TRACE_D3
L4	PJ7	LTDC_G0	TRACE_D13
H6	PJ8	LTDC_G1	TRACE_D14
L2	PJ9	LTDC_G2	TRACE_D15
J3	PJ10	LTDC_G3	-
K6	PJ11	LTDC_G4	-
B8	PJ12	LTDC_B0	-

LFBGA448 ball	IO Port	Main function	Motor Control connector
A7	PJ13	LTDC_B1	-
B7	PJ14	LTDC_B2	-
C7	PJ15	LTDC_B3	-
D8	PK0	LTDC_G5	-
E7	PK1	LTDC_G6	TRACE_D4
E8	PK2	LTDC_G7	TRACE_D5
B6	PK3	LTDC_B4	-
A6	PK4	LTDC_B5	-
C6	PK5	LTDC_B6	TRACE_D6
A5	PK6	LTDC_B7	TRACE_D7
B5	PK7	LTDC_DE	-
G2	PZ0	SPI1_SCK	-
H5	PZ1	SPI1_MISO	-
K5	PZ2	SPI1_MOSI	-
F4	PZ3	SPI1_NSS	-
G1	PZ4	I2C4_SCL	-
H4	PZ5	I2C4_SDA	-
G3	PZ6	SMARTCARD_CLK	-
H3	PZ7	SMARTCARD_IO	-

Appendix C Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

C.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC ID

FCC ID: YCP-MB1263-000.

C.2 IC Compliance Statement

This device complies with FCC and Industry Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

Compliance Statement

Notice: This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A)/NMB-3(A).

Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'Industrie Canada: CAN ICES-3 (A)/NMB-3(A).

Appendix D CE conformity

D.1 Warning

EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

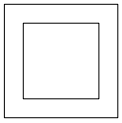
D.2 Simplified declaration of conformity

Hereby, STMicroelectronics declares that the radio equipment types STM32MP157A-EV1 and STM32MP157C-EV1 are in compliance with Directive 2014/53/EU.

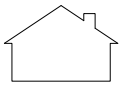
Appendix E Safety instructions

E.1 Safety instructions

- The STM32MP157x-EV1 Evaluation board is designed to be powered from the 5 V DC power supply unit provided in the package. The power supply acting as a disconnection device must remain easily accessible in case of issue.
- Marking observed on the power supply unit:

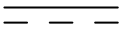


Marking for Class II product. Such product does not require a safety connection to electrical earth.



For indoor use only.

This marking indicates that the product operates with an alternating current (AC) source (mains). It is completed by afferent values (voltage, frequency and max current).



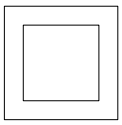
This marking indicates that the terminal is suitable for direct current (DC) only. It is completed by afferent values (voltage and max current).

The associated symbol means that WEEE and waste batteries must not be thrown away but collected separately and recycled.

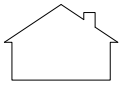
- Do not expose it to heat from any source.
- Do not expose it to water, moisture or place on a conductive surface while in operation.

E.2 Sicherheitshinweise

- Das Evaluierungsboard STM32MP157x-EV1 ist ausgelegt für den Betrieb mit dem im Lieferumfang enthaltenen 5V DC Netzteil. Das Netzteil muss frei zugänglich sein damit es jederzeit im Fall einer Gefahr oder einer Störung vom Netz getrennt werden kann.
- Kennzeichnung am Netzteil beachtet:

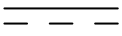


Kennzeichnung für Produkte der Klasse II. Für ein solches Produkt ist keine Erdung erforderlich.



Nur für den Innengebrauch.

Diese Markierung zeigt an, dass das Produkt nur mit einer Wechselspannung (Netz) betrieben werden darf.



Diese Markierung zeigt an, dass das Terminal nur für Gleichstrom (DC) geeignet ist. Das Netzteil versorgt das Terminal mit der angepassten Spannung.

Das zugehörige Symbol bedeutet, dass Elektro- und Elektronik-Altgeräte nicht weggeworfen, sondern getrennt gesammelt und recycelt werden müssen.

- Setzen Sie es keiner Wärmequelle aus.
- Setzen Sie es während des Betriebs weder Wasser noch Feuchtigkeit aus und legen Sie es nicht auf eine leitfähige Oberfläche.

Revision history

Table 48. **Document revision history**

Date	Version	Changes
20-Feb-2019	1	Initial release.
22-Aug-2019	2	Added certification appendices Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements, CE conformity, and Safety instructions.

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