Thundercomm

Thundercomm TurboX™ T95 SOM DATASHEET

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Revision History

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1.0	Sep 24, 2020	First release

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1 Overview

1.1 TurboX™ T95SOM Module Abstract

The T95 SOM (System On Module) is based on new generation of LTE Modem and purpose-built for the low power wide area Internet of Things (IoT) applications. It integrates all key innovations required to build cellular-enabled IoT products and services into a single module, including 3GPP Rel. 14 compliant LTE Cat M1/Cat NB2, E-GPRS connectivity, an ARM Cortex A7 application processor, integrated GNSS, hardware-based security, capable of cloud services, and rich set of development tools.

With a cost-effective LGA form factor of 19 mm × 16 mm × 2.2 mm and high integration level, T95 enables users to easily design their applications and take advantage from the module' s low power consumption and mechanical intensity. Comparing with its last generation, the T95 SOM reduces power consumption by about 70%, BOM cost by about 50% and total chipset size by about 50%. The T95 SOM is ideal for battery-powered IoT devices to keep nearly 10 years or longer in the IoT applications.

1.2 Reference Documents

Document
80-pl045-1 MDM9205 data sheet
80-pl045-41 MDM9205 + PME9205 + WCD9306 reference schematics
80-pj934-42 SDR105 with integrated PA+ASM CatM1, NB1 and GSM reference schematic
80-pj934-43 SDR105 with external PA for CatM1, NB1, and GSM reference schematic
80-pj600-1 PME9205 power management data sheet
80-pj934-1 SDR105 device specification

1.3 Terms and Acronyms

Acronym/Terminology	Description
ADC	Analog-to-digital converter
BER	Bit error rate
BLSP	BAM-based low-speed peripheral
GPIO	General Purpose Input/output
GNSS	Global navigation satellite system
LCD	Liquid crystal display
PMIC	Power Management Integrated Circuit
OSC	Oscillator
PA	Power amplifier
PCB	Printed circuit board
PCM	Pulse-coded modulation
PM	Power management
PWM	Pulse width modulation
SDC	Secure digital controller
SDRAM	Synchronous dynamic random access memory
SPI	Serial peripheral interface
SPMI	Serial power management interface
TCXO	Temperature-compensated crystal oscillator
SoC	System on Chip
XTAL	Crystal
SDIO	Secure Digital Input / Output
UART	Universal Asynchronous Receiver Transmitter
USB	Universal serial bus
I2S	Inter-IC Sound
I2C	Inter-integrated circuit
WCN	Wireless connectivity network
WLAN	Wireless local area network
SMPS	Switched-mode power supply
SOM	System On Module

2 TurboX™ T95 SOM Introduction

2.1 Key features

The following table shows the key features and performance of TurboX™ T95 SOM.

Applications Processor	ARM Cortex-A7@800 MHz 256KB L2 cache
Modem processing	Integrated Qualcomm® Hexagon™ DSP to support CatM1, CatNB1/CatNB2, Low-power audio supported in the modem system 512 KB L2 cache
RPM processor	Cortex-M3 up to 100 MHz
Operating System	ThreadX
Internal memory	Internally DRAM:32 MB/Internally Flash:64MB
External memory	EBI1—connected to internal DRAM
Display support	General display interfaces: DBI
Audio	Primary and Secondary I2S/PCM/TDM
RF transceiver	SDR105-integrated RF transceiver One multiplexed Tx and Rx interface with MDM
WAN air interfaces	LTE: Rel 14 Cat-M1 Rel 14 Cat-NB2
GNSS-Qualcomm Location services engine	Gen 9 VT with support for GPS, GLONASS, Beidou, Galileo and QZSS systems
USB	one USB 2.0 high-speed device only
BLSP	Can be configured as 4x SPI or 4x I2C or 4x UART
UART	up to 4 MHz
I2C	up to 1 MHz
SPI	up to 50MHz(master) up to 25MHz(slave)
USIM	One UIM single voltage 1.8V
USB	One USB 2.0 with build-in PHY only device mode
MI2S	Two MI2S/PCM/TDM ports

Misc	Support for 2x PWM
GPIO	57 GPIO ports
Digital die	28nm
Small thermally efficient package	177 PSP 5.9 x 6.2 x 0.98 mm 0.4mm pitch
ADC Interface	Support ADC interfaces used for input voltage sense, battery temperature detection and general purpose ADC
Physical size	Size: 19mm x 16mm x 2.3mm Weight: approx.1.8g LGA Form Factor
Voltage Range	3.3~4.3V, Typ. 3.8V
Working temperature	Operational:-30ºC ~ 75ºC(TBD) Storage: -40ºC ~ 85ºC
RoHS	All hardware components are fully compliant with EU RoHS directive

2.2 Hardware Block Diagram

N/A

3 Interfaces Description

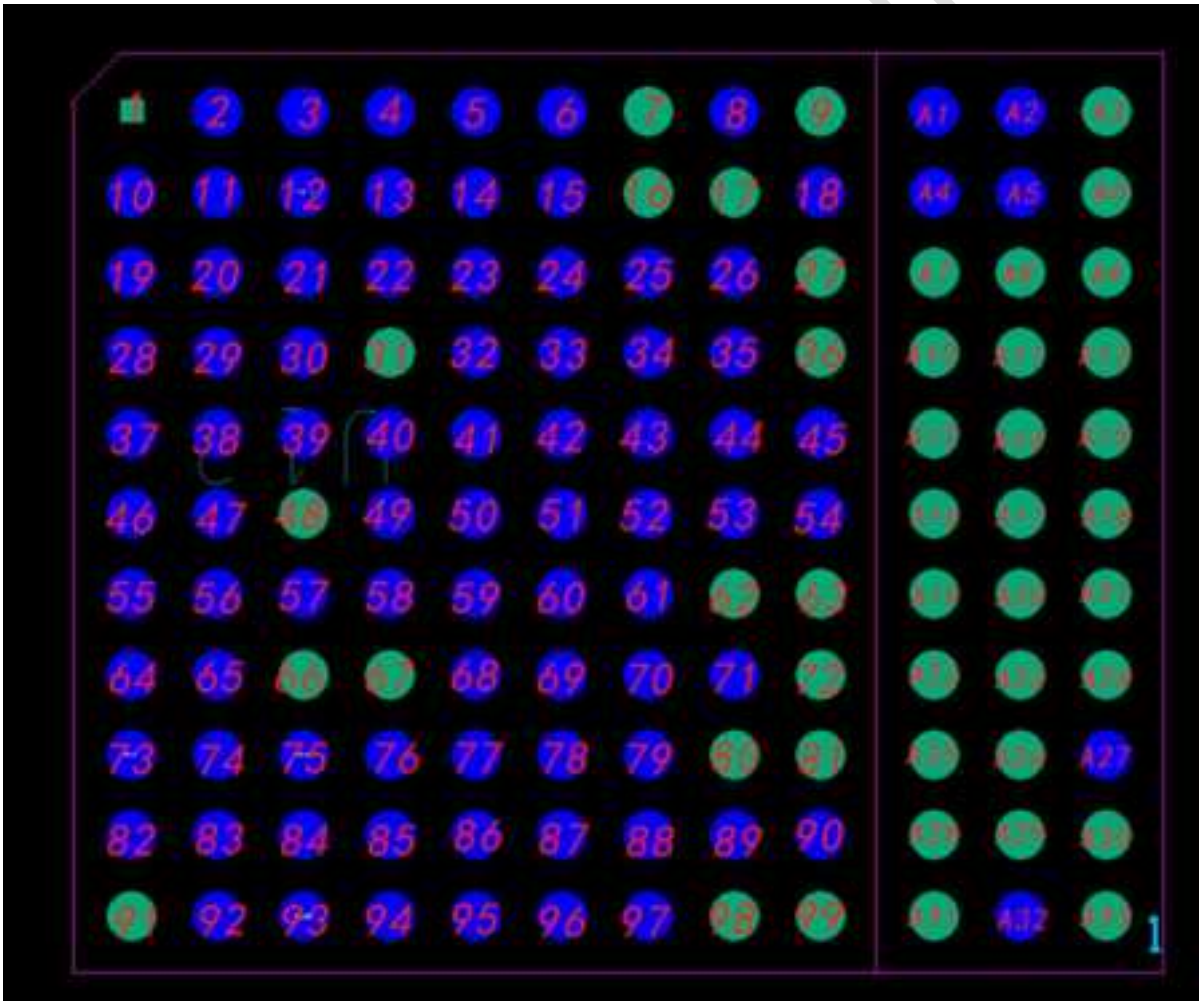
This chapter introduces all the interfaces definition to guide developer for easy-to-design and verifications.

3.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
DI	Digital input(CMOS)
DO	Digital output(CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z)output.
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters

	and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
PX_1	EBI Power group 1，it is 1.2V.
PX_3	Most peripherals Power group 3，it is 1.8V.

3.2 Pin Description



Pad#	Function	Voltage	Type	Function description
1	GND			

2	RCM_MARKER	1.8V	IO	MDM9205 GPIO28, Can be configured as GPIO
3	VREG_L7	1.8V	PO	Low voltage switch supply output 1.8V for SIM voltage;
4	VREG_L5	1.8V	PO	Low voltage switch supply output 1.8V for IO voltage;
5	VREG_S2	2.15V	PO	SMPS supply output 2.15V for LDO L7 input voltage
6	VPH_PWR	4.2V	PI	Power supply in for SOM system operations
7	GND			
8	NC			Do not connect
9	GND			
10	BLSP2_UART_TX	1.8V	IO	MDM9205 GPIO4, Can be configured as GPIO
11	BLSP2_UART_RX	1.8V	IO	MDM9205 GPIO5, Can be configured as GPIO
12	PON_1	1.8V	DI	Level-high triggered power-on input
13	VBUS_DET	1.8V	IO	PM9205 GPIO_01, Can be configured as GPIO
14	VREG_S2	2.15V	PO	SMPS supply output 2.15V for LDO L7 input voltage
15	VPH_PWR	4.2V	PI	Power supply in for SOM system operations
16	GND			
17	GND			
18	NC			Do not connect
19	BLSP2_I2C_SDA	1.8V	IO	MDM9205 GPIO6, Can be configured as GPIO
20	BLSP2_I2C_SCL	1.8V	IO	MDM9205 GPIO7, Can be configured as GPIO
21	SENSOR2_INT	1.8V	IO	MDM9205 GPIO27, Can be configured as GPIO
22	KPDPWR_N	1.8V	DI	Power-on trigger, level trigger (active low)
23	PMIC_GPIO2	1.8V	MV	PME9205 GPIO_02, Can be configured as GPIO
24	VPH_PWR	4.2V	PI	Power supply in for SOM system operations
25	EBI2_AD_1	1.8V	IO	MDM9205 GPIO32, Can be configured as GPIO
26	EBI2_AD_0	1.8V	IO	MDM9205 GPIO31, Can be configured as GPIO
27	GND			
28	USB_HS_VDDA_3P3	3.3V	PI	Power supply in for MDM9205 USB PHY 3.3V input
29	SENSOR1_INT	1.8V	IO	MDM9205 GPIO26, Can be configured as GPIO
30	BATT_THERM		AI	Battery temperature thermistor
31	GND			
32	SLEEP_CLK	2.1		SLEEP CLK output for modem IC and others.
33	PS_HOLD	1.8V	IO	Power supply hold control input
34	EBI2_AD_2	1.8V	IO	MDM9205 GPIO33, Can be configured as GPIO
35	EBI2_AD_3	1.8V	IO	MDM9205 GPIO34, Can be configured as GPIO
36	GND			
37	EXT_BOB_3V3_EN	1.8V	IO	MDM9205 GPIO20, Can be configured as GPIO
38	USB2_HS_DM	1.8V	IO	USB High-Speed Data-Minus

39	BATT_ID		AI	Battery ID detection
40	UIM_RST	1.8V	IO	MDM9205 GPIO18, Can be configured as GPIO
41	UIM_CLK	1.8V	IO	MDM9205 GPIO17, Can be configured as GPIO
42	EBI2_AD_4	1.8V	IO	MDM9205 GPIO35, Can be configured as GPIO
43	EBI2_AD_5	1.8V	IO	MDM9205 GPIO36, Can be configured as GPIO
44	EBI2_AD_6	1.8V	IO	MDM9205 GPIO37, Can be configured as GPIO
45	VREG_L6	1.8V	PO	Low voltage switch supply output 1.8V for GPS LNA voltage
46	EXT_USB_PWR_EN	1.8V	IO	MDM9205 GPIO29, Can be configured as GPIO
47	USB2_HS_DP	1.8V	IO	USB High-Speed Data-Plus
48	GND			
49	UIM_DATA	1.8V	IO	MDM9205 GPIO16, Can be configured as GPIO
50	UIM_PRESENT	1.8V	IO	MDM9205 GPIO19, Can be configured as GPIO
51	EBI2_AD_7	1.8V	IO	MDM9205 GPIO38, Can be configured as GPIO
52	EBI2_AD_8	1.8V	IO	MDM9205 GPIO51, Can be configured as GPIO
53	LCD_TE	1.8V	IO	MDM9205 GPIO46, Can be configured as GPIO
54	VREG_L6	1.8V	PO	Low voltage switch supply output 1.8V for GPS LNA voltage
55	CHAR_INT	1.8V	IO	MDM9205 GPIO30, Can be configured as GPIO
56	BLSP3_SPI_CLK	1.8V	IO	MDM9205 GPIO11, Can be configured as GPIO
57	BLSP3_SPI_CS_N	1.8V	IO	MDM9205 GPIO10, Can be configured as GPIO
58	RESOUT_N			Power-on reset control
59	LCD_CS_N	1.8V	IO	MDM9205 GPIO45, Can be configured as GPIO
60	RESETIN	1.8V	IO	PME9205 Power-on reset output signal (active low),
61	LCD_EN	1.8V	IO	MDM9205 GPIO47, Can be configured as GPIO
62	GND			
63	GND			
64	BLSP3_SPI_MOSI	1.8V	IO	MDM9205 GPIO8, Can be configured as GPIO
65	BLSP3_SPI_MISO	1.8V	IO	MDM9205 GPIO9, Can be configured as GPIO
66	GND			
67	GND			
68	EBI2_CLE_UB_N	1.8V	IO	MDM9205 GPIO41, Can be configured as GPIO
69	EBI2_WE_N	1.8V	IO	MDM9205 GPIO42, Can be configured as GPIO
70	EBI2_OE_N	1.8V	IO	MDM9205 GPIO40, Can be configured as GPIO
71	EBI2_BUSY_N	1.8V	IO	MDM9205 GPIO44, Can be configured as GPIO
72	GND			
73	PWM_1	1.8V	DO	MDM9205 GPIO50, Can be configured as GPIO

74	BLSP1_UART_TX	1.8V	DO	MDM9205 GPIO0, Can be configured as GPIO
75	PWM_2	1.8V	DO	MDM9205 GPIO52, Can be configured as GPIO
76	GRFC_2	1.8V	IO	MDM9205 GPIO59, Can be configured as GPIO
77	GRFC_1	1.8V	IO	MDM9205 GPIO58, Can be configured as GPIO
78	GRFC_3	1.8V	IO	MDM9205 GPIO60, Can be configured as GPIO
79	GRFC_0	1.8V	IO	MDM9205 GPIO57, Can be configured as GPIO
80	GND			
81	GND			
82	BLSP1_UART_RX	1.8V	DI	MDM9205 GPIO1, Can be configured as GPIO
83	BLSP1_UART_RFR_N	1.8V	DIO	MDM9205 GPIO3, Can be configured as GPIO
84	BLSP1_UART_CTS_N	1.8V	DIO	MDM9205 GPIO2, Can be configured as GPIO
85	CODEC_EN	1.8V	DO	MDM9205 GPIO48, Can be configured as GPIO
86	CODEC_INT	1.8V	DI	MDM9205 GPIO49, Can be configured as GPIO
87	I2S_WS	1.8V	IO	MDM9205 GPIO21, Can be configured as GPIO
88	I2S_CLK	1.8V	IO	MDM9205 GPIO24, Can be configured as GPIO
89	I2S_DIN	1.8V	IO	MDM9205 GPIO22, Can be configured as GPIO
90	I2S_DOUT	1.8V	IO	MDM9205 GPIO23, Can be configured as GPIO
91	GND			
92	BLSP4_UART_CTS_N	1.8V	DIO	MDM9205 GPIO14, Can be configured as GPIO
93	MCLK	1.8V	DIO	MDM9205 GPIO25, Can be configured as GPIO
94	BLSP4_UART_TX	1.8V	DIO	MDM9205 GPIO12, Can be configured as GPIO
95	BLSP4_UART_RX	1.8V	DIO	MDM9205 GPIO13, Can be configured as GPIO
96	BLSP4_UART_RFR_N	1.8V	DIO	MDM9205 GPIO15, Can be configured as GPIO
97	VREG_L6	1.8V	PO	Low voltage switch supply output 1.8V for GPS LNA voltage
98	GND			
99	GND			
A1	VPH_PWR_PA	4.2V	PI	Power supply in for SOM RF operations
A2	VPH_PWR_PA	4.2V	PI	Power supply in for SOM RF operations
A3	GND			
A4	VPH_PWR_PA	4.2V	PI	Power supply in for SOM RF operations
A5	VPH_PWR_PA	4.2V	PI	Power supply in for SOM RF operations
A6	GND			

A7	GND			
A8	GND	NC		
A9	GND			
A10	GND			
A11	GND			
A12	GND			
A13	GND			
A14	JTAG_SRST_N			
A15	JTAG_TCK			
A16	GND			
A17	JTAG_TRST_N			
A18	JTAG_TMS			
A19	GND			
A20	JTAG_TDO			
A21	JTAG_TDI			
A22	GND			
A23	GND			
A24	GND			
A25	GND			
A26	GND			
A27	MAIN_ANT_LGA		RF IO	Antenna port for LTE/GSM/GPS Tx/Rx
A28	GND			
A29	GND			
A30	GND			
A31	GND			
A32	GPS_ANT		RF I	Antenna port for GPS Rx
A33	GND			

3.3 Interfaces Detail Description

3.3.1 Pow4

Below table describes power supplies of T95SOM. Please refer chapters of Electrical specifications for detail parameters.

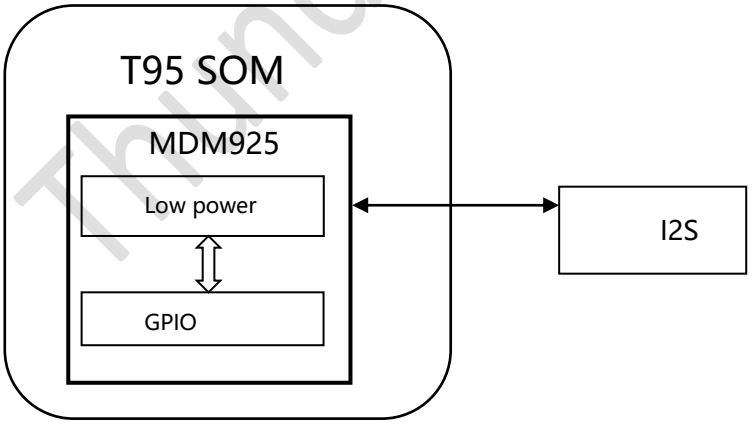
Power Supply				
Pin Name	PIN Location	Type	Description	Notes

VPH_PWR	6,15,24	PI	Power supply in for system operations.	
VPH_PWR_PA	A1,A2,A4,A5	PI	Power supply in for RF PA operations	
USB_HS_VDDA_3P3	28	PI	Power supply in for USB PHY;	
VREG_S2	5,14			
VREG_L7	3	PO	1.8V LDO power output, For SIM	
VREG_L5	4	PO	1.8V LDO power output, For IO	
VREG_L6	45,54,97	PO	1.8V LDO power output, For GPS LNA	
GND	1,7,9,16,17,27,31,36,48,62,63,66,67,72,80,81,91,98,99,A3,A6,A7,A8,A9,A10,A11,A12,A13,A16,A19,A20,A22,A23,A24,A25,A26,A28,A29,A30,A31,A33	GND		
JTAG	A14,A15,A17,A18,A20,A21	NC		

3.3.2 Audio Interface

The T95SOM integrates the audio system digital processing functions.

The T95SOM provide SLIMBUS, I2S, SWR and DMIC interfaces for audio system. Multiplexing of these interfaces is listed as follows.



I2S Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
I2S_DIN	89	1.8V	DO	I2S 1 SCK	
I2S_DOUT	90	1.8V	DO	I2S 1 WS	
I2S_SCK	88	1.8V	IO	I2S 1 Data0	
I2S_WS	87	1.8V	IO	I2S 1 Data1	

3.3.3 USB Interface

One USB 2.0 is supported with build-in USB PHY for device only.

HS USB0 (2.0) Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
USB2_HS_DM	38	-	IO	USB High-Speed Data-Minus	
USB2_HS_DP	47	-	IO	USB High-Speed Data-Plus	
VBUS_DET	13	1.8V	DI	PM9205 GPIO_01，VBUS detect	

3.3.4 BLSP Interface

GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, SPI, or I2C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus is supplemented by a 2.2kΩ pull-up resistor.

2-wire UART Tx/Rx and I2C SDA/SCL ports can be used simultaneously.

BLSP Interface-1								
BLSP Number	GPIO	PIN Location	Voltage	Type	Description			Notes
					SPI	UART	I2C	
1	0	74	1.8V	IO	MOSI	TX	-	
	1	82	1.8V	IO	MISO	RX	-	
	2	84	1.8V	IO	CS_N	CTS_N	SDA	
	3	83	1.8V	IO	CLK	RFR_N	SCL	
2	4	10	1.8V	IO	MOSI_A	TX	-	
	5	11	1.8V	IO	MISO_A	RX	-	
	6	19	1.8V	IO	CS_N_A	CTS_N	SDA	
	7	20	1.8V	IO	CLK_A	RFR_N	SCL	
3	8	64	1.8V	IO	MOSI	TX	-	
	9	65	1.8V	IO	MOSI	RX	-	
	10	57	1.8V	IO	CS_N	CTS_N	SDA	
	11	56	1.8V	IO	CLK	RFR_N	SCL	
4	12	94	1.8V	IO	MOSI	TX	-	
	13	95	1.8V	IO	MISO	RX	-	
	14	92	1.8V	IO	CS_N	CTS_N	SDA	

	15	96	1.8V	IO	CLK	RFR_N	SCL	

3.3.5 Power On Interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device’ s available power sources, enable the correct source.

There are two events that will be triggered.

When insert battery or power supply and KPDPWR_N key signal connected to ground, SOM will be power on automatically. It is longer than 1s with pressing power-on key, for power on event. And it is suggested for 3s powering on system.

Power-on input pad when transitioning from Low to High, will initiate the power-on sequence from the master.

PMIC device.

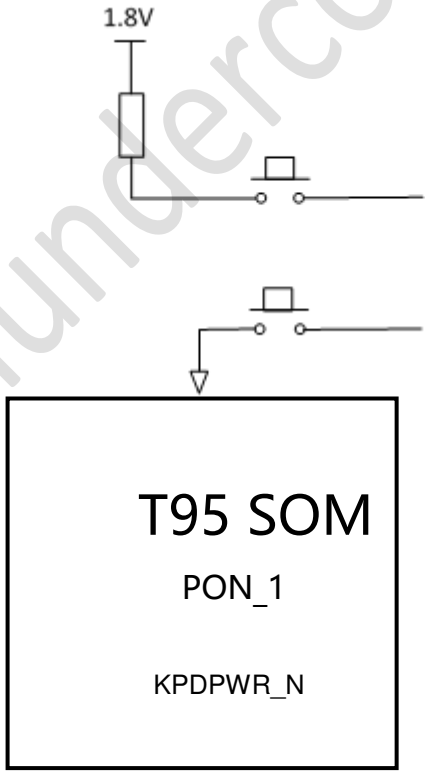


Figure-3 Power on signal

Power on Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
KPDPWR_N	22	V_INT	DI	Power-on trigger, level trigger (active low)	

PON_1	12	V_INT	DI	Level-high triggered power-on input	

3.3.6 Reset Interface

There are three stages resets.

- Stage 1 reset – software-configurable bark

PMIC generates interrupt, giving the SoC device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

The user can generate a mandatory reset by a long key press of KYPD_PWR to resets PMIC back to factory default.

Reset Pin					
Pin Name	PIN Location	Voltage	Type	Description	Notes
KPDPWR_N	22	V_INT	DI	Long press to reset PMIC. (active low)	
RESETIN	60	1.8V	DI	System reset input	
PS_HOLD	33	1.8V	DI	Power supply hold control input	

These reset triggers each have individual debounce and delay timers. Their default values are 10.256 seconds for stage 1 and 2 seconds for stage 2, respectively, and they share the stage 3 reset timer. Stage 1 and stage 2 timers run in series, and stage 3 timer runs independently (parallel) of stage 1 and stage 2 timers. If the stage 3 timer is set to a lower value than that of stage 1 and stage 2 combined, then the stage 3 reset happens first. The stage 3 default values is 128 seconds.

3.3.7 Boot Configuration Interface

There are two types of boot: secure boot and fastboot, which can be configured by using fuses or

BOOT_CONFIG pins.

- BOOT_CONFIG pins provide flexibility during product development.

■ Fuses must be blown for production devices.

■ BOOT_CONFIG[3:1] is MSB-aligned with FAST_BOOT[2:0].

There are two types of boot-related fuses:

■ Fastboot fuses are used by the boot code to determine which memory device the chip must use for boot.

■ Secure boot fuses use encryption to ensure that the code running on the MDM device is from a trusted source.

□ There are fuses for different code authentication schemes.

□ The read-only settings for these schemes are stored in software registers named SECURE_BOOT.

Boot Configurations:			
Boot segment	Feature	GPIOs	Function
Apps boot segment	APPS_BOOT_FROM_ROM	GPIO[44]	Boots from internal ROM
	FORCED_USB_BOOT(NPU)	GPIO[48]	Boots from internal USB
Fast boot option	FASTBOOT_SEL[0]	GPIO[32]	Selects boot media
	FASTBOOT_SEL[1]	GPIO[38]	Selects boot media
	FASTBOOT_SEL[2](unused)	GPIO[4]	Unused

Default boot configuration (0b000) is eMMC on internal.

Special boot-related GPIO features:

■ They are sensed for boot-purposes during IC reset (during fuse sense).

■ After bootup, use them for normal GPIO functions.

■ Do not have pull-ups on GPIO_62, GPIO_44, GPIO_32, GPIO_38 and GPIO_4x` prior to blowing FAST_BOOT fuses.

The boot configuration function of the preceding GPIOs is sampled at the rising edge of RESOUT_N reassertion.

Forced USB boot:

During development or factory production, boot from USB_HS port are forced by using GPIO_48.

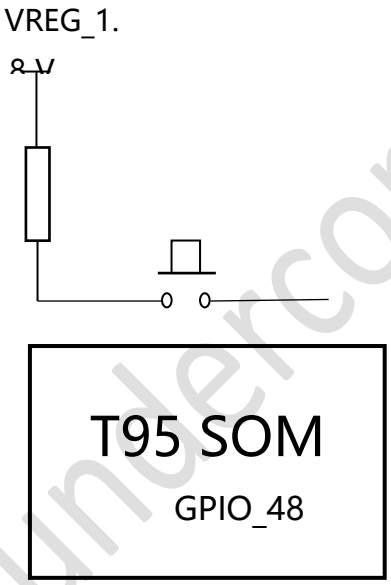
■ FORCED_USB_BOOT (GPIO_48) always takes precedence, regardless of the state of the BOOT_CONFIG

GPIOs or FAST_BOOT_SEL fuses.

■ FORCED_USB_BOOT is checked first during the boot device detection prior to BOOT_CONFIG GPIOs.

■ GPIO_48 = 1 forces the SDM device to boot from USB_HS port.

Blow the FORCE_USB_BOOT_DISABLE fuse to disable the feature that forces USB boot using GPIO_48.



3.3.8 Debug UART Interface

This is interface dedicate for debug.

Debug UART Pins					
Pin Name	PIN Location	Voltage	Type	Description	Notes
GPIO_0	74	1.8V	DO	MSM_UART_TX	
GPIO_1	82	1.8V	DI	MSM_UART_RX	

3.3.9 PWM

The GPIO_03 can be configured to send the output of the PWM waveform through special functions that can control the external current drivers for LED.

PWM Pin					
Pin Name	PIN Location	Voltage	Type	Description	Notes
PWM1	73	1.8V	DO	Configurable GPIO	
PWM2	75	1.8V	DO	Configurable GPIO	

3.3.10 Antenna Interface

T95SOM provides the fully-integrated LTE/GPS function.

- MAIN_ANT_LGA.
- GPS_ANT

Antenna interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
GPS_ANT	A32	-	RF I	Antenna port for GPS RX	
MAIN_ANT_LGA	A27	-	RF IO	Antenna port for LTE/GSM/GPS RX/TX	

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T95SOM is designed to be used in the operating conditons shown as below. Beyond this absolute maximum ratings may damage the device.

Parameter	Min	Max	Units
Input Power voltage			
Voltage on any input or output pin	-0.5	VXX+0.5	V
VPH_PWR	-0.5	6.0	V
ESD			
ESD-HBM model rating		(TBD)	KV
ESD-CDM model rating		(TBD)	KV

Notes: VXX is the supply voltage associated with the input or output pin to which

the test voltage is applied for the ESD, it will be valid and available only when the module is fully tested and approved in the Initial Production stage.

4.2 Operating Conditions

T95SOM needs to be designed in the operating conditons which is shown as below.

Parameters	Min	Typical	Max	Units
Input Power voltage				
VPH_PWR	+2.3	3.8	+4.8	V
Supply voltage, digital I/O	+1.75	-	+1.85	V
VPH_PWR	0.8			A
Thermal conditions				
Operating temperature	-20(TBD)	25	70(TBD)	°C
Storage temperature	-20 (TBD)	-	70(TBD)	°C

Note: For the thermal conditons, operating and storage min and max temperature is only when the module is fully tested and approved in the Initial Production stage.

4.3 Output Power

T95SOM provides power supply for external device which is shown as below.

Function	Default voltage(V)	Programble range(V)	Rated current(mA)	Default ON	Expected use
VREG_L5	+1.8	-	100	Y	1.8V IO pull up voltage;
VREG_L6	+1.8		100	Y	Power output for SD card data pull up
VREG_L7	+1.8		100	N	1.8V LDO power output,100mA
VREG_S2	+1.8		100	N	1.8V LDO power output,100mA

4.4 Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage.

The I2C, USB,SPI and UART are complied with their standards, no additional specifications are listed.

Performance specifications for all other digital I/Os are organized within this section.

4.4.1 Digital GPIO characteristics

The GPIOs can be programmed for a variety of configurations.

The followint table shows the electrical characteristics for GPIOs:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.65* P3	-	V
VIL	Low-level input voltage, CMOS/Schmitt,	-	0.35* P3	V
VSHYS	Schmitt hysteresis voltage	100	-	mV
VOH	High-level output voltage, CMOS	P3-0.45	-	V
VOL	Low-level output voltage, CMOS	-	0.45	V
RPULL-UP	Pull-up and Pull-down resistance	55	390	KΩ
Rk	Keeper resistance	30	150	KΩ

4.5 USB

USB standards and exceptions

Applicable standard	Feature exceptions	APQ variation
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS

4.6 I2S

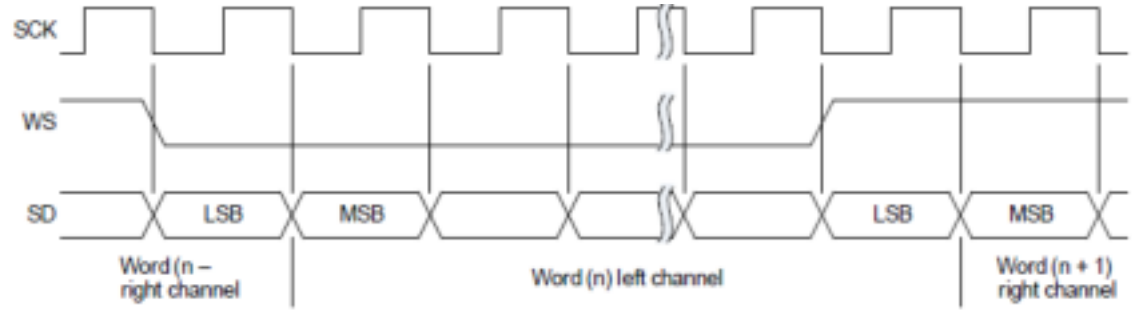
I2S standards and exceptions:

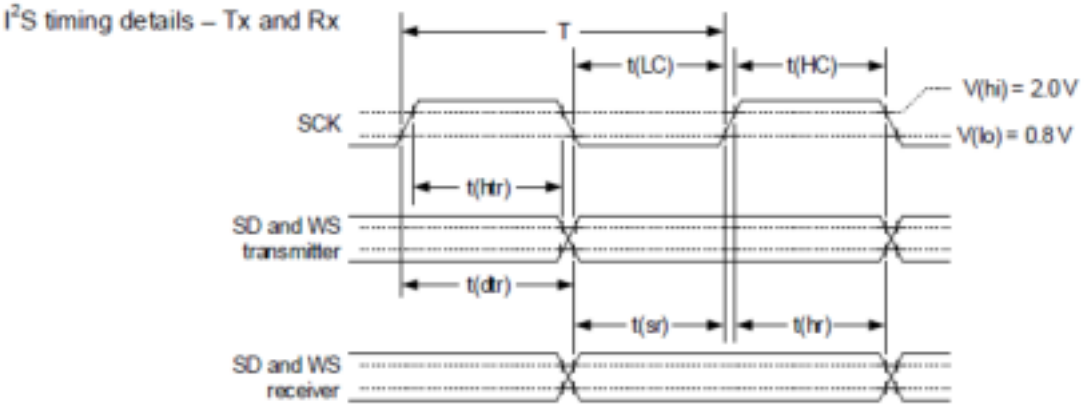
Legacy I2S interfaces for primary and secondary microphones and speakers.

The multiple I2S (MI2S) interface for microphone and speaker functions, including audio for HDMI.

Applicable standard	Feature exceptions	Device variations
Philips I2S Bus Specifications revised June 5, 1996	None	Timing – see Figure 5-14. When an external SCK clock is used, a duty cycle between 45% to 55% is required.

High-level I2S timing





I2S interface timing

Parameter	Description	Min	Typical	Max	Units
Using internal SCK					
F	Frequency. Load capacitance is between 10 and 40pF.			12.288	MHZ
T	Clock period. Load capacitance is between 10 and 40pF.	81.380	-	-	ns
t(HC)	Clock high. Load capacitance is between 10 and 40pF.	0.45 x		0.55 x	ns
t(LC)	Clock low. Load capacitance is between 10 and 40pF.	0.45 x		0.55 x	ns
t(sr)	SD and WS input setup time. Load capacitance is between 10	16.276	-	-	ns
t(hr)	SD and WS input hold time. Load capacitance is between 10	0	-	-	ns
t(dtr)	SD and WS output delay. Load capacitance is between 10 and	-	-	65.100	ns
t(htr)	SD and WS output hold time. Load capacitance is between 10	0	-	-	ns
Using external SCK					
F	Frequency. Load capacitance is between 10 and 40pF.			12.288	MHZ
T	Clock period. Load capacitance is between 10 and 40pF.	81.380	-	-	ns
t(HC)	Clock high. Load capacitance is between 10 and 40pF.	0.45 x		0.55 x	ns
t(LC)	Clock low. Load capacitance is between 10 and 40pF.	0.45 x		0.55 x	ns
t(sr)	SD and WS input setup time. Load capacitance is between 10	16.276	-	-	ns
t(hr)	SD and WS input hold time. Load capacitance is between 10	0	-	-	ns
t(dtr)	SD and WS output delay. Load capacitance is between 10 and	-	-	65.100	ns
t(htr)	SD and WS output hold time. Load capacitance is between 10	0	-	-	ns

I2S interface frequencies

Interface	Frequency achieved

I2S1	24.57 MHz
I2S2	12.288 MHz
I2S3A	12.288 MHz
I2S3B	12.288 MHz
I2S5	24.57 MHz
I2S6	12.288 MHz

4.7 I2C

I2C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 5.0, October 2012	None

4.8 SPI

The following are the SPI features and comparisons:

■ Supports 4-bit (MISO, MOSI, CS, CLK) synchronous serial data link.

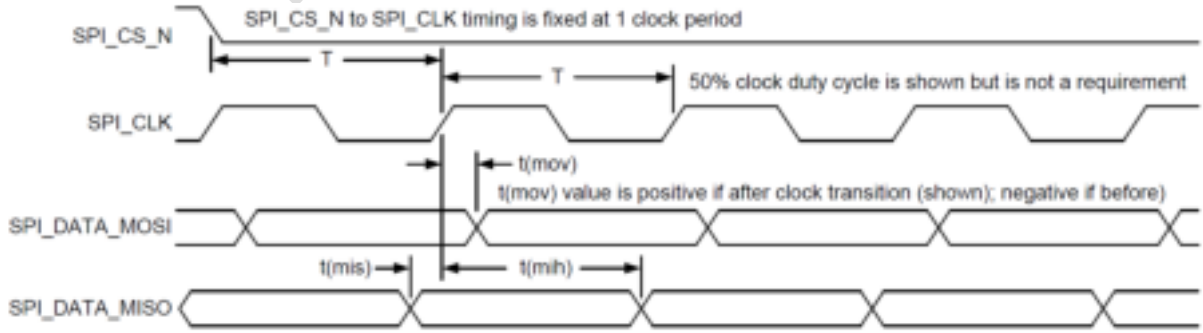
■ Support for master-only mode, up to 50 MHz on all SPI interfaces.

■ Master device initiates data transfers; Multiple slave devices are supported by using chip-selects.

■ No explicit communication framing, error-checking, or defined data word lengths; The transfers are strictly at the raw bit level.

■ As an SPI master, the core supports several SPI system configurations (as defined by the SPI protocol).

SPI master timing diagram



SPI master timing characteristics at 50 MHz

Parameter	Description	Min	Typical	Max	Units
T	SPI clock period: 50 MHz maximum	20	-	-	ns
t(ch)	Clock high	9.0	-	-	ns

t(cl)	Clock low	9.0	-	-	ns
t(mov)	Master output valid	-5.0	-	5.0	ns
t(mis)	Master input setup	5.0	-	-	ns
t(mih)	Master input hold	1.0	-	-	ns
T	SPI clock period: 26 MHz maximum	38	-	-	ns
t(ch)	Clock high	17	-	-	ns
t(cl)	Clock low	17	-	-	ns
t(mov)	Master output valid	-5.0	-	5.0	ns
t(mis)	Master input setup	5.0	-	-	ns
t(mih)	Master input hold	1.0	-	-	ns

4.9 Current Sink

PM_GPIO_03 is capable of sinking current (up to 10 mA). In addition, since the PWM module can be routed to the current sink, different blinking and dimming patterns can be achieved.

Parameter	Min	Typical	Max	Units
Rated current sink	9	-	12	mA

4.10 Power Consumption(TBD)

TBD

4.11 RF Performance

4.11.1 Modem RF performance

Note: All values in the following tables are preliminary, pending transceiver matching and testing.

TX performance					
Band	Comments	Min	Typ	Max	unit
LTE-FDD B2/B4/B12	PC3	< -40	23±3		dBm

Note: (1) are still under development. Therefore, details of them are currently not fixed and will be added in a future release of this document

RX performance				
Band	Comments	Cat M (3GPP)	NB 1&2 3GPP (-107.5)	unit
B2		TBD (-100.3)	<TBD -107.5	dBm
B4		TBD (-102.3)	<TBD -107.5	dBm
B12		TBD (-99.3)	<TBD -107.5	dBm

Note: TBD are means still under development. Therefore, details of them are currently not fixed and will be added in a future release of this document.

* B71 supports only with NB1; B14 and B27 supports only with cat M1

4.11.2 GPS Performance

GPS performance				
Mode	range	Cold start	TTFF	Tracking
GPS	1575.42±1.023MHZ	TBD	TBD	TBD
GLONASS	1597-1606 MHZ	TBD	TBD	TBD
BeiDou	1561.095±2.046 MHZ	TBD	TBD	TBD
Galileo	1575.42±2.046 MHZ	TBD	TBD	TBD
QZSS	1575.42±1.023 MHZ	TBD	TBD	TBD

5 Mechanical Size

5.1 Mechanical Size

The size of TurboX™ T95 SOM is 19X16mm. Thickness is 2.3mm; You can check the size of BTB connectors through their datasheets.

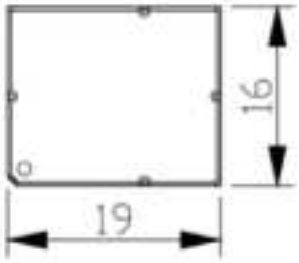


Figure 6-1 Top View

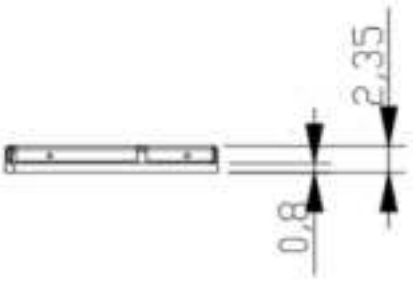
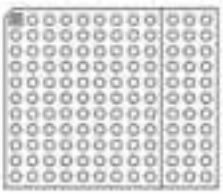


Figure 6-2 Side View



6 Compliance with FCC rules and regulations

The Equipment Authorization Certification for the Turbox M2M reference application described will be registered under the following identifier:

FCC Identifier: 2AOHHT95GNA

ISED Certification Number:

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment

Note: This equipment has been tested and found to comply with the limits for a Class

B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

The end product must carry a label stating "Contains FCC ID: 2AOHHT95GNA" or shall use e-labeling.

7. Warnings

① This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

② This equipment should be installed and operated with a minimum distance of 7.9 inches (20 cm) between the radiator and your body.

This radio transmitter 2AOHHT95GNA has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Maximum gain in operating band	**FCC limit**	**Unit**
LTE Band 2	7.01	dBi
LTE Band 4	4.00	dBi
LTE Band 12	7.70	dBi

③ If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the

following: “Contains Transmitter Module FCC ID: 2AOHHT95GNA Or Contains FCC ID: 2AOHHT95GNA”

④ When the module is installed inside another device, the user manual of the host must contain below warning statements:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference.
(2) This device must accept any interference received, including interference that may cause undesired operation.
Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.

Any company of the host device which install this modular with limit modular approval should perform the test of radiated & conducted emission and spurious emission, etc. According to FCC 47 CFR Part 22/24/27 and 15.209 & 15.207, 15B Class B requirement, only if the test result comply with FCC part FCC 47 CFR Part 22/24/27 and 15.209 & 15.207, 15B Class B requirement, then the host can be sold legally.

⑤ Information on test modes and additional testing requirements.
Any final host product with the modular transmitter installed should be under test according to guidance given in KDB 996369 D04. To enter test mode for module, Enter the signaling mode test. When something wrong happens in configuring test modes for host product with module, host product manufacturer should coordinate with module manufacturer for technical support. It is recommended that some investigative measurements should be taken to confirm that host product with module installed does not exceed the spurious emissions limits or band edge limits.

The module complies with FCC 47 CFR Part 22/24/27 and apply for Single module approval.

The module is limited to OEM installation ONLY.

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.