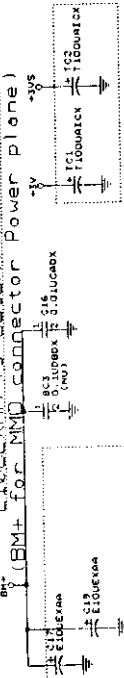


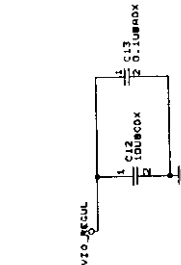
Appendix B

Circuit (Block) Diagram

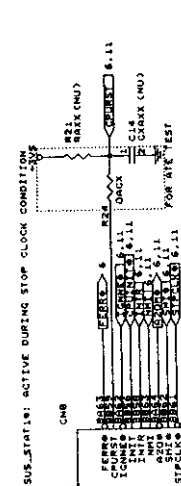
10LEXAA 15 OSCON PART NO: 10-300

[illegible]

SW4	port1&2	ON	port3&4	OFF	for T11a	book CPU
SW4 <th>port1&2</th> <th>OFF</th> <th>port3&4</th> <th>ON</th> <th>for MPII</th> <th>CPU</th>	port1&2	OFF	port3&4	ON	for MPII	CPU



NU PARTS :
R21,C14,R28,C15,BC3

[illegible]

MMO CONNECTOR



CHANG LIA PIN NAN

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65101-1 CHANGE WITH INTEL

RESERVED	993
FIOS	993

0-1234
0011
1111

SECRET

[illegible]

DATE TEST
CS

WITH INTEL C SOURCE

66149

RESERVED

0-4231
10111
10111
10111

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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Part Number	PIC AMBER
Title	MIO CONNECTOR
Size	DOCUMENT NUMBER
C	MIO-SC4 (PCB VER:0.B)
Date	OCTOBER 18, 1999 Sheet 2 OF 2

1000V 100A AC

主触头
灭弧罩
触头
底座

MS-3

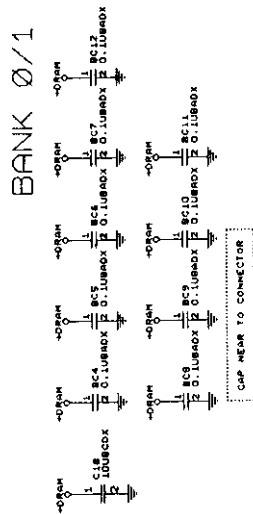
19-8-10TAC

19-8-10TAC


 DEPARTMENT OF EDUCATION
 GOVERNMENT OF KARNATAKA

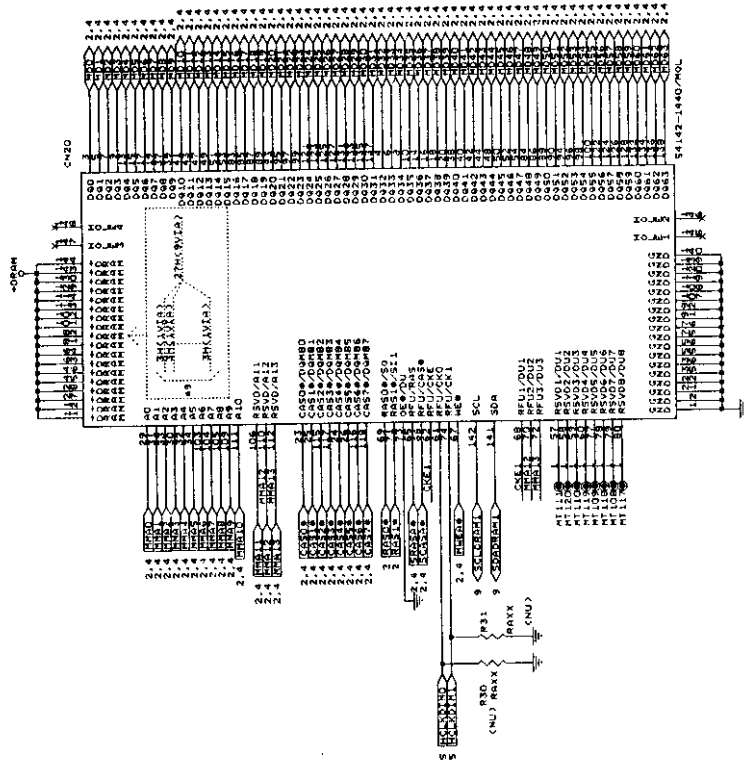
2.4 CKX CKE CKE1

INPUT
-2V
+0.5V
+0.5V



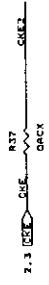
CAP NEAR TO CONNECTOR

NU PARTS :
R30, R31

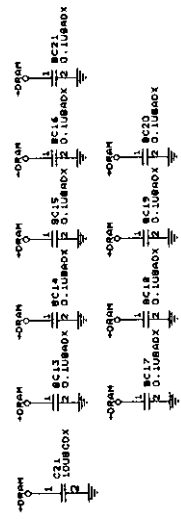


BANKS 0/1

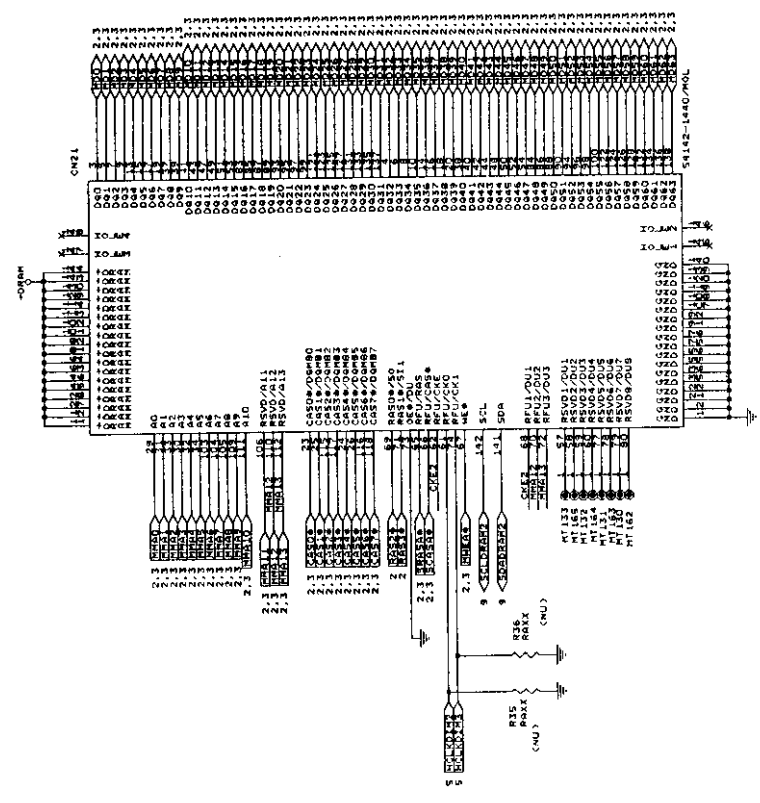
FILE	FIC AMBER
STEP	S001M144
DOCUMENT NUMBER	DRAM-1 SCH (PCB VER 0.8)
REV	0
DATE	2008-12-15



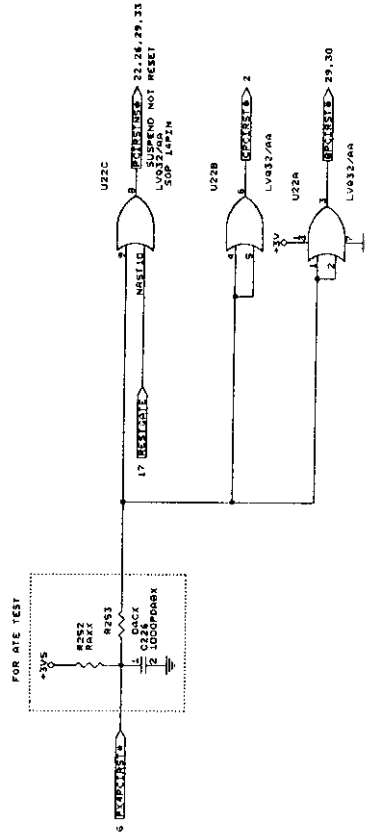
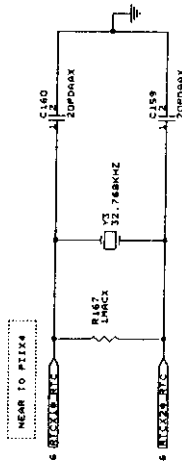
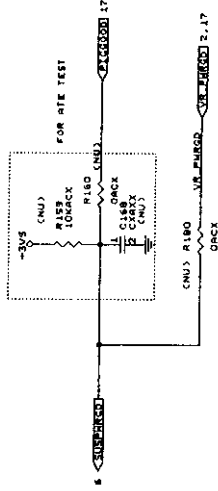
BANK 2/3



NU PARTS :
R35, R36

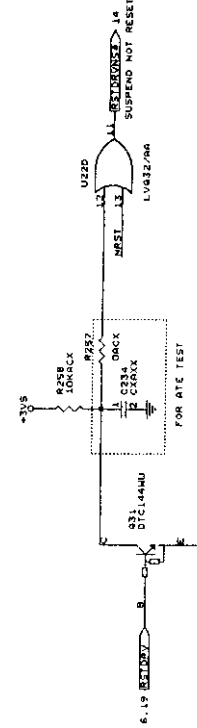
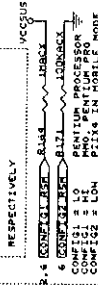


POWER GOOD circuit



NU PARTS :
R252, C234, R159, C168
R180

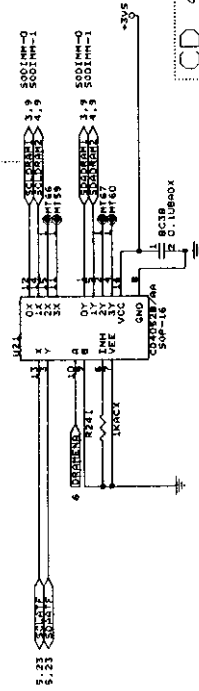
CONFIG10M SETS PI1X4
TO RUN A PENTIUM PROCESSOR
CONFIG20M SETS PI1X4
TO RUN IN MOBILE MODE
CONFIG12M SETS PI1X4
AND IN DESKTOP MODE.
RESPECTIVELY



The schematic diagram illustrates the test circuit for the DRAM and PEELME components. It features two parallel signal paths. The top path, labeled 'DRAM', consists of a 100 ohm resistor in series with a 100 pF capacitor, followed by another 100 ohm resistor. The bottom path, labeled 'PEELME', also consists of a 100 ohm resistor in series with a 100 pF capacitor, followed by another 100 ohm resistor. Both paths are connected to a 3V5 supply and a VCCBUS supply.

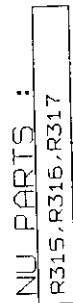
R255, R240, R242, R251

Read	SDRAM-2	slot	EPROM	need	program	DRAMENA:H
Read <td>SDRAM-1 <td>slot <td>EPROM <td>need <td>program <td>DRAMENA:L</td> </td></td></td></td></td>	SDRAM-1 <td>slot <td>EPROM <td>need <td>program <td>DRAMENA:L</td> </td></td></td></td>	slot <td>EPROM <td>need <td>program <td>DRAMENA:L</td> </td></td></td>	EPROM <td>need <td>program <td>DRAMENA:L</td> </td></td>	need <td>program <td>DRAMENA:L</td> </td>	program <td>DRAMENA:L</td>	DRAMENA:L



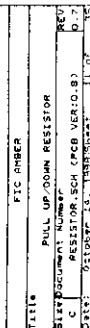
CD 4052 True table

I	I	I	I	I
N	N	N	N	N
D	D	D	D	D
B	B	B	B	B
X	X	X	X	X
Y	Y	Y	Y	Y
1	1	1	1	1
2	2	2	2	2
3	3	3	3	3
4	4	4	4	4
5	5	5	5	5

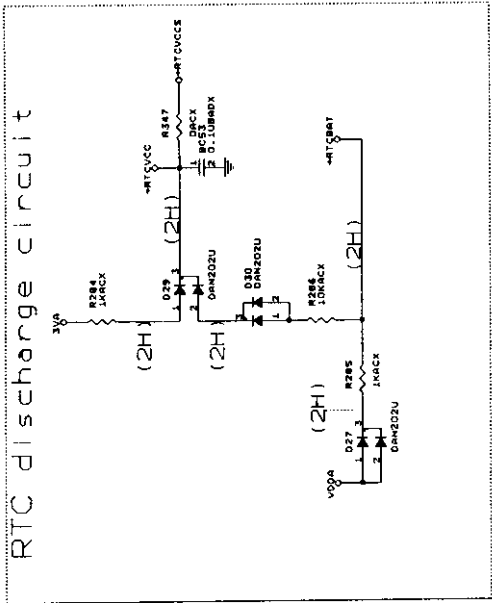


NOET: BIOS Socket 1002-B32T1R

File	Title	Size	Document Number	PLV
C	BIOS.SCH (PCB VER:0.9)	0.7		
Date:	October 14, 1998	13 of 15		



REV.0.4 33) REV.0.5
 8/22 ADD R347(D) THEN CONNECT TO +RTCVCDS



Under AC Adapter			
Power ON	Suspend	Power Off	
Charge	Charge	Charge	

Under Battery			
Power ON	Suspend	Power Off	
Charge	Charge	Charge	

5/28 U23 #1N79 R270 10K CHANGE TO 47K
CONNECT FROM +5V TO GND
THEN ADD MODULE WAKEUP TO PIC #1N16

5/28 U23 #1N74 174 CHANGE
CHANGE TO MODULE LYN_R31#

REVO. 2 --> REVO. 3

6/17 U23 PIN20.2L PULL-UP 10K TO -5V
6/17 U23 PIN75 ADD 0.01UF TO GND

REVQ.3 => REVQ.4

7/3 8139.8139 PULL UP TO +5VS

RTV-C 4 3 3 RI

0/2 MODIFY RTC CLEAN FUNCTION

```

SM3(5) CHANGE TO GND
SM3(4) ADD TWO PTH AND RESISTOR(R348,R349)

```

THEY #348 25 NO PART

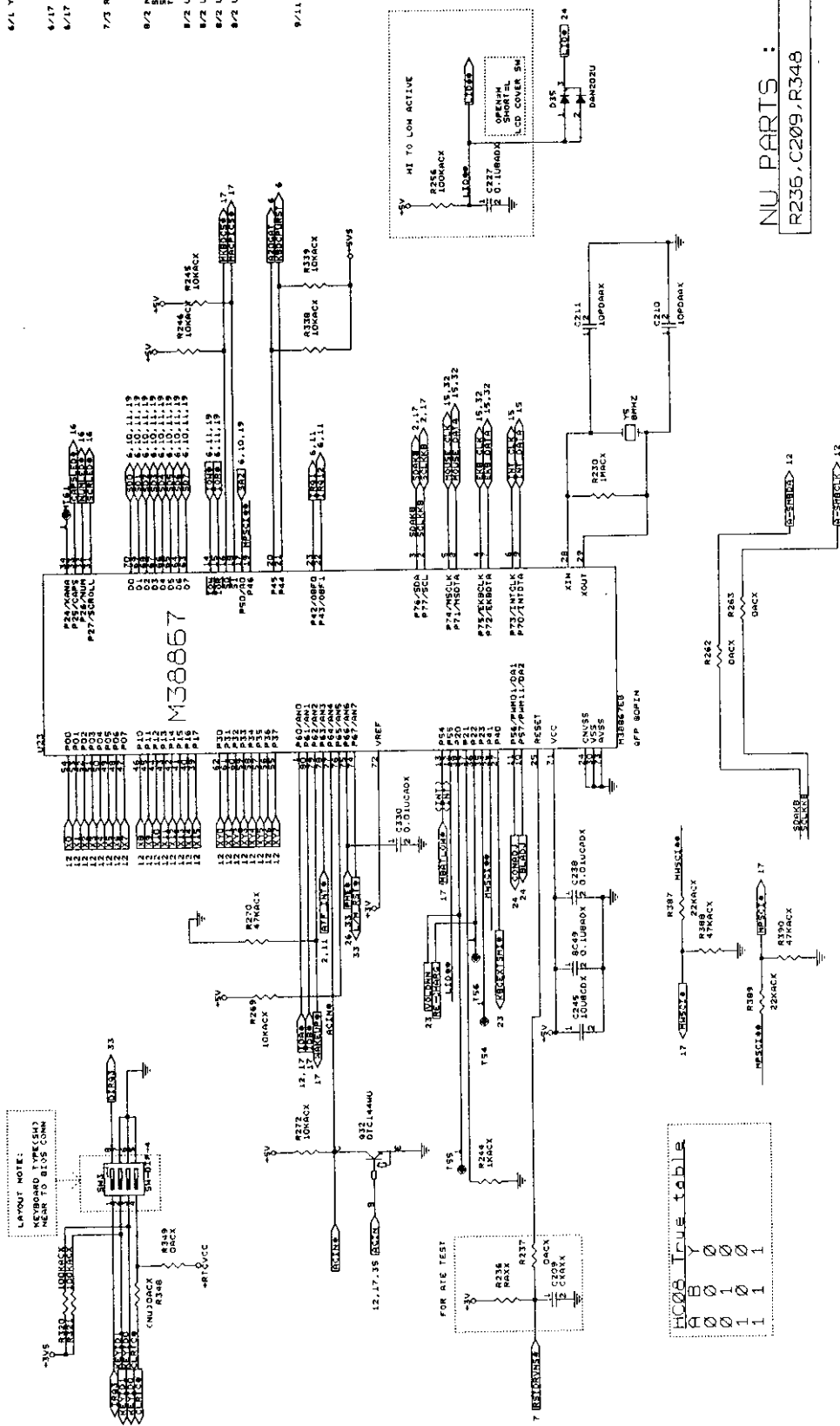
1/2 U23C123 ADD BIOECONOMY

012 1234567 000 0103 0700

072 025(10) 400 K307, N308

REV-0.6 ==> REV.0.7

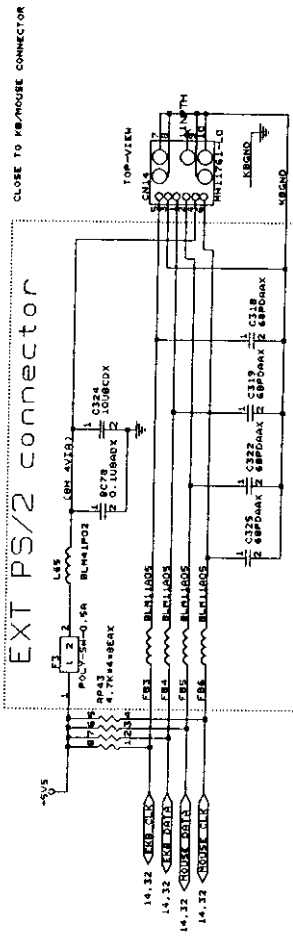
9/11 U23 PIN36 ADD MODULE "RE-CHARG"



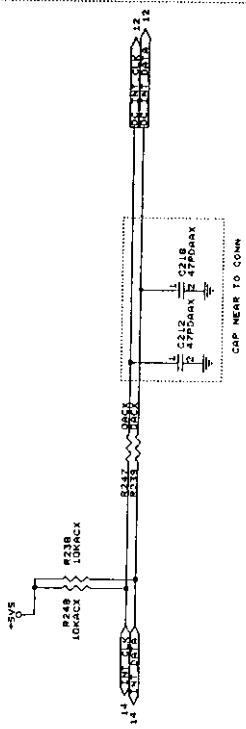
NU PARTS :
R236,C209,R348

HC08 True table	
A	B
0	0
0	0
0	1
1	0
1	1

Glide Pod TM41PDG-220-2 Synaptics

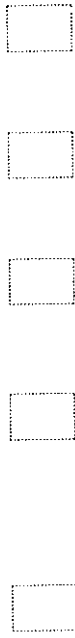


GLIDE PAD pull resistor

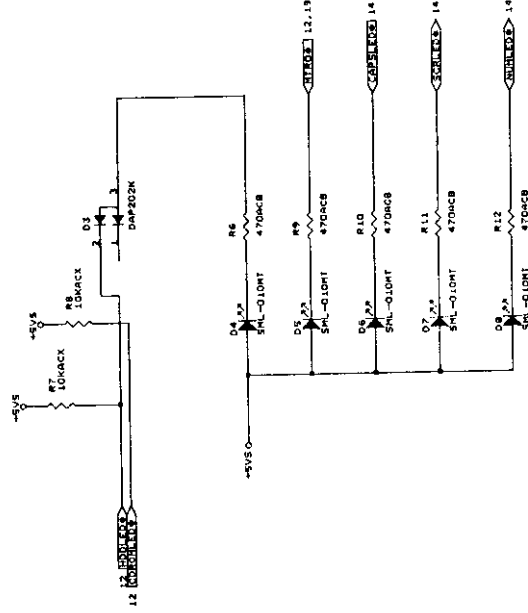


FILE	PTC NUMBER
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PTC199	PTC199
PTC200	PTC200

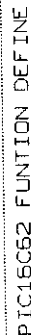
LED STATUS



HDD&CDROM FDD Caps Scr Num



3V transfer 5v
Include DIODE HT 1359



1. POWER ON/OFF
2. POWER GOOD SIGNAL GENERATE
3. INDICATOR LED ON/OFF
4. PANEL ON/OFF TIMING CONTROL
5. SUSPEND/RESUME CONTROL
7. SUSPEND NOT RESET GATE

RA4: OPEN DRAIN OUTPUT, SCHMITT TRIGGER INPUT

STAT 2

R353, R354

PTC 16072

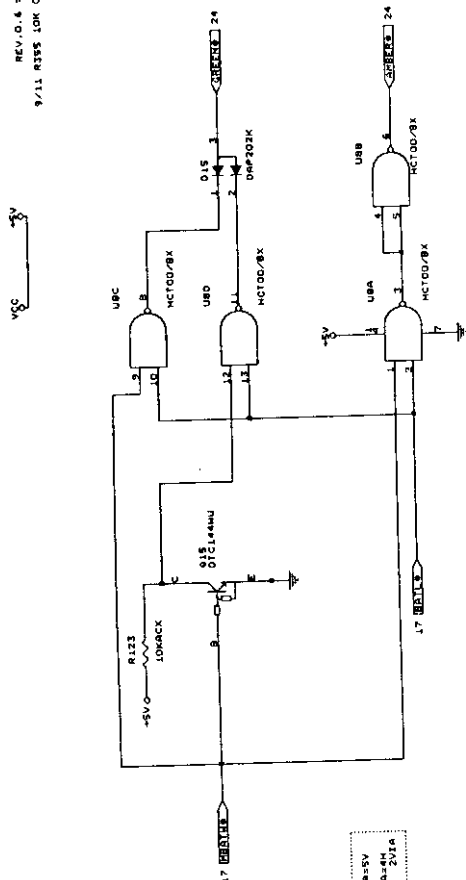
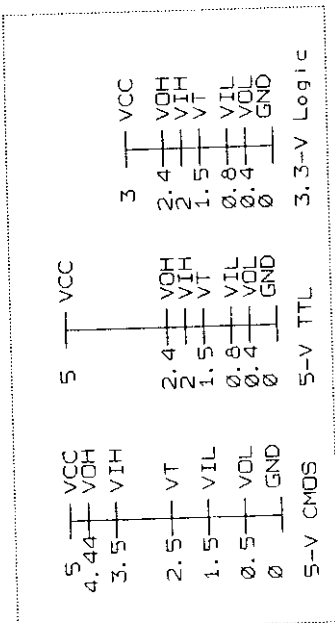
```
PIC16C72 IIC ADDRESS 04  
38A13 IIC BUS TO SMART BATTERY  
  
OTHER IIC BUS TYPE TO PIX4  
AFTER BOOT SAVE SUPEND TO RAM  
AND RECALL FROM TOSTO TIME  
THEN SAVE TO DISK+MER  
SUB-BATTERY DESIGN GUIDE  
1.5 X 20mm X 10mm = 1 X 3HP  
1.5 WATT CONSUMPTION DURING  
STANDBY MODE  
TO AGIL SUB-BATTERY WORKING FOR  
1. CHARGE SUB-BATTERY CURRENT
```

REV.0.3 22> REV.0.4
7/3 U16 CHANGE PART TO L22951

REV.0.4 22> REV.0.5
8/2 D24 CHANGE TO NU PART
8/2 D23 PART CHANGE TO 88411D
8/2 840(B,E) ADD R355
8/2 U16(9) ADD MODULE M21
8/2 U16(3) CONNECT TO 840(C)

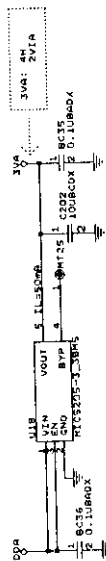
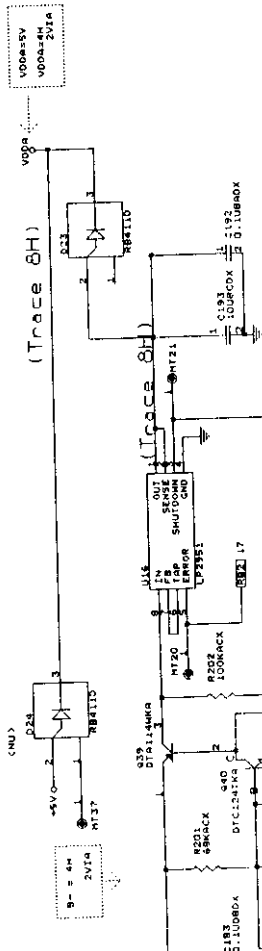
REV.0.6 22> REV.0.7
9/11 R355 10K CHANGE TO 18K

RB411D	Forward voltage
	V110-24V/0.3VCI(100mA)
	V1250-25V/0.3VCI(100mA)



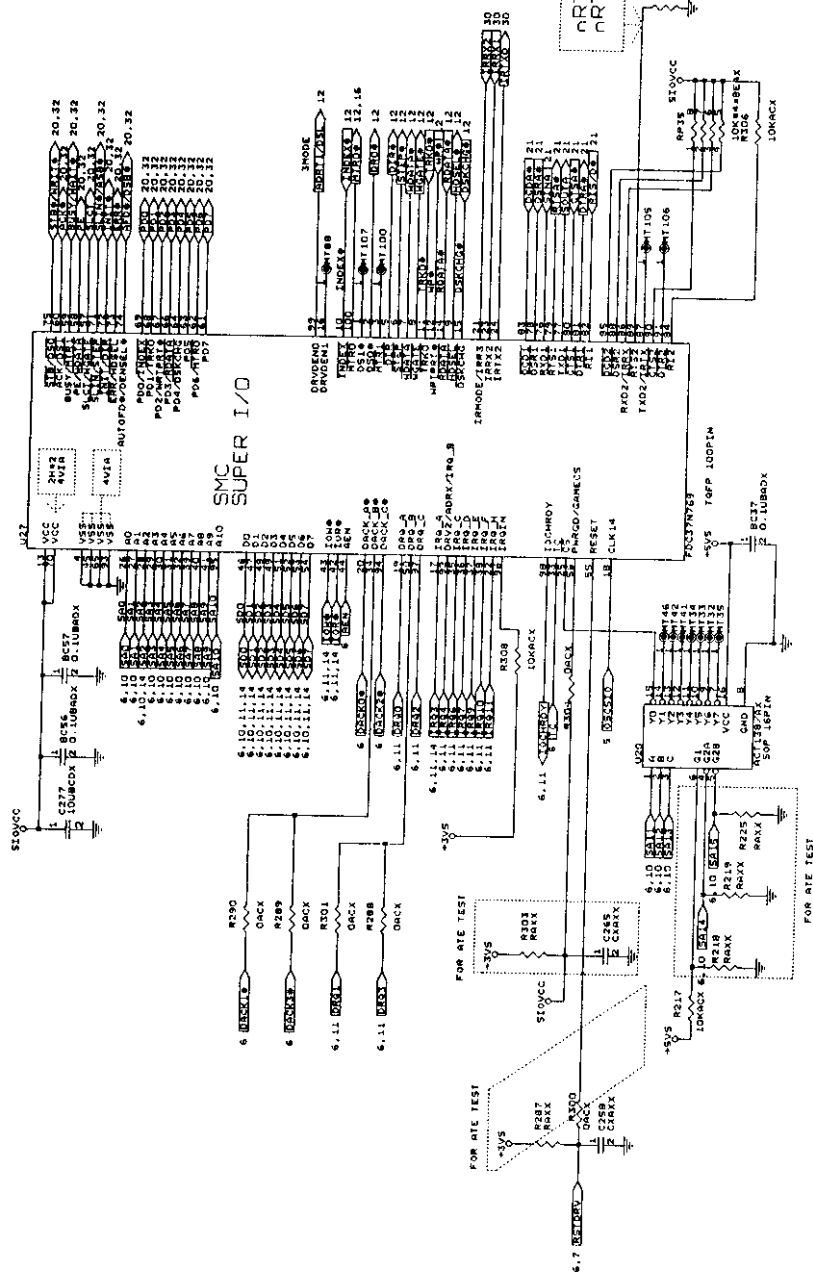
POWER STATUS LED TRUTH TABLE :

	UNDER AC		GREEN#	AMBER#
	MBATW#	BATL#		
NORMAL	1	1	0	1
BATTERY WARNING (8% OR LESS)	1	1	0	1
BATTERY LOW (3% OR LESS)	1	1	0	1
	UNDER AC		GREEN#	AMBER#
	MBATW#	BATL#		
	1	1	0	1
NORMAL	0	0	0	0
BATTERY WARNING (8% OR LESS)	0	0	0	0
BATTERY LOW (3% OR LESS)	0	0	0	0



NU PARTS:

D24



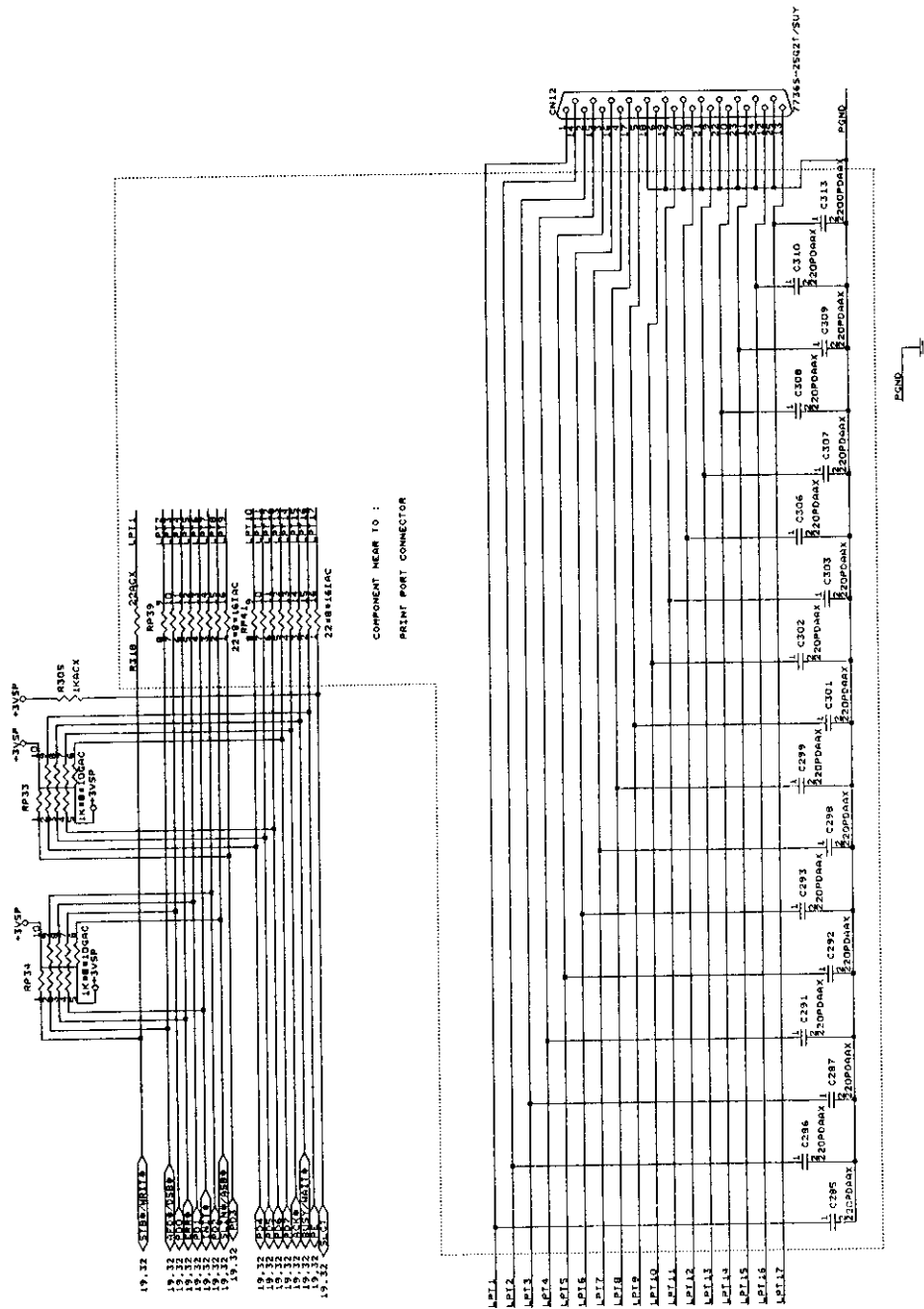
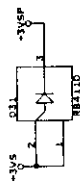
nRIS2 = 0: Index base I/O address 3F0
 nRIS2 = 1: Index base I/O address 370

NU PARTS :

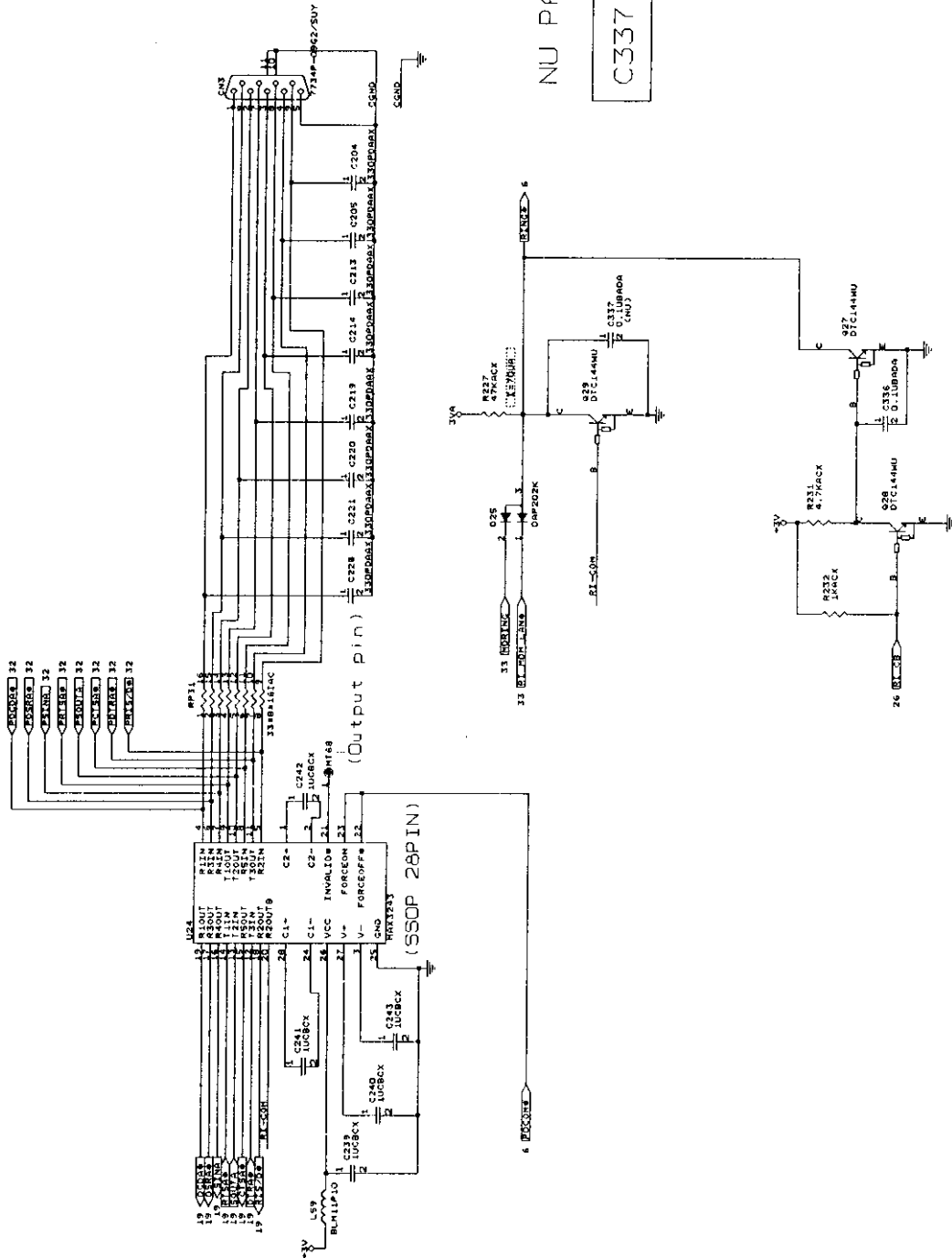
R289, R288, R287, C258, R303, C265
 R218, R219, R225

FILE	FIC 00000
NAME	SMC I/O SMC37C669PLV
DATE	1989.05.10
REV	0.1
BY	1358

PRINT PORT STANDARD CIRCUIT



REV. 0.4 => REV. 0.5
 8/2 ADD C337, C338 THEN C337 IS NU PART
 8/2 R232 VALUE CHANGE TO 1K
 8/2 R231 VALUE CHANGE TO 4.7K



NU PARTS:

C337

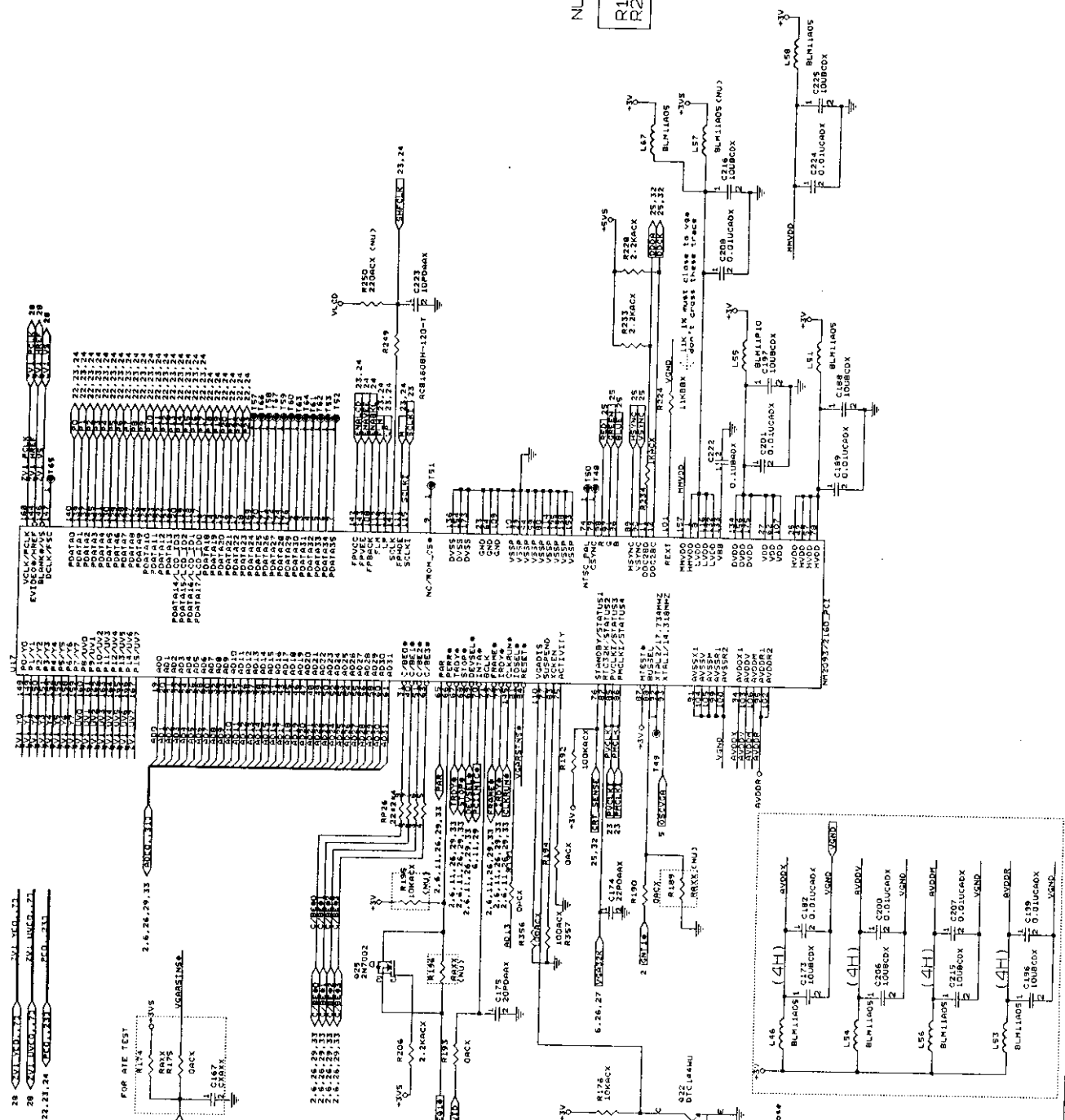
FILE	PIC AMBER
SHEET	1
SERIAL PORT	
DOCUMENT NUMBER	100
COMP. SCH. (PCB VER. 0.8)	0.7
DATE	12/01/91

REV.0.4 203 REV.0.5
 8/7 L57 CHANGE TO NU PART
 8/7 C216 AND L67 TO +3V
 8/7 U17(L10,83) MOD R356,R357 TO GND

REV.0.6 203 REV.0.7
 9/11 R249 0 CHANGE TO BEAD FOR EMI
 9/11 C223 FROM NU CHANGE TO 100P

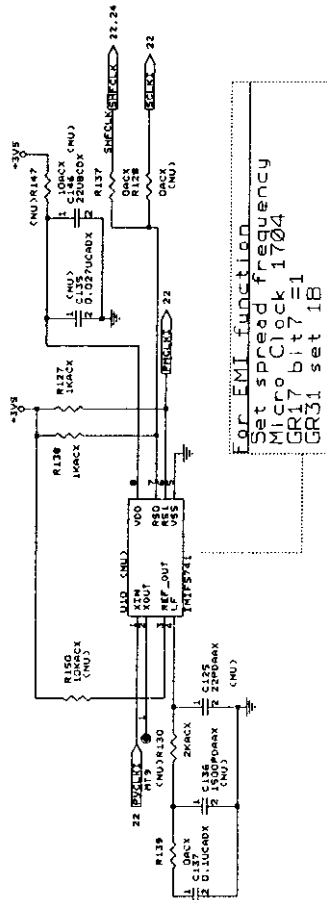
NU PARTS :

R174,C167,R196,R195,R189,C175
 R250,L57



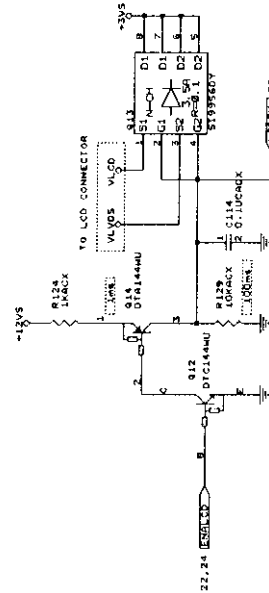
FILE	PCB AMBER
SHEET NUMBER	VGA CONTROLLER
REV	REV0.4 (PCB VER10.8)
DATE	05/09/13 13:59

VGA clock generator circuit



For EMI function
Set spread frequency
Micro Clock 1704
GR17 bit 7=1
GR31 set 1B

VGA & LCD power circuit

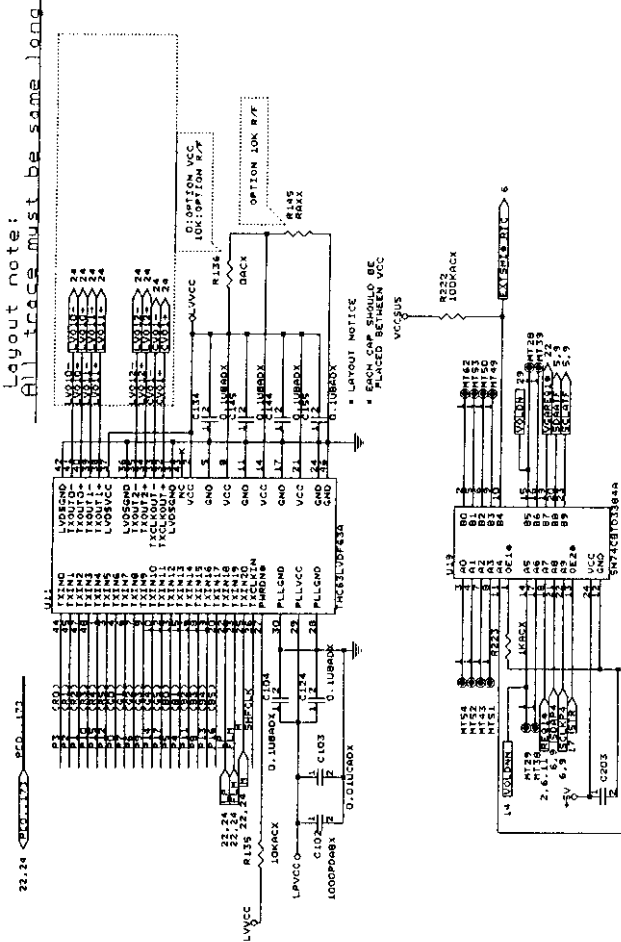


REV.0.2 -> REV.0.3
6/17 Q13 PIN4 ADD MODULE LCDSV
REV.0.4 -> REV.0.5
8/2 R129 CHANGE TO NU PART
8/2 U1K115 ADD R38R1384
8/2 U1K115 ADD MODULE VOLDMW
8/2 U1K115 ADD MODULE VOLDM
REV.0.6 -> REV.0.7
9/11 CHANGE SOME PARTS TO NU
U10,C145,C139,C138,C146,R150,R150,R147
9/11 R222 FROM 32K CHANGE TO 100K

JHC63LVDF63Apin14 NC

18bit LVDS Panel (65MHz)

Layout note:
All trace must be same long



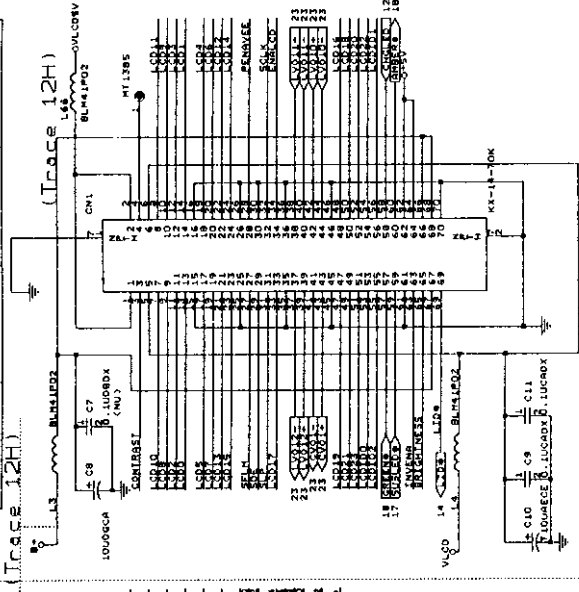
NU PARTS :

R137, R136, R145, U10, C125, C135, C146
C137, R139, R128, R150, R130, R147

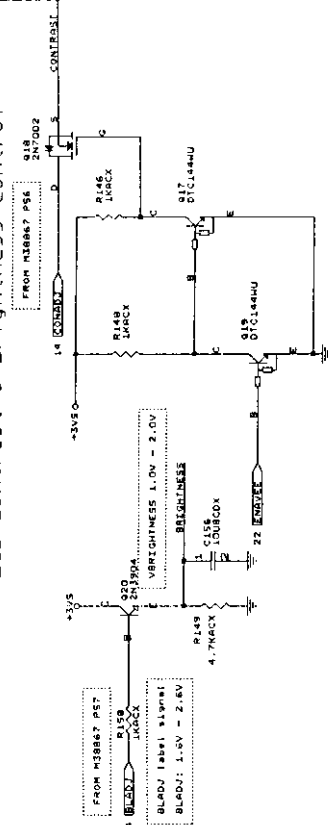
FILE#	EIC AMBER
SIZE	VGA POWER
REVISION	NSPOWER SCH (PCB VER:0.9)
DATE	2008/07/14
BY	07

LCD connector

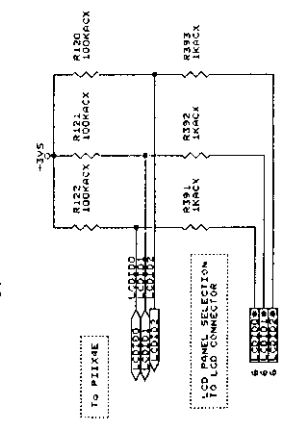
Rated current	Resistance	Size
BLM41P01 1A	0.15	4.5x1.6



LCD contrast & brightness control



LCD type selection

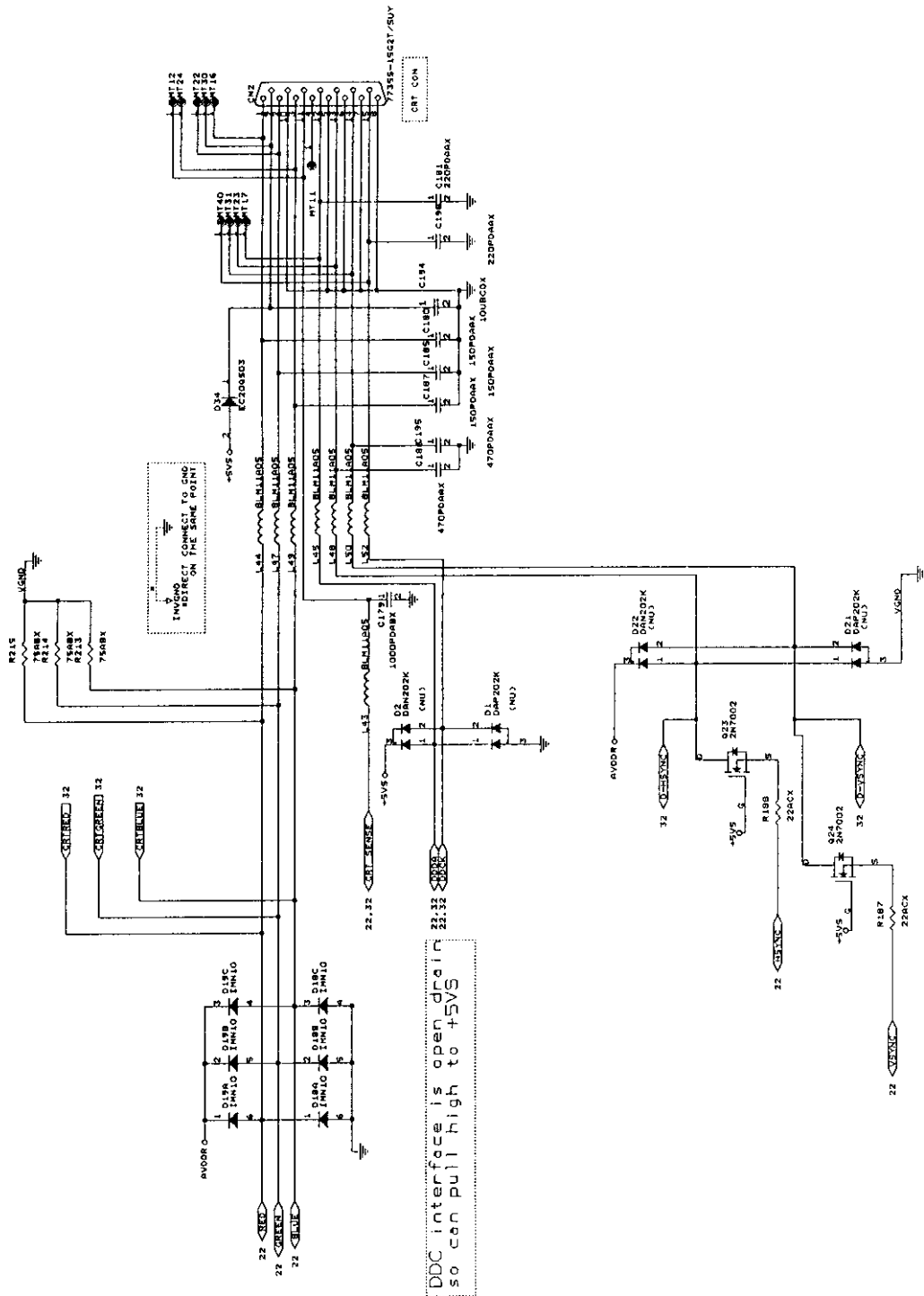


REV.0.2 -> REV.0.3
6/17 C8 CHANGE TO 1000GGA
6/17 C81 PIN1.2 CHANGE TO VCC0V
6/17 C81 PIN4 CHANGE TO MT1385
REV.0.4 -> REV.0.5
8/2 C7 CHANGE TO 1000GGA
8/2 R132, R133, R134 CHANGE VALUE TO 100K
THEN ADD R331, R332, R333 TO LCD.009,
LCD.010, LCD.008

NU PARTS :

U12, BC34, C7

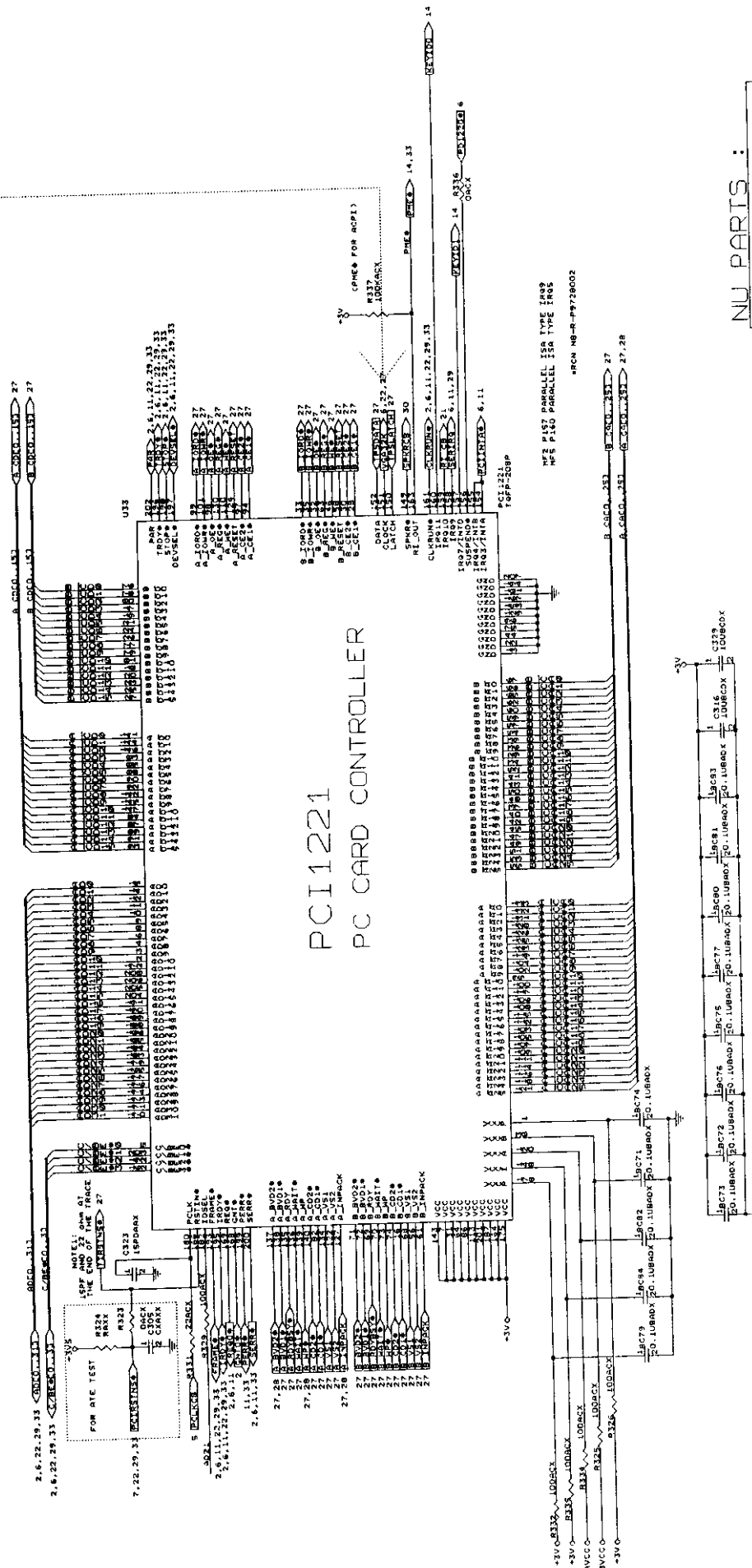
Rev	Doc	Rev	Doc
1.1	1.1	1.1	1.1
1.2	1.2	1.2	1.2
1.3	1.3	1.3	1.3
1.4	1.4	1.4	1.4
1.5	1.5	1.5	1.5
1.6	1.6	1.6	1.6
1.7	1.7	1.7	1.7
1.8	1.8	1.8	1.8
1.9	1.9	1.9	1.9
2.0	2.0	2.0	2.0
2.1	2.1	2.1	2.1
2.2	2.2	2.2	2.2
2.3	2.3	2.3	2.3
2.4	2.4	2.4	2.4
2.5	2.5	2.5	2.5
2.6	2.6	2.6	2.6
2.7	2.7	2.7	2.7
2.8	2.8	2.8	2.8
2.9	2.9	2.9	2.9
3.0	3.0	3.0	3.0
3.1	3.1	3.1	3.1
3.2	3.2	3.2	3.2
3.3	3.3	3.3	3.3
3.4	3.4	3.4	3.4
3.5	3.5	3.5	3.5
3.6	3.6	3.6	3.6
3.7	3.7	3.7	3.7
3.8	3.8	3.8	3.8
3.9	3.9	3.9	3.9
4.0	4.0	4.0	4.0
4.1	4.1	4.1	4.1
4.2	4.2	4.2	4.2
4.3	4.3	4.3	4.3
4.4	4.4	4.4	4.4
4.5	4.5	4.5	4.5
4.6	4.6	4.6	4.6
4.7	4.7	4.7	4.7
4.8	4.8	4.8	4.8
4.9	4.9	4.9	4.9
5.0	5.0	5.0	5.0
5.1	5.1	5.1	5.1
5.2	5.2	5.2	5.2
5.3	5.3	5.3	5.3
5.4	5.4	5.4	5.4
5.5	5.5	5.5	5.5
5.6	5.6	5.6	5.6
5.7	5.7	5.7	5.7
5.8	5.8	5.8	5.8
5.9	5.9	5.9	5.9
6.0	6.0	6.0	6.0
6.1	6.1	6.1	6.1
6.2	6.2	6.2	6.2
6.3	6.3	6.3	6.3
6.4	6.4	6.4	6.4
6.5	6.5	6.5	6.5
6.6	6.6	6.6	6.6
6.7	6.7	6.7	6.7
6.8	6.8	6.8	6.8
6.9	6.9	6.9	6.9
7.0	7.0	7.0	7.0
7.1	7.1	7.1	7.1
7.2	7.2	7.2	7.2
7.3	7.3	7.3	7.3
7.4	7.4	7.4	7.4
7.5	7.5	7.5	7.5
7.6	7.6	7.6	7.6
7.7	7.7	7.7	7.7
7.8	7.8	7.8	7.8
7.9	7.9	7.9	7.9
8.0	8.0	8.0	8.0
8.1	8.1	8.1	8.1
8.2	8.2	8.2	8.2
8.3	8.3	8.3	8.3
8.4	8.4	8.4	8.4
8.5	8.5	8.5	8.5
8.6	8.6	8.6	8.6
8.7	8.7	8.7	8.7
8.8	8.8	8.8	8.8
8.9	8.9	8.9	8.9
9.0	9.0	9.0	9.0
9.1	9.1	9.1	9.1
9.2	9.2	9.2	9.2
9.3	9.3	9.3	9.3
9.4	9.4	9.4	9.4
9.5	9.5	9.5	9.5
9.6	9.6	9.6	9.6
9.7	9.7	9.7	9.7
9.8	9.8	9.8	9.8
9.9	9.9	9.9	9.9
10.0	10.0	10.0	10.0

REV. 0.4 22 REV. 0.5
0/2 F1 CHANGE TO 034 (EC20Q503)

Title	VGA CRY CONNECTOR	REV	0.7
Size	Document Number		
C	NSCRTCEN.SCH (PCB VER:0.8)		
Date:	October 14, 1998	23	15

BIOS note:

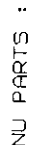
BIOS program: 83 BIT3 1 change to 0



NU PARTS :

R324, C305, C323

REVQ.2 —> REVQ.3

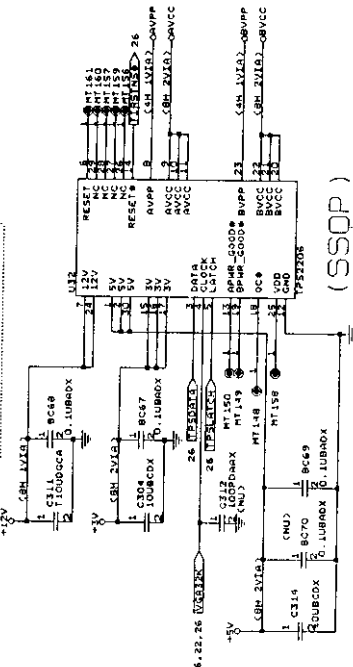


Feb. 29 1925

A CORUS 07 26

26 9-680-25 B. G. G. O. 751

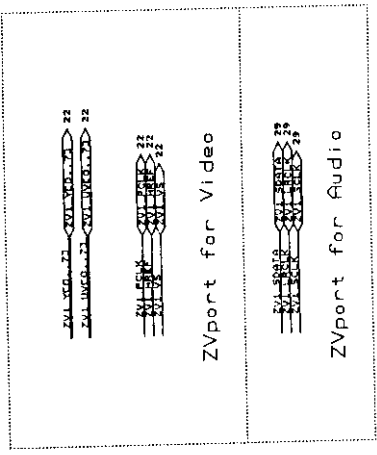
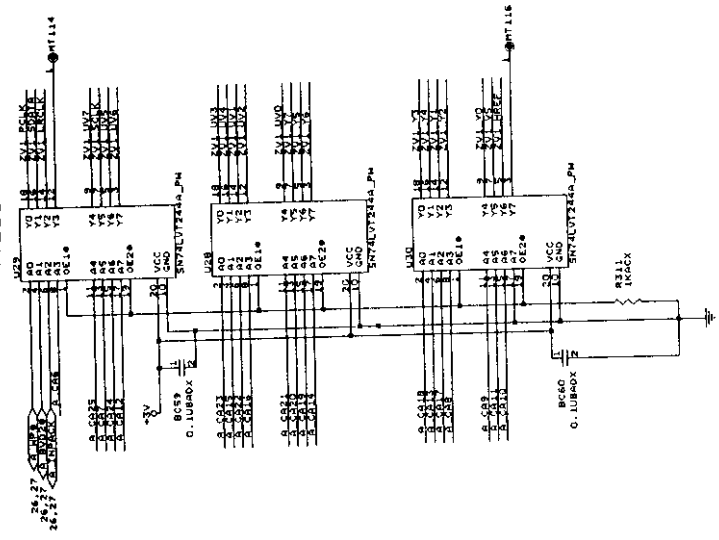
CO-51200 B



U21 use SSOP package

FIC AMBER	
CARD BUS SOCKET	
Title	
Size	Document Number
C	PCCARD SCH (PCB VER:0.8)
Date	October 11 1985
	Page 27 of 27

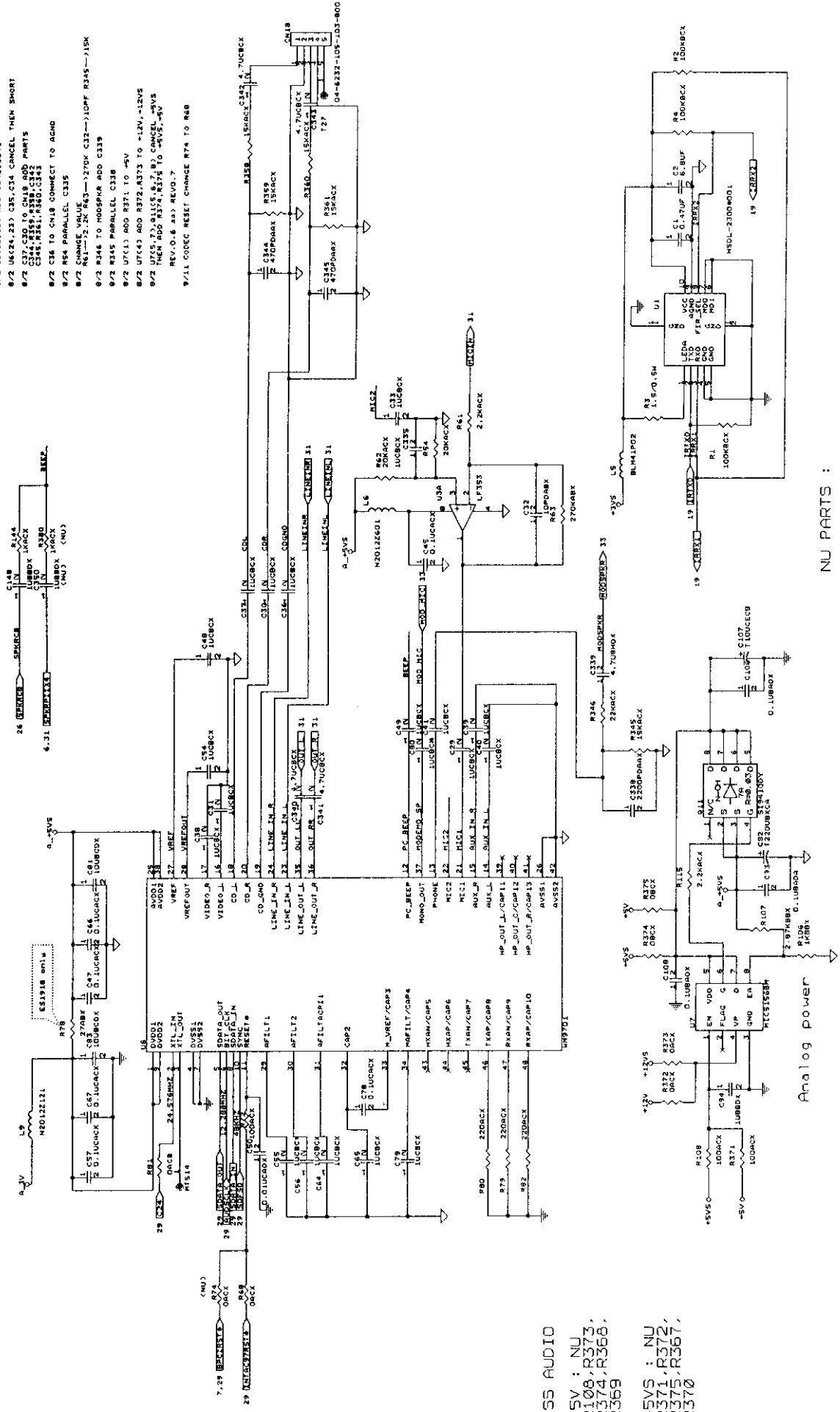
24.27 (TSSOP)



NU PARTS :
R97,C86,R57

Title		FIC AMBER	
SIZE	Document Number	MAESTRO 2	
C	AUDH2.SCH (PCB VER:0.8)		
Date:	October 14, 1998	REV	0.7

REV. 2 --> REV. 3
6/17 MODS PKR CHANGE TO R346, R345 22K
REV. 0.4 --> REV. 0.5
8/2 L9 CONNECT TO A1V
8/2 C59, C58, R31, R1 CANCEL
8/2 UC318, R400 C340, C341
8/2 UC318, R400 C340, C341
8/2 C37, C36 TO CH18 ADD PARTS
C37, C36, R341, R340, C343
8/2 C36 TO CH18 CONNECT TO AGND
8/2 R54 PARALLEL C335
8/2 CHANGE VALUE
R61 --> 2.2K R62 --> 10K R345 --> 15K
8/2 R346 TO MODS PKR ADD C339
8/2 R345 PARALLEL C338
8/2 U7(1) R371 TO +5V
8/2 U7(4) R372, R373 TO +12V, +12V5
8/2 U7(3) R374, R375 TO +5V
8/2 U7(2) R376 TO +5V
REV. 0.4 --> REV. 0.7
8/11 CODEC RESET CHANGE R74 TO R40



NU PARTS :

R78, C59, C58, Y1, R73
R74, C78, C79, R80
R79, R82, C350, R380

ESS AUDIO

+5V : NU
R100, R373,
R374, R368,
R369

+5V5 : NU
R371, R372,
R375, R367,
R370

Analog power

11111

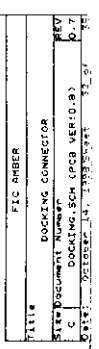
Garnet audio board AC97 Codec
SHEET NUMBER (GDS VER. 0.3)
REV. 0.3
DATE: 03/04/97 13:13

REV. 0.3

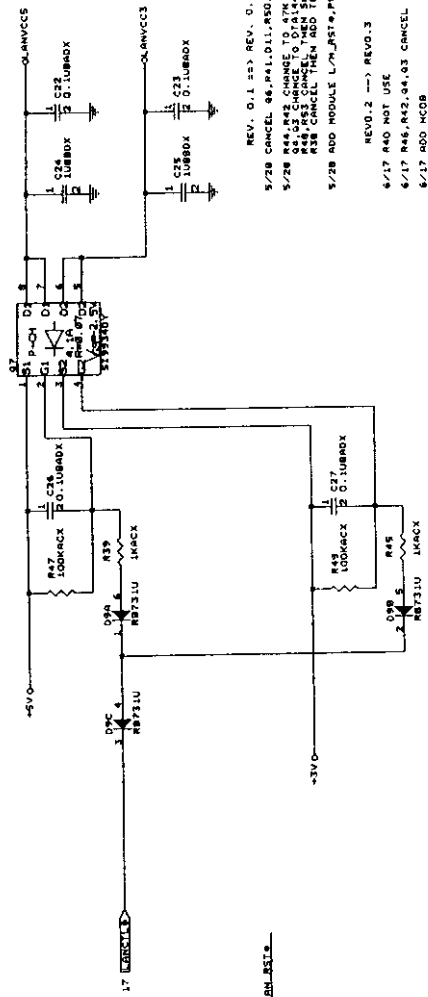

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REVO.2 --> REVO.3
6/17 U25 PIN2 ADD 0.1UF TO GND
6/17 U25 PIN3 CHANGE TO VLCD5V
U25 PIN4 CHANGE TO LCD5V
6/17 C96 PIN1A,73,75,77,79 SHORT

```

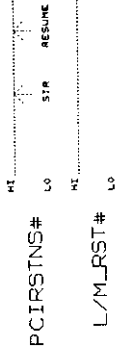


MODEM/LAN CONNECTOR



REV. 0.1 => REV. 0.2 MODIFICATION
 5/28 CANCEL R46, R41, 0.1, R50, R52, 0.1, R43, U2
 5/28 R44, R42 CHANGE TO 47K
 5/28 R45, R43 CHANGE TO 47K
 5/28 R46, R42 CHANGE TO 47K
 5/28 R45, R43 CHANGE TO 47K
 5/28 ADD MODULE L/M_JRST4.PHE9
 REV. 0.2 --> REV. 0.3
 6/17 R40 NOT USE
 6/17 R46, R42, 0.1, 0.3 CANCEL
 6/17 R40 NOT USE

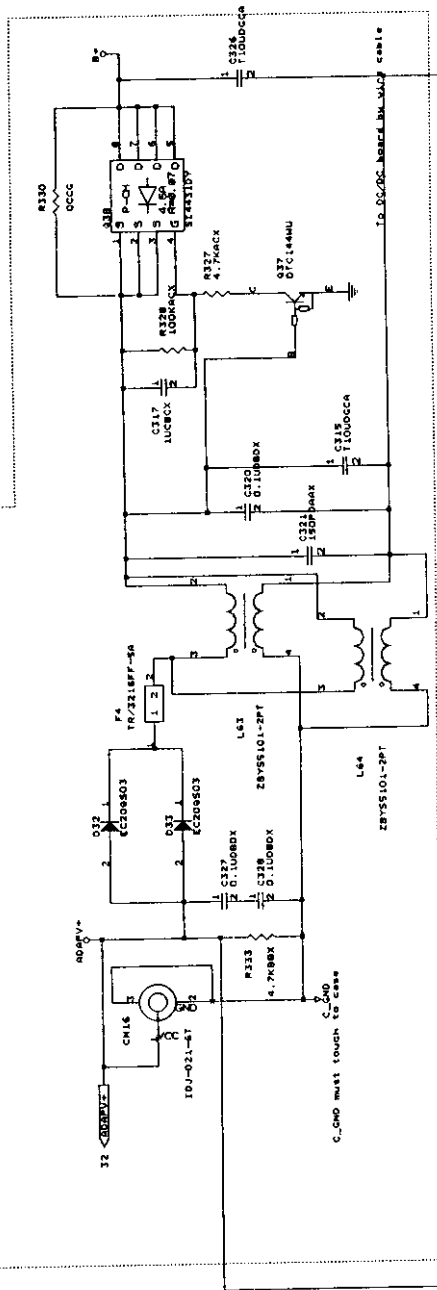
STR RESET TIMING



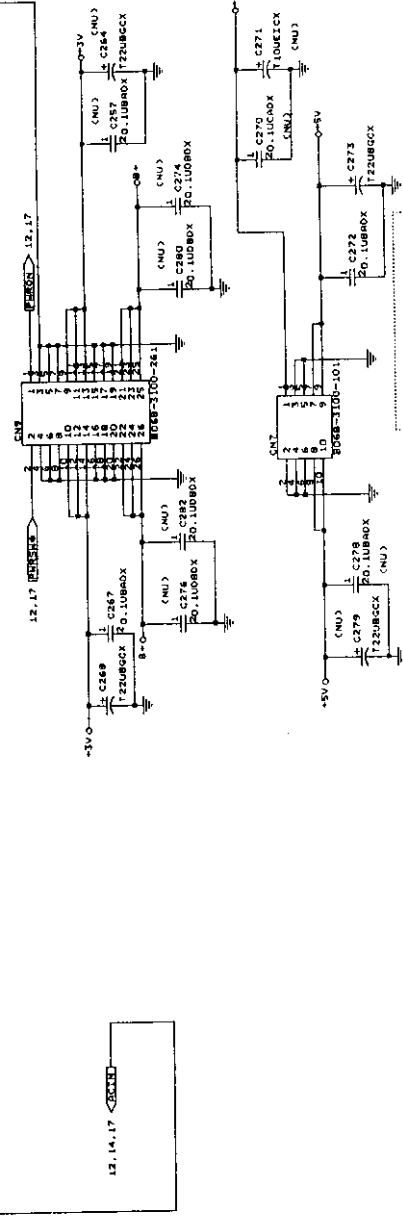
LAN/MODEM POWER CONTROL TRUTH TABLE

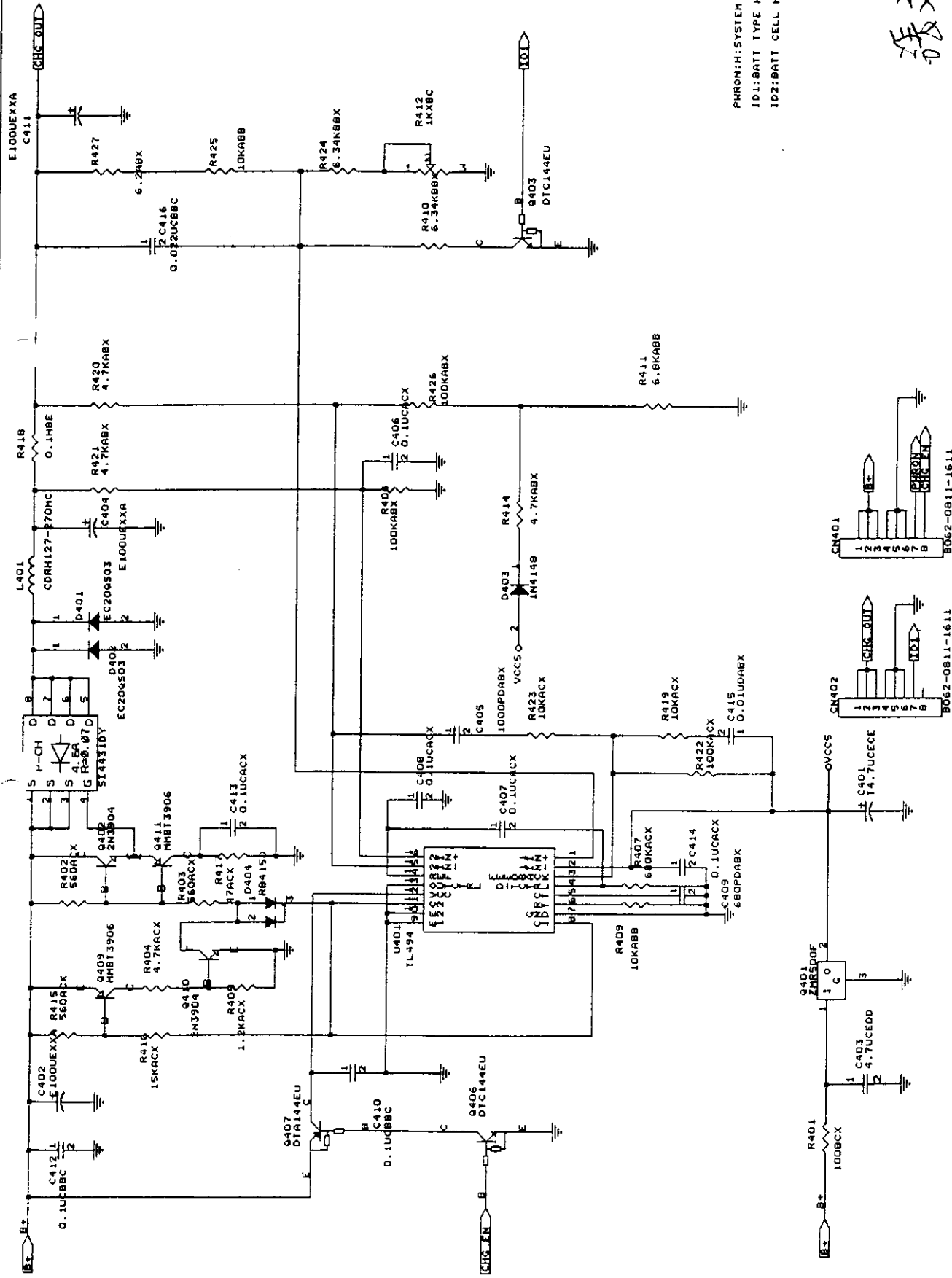
POWER	STR#	MODEM#	ACTN	LAN_TYPE	LANCTL#
1	1	0	1	1	0
1	0	0	1	1	0
0	1	1	1	1	1
1	0	1	1	1	1
1	1	0	0	1	0
1	0	1	0	1	1
0	1	1	0	1	1
1	1	0	1	0	0
1	0	0	1	0	0
0	1	1	0	0	1
1	0	1	0	0	1
0	1	0	0	0	0
1	0	0	0	0	0
0	1	1	0	0	1
1	0	1	0	0	1

INRUSH current circuit



DC/B to M/B connector



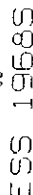
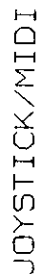


PHARON H: SYSTEM POWER ON CURRENT 1.0A
 ID1: BATT TYPE MINI-MH L: LI-ION
 ID2: BATT CELL N: 4 CELLS L: 8 CELLS

張文湧 10/9

FIRST INTERNATIONAL COMPUTER, INC.	
BY JASON CHANG	
Title	
ANBER 2.0 CHARGER CIRCUIT	
Size	Document Number
B	BATTERY CHARGER (PCB VER: D.8)
Date	October 15, 1998
	Page 1 of 1

- 1) U23 min20 change to K1524 from R6009
- 2) U22 min09 change to GNT02 from GNT09
- 3) Cancel 8C134
- 4) U23 min 58 add resister for DOCKING
- 5) Cancel 1251, 1250, CG9, CG48
- 6) Cancel R246, R247, CG7, CG46
- 7) Cancel 1252, 1245

[illegible]

243, C244, R750, 0750

084