DESCRIPTION OF CIRCUITRY

RULE PART NUMBER: 2.983 (d)(10)

THEORY OF OPERATION

1.0 PURPOSE

This report has been prepared to support the application for FCC Type Acceptance PER CODE OF FEDERAL REGULATIONS, TITLE 47, PARTS 2 AND 90 for the transmitter subsystem of the Transcrypt International / E.F. Johnson Radio Systems Model 242-538X Mobile. The report presents necessary information concerning electrical circuit description, measured performance and physical construction and configuration.

2.0 MOBILE

Introduction
The 5300-series transceivers contain the PC board assemblies listed below. Components are mounted on only the top side of all boards. Therefore, most components can be changed without removing the board from the chassis. General descriptions of the main sections such as the receiver, synthesizer, and exciter follow and detailed descriptions are located in later sections.
RF Board - Contains the receiver, synthesizer, and exciter sections.
PA Board - Contains the transmitter power amplifier section.
Audio/Logic - Contains the control logic and audio processing sections.
Display - Contains the display, display controller, and interface processor.
Interface - This small board provides the electrical connections between the display and audio/logic boards. It also contains the front panel controls and microphone jack.

Circuit Protection (Fuses)
Circuit protection is provided by a 15-ampere in-line power cable fuse, 3-ampere fuse F500 on the RF board (in the UN-switched battery supply line from the PA board), and by voltage regulators which automatically limit current. The 15-ampere power cable fuse protects the driver and final stages on the power amplifier board, and the 3-ampere fuse protects the remainder of the circuitry. In addition, there are two 0.6-ampere fuses on the audio/logic board. One fuse (F100) limits the current of the switched battery supply fed to accessory connector J101 and the microphone jack on the interface board. The other fuse (F300) limits the current of the 8-volt supply fed to modem jack J301.

Analog Mode

Receive Mode
The signal is routed from the antenna connector to the RF Board where it is filtered, amplified, and mixed with the first local oscillator frequency generated by the synthesizer. The resulting IF signal is also filtered and amplified and sent to the ABACUS chip.
The signal is then mixed with the second local oscillator frequency to create a second IF signal of 450 kHz. The second IF signal is then sampled at 14.4 Msps and downconverted to baseband. The baseband signal is then decimated to a lower sample rate that is selectable at 20 kHz. This signal is then routed via a serial interface using a differential current output to the ADSIC chip on the Digital Board.
On the Digital Board the ADSIC digitally filters the input signal, performs frequency discrimination to obtain the message signal and then routes the message signal to the DSP. The DSP first performs a carrier- detection squelch function on the radio. If a signal is determined to be present, the audio portion of the signal is resampled to an 8 kHz rate and then filtered appropriately. The filtered signal is then routed back to a D/A in the ADSIC to produce an analog signal for output to the audio power amplifier (PA) and then the speaker. Any detected signaling information is decoded and the resulting information is sent to the microcontroller.

Transmit Mode
The signal from the microphone is amplified by the audio PA and is then routed to the ADSIC chip where it is first digitized at a 16 ksps rate and then sent to the DSP. The DSP performs the required filtering, adds the desired signaling, converts the sample rate to 48 ksps and then sends the resulting signal back to a D/A in the ADSIC to produce the analog modulation signal for the VCO. The modulated VCO signal is then sent to the RF PA for transmission.

APCO 25 Digital Mode

Introduction
In APCO 25 Digital Mode, the carrier is modulated with 4 discrete deviation levels. These levels are ± 600 Hz and ± 1800 Hz. Digitized voice is created using an IMBE™ vocoder.

Receive Mode
The signal is processed in the same way as an analog mode transmission until after the squelch function is performed. If a signal is detected to be present, the DSP resamples the signal from 20 kHz to 24 kHz. This is done so that the sample rate is an integer multiple (5x) of the data rate of the digital modulation which is 4800 symbols/sec (9600 bits/sec). The resampled signal is then processed by a demodulator routine to extract the digital information. The resulting bit stream (9600 bps) is sent to a routine that performs unframing, error-correction, and voice decoding. The result of these operations is a reconstructed voice signal sampled at 8 kHz. The sampled voice signal is sent to a D/A in the ADSIC to produce an analog signal for output to the audio power amplifier and speaker.

Transmit Mode
The microphone signal is processed as in analog mode until it reaches the DSP. At this point the audio signal is processed by a voice encoding routine to digitize the information. The resulting samples are then converted to a bit stream that is placed into the proper framing structure and error protected. The resulting bit stream has a bit rate of 9600 Hz.
This bit stream in then encoded, two bits at a time, into a digital level corresponding to one of the four allowable frequency deviations. This produces 16-bit symbols with a rate of 4800 Hz. The symbols are resampled to a rate of 48 kHz and filtered to comply with channel bandwidth requirements. The filtered signal is then sent to a D/A in the ADSIC to produce the analog modulation signal for the VCO. The modulated VCO signal is then mixed up to the final transmit frequency and then sent to the RF PA for transmission.

RF Board
NOTE: The RF Board is not field serviceable. It must be replaced as a unit with a new board.

The receiver front end consists of a preselector, RF amplifier, second preselector, and mixer. The 800 MHz board uses stripline technology for the preselector. The RF amplifier is a dual-gate gallium-arsenide IC. The mixer is a double-balanced, transformer-coupled active mixer. Injection is provided by the VCO through an injection filter. See Table 2-1 for local oscillator (LO) and first IF information.

Table 2-1 LO and First IF Frequencies

	800 MHz
LO Frequency range	776.65 - 796.65 MHz
First IF Frequency	73.35 MHz

The frequency generation function is performed by three ICs and associated circuitry. The reference oscillator provides a frequency standard to the synthesizer/prescaler IC which controls the VCO IC. The VCO IC actually generates the first LO and transmit injection signals and buffers them to the required power level. The synthesizer/prescaler circuit module incorporates frequency division and comparison circuitry to keep the VCO signals stable. The synthesizer/ prescaler IC is controlled by the microcontroller through a serial bus. Most of the synthesizer circuitry is enclosed in rigid metal on the RF Board to reduce microphonic effects.
The receiver back end consists of a two-pole crystal filter, IF amplifier, a second two-pole crystalfilter, and the ABACUS digital back-end IC. The two pole filters are wide enough to accommodate 5 kHz modulation. Final IF filtering is done digitally in the ADSIC.
The ABACUS digital back-end chip consists of an amplifier, second mixer, IF analog-to-digital converter, a baseband down-converter, and a 2.4 MHz synthesis circuit to provide a clock to the ADSIC on the Digital Board. The second LO is generated by discrete components external to the ABACUS. The output of the ABACUS is a digital bit stream that is current driven on a differential pair to reduce noise generation.

The exciter consists of an RF power amplifier IC that amplifies an injection signal from the VCO. Transmit power is controlled by two custom ICs that monitor the output of a directional coupler and adjust the power amplifier control voltages correspondingly. The signal passes through a Rx/Tx switch that uses PIN diodes to automatically provide an appropriate interface to transmit or receive signals. Antenna selection is done mechanically on the front panel.

Digital and Audio/Logic Board
The Digital and Audio/Logic Board contains the ADSIC, DSP (TMS320C50), static RAM, FLASH memory, and a programmable logic IC (revised versions only). The RF Board and Keypad/Display Board are connected to the Digital Board. The ADSIC performs the Frequency Discrimination and receiver filtering functions. It also performs analog-to-digital (A/D) and digital-to-analog (D/A) conversion. The DSP performs demodulation and modulation, voice encoding and decoding, audio filtering, and squelch signaling. The software for the radio is stored in FLASH memory that is loaded in to static RAM at turn-on. The programmable logic IC controls which device (Flash, SRAM, or UART) is connected to the DSP address and data bus.

Display Board
The Display Board contains the microcontroller (HC08), audio circuits, front LCD display assembly, display driver, and 5V analog and 5V digital regulators. All interfaces to the side connector and the switches are on this board. The microcontroller determines transmit/receive frequencies, power levels, and display content. It communicates with the DSP via a serial interface.

3.0 RF BOARD CIRCUIT DESCRIPTION

Frequency Generation Unit
The Frequency Generation Unit (FGU) consists of these three major sections: (1) high stability reference oscillator, (2) fractional-N synthesizer, and (3) VCO buffer. A 5-volt regulator supplies power to the FGU. The regulator output voltage is filtered and then distributed to the transmit and receive VCOs and the VCO buffer IC. The mixer LO injection signal and transmit frequency are generated by the receive VCO and transmit VCO, respectively. The receive VCO uses an external active device, and the transmit VCO active device is a transistor inside the VCO buffer.
The receive VCO is a Colpitts-type oscillator. The receive VCO signal is received by the VCO buffer where it is amplified by a buffer inside the IC. The amplified signal is routed through a low-pass filter and injected as the first LO signal into the mixer. In the VCO buffer, the receive VCO signal is also routed to an internal prescaler buffer. The buffered output is applied to a low-pass filter. After filtering, the signal is routed to a prescaler divider in the synthesizer.
The divide ratios for the prescaler circuits are determined from information stored in an EEPROM. The microprocessor extracts data for the division ratio as determined by the position of the channel-select switch and routes the signal to a comparator in the synthesizer. A 16.8 MHz reference oscillator applies the 16.8 MHz signal to the synthesizer. The oscillator signal is divided into one of three pre-determined frequencies. A time-based algorithm is used to generate the fractional-N ratio.
If the two frequencies in the synthesizer's comparator differ, an error voltage is produced. The phase detector error voltage is applied to the loop filter. The filtered voltage alters the VCO frequency until the correct frequency is synthesized.
In the transmit mode, the modulation of the carrier is achieved by using a two-port modulation technique. The modulation for low frequency tones, such as CTCSS and DCS, is achieved by injecting the tones into the A/D section of the fractional-N divider, generating the required deviation. Modulation of the high frequency audio signals is achieved by modulating the varactor through a frequency compensation network.
The transmit VCO signal is amplified by an internal buffer, routed through a low-pass filter, and then sent to the transmit power amplifier module. The reference oscillator supplies a 16.8 MHz clock to the synthesizer where it is divided down to a 2.1 MHz clock. This divided down clock is fed to the ABACUS IC.

Antenna Switch
A pair of diodes is used to electronically steer the RF signal between the receiver and transmitter. In transmit mode, RF is routed through a transmit switching diode and sent to the antenna. In receive mode, RF is received from the antenna, routed through a receive switching diode and applied to the RF amplifier.

Receiver Front End
The RF signal from the antenna is sent through a bandpass filter. The bandpass filter is electronically tuned by the microcontroller via the D/A IC by applying a control voltage to the varactor diodes in the filter. The D/A output range is extended through the use of a current mirror. Wideband operation of the filter is achieved by retuning the bandpass filter across the band.
The output of the bandpass filter is applied to a wideband amplifier. After being amplified by the RF amplifier, the RF signal is further filtered by a second broadband, fixed tuned, bandpass filter to improve spurious rejection.

The filtered RF signal is routed via a broadband 50 Ω transformer to the input of a broadband mixer/buffer. The mixer uses GaAs FETs in a double-balanced Gilbert Cell configuration. The RF signal is mixed with a first LO signal of about –10 dBm supplied by the FGU. Mixing of the RF and the first LO results in an output signal which is the first IF frequency according to Figure 2-1. The first IF signal output is routed through a transformer and impedance matching components and is then applied to a two- pole crystal filter. The 2-pole crystal filter removes unwanted mixer products.

Receiver Back End

The output of the crystal filter is matched to the input of the IF buffer amplifier transistor. The output of the IF amplifier is applied to a second crystal filter through a matching circuit. This filter supplies further attenuation at the IF sidebands to increase radio selectivity.

In the ABACUS IC the first IF frequency is amplified and then downconverted to 450 KHz, the second IF frequency. At this point, the analog signal is converted into two digital bit streams via a sigma-delta A/D converter. The bit streams are then digitally filtered and mixed down to baseband and filtered again. The differential output data stream is then sent to the ADSIC on the Digital Board where it is processed to produce the recovered audio.

The ABACUS IC is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing and signal type, is controlled by the microcontroller. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal digital filters in the ABACUS IC. The ABACUS IC contains a feedback AGC circuit to expand the dynamic range of the sigma-delta converter. The differential output data contains the quadrature (I and Q) information in 16-bit words, the AGC information in a 9-bit word, imbedded word sync information and fill bits dependent on sampling speed. A fractional-N synthesizer is also incorporated on the ABACUS IC for 2nd LO generation.

The 2nd LO/VCO is a Colpitts oscillator. The VCO has a varactor diode to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter.

4.0 DISPLAY BOARD

Introduction

The Display Board contains a LCD Display and Display Driver. The Display Board interfaces with the Digital board via J4, with the Accessory rigid flex circuit via J13, and with the side buttons, PTT switch, and accessory connector through J5.

4.1 AUDIO/LOGIC BOARD

Functional Description

The microcontroller provides an interface between the hardware and the DSP (on the Digital Board). When the user presses a control such as the channel selector switch, a side option or PTT switch the microcontroller signals the change to the DSP. Conversely, when the DSP needs to change the display or an LED, it signals the microcontroller which then performs the action. The microcontroller also controls peripheral ICs such as the synthesizer, reference oscillator, display, and ADSIC.

The microcontroller uses a serial bus to communicate with the DSP and another RS232 bus to communicate with the side port connector. The side connector bus is used for external communication with a computer running the programming or tuning software. Finally, the microcontroller maintains certain operating parameters in the associated EEPROM which is controlled via a two-wire serial bus.

Microcontroller

The microcontroller is a Motorola M68HC08XL36 chip. It includes 28K bytes of internal ROM memory and 1K byte of internal SRAM. It does not have an external bus and therefore cannot access any external program memory.

The clock to the microcontroller is provided by Y1 and an internal oscillator. The frequency of the clock can be slightly offset by polarizing the base of Q3 through software control. This prevents RF interference on some channels caused by the clock.

The microcontroller contains an SPI-compatible synchronous serial bus. This bus consists of pins MISO (U1-53), MOSI (U1-52), SPSCK (U1-50), and a chip enable for each device with which it communicates. The devices which communicate with the microcontroller through this bus are as follows:

- Top Display driver chip (Top Display board)
- Front Display driver chip (Digital board)
- ADSIC chip (Digital board)

• Reference Oscillator (RF Board)
• Front-End DAC (RF Board)
• Synthesizer chip (RF Board)
• Optional DES board.

The microcontroller communicates with the DSP chip (Digital board) through a custom serial bus. This serial port includes pins PTA3 (U1-8), PTA4 (U1-9), PTA5 (U1-10), PTA6 (U1-11), and PTA7 (U1-12).

The microcontroller uses its SCI asynchronous serial bus for external communication with a computer running programming or tuning software. The SCI pins RxD (U1-42) and TxD (U1-43) are connected to RS232 driver receiver U5. The other signals of a standard RS232 computer port (DSR, DTR, CTS, RTS) are generated using microcontroller input/outputs.

The RS232 driver U5 converts signals from a logic level of 0 and 5 V to a logic level of –10 and +10V. The chip contains an internal charge pump to generate –10V and +10V from the 5V power supply. The RS232 chip can be put in standby mode by leaving the line K/F-RS232* floating. This line is connected to the side connector which allows it to turn on U5 only when a computer is connected to the radio.

The keypad interfaces with the microcontroller through eight lines (4 rows x 4 columns). The microcontroller regularly polls these lines to detect a key closure.

Serial EEPROM U3 is used to store some important radio parameters. The EEPROM is read to or written from using I/O lines PTC6 and PTC7 of the microcontroller. PTC6 is used for the Data line, and PTC7 is used as a clock line.

Shift register U14 expands the number of I/O lines of the microcontroller. It uses the same data and clock as the EEPROM plus an additional line (U1-45) to control the latch. Other user interface inputs such as the PTT and toggle switches are directly connected to an I/O line of the microcontroller.

Audio Circuits

The audio circuits on the Audio/Logic Board consist of four op amps, two audio power amplifiers, and an analog switch.

In receive mode, the analog receive waveform created by the ADSIC (on the Digital Board) is fed to an op amp summing amplifier (U9B). This amplifier sums in the audio tones that are generated by the microcontroller. The output of the summing amplifier is then fed through the volume control potentiometer to a second op amp buffer.

The buffer output is routed to a pair of audio power amplifiers: one to drive the internal speaker and another to drive the external speaker. Only one of these audio power amplifiers can be active at a time. The active power amplifier is selected by the OPT SEL 1 line (J5-12). The MUTE line turns the active power amplifier on or off by disconnecting the battery voltage from the audio power amplifier IC using the transistor Q4. Transistors Q8 and Q9 and their associated RC networks remove popping sounds from the speaker audio by delaying the unmuting of the audio amp compared to the unMUTE command.

In transmit mode, the audio for transmission can be selected from either an internal or external microphone, depending upon the presence of an external microphone and which PTT is pressed. An analog switch is used to route either the internal or external microphone signal to the microphone amplifier. The external microphone signal is buffered by an op amp. The microphone amplifier has a gain of ten, and is equipped with a pair of clipping diodes to prevent the amplified microphone signal from over-driving the A/D input on the ADSIC.

5.0 TRANSMIT FREQUENCY DETERMINATION

The operational frequency of the transmitter is determined by the PLL (Phase-Locked-Loop) consisting of synthesizer U204 and VCO circuit Q202/U201. Reference oscillator U203 generates and supplies a reference signal of 16.8 MHz to synthesizer. The synthesizer contains a programmable reference divider, programmable A and B dividers, a programmable prescaler counter (P), and a programmable fractional N divider with two programmable values (N numerator and N denominator).

All of these dividers are programmed through the serial interface which connects the synthesizer to the controller microprocessor. The 16.8 MHz reference oscillator frequency is divided down to a synthesizer reference frequency of 2.1, 2.4, or 2.225 MHz. This signal is fed to the phase detector which generates the steering voltage for the VCO. The output of the VCO circuit is coupled back and divided by AP+B and then divided by the fractional divider and fed into the second input of the phase detector. The VCO buffer has two outputs. One input goes to the input of Rx mixer chip U2, and the other is applied to the input of power amplifier module U105.

6.0 TRANSMITTER

The transmitter consists of three major sections: Harmonic Filter, RF Power Amplifier, Directional Coupler and the Over Current shutdown circuit.
The RF signal from the PA module is routed through a coupler, then through the harmonic filter, then to the antenna switch. The RF power amplifier module is a wide-band multi-stage amplifier. The nominal input and output impedance of the power amplifier is 50 Ω. The DC bias for the RF power amplifier is controlled by a switching transistor. The microcontroller uses the D/A IC to produce a ready signal for the transmit ALC IC. The synthesizer sends a LOC signal to the transmit ALC IC. When both the ready signal and LOC signal are available to the transmit ALC IC, the switching transistor for the RF power amplifier is turned on.
A coupler module samples the forward power and the reverse power of the PA output voltage. Reverse power is present when there is other than 50 Ω impedance at the antenna port. Sampling is achieved by coupling some of the forward and/or reverse power for rectification and summing. The resulting DC voltage is then applied to the transmit ALC IC as an RF strength indicator.
The transmit ALC circuit is the core of the power control loop. Circuits in the transmit ALC module compare the RF strength indicator to a reference value and generate a bias signal that is applied to the base of a transistor. This transistor varies the DC control voltage applied to the RF PA controlling the RF power.

6.1 HARMONIC FILTER

The transmitter harmonic filter consists of C148-C151, L126, L127, and L128.The circuit is essentially a seven-pole low-pass filter.

6.2 POWER AMPLIFIER MODULE (U600), FINAL (Q651)

Power amplifier module U600 on the PA board has approximately 17.9 dB of gain which amplifies the exciter signal to approximately 23 watts. Pins 2, 3, and 4 of U600 are the supply voltage inputs to three separate gain stages. The supply voltage on pin 2 (VS1) is switched by Q600 and limited to 12 volts by CR601 and R600. Switch Q600 is controlled by the same signal used to control 8V transmit switch Q505/Q504.
The supply voltage applied to pins 3 and 4 (VS2/VS3) is the UN-switched battery supply from the power jack. Therefore, power is applied to these pins even when transceiver power is turned off. The current to pin 4 flows through R601, and the power control circuit senses transmitter current by monitoring the voltage drop across this resistor.

6.3 DIRECTIONAL COUPLER, LOW-PASS FILTER

The transmit signal is coupled by C621 to a directional coupler formed by adjacent sections of microstrip. The forward component of output power is rectified by CR603 and developed across R606 and then fed to the power control circuit. Reverse power is not detected in this transceiver.
From the directional coupler the transmit signal is fed to a low-pass harmonic filter formed by C624-C627 and several sections of microstrip. This filter attenuates harmonic frequencies occurring above the transmit band. R607 dissipates static buildup on the antenna.
The ambient power amplifier temperature is sensed by thermistor R601. The resistance of a thermistor decreases as temperature increases. R601 and R143 on the audio/logic board form a voltage divider, and the voltage across this divider is monitored by an A/D converter input of the microcontroller (pin 63). If the PA temperature increases above limits set in software, the power is first cut back. Then if it continues to rise, the transmitter is turned off.

6.4 OVERCURRENT SHUTDOWN

The circuit consisting of U505 and U502-b monitors the current flowing through R550 into the collector terminal of Q509, the final RF amplifier stage. When the current exceeds approximately 10 A, the monitoring circuit reduces the RF drive to Q509 and through hysteresis holds the drive in its low state until the Push-to-Talk button has been released.
U505 converts the voltage appearing across R550 to a ground referenced voltage at R553 that is proportional to the collector current drawn by the final rf stage. Following this circuit, a comparator circuit, U502-b, actuates when the voltage across R553 exceeds a preset threshold and pulls down the reference voltage at U502, pin 3 to a low value. Once triggered, the comparator remains in the low state until the transmitter has been turned off.