SECTION 5 CIRCUIT DESCRIPTION

5.1 GENERAL TRANSCEIVER DESCRIPTION

5.1.1 INTRODUCTION

The E.F. Johnson 5300 is a microcontroller-based radio that uses a Digital Signal Processor (DSP) to provide the following modes of operation:

Narrowband Analog - FM modulation with a maximum deviation of 2.5 kHz. This mode is usually used in systems where the channel spacing is 12.5 kHz. Call Guard (CTCSS or DCS) subaudible squelch signaling can be used in this mode.

Wideband Analog - FM modulation with a maximum deviation of 5 kHz. This mode is usually used in systems where the channel spacing is 25 kHz or 30 kHz. Call Guard (CTCSS or DCS) subaudible squelch signaling can be used in this mode.

Project 25 Digital - The voice is digitized, error corrected, optionally encrypted and transmitted using C4FM modulation according to the Project 25 standard. This mode can be used in channel spacings of 12.5 kHz.

DES/DES-XL Encryption - This mode is compatible with the Motorola DES and DES-XL protocols. Voice is digitized, encrypted, and transmitted using FSK modulation. This mode can be used in channel spacings of 25 kHz. The DSP processes the received signals and generates the appropriate output signals. The microcontroller controls the hardware and provides an interface between hardware and DSP.

5.1.2 PC BOARDS

The 5300-series mobile contains the following PC board assemblies:

RF Board - Contains the receiver, synthesizer, and exciter sections.

PA Board - Contains the transmitter power amplifier, power control, and main DC power switching sections.

Logic Board - Contains the digital signal processing (DSP), control logic, and audio processing sections.

Interface Board - A small board that provides the electrical connections between the logic and RF/PA boards. It also contains the audio amplifier and volume control circuits for internal and external speakers.

Display Controller - Contains a microcontroller which provides an interface between the controller on the logic board and the front panel display and switches.

Display Board - Contains the liquid crystal display, option switch keypad, and display drivers. In addition, it contains the backlight for the display and keypad.

5.1.3 CIRCUIT PROTECTION (FUSES)

Circuit protection is provided as follows:

- A 15-ampere fuse in the power cable provides overall transceiver protection.
- A 2-ampere fuse on the RF board protects circuits on that board.
- F700 (2-ampere) on the display controller board protects the Sw B+ output of the microphone connector.
- F1 on the logic board protects the Sw B+ output of universal interface connector J5.
- The various voltage regulators provide circuit protection by automatically limiting current.

5.1.4 ANALOG MODE DESCRIPTION

Receive Mode

The RF signal is routed from the antenna connector to the RF Board where it is filtered, amplified, and mixed with the first local oscillator frequency generated by the synthesizer. The resulting IF signal is also filtered and amplified and sent to the ABACUS chip.

The signal is then mixed with the second local oscillator frequency to create a second IF signal of 450 kHz. The second IF signal is then sampled at 14.4 Msps and downconverted to baseband. The baseband

signal is then decimated to a lower sample rate that is selectable at 20 kHz. This signal is then routed via a serial interface using a differential current output to the ADSIC U3 on the logic board.

On the logic board ADSIC U3 digitally filters the input signal, performs frequency discrimination to obtain the message signal, and then routes the message signal to DSP (Digital Signal Processor) U12. The DSP first performs a carrier-detection squelch function on the radio. If a signal is determined to be present, the audio portion of the signal is resampled to an 8 kHz rate and then filtered appropriately. The filtered signal is then routed back to a D/A in the ADSIC to produce an analog signal for output to the audio power amplifier (PA) and then the speaker. Any detected signaling information is decoded and the resulting information is sent to the microcontroller.

Transmit Mode

The signal from the microphone is amplified by the audio PA and is then routed to ADSIC U3 where it is first digitized at a 16 ksps rate and then sent to DSP U12. The DSP performs the required filtering, adds the desired signaling, converts the sample rate to 48 ksps and then sends the resulting signal back to a D/A in the ADSIC to produce the analog modulation signal for the VCO. The modulated VCO signal is then sent to the RF PA for amplification.

5.1.5 PROJECT 25 DIGITAL MODE

Introduction

In Project 25 Digital Mode, the carrier is modulated with four discrete deviation levels of ± 600 Hz and ± 1800 Hz. Digitized voice is created using an IMBE™ vocoder.

Receive Mode

The signal is processed in the same way as an analog mode transmission until after the squelch function is performed. If a signal is detected to be present, DSP U12 resamples the signal from 20 kHz to 24 kHz. This is done so that the sample rate is an integer multiple (5x) of the data rate of the digital modulation which is 4800 symbols/sec (9600 bits/sec).

The resampled signal is then processed by a demodulator routine to extract the digital information. The resulting bit stream (9600 bps) is sent to a routine that performs unframing, error-correction, and voice decoding. The result of these operations is a reconstructed voice signal sampled at 8 kHz. The sampled voice signal is sent to a D/A in ADSIC U3 to produce an analog signal for output to the audio power amplifier and speaker.

Transmit Mode

The microphone signal is processed as in the analog mode until it reaches DSP U12. At this point the audio signal is processed by a voice encoding routine to digitize the information. The resulting samples are then converted to a bit stream that is placed into the proper framing structure and error protected. The resulting bit stream has a bit rate of 9600 Hz.

This bit stream is then encoded, two bits at a time, into a digital level corresponding to one of the four allowable frequency deviations. This produces 16-bit symbols with a rate of 4800 Hz. The symbols are resampled to a rate of 48 kHz and filtered to comply with channel bandwidth requirements. The filtered signal is then sent to a D/A in ADSIC U3 to produce the analog modulation signal for the VCO. The modulated VCO signal is then mixed up to the final transmit frequency and then sent to the RF board power amplifier section.

5.2 REVISED VHF RF BOARD

NOTE: The RF Board is not field serviceable. Therefore, it must be replaced if it is defective.

5.2.1 RF BOARD OVERVIEW

This description applies to the revised VHF RF board. Refer to Section 5.3 for information on the unrevised VHF RF board and all 800 MHz RF boards. The revised VHF RF board is used in standard power transceivers that have a revision letter of “H” or higher or 100W models that have a revision letter of “C” or higher (see page 1-8).

The receiver front end consists of a preselector, an RF amplifier, a second preselector, and a mixer (see Figure 5-1). Both preselectors are varactor-tuned, two-

REVISED VHF RF BOARD DESCRIPTION (Cont'd)

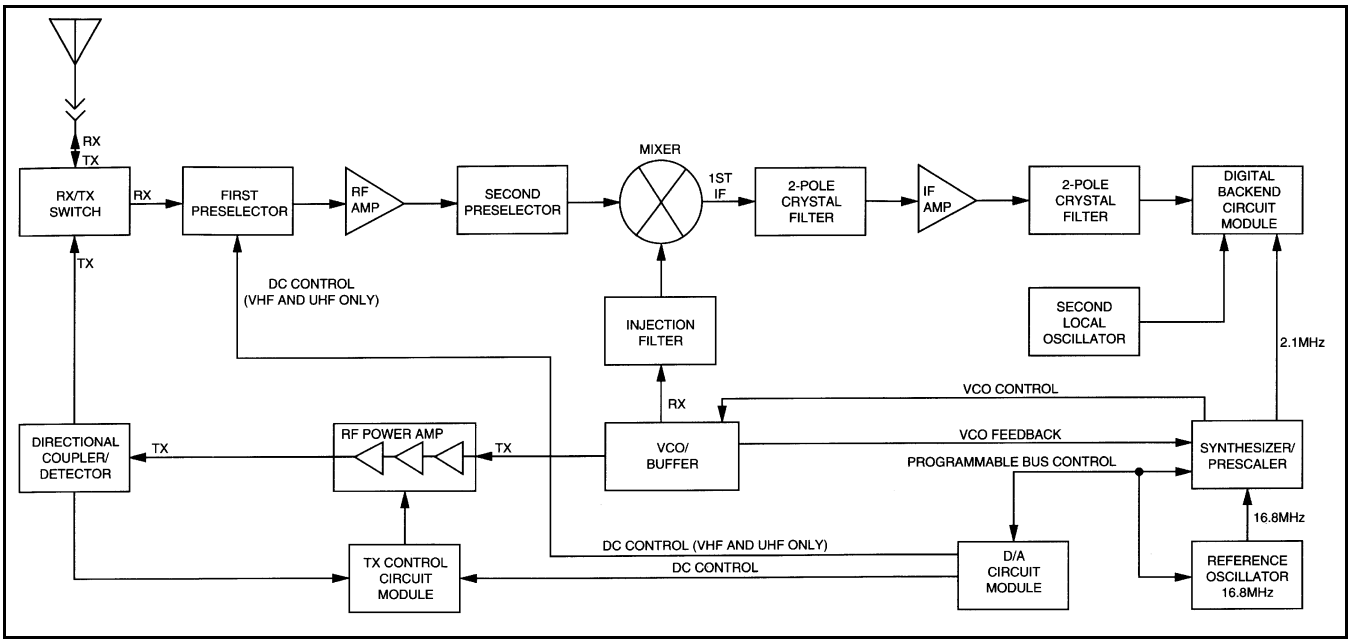


Figure 5-1 RF Board Block Diagram

pole filters controlled by the control logic. The RF amplifier is a dual-gate, gallium-arsenide based IC. The mixer is a double-balanced, active mixer coupled by transformers. Injection is provided by the VCO through an injection filter.

The frequency generation function is performed by three ICs and associated circuitry. The reference oscillator provides a frequency standard to the synthesizer/prescaler IC which controls the VCO IC. The VCO IC actually generates the first LO and transmit-injection signals and buffers them to the required power level. The synthesizer/prescaler circuit module incorporates frequency-division and comparison circuitry to keep the VCO signals stable. The synthesizer/prescaler IC is controlled by the control logic through a serial bus. Most of the synthesizer circuitry is enclosed in rigid metal cans to reduce microphonic effects.

The receiver back end consists of a two-pole crystal filter, an IF amplifier, a second two-pole crystal filter, and the digital back-end IC (ABACUS). The two-pole filters are wide enough to accommodate 5 kHz modulation. Final IF filtering is done digitally in the ADSIC.

The digital back-end IC (ABACUS) consists of an amplifier, the second mixer, an IF analog-to-digital converter, a baseband down-converter, and a 2.4 MHz synthesis circuit. The second LO is generated by discrete components external to the IC. The output of the ABACUS IC is a digital bit stream that is current driven on a differential pair for a reduction in noise generation.

The transmitter consists of an RF PA IC that gets an injection signal from the VCO. Transmit power is controlled by two custom ICs that monitor the output of a directional coupler and adjust PA control voltages correspondingly. The signal passes through a Rx/Tx switch that uses PIN diodes to automatically provide an appropriate interface to transmit or receive signals.

5.2.2 FREQUENCY GENERATION UNIT (FGU)

The frequency generation unit (FGU) consists of three major sections: the high stability reference oscillator (U203), the fractional-N synthesizer (U204,) and the VCO buffer (U201). A 5V regulator (U202), supplies power to the FGU. The synthesizer receives the 5V REG at U204, and applies it to a filtering circuit within the module and capacitor C253. The well-filtered 5-volt output at U204, pin 19 is distributed to the Tx and Rx VCOs and the VCO buffer IC. The mixer's LO injection signal and transmit frequency are generated by the Rx VCO and Tx VCO, respectively. The Rx VCO uses an external active

REVISED VHF RF BOARD DESCRIPTION (Cont'd)

device (Q202), whereas the VHF Tx VCO's active device is a transistor inside the VCO buffer. The base and emitter connections of this internal transistor are pins 11 and 12 of U201.

The Rx VCO is a Colpitts-type oscillator, with capacitors C235 and C236 providing feedback. The Rx VCO transistor (Q202) is turned on when pin 38 of U204 switches from high to low. The Rx VCO signal is received by the VCO buffer at U201, pin 9, where it is amplified by a buffer inside the IC. The amplified signal at pin 2 is routed through a low-pass filter (L201 and associated capacitors) and injected as the first LO signal into the mixer (U2, pin 8). In the VCO buffer, the Rx VCO signal (or the Tx VCO signal during transmit) is also routed to an internal prescaler buffer. The buffered output at U201, pin 16 is applied to a low-pass filter (L205 and associated capacitors). After filtering, the signal is routed to a prescaler divider in the synthesizer at U204, pin 21.

The divide ratios for the prescaler circuits are determined from information stored in memory during programming. The microcontroller extracts data for the division ratio as determined by the selected channel and sends that information to a comparator in the synthesizer via a bus. A 16.8 MHz reference oscillator, U203, applies the 16.8 MHz signal to the synthesizer at U204 pin 14. The oscillator signal is divided into one of three pre-determined frequencies. A time-based algorithm is used to generate the fractional-N ratio.

If the two frequencies in the synthesizer's comparator differ, a control (error) voltage is produced. The phase detector error voltage (V control) at pins 31 and 33 of U204 is applied to the loop filter consisting of resistors R211, R212, and R213, and capacitors C244, C246, C247, and C248. The filtered voltage alters the VCO frequency until the correct frequency is synthesized. The phase detector gain is set by components connected to U204, pins 28 and 29.

In the Tx mode, U204, pin 38 goes high and U201, pin 14 goes low, which turns off transistor Q202 and turns on the internal Tx VCO transistor in U204. The Tx VCO feedback capacitors are C219 and C220. Varactor diode CR203/CR207 sets the Tx frequency while varactor CR202 is the Tx modulation varactor. The modulation of the carrier is achieved by using a two-port modulation technique. The modulation of low frequency tones is achieved by injecting the tones into the A/D section of the fractional-N synthesizer. The digitized signal is modulated by the fractional-N divider, generating the required deviation. Modulation of the high-frequency audio signals is achieved by modulating the varactor (CR203) through a frequency compensation network. Resistors R207 and R208 form a potential divider for the higher-frequency audio signals.

In order to cover the very wide bandwidths, positive and negative Vcontrol voltages are used. High control voltages are achieved using positive and negative multipliers. The positive voltage multiplier circuit consists of components CR204, C256, C257, and reservoir capacitor C258. The negative multiplier circuit consists of components CR205, CR206, C266, C267, and reservoir capacitor C254.

Out-of-phase clocks for the positive multiplier appear at U204, pins 9 and 10. Out-of-phase clocks for the negative multiplier appear at U204, pins 7 and 8, and only when the negative V-control is required (that is, when the VCO frequency exceeds the crossover frequency). When the negative V-control is not required, transistor Q201 is turned on, and capacitor C259 discharges. The 13V supply generated by the positive multiplier is used to power-up the phase detector circuitry. The negative V-control is applied to the anodes of the VCO varactors.

The Tx VCO signal is amplified by an internal buffer in U201, routed through a low pass filter and routed to the Tx PA module, U105, pin 1. The Tx and Rx VCOs and buffers are activated via a control signal from U204, pin 38.

The reference oscillator supplies a 16.8 MHz clock to the synthesizer where it is divided down to a 2.1 MHz clock. This divided-down clock is fed to the ABACUS IC (U401), where it is further processed for internal use.

5.2.3 ANTENNA SWITCH

The antenna switch is a current device consisting of a pair of diodes (CR108/ CR109) that electronically steer RF between the receiver and the transmitter. In the transmit mode, RF is routed through transmit

switching diode CR108, and sent to the antenna. In the receive mode, RF is received from the antenna, routed through receive switching diode CR109, and applied to the RF amplifier Q1. In transmit, bias current, sourced from U101, pin 21, is routed through L105, U104, CR108, and L122. Sinking of the bias current is through the transmit ALC module, U101, pin 19. In the receive mode, bias current, sourced from switched B+, is routed through Q107 (pin 3 to pin 2), L121, CR109, and L122. Sinking of the bias current is through the 5-volt regulator, U106, pin 8.

5.2.4 RECEIVER FRONT END

The RF signal is received by the antenna and coupled through the external RF switch. The filtered RF signal is passed through the antenna switch (CR109) and applied to a bandpass filter consisting of L11 through L14, CR1 through CR9, C4, C2, and C3. The bandpass filter is tuned by applying a control voltage to the varactor diodes in the filter (CR1 through CR9).

The bandpass filter is electronically tuned by the D/A IC (U102), which is controlled by the microcomputer.The D/A output range is extended through the use of a current mirror consisting of Q108 and R115 and R116. When Q108 is turned on via R115, the D/A output is reduced due to the voltage drop across R116. Depending on the carrier frequency, the microcomputer will turn Q108 on or off. Wideband operation of the filter is achieved by retuning the bandpass filter across the band.

The output of the bandpass filter is applied to RF amplifier Q1. The RF signal is then further filtered by a second broadband, fixed-tuned, bandpass filter consisting of C6, C7, C8, C80, C86, C87, C88, C97, C99, L3, L4, L5, and L30 to improve the spurious rejection.

The filtered RF signal is routed through a broadband 50-ohm transformer (T1) to the input of a broadband mixer/buffer (U2). Mixer U2 uses GaAs FETs in a double-balanced, Gilbert Cell configuration.

The RF signal is applied to the mixer at U2 pins 1 and 15. An injection signal (1st LO) of about –10 dBm supplied by the FGU is applied to U2, pin 8. Mixing of the RF and the 1st LO results in an output signal that is the first IF frequency. The first IF frequency is 45.15 MHz higher than the carrier frequency. The 1st IF signal output at U2, pins 4 and 6 is routed through transformer T2 and impedance matching components, and applied to a two-pole crystal filter (FL1), which is the final stage of the receiver front end. The two-pole crystal filter removes unwanted mixer products. Impedance matching between the output of the transformer (T2) and the input of the filter (FL1) is accomplished by C605 and L605.

5.2.5 RECEIVER BACK END

The output of crystal filter FL1 is matched to the input of IF buffer amplifier transistor Q601 by components C610 and L604. Transistor Q601 is biased by the 5V regulator (U202). The IF frequency on the collector of Q601 is applied to a second crystal filter through a matching circuit. The second crystal filter (FL2) input is matched by C604, C603, and L601. The filter supplies further attenuation at the IF sidebands to increase the radios selectivity. The output of FL2 routed to pin 32 of U401 through a matching circuit which consists of L603, L606, and C608.

In the ABACUS IC (U401), the first IF frequency is amplified and then down-converted to the second IF frequency of 450 kHz. At this point, the analog signal is converted into two digital bit streams by a sigma-delta A/D converter. The bit streams are then digitally filtered, mixed down to baseband, and filtered again. The differential output data stream is then sent to the logic board where it is decoded to produce the recovered audio.

The ABACUS IC (U401) is electronically programmable. The amount of filtering, which is dependent on the radio channel spacing and signal type, is controlled by the microcontroller. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal digital filters in the ABACUS IC. The ABACUS IC contains a feedback AGC circuit to expand the dynamic range of the sigma-delta converter. The differential output data contains the quadrature (I and Q) information in 16-bit words, the AGC information in a 9-bit word, imbedded word sync information, and fill bits dependent on sampling speed. A fractional N synthesizer is also incorporated on the ABACUS IC for 2nd LO generation.

The 2nd LO/VCO is a Colpitts oscillator built around transistor Q401. The VCO has a varactor diode, VR401, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C426, C428, and R413.

5.2.6 TRANSMITTER

The transmitter consists of three major sections:

- Harmonic Filter
- RF Power Amplifier Module
- ALC Circuits

RF from the PA module (U105) is routed through the coupler (U104), then through the harmonic filtering network, and on to the antenna switch (CR108). The harmonic filtering circuit is composed of the following components: L126, L127, L128, C149, C150, and C151. Resistor R117 provides a current-limited 5V to J2.

The RF power amplifier module (U105) is a wide-band, three-stage amplifier. Nominal input and output impedance of U105 is 50 ohms. The DC bias for U105 is on pins 2, 4, 5. In the transmit mode, the voltage on U105, pins 2 and 4 (close to the B+ level) is obtained via switching transistor Q101. Transistor Q101 receives its control base signal as follows:

- The microcomputer keys the D/A IC to produce a ready signal at U 102 pin 3,
- the ready signal at U102 pin 3 is applied to the Tx ALC IC at U101 pin 14 (5V), and
- the synthesizer sends a LOC signal to the Tx ALC IC (U204 pin 40 to U101 pin 16).

When the LOC signal and the ready signal are both received, the Tx ALC IC (pin 13) sends a control signal to turn on transistor Q101.

Coupler module U104 samples the forward and reverse power of the PA output voltage. Reverse power is present when there is other than 50 ohms impedance at the antenna port. Sampling is achieved by coupling some of the forward and/or reverse power, and applying it to CR102 and CRI03 for rectification and summing. The resultant DC signal is then applied to the Tx ALC IC (U101, pin 2) as RFDET to be used as an RF strength indicator.

The transmit ALC circuit, built around U101, is the heart of the power control loop. Circuits in the Tx ALC module compare the signals at U101, pins 2 and 7. The resultant signal, C BIAS, at U101, pin 4 is applied to the base of transistor Q110. In response to the base drive, transistor Q110 varies the DC control voltages applied to the RF PA at U105, pin 3, thus controlling the RF power of module (U105).

Thermistor RT101 senses the temperature of the Tx ALC IC. If an abnormal operating condition exists that causes the PA temperature to rise to an unacceptable level, the thermistor forces the ALC to reduce the set power.

5.3 REVISED 800 MHz RF BOARD

NOTE: The RF Board is not field serviceable. Therefore, it must be replaced if it is defective.

5.3.1 FREQUENCY SYNTHESIS

The complete synthesizer subsystem consists of the reference oscillator (U304), the voltage-controlled oscillator (VCO U307), a buffer IC (U303), and the synthesizer (U302).

The reference oscillator contains a temperature-compensated 16.8 MHz crystal. This oscillator is digitally tuned and contains a temperature-referenced, five-bit, analog-to-digital (A/D) converter. The output of the oscillator (pin 10 on U304) is applied to pin 14 (XTAL1) on U302 through capacitor C309 and resistor 8306.

Voltage-controlled oscillator module U307 is varactor tuned. Therefore, as the voltage being applied to pins 1 and 7 of the VCO varies (2-11V), so does the varactor's capacitance which changes the VCO output frequency. The 800 MHz VCO is a dual-range oscillator that covers the 806-825 MHz and the 851-870 MHz frequency bands.

The low-band VCO (777-825 MHz) provides the first LO injection frequencies (777-797 MHz) that are

REVISED 800 MHz RF BOARD DESCRIPTION (Cont'd)

73.35 MHz below the carrier frequency. In addition, in the transmit mode when the radio is operated through a repeater, the low-band VCO generates the transmit frequencies (806-825 MHz) that are 45 MHz below the receiver frequencies. The low band VCO is selected by pulling pin 3 high and pin 8 low on U307. When radio-to-radio or talk-around operation is necessary, the high band VCO (851-870 MHz) is selected. This is accomplished by pulling pin 3 low and pin 8 high on U307.

The buffer IC (U303) includes a Tx, Rx, and prescaler buffer which maintain a constant output level and provides isolation. The Tx buffer is selected by setting pin 7 of U303 high, and the Rx buffer is selected by setting pin 7 of U303 low. The prescaler buffer is always on. In order to select the proper combination of VCO and buffer, the following conditions must be true at pin 6 of U303 (or pin 38 of U302) and pin 7 of U303 (or pin 39 of U302):

- For first LO injection frequencies 777-797 MHz, pins 6 and 7 must both be low.
- For Tx repeater frequencies 806-825 MHz, pins 6 and 7 must both be high.
- For talkaround Tx frequencies 851-870 MHz, pin 6 must be low and pin 7 must be high.

The synthesizer IC (U302) consists of a prescaler, a programmable loop divider, a divider control logic, a phase detector, a charge pump, an A/D converter for low-frequency digital modulation, a balance attenuator to balance the high-frequency analog modulation to the low-frequency digital modulation, a 13V positive-voltage multiplier, a serial interface for control, and finally, a filter for the regulated 5-volt supply. This filtered five volts is present at pin 19 of U302, pin 9 of U307, and pins 2, 3, 4, and 15 of U303. It is also applied directly to resistors R309, R315, and R311. Additionally, the 13V supply generated by the positive voltage multiplier circuitry should be present at pin 35 of U302. The serial interface (SRL) is connected to the microprocessor via the data line (pin 2 of U302), clock line (pin 3 of U302), and chip-enable line (pin 4 of U302).

The complete synthesizer subsystem operates as follows:

- The output of the VCO, pin 4 on U307, is fed into the RF input port (pin 9) of U303. In the Tx mode, the RF signal is present at pin 4 of U303; in the RX mode, the RF signal is present at pin 3 of U303.
- The output of the prescaler buffer, pin 15 of U303, is applied to the PREIN port (pin 21) of U302. The prescaler in U302 is a dual modulus type with selectable divider ratios. This divider ratio is controlled by the loop divider, which in turn receives its inputs from the SRL. The loop divider adds or subtracts phase to the prescaler divider by changing the divide ratio via the modulus control line.
- The output of the prescaler is then applied to the loop divider.
- The output of the loop divider is then applied to the phase detector. The phase detector compares the loop divider's output signal with the signal from U304 (that is divided down after it is applied to pin 14 of U302). The result of the signal comparison is a pulsed DC signal which is applied to the charge pump.
- The charge pump outputs a current that is present at pin 32 of U302. The loop filter (which consists of capacitors C322, C317, C318, C329, C324, and C315, and resistors R307, R305, and R314) transforms this current into a voltage that is applied to pins 1 and 7 of U307 to alter the VCO's output frequency.

In order to modulate the PLL, the two-port modulation method is utilized. The analog modulating signal is applied to the A/D converter as well as the balance attenuator, via U302, pin 5. The A/D converter converts the low-frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high-frequency modulating signals.

5.3.2 ANTENNA SWITCH

An electronic PIN diode switch steers RF between the receiver and transmitter. The common node of the switch is at capacitor C101. In the transmit mode, RF is routed to the anode of diode CR104. In

REVISED 800 MHz RF BOARD DESCRIPTION (Cont'd)

receive mode, RF is routed to pin 1 of U201. In the transmit mode, bias current sourced from U504, pin 21, is routed through PIN diodes CR104 and CR102 which biases them to a low-impedance state. Bias current returns to ground through U504, pin 20. In receive, U504, pin 21, is pulled down to ground and pin 20 is pulled up to B+ which reverse-biases diodes CR104 and CR102 to a high impedance.

5.3.3 RECEIVER FRONT END

The 800 MHz receiver front end converts the received RF signal to the first IF frequency of 73.35 MHz and also provids spurious immunity and adjacent channel selectivity. The received RF signal is passed through antenna switch input matching components C101, L105, and C114, through tank components C106 and L103 (which are anti-resonant at the radios transmitter frequencies), and through output matching components C103 and L104. Both pin diodes CR102 and CR104 must be back-biased to properly route the received signal.

The stage following the antenna switch is a 50-ohm, inter-digitated, three-pole, stripline preselector (U201). The preselector is positioned after the antenna switch to provide the receiver preamp with some protection against strong, out-of-band signals.

After the preselector (U201), the received signal is processed through receiver preamp U202. The preamp is a dual-gate, GaAs MESFET transistor which has been internally biased for optimum IM, NF, and gain performance. Components L201 and L202 match the input (gate 1) of the amp to the first preselector, while at the same time connecting gate 1 to ground potential. The output (drain) of the amp is pin 7, and is matched to the subsequent receiver stage by L204 and C222.

A supply voltage of 5V DC is provided to pin 3 through RF choke L203 and bypass capacitor C204. The 5-volt supply is also present at pin 4, which connects to a voltage divider network that biases gate 2 (pin 5) to a predefined quiescent voltage of 1.2V DC. Resistor R202 and capacitor C203 are connected to pin 5 to provide amp stability. The FET source (pin 3) is internally biased at 0.55 to 0.7VDC for proper operation with bypass capacitors C201 and C202, connected to the same node.

The output of the amp is matched to a second three-pole preselector (U203) of the type previously discussed. The next stage in the receiver chain is first mixer U205 which uses low-side injection to convert the RF carrier to an intermediate frequency (IF) of 73.35 MHz.

Since low-side injection is used, the LO frequency is offset below the RF carrier by 73.35 MHz, or fLO = fRF - 73.35 MHz. The mixer utilizes GaAs FETs in a double-balanced, Gilbert Cell configuration. The LO port (pin 8) incorporates an internal buffer and a phase shift network to eliminate the need for a LO transformer. The LO buffer bypass capacitors (C208, C221, and C216) are connected to pin 10 of U205, and should exhibit a nominal DC voltage of 1.2 to 1.4V DC. Pin 11 of U205 is LO buffer Vdd (5V DC), with associated bypass capacitors C226 and C209 connected to the same node. An internal voltage divider network within the LO buffer is bypassed to virtual ground at pin 12 of U205 through bypass capacitor C213. The mixer's LO port is matched to the radio's PLL by a capacitive tap, C207 and C206.

A balun transformer (T202) is used to couple the RF signal into the mixer. The primary winding of T202 is matched to the preceding stage by capacitor C223, with C227 providing a DC block to ground. The secondary winding of T202 provides a differential output, with a 180° phase differential being achieved by setting the secondary center tap to virtual ground using bypass capacitors C210, C211, and C212. The secondary of transformer T202 is connected to pins 1 and 15 of the mixer IC, which drives the source leg of dual FETs used to toggle the paralleled differential amplifier configuration within the Gilbert Cell.

The final stage in the receiver front end is a two-pole crystal filter (FL1). The crystal filter provides some of the receiver's adjacent channel selectivity. The input to the crystal filter is matched to the first mixer using L605, C600, and C614. The output of the crystal filter is matched to the input of IF buffer amplifier transistor Q601 by L600, C609, and C610.

5.3.4 RECEIVER BACK END

The IF frequency on the collector of Q601 is applied to a second crystal filter (FL2) through a matching circuit consisting of L601, L602, C604, and

C612. The filter supplies further attenuation at the IF sidebands to increase the radio's selectivity. The output of FL2 is routed to pin 32 of U401 through a matching circuit consisting of L603, C603, and C606, and DC blocking capacitor C613.

In the ABACUS IC (U401), the first IF frequency is amplified and then down-converted to the second IF of 450 kHz. The analog signal is then converted into two digital bit streams by a sigma-delta A/D converter. The bit streams are then digitally filtered, mixed down to baseband, and filtered again. The differential output data stream is then sent to the ADSIC on the logic board, where it is decoded to produce the recovered audio.

The ABACUS IC (U401) is electronically programmable. The amount of filtering is dependent on the radio channel spacing and signal type, and is controlled by the microcomputer. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal digital filters in the ABACUS IC. The ABACUS IC contains a feedback AGC circuit to expand the dynamic range of the sigma-delta converter. The differential output data contains the quadrature (I and Q) information in 16-bit words, the AGC information in a 9-bit word, imbedded word sync information, and fill bits which are dependent on sampling speed. A fractional N synthesizer is also incorporated on the ABACUS IC for 2nd LO generation.

The second LO/VCO is a Colpitts oscillator built around transistor Ql. The VCO has a varactor diode (VR401), which is used to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C426, C428, and R413.

5.3.5 TRANSMITTER

The 800 MHz RF power amplifier (PA) is a five-stage amplifier (U502). The RF power amplifier has a nominal input and output impedance of 50 ohms.

An RF input drive level of approximately +3 dBm, supplied from the VCO buffer IC (U303), is applied to pin 1 of U502. The DC bias for the internal stages of U502 is applied to pins 3 and 4 of the module. Pin 3 is switched through Q502 and pin 4 is unswitched B+ to the final amplifier stage. Power

control is achieved by varying of the DC bias to pin 2, the third and fourth amplifier stages of the module. The amplified RF signal leaves the PA module at pin 5 and is applied to the directional coupler (U501).

The purpose of U501 is to sample both the forward power and the reverse power. Reverse power is present when a load other than 50 ohms exists at the antenna port. The sampling is achieved by coupling some of the reflected power, forward and/or reverse, to a coupled leg on the coupler. The sampled RF signals are applied to diode CR501 for rectification and summing. The resultant DC signal is applied to the ALC IC (U504, pin 2) as RFDET, to be used as an indicator of the strength of the RF signal being passed through the directional coupler (U501).

The transmit ALC IC (U504) is the main part of the power control loop. The REF V line (U504 pin 7), a DC signal supplied from the D/A IC (U503), and the RF DET signal described earlier, are compared internally in the ALC IC to determine the amount of C BIAS, pin 4, to be applied to the base of transistor Q501. Transistor Q501 responds to the base drive level by varying the DC control voltages applied to pin 2 of the RF PA which controls the RIF power level of module U502. The ALC IC also controls the base switching to transistor Q502 via pin 12, BIAS.

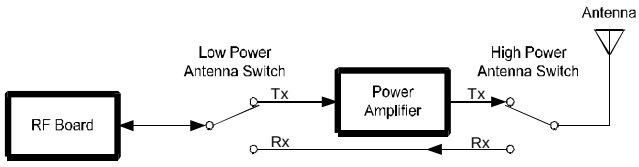
The D/A IC (U503) controls the DC switching of the transceiver board. Its outputs, SC1 and SC3 (pins 12 and 14, respectively), control transistor Q503 which then supplies Tx 5V and Rx 5V to the transceiver board. The D/A also supplies DC bias to the detector diode (CR501) via pin 7, and the REF V signal to the ALC IC (U504).

5.4 VHF PA BOARD

5.4.1 ANTENNA SWITCHES

The RF signal from the RF board is fed by a coaxial cable to the PA board. Since both the receive and transmit signals are present on the input of the PA board, special antenna switching is required on the PA board to route the receive signal around the amplifier section to the antenna. Both a high power and a low power antenna switch are used as shown below.

VHF PA BOARD DESCRIPTION (CONT'D)



The low power switch consists of pin diodes* CR512 and CR513 and other components. The Q7 output of shift register U501 is high in the transmit mode and low in the receive mode. Therefore, in the transmit mode, Q507 and Q514 are on and Q508 and Q513 are off. This forward biases CR513 and reverse biases CR512. The transmit signal from the RF board then has a low impedance path through C533 and CR513 to driver Q509, and the high impedance provided by CR512 blocks it from the receive path.

In the receive mode, the opposite occurs, so CR513 is reverse biased and CR512 forward biased. The receive signal from the high power antenna switch (see following) then has a low impedance path through C544, CR512, and C534 to the RF board, and is blocked from the power amplifier by CR513.

The high power antenna switch consists of pin diodes* CR501, CR502, and CR503. This switch effectively switches the antenna between the power amplifier and the receive bypass path to the RF board (see preceding illustration).

Transistor Q501 is on in the transmit mode and off in the receive mode. Therefore, in the transmit mode, all three diodes are forward biased (CR501 and CR502 are biased by voltage applied from the collector of Q510). The transmit signal then has a low impedance path through CR502 to the low-pass filter and is blocked from the bypass path by L504/C511 and L505/C515 which present a high impedance at the transmit frequency. In the receive mode, all three diodes are reverse biased. Therefore, the receive signal from the antenna is blocked from the power amplifier by CR502 and has a low impedance path through L504 and L505 to the RF board.

5.4.2 AMPLIFIERS (Q509, Q510)

Impedance matching between the low power antenna switch and Q509 is provided by L511 and several capacitors and sections of microstrip. Class C biasing is provided by L510 and ferrite bead EP503, and negative feedback for stabilization is provided by R557 and R543. Supply voltage to Q509 is controlled by the power control circuit to regulate the power output of the transmitter. Conditioning and isolation of the DC supply to Q509 is provided by L509, L514, EP501, and C540-C542.

Impedance matching between Q509 and final amplifier Q510 is provided by several capacitors and sections of microstrip. Class C biasing of Q510 is provided by L515, EP502, R559, and R560. The current for this stage flows through L516, R561, and L517. The voltage drop across R561 is sensed by the power control circuit to detect an over-current condition.

From Q510 the transmit signal is fed through another impedance matching network to a directional coupler, to the high power antenna switch (see preceding section), and then to the low-pass filter. This filter attenuates harmonics occurring above the transmit frequency band to prevent adjacent channel interference. The directional coupler detects the forward component of the output power for use by the power control circuit.

5.4.3 POWER CONTROL

Introduction

The power control circuit maintains a constant power output as changes occur in temperature and voltage. It does this by sensing forward power and then varying the drive to Q510 to maintain a constant output power. The drive to Q510 is controlled by varying the supply voltage to driver Q509. The current to final amplifier Q510 is also sensed, but power output is affected by this input only if current becomes excessive. Power output is then cut back to approximately 25% of full power.

The power output level is set in 127 steps by D/A converter U801 which is controlled by the microcontroller. This allows power to be adjusted using the PCTune software and computer and also different power levels to be programmed. In addition, it allows the microcontroller to cut back power if the power amplifier temperature is excessive. Temperature is sensed via thermistor RT501.

* A reverse biased pin diode presents a high impedance to RF signals. Conversely, and a forward biased pin diode presents a variable low impedance that changes inversely to current.

VHF PA BOARD DESCRIPTION (CONT'D)

U502A, Q500/Q502 Operation

The forward power signal from the directional coupler is applied to pin 2 of amplifier U502A. This is a DC signal that increases proportionally to forward power. The other input to U502A is a DC reference voltage from a D/A converter formed by shift register U801 and several resistors. The voltage from this D/A converter sets the voltage on pin 3 which sets the power output of the transmitter.

U502A is a difference amplifier which amplifies the difference between the reference voltage on pin 3 and the forward power signal on pin 2. The turn-on time of U502A is controlled by the time constant of C528 and R534, and negative AC feedback to prevent oscillation is also provided by C528. This circuit operates as follows: Assume the output power attempts to increase. The DC voltage applied to U502A, pin 2 then increases which causes the output voltage on pin 1 to decrease. Transistors Q505 and Q506 then turn off slightly which decreases the supply voltage to driver Q509. The output power then decreases to maintain a constant power output. R541 and R542 limit the voltage gain of Q505 and Q506 to approximately two.

Delayed PTT

Transistor Q504 is used to delay power output for a short time after the transmitter is keyed. This allows the synthesizer and exciter to stabilize so that the transmitter does not transmit off-frequency. The signal which controls Q504 is from microcontroller U9 on the logic board. In the receive mode this output is low, so Q504 is off. Pin 2 of U500A is then pulled high by the 7.2-volt supply applied through R537 and CR506. This causes the output on pin 1 of U502A to go low which shuts off power to Q509. Then when the transmitter is keyed, the Q504 control signal goes high after a short delay. Q504 then turns on and diode CR506 is reverse biased. Only the forward power signal is then applied to pin 2 of U502A.

Over-Current Shutdown

Current to final amplifier Q510 is monitored by sensing the voltage drop across R561. Pins 3 and 6 of U506 are connected across this resistor. As current increases, the output voltage on U506, pin 8 decreases. This causes the output voltage of voltage follower

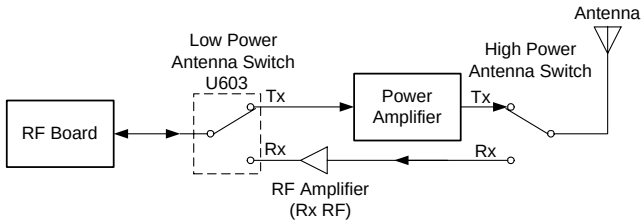
800 MHz PA BOARD DESCRIPTION

U507A to decrease. This signal is applied to Schmitt trigger U502B. When the voltage on pin 6 rises above the reference on pin 5, the output on pin 7 goes low. This lowers the power control voltage applied to U502A, pin 3 which lowers the power output to approximately 25% of full power.

5.5 800 MHz PA BOARD

5.5.1 LOW POWER ANTENNA SWITCH

The RF signal from the RF board is fed by a coaxial cable to the PA board. Since both the receive and transmit signals are present on the input of the PA board, special antenna switching is required on the PA board to route the receive signal around the power amplifier section to the antenna. Both high power and a low power antenna switches are used as shown below.



Low power antenna switching is provided by electronic antenna switch U603. Pin 5 is effectively connected to pin 1 when pin 6 is high (and pin 4 is low). Conversely, pin 5 is connected to pin 3 when pin 4 is high and pin 6 is low. These control signals are provided by the Q7 output of shift register U501 and inverters Q516/Q517. In the transmit mode, the signal from the RF board is then routed through C532 to the PA module, and blocked from RF amplifier Q503. In the receive mode, the opposite occurs. Refer to Section 5.5.4 for a description of the high power antenna switch.

5.5.2 POWER DETECTOR AND ATTENUATOR

The transmit RF output signal of pin 3 of antenna switch U603 is coupled by C595 to a power detector circuit formed by CR521, R591, and other components. When RF power is detected, the voltage on pin 13 of op amp U502 increases. When it rises above the reference on pin 12, the output on pin 14 goes low and turns off Q507. The base of Q505 is then no longer

800 MHz PA BOARD DESCRIPTION (Cont'd)

grounded which allows it to be controlled by the power control circuit. This provides maximum attenuation in the receive mode to minimize the amplification of any low level receive signal that may be present (see following).

A 3-dB pad formed by R541, R542, and R543 provides attenuation of the RF signal and also a 50-ohm impedance. Matching between U603 and this pad is provided by C532 and L514. This pad is then matched by a section of microstrip and L503 to a limiter and variable 50-ohm attenuator formed by pin diodes* C516-C518 and other components. This attenuator provides approximately 0-20 dB attention of the RF signal input to PA module. This controls the power output of the transceiver.

The limiter section formed by CR516, CR517, C535 and biasing resistors R580/R581 attenuates high level input signals that could cause improper operation of the attenuator. The attenuator circuit is formed by CR518 and CR519 and controlled by Q505 and the rest of the power control circuit (see Section 5.5.6). Biasing of these diodes is provided by CR520, R597, R584, R582, R586, and R538 connected to the emitter of Q505. When Q505 is turned off, CR518 is reverse biased by the voltage applied through R537. It then provides maximum attenuation of the RF signal.

A shunt path is provided around CR518 by R583, C537, and R585. Pin diode CR519 is at its maximum forward biased condition when Q505 is off, and connects R583 to AC ground through C538. This maintains a constant 50-ohm impedance. Then as Q505 turns on, CR518 becomes forward biased and provides less attenuation. Likewise, CR519 becomes less forward biased which increases the impedance of the path to ground. From the attenuator the signal is coupled by C542 to a 1 dB, 50-ohm pad formed by R544-R546 and then applied to PA module U504.

5.5.3 POWER AMPLIFIER MODULE (U504), FINAL (Q509)

Power amplifier module U504 provides approximately 19 dB of gain. Pins 2, 3, and 4 are the supply voltage inputs to three separate gain stages. The supply voltage on pin 2 (VS1) is switched by Q508 and limited to 12 volts by CR508 and R549. Switch Q508 is controlled by the same signal used to control the high power antenna switch (see Section 5.5.4).

The supply voltage applied to pins 3 and 4 (VS2/VS3) is the unswitched battery from the power jack. Therefore, power is applied to these pins even when transceiver power is turned off.

The output signal on U504, pin 5 is then applied to final amplifier Q509 which provides about 5 dB of gain. Current to this stage flows through R550, and transmitter current is monitored by sensing the voltage drop across this resistor (see Section 5.5.6). The output impedance on U504, pin 5 is 50 ohms, and it is matched to Q509 by a section of microstrip, C556, C557, and C558. Class C biasing of Q509 is provided by L507. The unswitched battery supply applied to Q509 is isolated from RF by ferrite bead EP503, inductor L508, and several capacitors. Impedance matching is provided on the output by C559, C561, C562, C566, and a section of microstrip.

5.5.4 HIGH POWER ANTENNA SWITCH

The high power antenna switch consists of pin diodes* CR501, CR502, CR503, and other components. This switch effectively switches the antenna to the power amplifier in the transmit mode, and the receive RF amplifier path in the receive mode (see preceding illustration).

Transistors Q506 and Q501 controlled by the Q7 output of shift register U501 after it is double inverted by Q516 and Q517. This signal is high in the transmit mode and low in the receive mode. Therefore, Q506 and Q501 are on in the transmit mode which forward biases CR501, CR502, and CR503. One current path is through Q501, R503, R504, CR501, L508, CR502, and L508, and the other is through Q506, R559, CR503, and R560.

Since a forward biased pin diode has a low impedance, the RF signal passes through CR502 to the low-pass filter. The signal is blocked from the RF amplifier by two discrete grounded quarter-wave lines. One line is formed by L508/C507 and the other by L502/C514. Diode CR501 is effectively AC grounded by C507, and CR503 is AC grounded by C514. When one end of a quarter-wave line is grounded, the other end presents a high impedance to the quarter-wave frequency.

In the receive mode, all three diodes are reverse biased. Therefore, the receive signal from the antenna

* A reverse biased pin diode presents a high impedance to RF signals. Conversely, and a forward biased pin diode presents a variable low impedance that changes inversely to current.

is blocked from the power amplifier by CR502 and has a low impedance path through the quarter-wave lines which are no longer grounded. Resistors R505 and R506 improve the isolation provided by CR501 and CR502 when they are reverse biased in the receive mode.

5.5.5 DIRECTIONAL COUPLER, LOW-PASS FILTER, TEMP SENSE

A directional coupler is formed by adjacent sections of microstrip near C566. The forward component of output power is rectified by CR509 and developed across R557 and then fed to the power control circuit. Reverse power is not detected in this transceiver.

From the directional coupler the transmit RF signal is coupled by C511 to a low-pass harmonic filter formed by C501-C505 and several sections of microstrip. This filter attenuates harmonic frequencies occurring above the transmit band. Resistor R501 dissipates static buildup on the antenna.

The ambient power amplifier temperature is sensed by thermistor RT501. The resistance of a thermistor decreases as temperature increases. The thermistor forms a voltage divider with R147 on the audio/logic board, and the voltage across this divider is monitored by A/D converter U21. If the PA temperature increases above limits set in software, the power is first cut back. Then if it continues to rise, the transmitter is turned off.

5.5.6 POWER CONTROL

Introduction

The power control circuit maintains a constant power output as changes occur in temperature and voltage. It does this by sensing the forward power and then varying the output of Q505 to maintain a constant output power (see Section 5.5.2). Although current to final amplifier Q509 is also sensed, power output is affected by this input only if current becomes excessive. Power output is then cut back to approximately 25% of full power.

The power output level is set in 127 steps by D/A converter U501 which is controlled by the microcontroller. This allows power to be adjusted using the PCTune software and computer and also different power levels to be programmed. In addition, it allows the microcontroller to cut back power if the power amplifier temperature is excessive. Temperature is sensed via thermistor RT501 (see Section 5.5.5).

U502A Operation

The forward power signal from the directional coupler is applied to pin 2 of amplifier U502A. This is a DC signal that increases proportionally to forward power. The other input to U502A is a DC reference voltage from a D/A converter formed by shift register U501 and several resistors. The voltage from this D/A converter sets the voltage on pin 3 which sets the power output of the transmitter.

U502A is a difference amplifier which amplifies the difference between the reference voltage on pin 3 and the forward power signal on pin 2. The turn-on time of U502A is controlled by the time constant of C525 and R527. This circuit operates as follows: Assume the output power attempts to increase. The DC voltage applied to U502A, pin 2 then increases which causes the output voltage on pin 1 to decrease. Transistor Q505 then turns off slightly which increases the attenuation provided by the attenuation circuit (see Section 5.5.2). The output power then decreases to maintain a constant power output.

Delayed PTT

Transistor Q504 is used to delay power output for a short time after the transmitter is keyed. This allows the synthesizer and exciter to stabilize so that the transmitter does not transmit off-frequency. The signal which controls Q504 is from pin 14 of microcontroller U9 on the logic board. In the receive mode this output is low, so Q504 is off. Pin 2 of U500A is then pulled high by the 7.2-volt supply applied through R530 and CR505. This causes the output on pin 1 of U502A to go low which shuts off Q505 and produces maximum attenuation. Then when the transmitter is keyed, the Q504 control signal goes high after a short delay. Q504 then turns on and diode CR505 is reverse biased. Only the forward power signal is then applied to pin 2 of U502A.

Over-Current Shutdown

Current to final amplifier Q509 is monitored by sensing the voltage drop across R550. Pins 3 and 6 of

U505 are connected across this resistor. As current increases, the output voltage on U505, pin 8 decreases. This signal is applied to Schmitt trigger U502B. When the voltage on pin 6 rises above the reference on pin 5, the output on pin 7 goes low. This lowers the power control voltage applied to U505 which lowers the power output to approximately 25% of full power.

5.5.7 RF AMPLIFIER (Q503)

The receive signal from the antenna switch is applied to bandpass filter Z501. This is a three-pole filter with a center frequency of 860 MHz and a bandwidth of 18 MHz. This filter attenuates frequencies outside the receive band such as the first injection, image, and half IF frequencies.

The signal is then applied to RF amplifier Q503 which improves and stabilizes receiver sensitivity and also recovers filter losses. A section of microstrip and C515 provide impedance matching on the input. CR504 protects the base-emitter junction of Q503 from damage caused by high level input signals.

The bias current of Q503 is fixed at a constant level by Q502. The collector current of Q503 flows through R511, and the voltage drop across that resistor (and therefore the current) is set by R508 and R509. For example, if current through R2511 attempts to increase, the emitter voltage of Q502 decreases. Q502 then conducts less and turns Q503 off slightly to maintain a constant bias current. This provides a stable bias over changes in temperature. The output signal of Q503 is applied to a 3 dB, 50-ohm pad formed by R587-R589, and then coupled by C531 to antenna switch U603. From U603 it is applied to the RF board.

5.6 DC POWER DISTRIBUTION

5.6.1 POWER ON OPERATION

When the On-Off/Volume knob is pressed to turn power on (this is a push on/push off switch), the following sequence of events occurs:

1. The power switch closes and grounds the emitter of Q8 on the logic board.

2. If ignition switch sense is used, the 13V signal from the ignition switch is applied to the base of Q8 and

pin A7 of microcontroller U6 (or pin 48 of microcontroller U9 with the Rev 3 logic board). If ignition sense is not used, pull-up resistor R145 can be installed to make the transceiver functional.

3. Q8 then turns on which grounds the base of Q512 on the PA board and turns it on. This turns on main power switching transistor Q511 and applies power to the switched portions of the transceiver.

5.6.2 POWER OFF OPERATION

When power is turned off, the following sequence of events occur:

1. If the power switch is pressed, it opens and the base of Q8 is no longer grounded. This also applies a high signal to the microcontroller which then detects the power-off condition.

2. If ignition switch control of power is used, turning the ignition switch off causes the signal applied to the base of Q8 to go low. This signal is also inverted by Q5 and applied the microcontroller.

3. Q8 then turns off. However, when the controller detects the power-down request, it holds Q2 on to delay power turn-off until all the required save operations are complete.

4. The controller then turns off Q2 and both Q511 and Q512 on the PA board turn off which turns off transceiver power.

5.7 LOGIC BOARD (REV. 3 VERSION)

NOTE: The following description applies to the Revision 3 Logic Board shown on page A-8.

5.7.1 LOGIC BOARD OVERVIEW

The Logic Board contains ADSIC U3, Digital Signal Processor U12 (TMS320C50), static RAM U5/U6, FLASH memory U2, and a programmable logic IC U1. In addition, it contains microcontroller U9, audio circuits, and a 5V power supply. The logic board connects with the interface board via J9 and the display controller board via J1.

REV 3 LOGIC BOARD DESCRIPTION (Cont'd)

The ADSIC performs the frequency discrimination and receiver filtering functions. It also performs analog-to-digital (A/D) and digital-to-analog (D/A) conversion. Functions previously performed in hardware like filtering and limiting are performed by software running in the DSP chip. The DSP performs demodulation and modulation, voice encoding and decoding, audio filtering, and squelch signaling. The software for the radio is stored in FLASH memory that is loaded in to static RAM at turn-on. The programmable logic IC controls which device (Flash, SRAM, or UART) is connected to the DSP address and data bus.

5.7.2 DIGITAL SIGNAL PROCESSING OVERVIEW

The DSP section consists of a DSP chip (U12), the ADSIC (U3), two 128K x 8-bit Static RAM chips (U5, U6), one 512K x 16-bit FLASH ROM memory chip (U2), a UART chip (U20), a programmable logic IC (U1), and a glue-logic chip (U4). The FLASH ROM contains the program code executed by the DSP. Depending on the operational mode selected for the radio, different sections of the program code in the FLASH ROM are copied into SRAM for faster execution.

The ADSIC is a support chip for the DSP. It provides the interface between the DSP and the analog signal paths, and between the DSP and the ABACUS chip on the RF Board. Configuration of the ADSIC is handled primarily by the microcontroller. The DSP has access to a few memory-mapped registers on the ADSIC.

In receive mode, the ADSIC interfaces the DSP with the ABACUS IC on the RF board. The ADSIC collects the I and Q samples from the ABACUS and performs channel filtering and frequency discrimination on the signals. The resulting demodulated signal is routed to the DSP via the serial port for further processing. After the DSP processing, the signal is sent to the ADSIC Speaker D/A by writing to a memory-mapped register. The ADSIC then converts the processed signal from the DSP to an analog signal and then outputs this signal to the speaker power amplifier on the interface board.

In transmit mode the ADSIC Microphone A/D digitizes the analog signal from the microphone. The DSP reads these values from a memory-mapped register in the ADSIC. After processing, the DSP sends the modulation signal to the ADSIC via the serial port. In the ADSIC, the VCO D/A converts the sampled modulation signal into an analog signal and then routes this signal to the VCO on the RF board.

5.7.3 RECEIVE SIGNAL PATH

The ABACUS IC on the RF board provides a digital back end for the receiver section. It provides a digital output of I (in phase) and Q (quadrature) samples which represent the IF signal at the receiver back end. These samples are routed to the ADSIC where the signal is filtered and frequency discriminated to recover the modulating signal.

The recovered signal is sent to the DSP chip for processing. The ADSIC interface to the ABACUS is comprised of four signals SBI, DIN, DIN*, and ODC. The ODC signal is a clock the ABACUS provides to the ADSIC. Most internal ADSIC functions are clocked by this ODC signal at a rate of 2.4 MHz and are available as soon as the power is supplied to the circuitry. This signal initially may be 2.4 or 4.8 MHz after power-up. It is programmed by the ADSIC through the SBI signal to 2.4 MHz when the ADSIC is initialized by the microcontroller through the SPI bus. For any functionality of the ADSIC to exist, including initial programming, the reference clock must be present.

SBI is a programming data line for the ABACUS. This line is used to configure the operation of the ABACUS and is driven by the ADSIC. The microcontroller programs many of the ADSIC operational features through the SPI interface. There are 36 configuration registers in the ADSIC of which 4 contain configuration data for the ABACUS. When these particular registers are programmed by the microcontroller, the ADSIC in turn sends this data to the ABACUS through the SBI.

DIN and DIN* are the data lines in which the I and Q data words are transferred from the ABACUS. These signals make up a differentially encoded current loop. Instead of sending TTL-type voltage signals, the data is transferred by flowing current one way or the other through the loop. This helps reduce internally

generated spurious emissions on the RF board. The ADSIC contains an internal current loop decoder which translates these signals back to TTL logic and stores the data in internal registers.

The ADSIC performs digital IF filtering and frequency discrimination on the signal, sending the baseband demodulated signal to the DSP. The internal digital IF filter is programmable with up to 24 taps. These taps are programmed by the microcontroller through the SPI interface.

The DSP processes this data through the SSI serial port. This is a six-port synchronous serial bus. The ADSIC transfers the data to the DSP on the TxD line at a rate of 2.4 MHz. This is clocked synchronously by the ADSIC which provides a 2.4 MHz clock on SCKT. In addition, a 20 kHz interrupt is provided on TFS to signal the arrival of a data packet. This means a new I and Q sample data packet is available to the DSP at a 20 kHz rate which represents the sampling rate of the received data. The DSP then processes this data to extract audio, signaling, and other information based on the 20 kHz interrupt.

In addition to the SPI programming bus, the ADSIC also contains a parallel configuration bus. This bus is used to access registers mapped into the DSP memory. Some of these registers are used for additional ADSIC configuration controlled directly by the DSP. Some of the registers are data registers for the speaker D/A. Analog speaker audio is processed through this parallel bus where the DSP outputs the speaker audio digital data words to this speaker D/A. In addition, an analog waveform is generated which is output to SDO (Speaker Data Out).

In conjunction with speaker D/A, ADSIC contains a programmable attenuator to set the rough signal attenuation. However, the fine levels and differences between signal types are adjusted through the DSP software algorithms. The speaker D/A attenuator setting is programmed by the microcontroller through the SPI bus.

The ADSIC provides an 8 kHz interrupt to the DSP on IRQB for processing the speaker data samples. This 8 kHz signal must be enabled through the SPI programming bus by the microcontroller and is necessary for any audio processing to occur.

5.7.4 TRANSMIT SIGNAL PATH

The ADSIC contains an analog-to-digital (ADC) converter for the microphone. The microphone path in the ADSIC also includes an attenuator that is programmed by the microcontroller through the SPI bus. The microphone input in the ADSIC is on pin MAI (U3-19). The microphone ADC converts the analog signal to a series of data words and stores them in internal registers. The DSP accesses this data through the parallel data bus. As with the speaker data samples, the DSP reads the microphone samples from registers mapped into its memory space. The ADSIC provides an 8 kHz interrupt to the DSP on IRQB for processing the microphone data samples.

The DSP processes these microphone samples and generates and mixes the appropriate signaling and filters the resultant data. This data is then transferred to the ADSIC on the DSP SSI port. The ADSIC generates a 48 kHz interrupt so that a new sample data packet is transferred at a 48 kHz rate and sets the transmit data sampling rate at 48 ksps. These samples are then input to a transmit D/A which converts the data to an analog waveform. This waveform is the modulation signal from the ADSIC and is connected to the VCO on the RF Board.

5.7.5 DSP CHIP (U12)

DSP chip U12 has a 16-bit data bus and a 16-bit address bus. It has 10K words of internal SRAM from which 0.5K are used only to store data and 9.5K are used either for data or for program storage. The DSP bus can access through its buses the following external devices:

SRAM U5 and U6 - These two chips are 128K x 8 chips. U5 stores the lower byte of the word while U6 stores the higher byte. Those chips are selected by asserting CE2 high and CE1* low. The programmable logic IC is responsible for controlling the select lines of these ICs.

FLASH ROM U2 - This chip is 512K x 16 words in size. It is selected by asserting CE* low. The programmable logic IC is responsible for controlling the select line of this IC.

REV 3 LOGIC BOARD DESCRIPTION (Cont'd)

ADSIC U3 - The ADSIC contains several registers which can be read from or written to by the DSP. The ADSIC IC has an output which drives a data/address bus enable signal for the programmable logic IC.

UART U7 - This chip converts data from the DSP into serial data. It is used to interface with the optional encryption board.

Programmable Logic U1 - This IC arbitrates access to the DSP's address/data bus between the flash (U2), SRAMs (U5,U6), and UART (U7). The DSP can modify the memory configuration by writing to a series of registers in the programmable logic IC. In order to reduce power consumption, the programmable logic IC can be 'disconnected' from the DSP's address/data bus using the bus enable input on the programmable logic IC (pin 44).

The DSP uses memory as data space, program space, and I/O space as follows. Refer to Figure 5-2 for more information.

Program Space - Internal SRAM, external SRAM, and FLASH memory.
Data Space - Internal SRAM and external SRAM.
I/O Space - Programmable logic IC, ADSIC, and the UART.

The DSP accesses the difference spaces by setting the corresponding lines PS*, DS*, IS* low. Only one of these three signals can be low at a given time. When the DSP accesses internal SRAM, none of these lines is activated.

The programmable logic IC (PLD) acts as the primary arbitrator of the DSP's memory map. The FLASH ROM and the SRAM are both mapped in the program space and cannot both be active at the same time. The DSP may control which type of memory is mapped in program space by enabling the programmable logic IC (PLD), then manipulating a register in the PLD. In addition, the DSP can manipulate other registers to control paging of both the Flash and the SRAM. Paging refers to the swapping of 64K word blocks of Flash or SRAM into or out of the DSP's memory map.

FLASH ROM U2 is used to permanently store the program to be executed in the DSP. However, it is slow to access, so to fully utilize the speed of the DSP, the program stored in the FLASH ROM must be copied into the SRAM. As the size of the SRAM is half the size of the FLASH ROM, only the code required for the current mode of operation is copied in the SRAM. As previously mentioned, the FLASH ROM and the SRAM cannot be active at the same time. Therefore, the internal data memory is used as a temporary buffer to transfer the program from the FLASH ROM to the SRAM.

The following hardware interrupts are used on the DSP:

Interrupt	Description
INT1*	8 kHz interrupt for speaker DAC and microphone ADC from ADSIC
INT2*	125 kHz signal from ADSIC
INT3*	2 kHz timer interrupt from the Controller on the Keypad Board.
INT4*	Interrupt from the UART
NMI*	Not used

Connector J3 allows connection to an emulator for debugging purposes. The emulator connects to some dedicated pins on the DSP.

5.7.6 UART (U20)

UART U20 performs parallel to serial and serial to parallel conversion. The serial format used is a 9-bit format with start and stop bits. The serial transmission speed is 19200 bps. The UART appears as eight registers visible in the I/O space of the DSP starting at every multiple of 0008h from 0000h to 07FFh. U1 performs the address decoding by selecting the UART (pin 39) when both IS* and A15 are low. Crystal Y2 along with the internal oscillator of the UART provides the clock required to generate the correct bit rate on the serial output of the UART.

When the UART receives a new serial word or is ready to accept a new word to send from the DSP, it generates an interrupt on INTRN. This pin is connected to one of the hardware interrupt lines on the DSP. The DSP responds by reading the status register in the UART and by answering accordingly.

REV 3 LOGIC BOARD DESCRIPTION (Cont'd)

5.7.7 ADSIC

The ADSIC is a complex custom IC which performs many analog-to-digital, digital-to-analog, and purely digital functions as previously described. The ADSIC has four internal registers accessible by the DSP. They are selected through the use of address lines A15, A14, A13, A2, A1, A0, IS* (IS* needs to be inverted with U4 to be compatible with the logic level required by the ADSIC), RD*, and WR*. Two of these registers are read-only while the two others are write-only. Therefore, they can be accessed as two locations in the I/O spaces. Due to the decoding performed, those locations appear at the following addresses: Fxx0h, Fxx1h, Fxx8h, Fxx9h, Exx0h, Exx1h, Exx8h, and Exx9h.

Crystal Y1 along with the internal oscillator in the ADSIC provide a 20 MHz clock. This clock signal is used internally by the ADSIC and is also multiplied by two to provide a 40 MHz clock to the DSP. The frequency of the clock can be electronically shifted a small amount by controlling varicap D1 through the OSCW pin (U3-97). This removes interference created on some channels by the clock.

The ADSIC and DSP exchange the sampled receive data and the sampled VCO modulation signal through a serial port. This serial port consists of pins SCKR*, RFS, RxD, TxD, SCKT, and TFS on the ADSIC. U21 and U1 modify the relative phase of TxD and TFS to be compatible with the timing required on the serial port of the DSP.

SDO is the output of the internal speaker DAC. MAI is the input of the internal microphone attenuator and is followed by the microphone ADC.

The ADSIC is configured partially by the DSP through its data and address bus (see preceding). However, most of the configuring is provided through an SPI compatible serial bus. This SPI serial bus consists of pins SEL*, SPD, and SCLK. The other side of this bus is connected to microcontroller U9.

5.7.8 MICROCONTROLLER U9 OVERVIEW

The microcontroller provides an interface between the hardware and DSP U12. When the user presses or rotates a control such as the Select switch, an option button, or the PTT switch, the microcontroller signals the change to the DSP. Conversely, when the DSP needs to change the display or an LED, it signals the microcontroller which then performs the action. The microcontroller also controls peripheral ICs such as the synthesizer, reference oscillator, display processor, and ADSIC.

The microcontroller uses a serial bus to communicate with the DSP and another RS-485 bus to communicate with the front panel/remote control unit. The RS-485 bus is used for external communication with a computer running the programming or tuning software. Finally, the microcontroller maintains certain operating parameters in the associated EEPROM which is controlled via a two-wire serial bus.

5.7.9 MICROCONTROLLER DESCRIPTION

Microcontroller U9 is a Motorola 68HC08XL36 chip. It includes 28K bytes of internal ROM memory and 1K byte of internal SRAM. It does not have an external bus and therefore cannot access any external program memory.

The clock to the microcontroller is provided by Y3 and an internal oscillator. The frequency of the clock can be slightly offset by polarizing the base of Q1 through software control. This prevents RF interference on some channels caused by the clock.

The microcontroller contains an SPI-compatible synchronous serial bus. This bus consists of pins MISO (U1-53), MOSI (U1-52), SPSCK (U1-50), and a chip enable for each device with which it communicates. The devices which communicate with the microcontroller through this bus are as follows:

- PA temperature sense ADC U21
- ADSIC chip U3
- Reference Oscillator (RF Board)
- Front-End DAC (RF Board)
- Synthesizer chip (RF Board)
- Shift register U801 (PA board)
- Optional DES board

The microcontroller communicates with the DSP chip through a custom serial bus. This serial port includes pins PTA3 (U9-8), PTA4 (U9-9), PTA5 (U9-10), PTA6 (U9-11), and PTA7 (U9-12).

REV 3 LOGIC BOARD DESCRIPTION (Cont'd)

The microcontroller SCI asynchronous serial bus is converted to an RS-485 bus by U14. The RS-485 bus is then used for communication with the front panel/remote control unit controller and the external computer running the programming or tuning software. The SCI bus consists of RxD (U9-42) and TxD (U9-43). The RS-485 driver (U14) converts U9 signals at a logic level of 0 and 5 V to three-state RS-485 logic levels.

Serial EEPROM U10 is used to store some important radio parameters. The EEPROM is read to or written from using I/O lines PTC6 and PTC7 of the microcontroller. PTC6 is the data line, and PTC7 is the clock line.

5.7.10 RECEIVE AUDIO CIRCUIT

In receive mode, the analog receive waveform created by the ADSIC is fed to summing amplifier U19A. This amplifier sums this signal with the audio tones generated by the microcontroller on pin 46. The output of the summing amplifier is then fed to buffer amplifiers U19B and U18B, and to U17A/U17B which provide a differential output.

The output signal from U19B is fed to volume control IC U4 on the interface board and then to audio amplifier U1. The output signal from U18B provides the External PA output to the accessory cable, and the output signal from U17A/U17B is fed to the display controller board. It is then converted back to a single-ended signal and fed to the Rx Audio pin of the front panel microphone jack. If a remote control unit is used, the U17A/U17B output signal is also routed to the audio amplifier in the remote control unit.

5.7.11 TRANSMIT AUDIO CIRCUIT

In transmit mode, the audio for transmission can be selected from the microphone connected to the front panel microphone jack or the microphone connected to a remote control unit. U15A and U15B convert a differential input to a single-ended output, and analog switch U18A selects the desired microphone signal.

The microphone signal is then buffered by U15C and fed to analog switch U18B and to the microphone output pin of the universal interface connector. U18B which selects either the microphone or universal interface microphone input signal. Additional buffering is provided by U15D and the signal is then fed to the A/D input of the ADSIC.

5.7.12 VOLTAGE REGULATION

The 5-volt supply is produced by switching DC-DC converter U11. This device is powered by the switched 7.2V supply, and the switching frequency is approximately 160 kHz. A switching regulator provides improved efficiency compared to a standard linear regulator. The 5-volt supply power provides a large percentage of the total power consumed by the radio. The peak-to-peak residual ripple on the 5-volt supply is approximately 50 mV.

The DC-DC converter has a soft-start feature (R27, C141) to prevent chattering of the output regulated voltage due to "bouncing" of the on/off switch. The converter has current limiting that limits output current to 1.5 A. The under voltage protection turns the converter off if the input (switched B+) voltage drops below 5.45 V.

LOGIC BOARD DESCRIPTION (Cont'd)

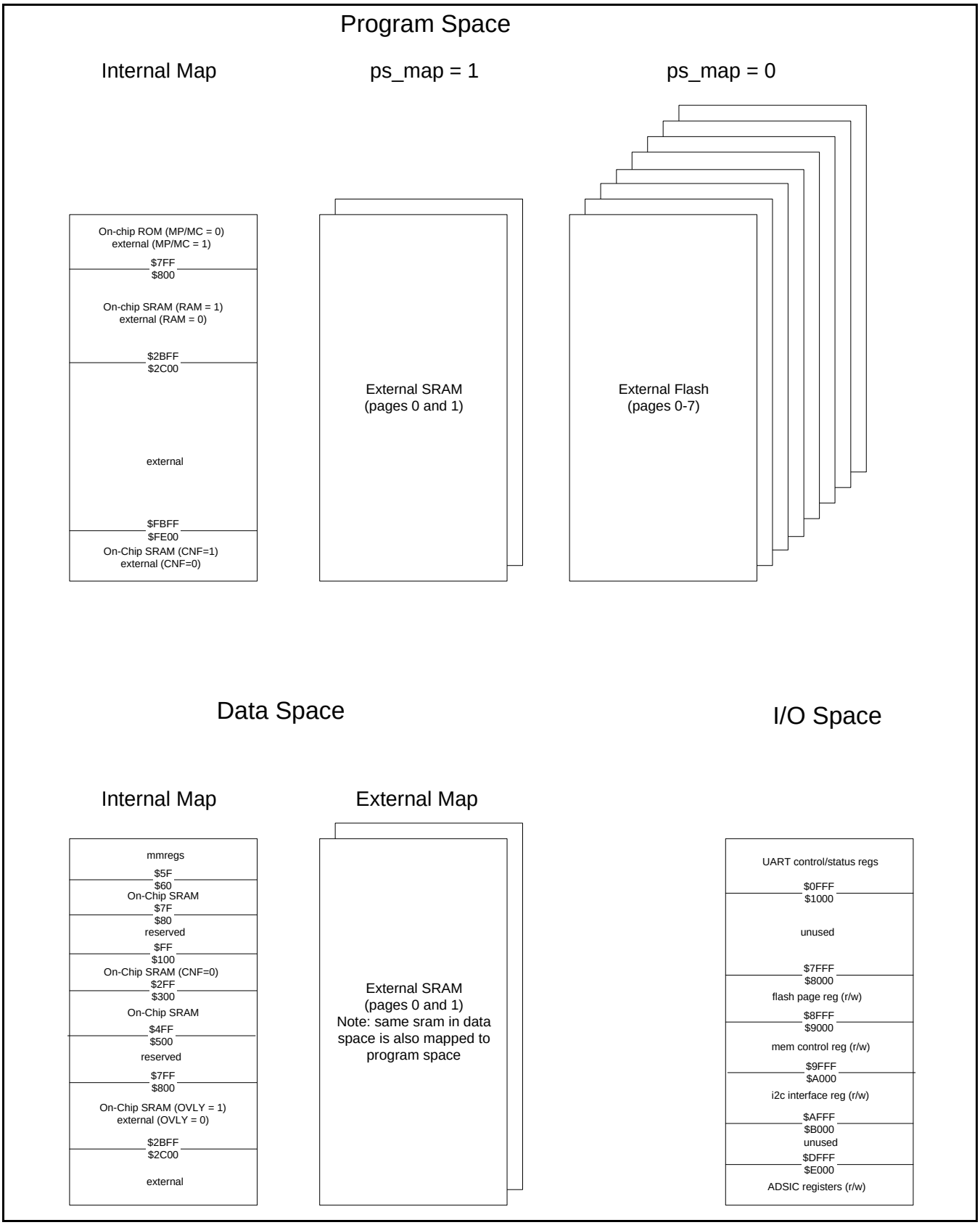


Figure 5-2 Memory Utilization