THEORY OF OPERATION

4.1 INTRODUCTION

This section contains the theory of operation for the DPH Flex•Mode radio. To help you understand the operation of the equipment, refer to the schematic diagrams in Section VI of this manual.

4.2 EQUIPMENT DESCRIPTION

The DPH Flex•Mode radio is a self-contained VHF FM radio operating in the 148 MHz to 174 MHz band.

The radio is digitally synthesized and uses a single crystal for frequency control. An EEPROM is incorporated for the storage of channel frequency, Code Guard™ values, Automatic Numeric Identifier (ANI), hardware tuning, and other operating information.

Connectors are provided on the side of the radio for the external antenna, microphone, speaker, and other optional accessories. Twist-off battery packs are also available. The 16 channels are fully programmable. The radio is shipped with stop pins so that the channel selector switch can be moved to limit the number of positions to any value.

4.3 THEORY OF OPERATION

Circuitry for the DPH Series radio comprises five major circuits:

- The RECEIVER, which consists of RF preselectors, RF amplifier, mixer, IF filters, IF amplifiers, FM IF IC, and noise squelch circuitry.
- The TRANSMITTER, which consists of a power amplifier, harmonic filter, antenna switch, and power control circuitry.
- The SYNTHESIZER, which consists of a voltage controlled oscillator (VCO), VCO buffer, prescaler buffer, prescaler, synthesizer IC, reference oscillator, loop filter, and acquisition aid bit circuit.
- The SYSTEMS area, which consists of a microprocessor, microprocessor oscillator, EEPROM, signaling and switching, front-end tuning amplifier, 5V and 8.2V regulators, transmitter audio processing, deviation compensation, squelch threshold circuitry, and receiver audio processing.
- The Digital Signal Processing (DSP) area, which consists of a Digital Signal Processor, Flash Memory, CODEC, TCXO, 1.8V and 3.3V regulators.

4.3.1 Receiver

The receiver is a dual-conversion design with intermediate frequencies of 16.9 MHz and 455kHz. RF signals received at the antenna pass through the antenna switch and front end. The front end consists of an amplifier and two microprocessor-tuned bandpass filters. The front end amplifies the receive frequency and attenuates image, half IF, and other frequencies that degrade receiver performance.

RF signals from the front end enter a mixer that converts them to 16.9 MHz. The 16.9 MHz IF signal passes through two crystal filters that provide adjacent channel selectivity. The IF amplifier then amplifies the signal and couples it to the 455 kHz IF integrated circuit. The 455 kHz IF IC consists of a mixer, limiter, demodulator, and squelch circuit. The 16.9 MHz signal enters the mixer and is converted to a 455 kHz IF signal. A ceramic filter at 455 kHz provides more adjacent channel selectivity. The signal is then amplified by the limiter and demodulated. Audio processing is then done on the options board. Filtered audio noise is used to provide a squelch indication.

A. RF Preselectors

The preselectors provide greater than 75 dB of attenuation at the image frequency. Both bandpass filters are varactor tuned, which allows a wide frequency spread. Overall, the preselectors exhibit a bandwidth of 4.5 MHz. The preselectors consist of **L2**, **L3**, **L4**, **L5**, and associated circuitry.

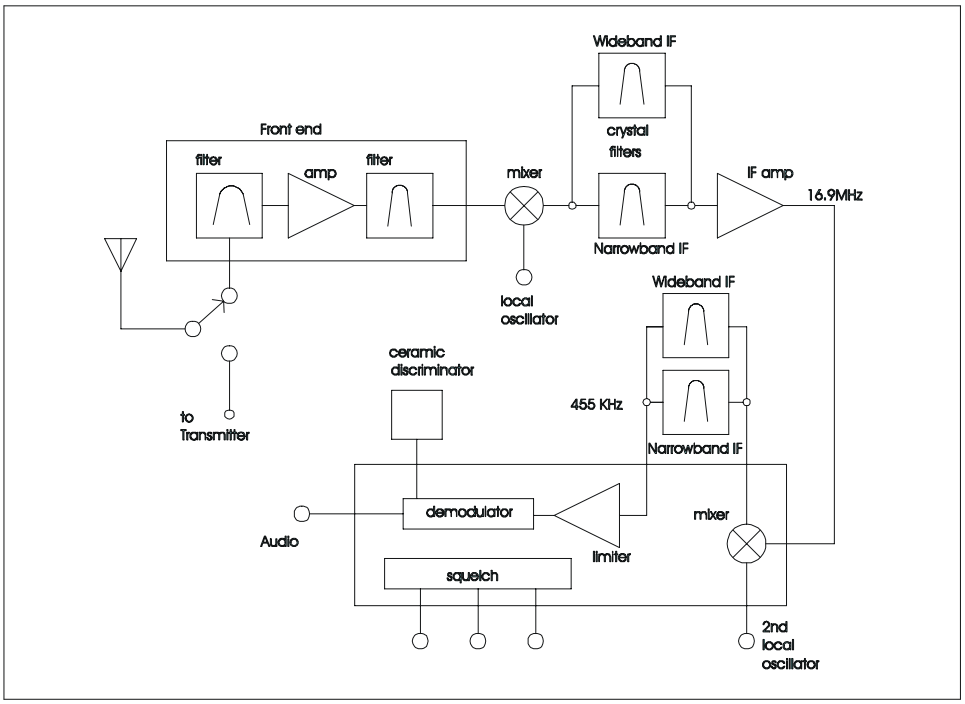

Figure 4-1 Receiver block diagram

B. RF Preamplifier

The RF amplifier is a single-transistor amplifier providing 22 dB of gain.

C. Mixer

The balanced diode mixer converts the RF frequency to 16.9 MHz.

D. 1st IF Filters and IF Amplifier

The crystal filters are centered at 16.9 MHz and provide attenuation to frequencies adjacent to the receive frequency. There are two sets of 1st IF filters - one for wideband (25/30 kHz) mode, and the other for narrowband (12.5/15 kHz) mode. The IF amplifier provides 26 dB of gain at 16.9 MHz.

E. FM IF IC

The FM IF IC provides a second mixer, a high-gain limiter, a demodulator, an OP-AMP, and a Schmitt trigger. The mixer converts the 16.9 MHz signal to 455 kHz. The local oscillator for the mixer consists of a 17.355 MHz crystal and associated circuitry. The 455 kHz signal is filtered by a ceramic filter. A limiter provides most of the gain for the receiver. The FM signal is demodulated by the demodulator, the ceramic discriminator, and associated circuitry.

F. Noise Squelch

The demodulated audio is bandpass filtered with an active filter consisting of the internal OP-AMP of the FM IF IC and external circuitry. Squelch gain control is provided by **Q6** and associated circuitry. The squelch noise is detected by the internal Schmitt trigger of the FM IF IC. The microprocessor samples the Schmitt trigger output to determine signal level and squelch information.

4.3.2 Transmitter

The transmitter consists of four major blocks (see figure below):

(1) Power Amplifier

(2) Harmonic Filter

(3) Antenna Switch

(4) Power Control

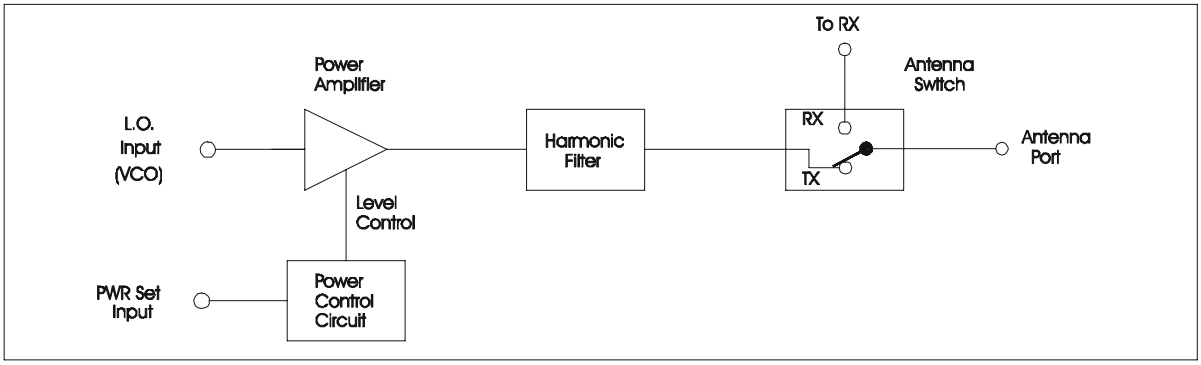

Figure 4-2 Transmitter block diagram

The power amplifier provides the necessary gain to amplify the VCO signal to a level of 5 Watts (1.5 Watts on low power models).

The harmonic filter is a seven-pole low-pass filter that provides rejection of the harmonics of the transmit frequency.

The antenna switch routes the RF signal from the antenna port to the transmitter while in transmit mode. In receive mode, the antenna port is routed to the receiver.

The power control circuit uses feedback to level the RF power from the transmitter.

A. Power Amplifier

The power amplifier comprises five RF amplifier stages (see Figure 4-3 below). These are:

(1) VCO Isolation buffer

(2) Low-Level Amplifier

(3) Predriver Stage

(4) Driver Stage

(5) Final Stage

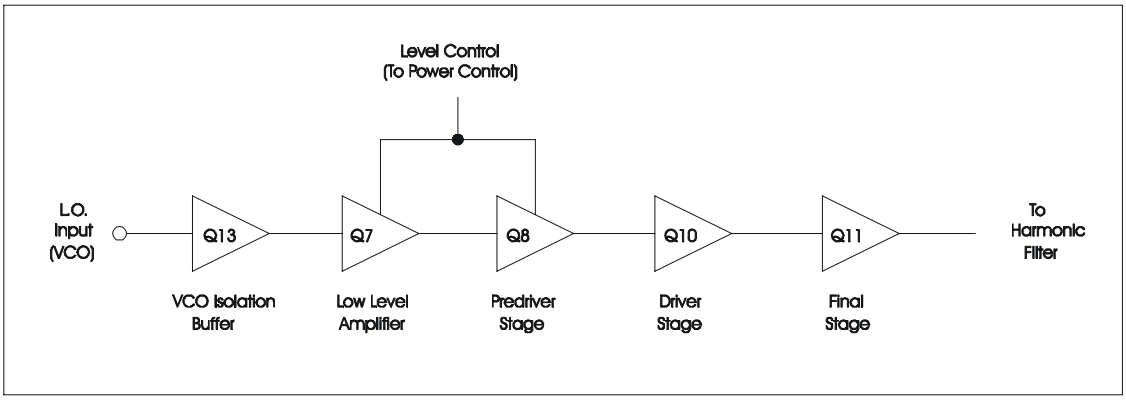

Figure 4-3 Power amplifier block diagram

The VCO Isolation Buffer (5W models only) prevents load changes from affecting the frequency of the VCO.

The Low Level Amplifier and Pre-Driver stages provide power gain. The bias current for these stages is controlled by the power control circuit. The transmitter is turned off by removing bias from these stages.

The Driver and Final stages provide power gain and are operated in class-C mode. The Final supplies sufficient RF power to meet the radio's output power specification after losses in the harmonic filter and antenna switch. The DC current to this combination is monitored by the power control circuit.

B. Harmonic Filter

The Harmonic Filter attenuates the harmonics created by the power amplifier to meet or exceed the transmit spurious and harmonic specification. The passband input and output impedances of the filter are 50 Ohms.

C. Antenna Switch

The antenna switch connects either the transmitter or receiver to the antenna.

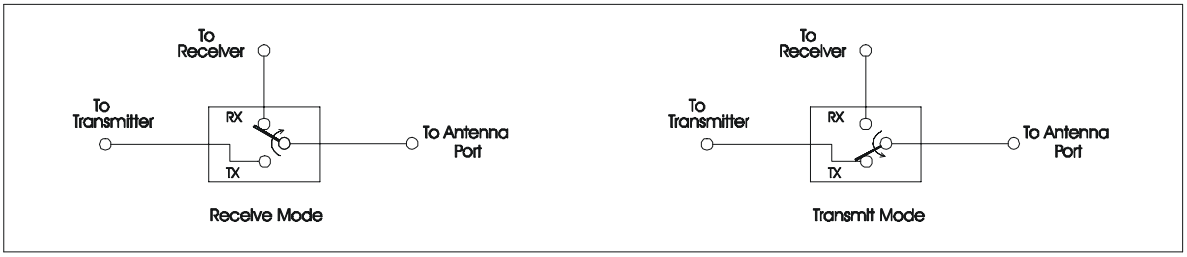

Figure 4-4 Antenna switch functional block diagram

In receive mode, both pin diodes in the antenna switch are turned on, completing a signal path to the transmitter and shunting the receiver path to ground. In transmit mode, both pin diodes are turned off, allowing RF signals to flow to the receiver with the transmitter output port removed from the circuit.

D. Power Control Circuit

The power control circuit monitors the DC supply current to the Driver and Final stages of the power amplifier. This current increases with RF output power and is kept constant by the power control circuit.

Current sensing is accomplished using a small resistance in the DC supply to the last two amplifier stages. The voltage developed across this resistance is fed to a bridge circuit and amplifier where it is compared to the "PWR SET" voltage. Any difference in the levels is amplified and used to control the bias current to the Low Level Amplifier and Pre-Driver stages.

4.3.3 Synthesizer

The synthesizer generates an RF signal either to down-convert a desired receive frequency to a fixed IF or to drive the transmitter. The synthesizer is essentially a phase-locked loop that locks the RF output of a voltage controlled oscillator (VCO) to a very stable lower frequency reference. The microcontroller determines the frequency that the synthesizer produces by programming the dividers contained within the synthesizer IC or the reference oscillator.

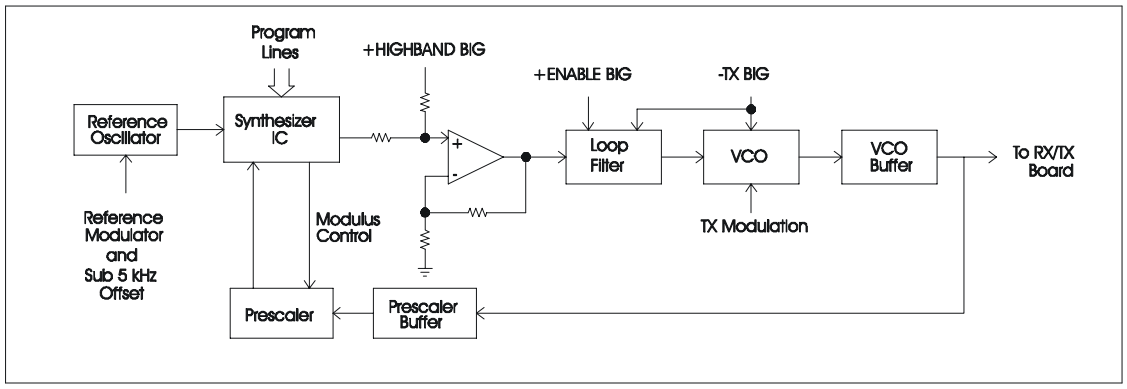

Figure 4-5 Synthesizer block diagram

A. Voltage-Controlled Oscillator (VCO)

Transistor **Q4** provides the gain, and an L-C resonant tank circuit provides the frequency selectivity and phase shift necessary to produce an oscillator. Frequency control of the oscillator is accomplished by the tuning tank circuit comprised of mechanically adjustable transformer **T1** and varactors **CR4** and **CR5**. **CR4** is used to lock the VCO to the desired carrier frequency while **CR5** is used in the transmit mode to modulate the carrier. The oscillator frequency range is 148-174 MHz in the transmit mode and 131.1-157.1 MHz in the receive mode (low side injection). The 16.9 MHz shift from transmit to receive is achieved by turning on PIN diode **CR3**, thus adding **L4** to the tank circuit. **Q5** and associated circuitry provide additional power supply filtering for the VCO. Diode **CR6** gives the filter a rapid power up response while maintaining a very low cutoff frequency.

B. VCO Buffer

The VCO buffer is a cascode configuration with bipolar transistor **Q3** feeding common gate FET **Q21**. It isolates the VCO from the receiver/transmitter circuitry and provides enough power gain to supply a nominal level of +3 dBm in receive and +0 dBm in transmit.

C. Prescaler Buffer

Prescaler buffer Q2 provides isolation between the prescaler and receiver/transmitter circuitry and additional isolation between the prescaler and the VCO.

D. Prescaler

Prescaler U11 divides the RF signal provided by the prescaler buffer to a frequency that can be processed by the synthesizer IC. The prescaler is of the dual modulus type, which allows the divide value to be set by the synthesizer IC to either divide-by-40 (modulus control line high) or divide-by-41 (modulus control line low). This capability allows the RF signal frequency to be divided by integers that are not multiples of either 40 or 41.

E. Synthesizer IC

Synthesizer chip **U12** contains three programmable CMOS dividers, a sample-and-hold phase detector, and an amplifier that forms an on-chip reference oscillator when connected to the terminals of an external crystal **Y1**. The first divider (divide-by-R) divides the reference oscillator to a frequency that is used as a reference by the sample-and-hold phase detector. The second divider (divide-by-N) divides the output of the prescaler to a frequency equal to the divided reference frequency when the loop is locked. The third divider (divide-by-A) controls the modulus control line of the prescaler. The sample-and-hold phase detector provides a DC voltage that is proportional to the phase error between the divided reference and the divided carrier. This voltage is fed through the loop filter to the VCO and adjusts the VCO frequency in a direction to maintain phase and frequency lock between the two signals.

F. Reference Oscillator

The reference oscillator provides the reference frequency from which the receiver and transmitter injection signals are synthesized. The oscillator frequency is controlled by crystal **Y1**, which operates in the parallel resonant mode across an amplifier built into the synthesizer IC. This crystal is compensated to ±3 PPM by a temperature-compensating circuit built around a temperature-sensing IC, **U19**, varactors **CR1** and **CR2** and the microcontroller, **U1**. The crystal frequency/temperature characteristics have been loaded into the EEPROM. The microcontroller monitors the temperature and applies the correct voltage to the varactors to stabilize the operating frequency. When operating on a channel frequency that is not an integer multiple of 5 kHz, the reference frequency is moved the appropriate amount. In addition, a method of modulation is provided to improve the synthesizer frequency response to low frequency modulation.

G. Loop Filter

The loop filter removes noise and unwanted frequency components from the output of the sample-and-hold phase detector that would otherwise modulate the VCO. The loop filter uses a multiple filter bandwidth design that allows fast response during frequency changes (such as in Channel Scan) without degrading the noise and spurious performance of the synthesizer during steady-state receive or transmit conditions. The filter is switched to a wide bandwidth condition when the +ENABLE BIG line pulses high for approximately 4 mSec during a frequency change. This allows the new frequency to be reached quickly. When the +ENABLE BIG line returns to the low state, the filter bandwidth changes to a narrow condition and provides for good noise and spurious performance. Finally, different filter bandwidths are used from transmit to receive to provide better hum and noise performance on transmit and better response time on receive. This is accomplished by changing the filter bandwidth to a narrower value when the -TX BIG line goes low during transmit.

H. Acquisition Aid Bit

The +HIGHBAND BIG signal summed with the synthesizer IC phase-detector output prior to the loop filter helps to keep the phase detector operating near the middle of its range. This bit is low for the lower half of either the receive or transmit band and is high for the upper half of either band.

4.3.4 Systems Area

A variety of functions are included in the systems area.

A 5-volt precision voltage regulator provides power to the microprocessor and several other ICs in the radio. The -RESET signal from this circuit will prevent any radio functions if the battery voltage falls too low. The 8.2-volt regulator is used for synthesizer and VCO functions. An output signal will alert the processor if the battery voltage falls too low for proper operation.

Several special transmitter features are implemented by the microprocessor. These include repeater-talk-around, busy channel lockout, DTMF generation, ANI generation, sub-audible Code Guard generation, and transmit timeout timer.

Receive mode special features provided by the microprocessor include channel scan, dual priority scan, scan hold timer, battery saver, and tone and digital guard decoding.

Other functions performed by the microprocessor are synthesizer control and data loading, channel and hardware information storage, reference oscillator temperature compensation, provision of a receiver front-end tuning voltage, interpretation of the user switches, generation of display information, and remote and keypad programming mode.

A. Microprocessor

The microprocessor **U1** receives inputs from user switches and controls radio functions such as loading the synthesizer, adjusting the transmitter deviation, tuning the receiver, setting transmit power, time-out functions, etc.

B. Microprocessor Oscillator

The microprocessor oscillator consists of **Y2** and associated circuitry. The frequency of oscillation can be altered slightly by **Q22** and **Q29** to prevent interference when tuned to receive channels that are exact multiples of 4 MHz.

C. EEPROM

The EEPROM **U7** stores channel information and hardware compensation values.

D. Signaling and Switching

The signaling D/A and switching network consists of **RN1**, **U4**, and **U14**. This circuitry allows the microprocessor to generate transmit Code Guard, DTMF and ANI, and various audio beeps heard in the speaker.

E. Front-End Tuning and Power-Set

The front-end tuning and power-set D/A converter is composed of **U17** and amplifier **U3**. In receive mode, the voltage from **U17** is used to tune the front-end filters on the RX/TX board. In transmit mode, it is used to set the transmitter power.

F. 5V Regulator and Low-Voltage Reset

U8 provides a regulated 5-volt supply for the radio. An output signal from the regulator will force the microprocessor into a reset condition if the battery voltage drops below about 5 volts.

G. 8.2V Regulator and Low-Battery Shutdown

An 8.2 volt regulator is composed of **U3**, **Q10**, and associated circuitry. Regulator operation is monitored via **Q11**. The microprocessor will shut down radio operation if a low-battery or 8.2-volt short circuit occurs. **U14** is used to switch the regulator off during battery-saver mode.

H. Receive Audio

U9 is a 0.5 Watt audio amplifier. Muting is controlled by the microprocessor.

I. Deviation Compensation

The transmit deviation compensation is accomplished by digital potentiometer **U18**. At higher transmitter frequencies, less voltage is needed for VCO modulation, so this circuit attenuates the signal. Also, when Code Guard tones are being transmitted, the deviation sensitivity is reduced; overall deviation remains constant.

J. Channel Switch Multiplexer

The channel switch multiplexer **U5** allows four lines to the microprocessor to be shared between two different functions. In receive mode, the channel selector switch position can be examined via **U5**. In transmit mode, **U5** is used to disconnect the channel switch from the microprocessor so that these signals can be used for the signaling D/A converter.

K. Squelch Threshold Preset

Pin 11 of **U5** is used to switch a resistor into the squelch circuit, thus lowering the squelch threshold when the Squelch knob is in the "preset" position.

4.3.5 Digital Signal Processing

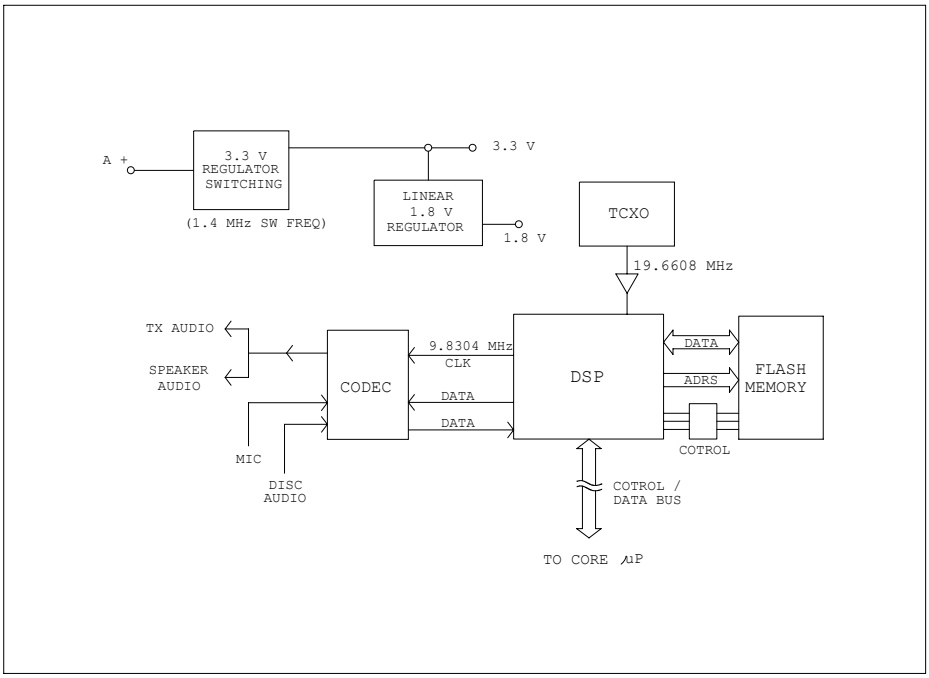

Figure 4-6 Digital Signal Processing Block Diagram

A. Digital Signal Processor

Implements filters and other signal processing algorithms.

B. Flash Memory

The flash memory stores DSP code.

C. CODEC

Converts analog signals to digital signals and vice versa.

D. TCXO

Provides stable oscillator frequency for DSP.

E. 3.3V Switching Regulator

Provides 3.3V for circuits on board.

F. 1.8V Regulator

Provides 1.8V for DSP core.

4.3.6 Internal Oscillators and Clocks

Frequency	Osc./Clock Description
200 kHz	LCD Driver
19.6608 MHz	DSP TCXO
78.6432 MHz	DSP Clock
1.4 MHz	Switching Regulator, 3.3V
9.8304 MHz	CODEC Clock
38.400 kHz	CODEC Data Transfer
1200 Hz	Low Frequency Digital Sample Transfer
1280 Hz	Low Frequency Analog Sample Transfer
32.768 kHz	Core μP Crystal
7.3728 MHz	Core μP Clock
10 MHz	Reference Oscillator
17.355 MHz	2nd Local Oscillator

Table 4-1 Internal Oscillators & Clocks