THEORY OF OPERATION

MRHH400

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This PLL - controlled VHF marine transceiver provides an accurate and stable multi-channel operation.

The transceiver consists of 6 main sections:

- **Transmitter**
- **Receiver**
- **Low voltage detection**
- **Weather alert**
- **Local oscillator PLL (Phase Lock Loop) Circuit**
- **Memory backup**

- **Transmitter**

  The audio is picked up from the internal MIC, the audio signal is then amplified by Audio Amplifier, IC8 LM324 (3/4), IC7 (2/4) and filtered by a low pass filter IC8 (1/4). The audio is adjusted with VR3 to obtain a suitable Audio frequency response, and then modulated with the carrier by VCO, through Varicap (D6).

  The modulated signal output from the VCO is pre-amplified by Q3, Q4 and Q2. Then it is amplified by Q25, Q24 .The amplified signal then passes through a low -pass filter network which consists of L7, C83, C11, L6, C60 filters out spurious emission, and the antenna switching circuit, D3, D1. The signal is filtered by another low-pass filter circuit which consists of C9, L2, C6, C8, L1, C5, C1. These low pass filters are necessary to suppress the second and third harmonics. The signal is then fed into the antenna input and radiated out. The signal is also fed into another path consisting of C82,D2, R35 for sampling, and is converted into a direct current voltage for the Automatic power control (APC) circuit IC1, Q12, VR6, Q15.

  When the unit is transmitting, the audio signal is added to the TX VCO Varicap D6. The capacitance of D6 is varied following the audio signal and when mixed with the carrier to form the modulated signal.

- **Receiver**

  The receiver uses a double frequency super-heterodyne circuit. The first Immediate Frequency (IF) is 21.4 MHz and the second is 450 kHz.

  The RF signal is received by the antenna, and passes through a low-pass filter network C1, L1, C5, C8, L2, C6, C9, C12, L3 to filter out the unwanted signals, the antenna switching circuit D1 switching circuit to receive. The received RF signal then passes through a band RF transformer L4, L24, C53, D8, D9, L15. And is amplified by RF amplifier Q21. L26, L15, L11, D10, D7, C170, L16 form the band pass filter. The RF signal then is mixed with the local oscillation frequency by the mixer Q23. A first IF (Immediate Frequency) 21.4 MHz is

produced. The IF is passed through a pair of crystal filter F1 (1/2), F2 (2/2) to further filter other unwanted signals. The first IF then is amplified by Q1 and the IF amplifier IC4 (BA4116). IC4 is a integrated RF amplifier which consists of a local oscillator, a demodulator, a second mixer, squelch control circuit, and RF amplifier. The 21.4 MHz IF then is mixed here with second mixer and converted into 2nd Immediate Frequency (IF) 450 kHz. The 2nd IF passes through a ceramic filter F3 to filter out the residue unwanted signal at pin 5 of IC4 (BA4116) output this final IF signal and the Audio signal is output at pin 9 of IC4 (BA4116).

The audio signal is fed through a volume control VR4 and finally amplified by Audio amplifier IC3 (NJM2070) and heard in the speaker.

The squelch control is also controlled by IC4 (BA4116). The second IF passes through IC4 (BA4116) internal squelch control R76, C143, C142 form as a squelch amplifier. The ceramic filter produces a squelch signal (RF noise). Pin 14 of IC4 sends the digital squelch control signal to the CPU mute the audio speaker path. Pin 12 of IC4 output a RSSI level to the CPU.

- **Low Voltage Detection**

  The battery voltage, divided by R75, R74 is input to IC6 Pin 41 for voltage level sample.

- **PLL (Phase Lock Loop) Circuit:**

  The receiver and transmitter both share the same PLL (Phase Lock Loop) Circuit to produce the carrier or the receive frequency. The local oscillator consists of a fundamental frequency oscillator X1 20.95MHz and IC5 (KB8825). A phase Lock Loop (PLL) IC5 (KB8825), TX VCO Q22 and RX VCO Q20. The fundamental frequency is frequency divided by IC5 and a 25 kHz signal is produced. When the VCO frequency applied to and frequency divided by IC5 produces a frequency comparable to 25 kHz, PLL will control the VCO. When these two frequencies are matched, a constant control voltage is output from PLL to lock VCO in desired frequency. The PLL also will output a lock indication to cpu to indicate the PLL is in frequency lock state.

- **Memory Backup**

  IC2 is an EEPROM AT24C16 which acts as a memory backup for the working channel code and the system parameters. Every time when the unit is switched on, the cpu will reset the system, clear the RAM, and recall in the memory from the EEPROM to refresh the RAM in CPU IC2.