SIM7500A Hardware Design

LTE Module

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2016-07-06	1.00	Original	Yuan Shijie Tenglili
2016-11-01	1.01	Modify Document name	Shengwu.sun Shijie.yuan LiLi.teng
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		Modify GPIO_49 to FlightMode	
		Modify VBUS Minimum Voltage from 3.6V to 3.0V	
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Contents

Table Index

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1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics and testing results of the SIMCom SIM7500A. With the help of this document and other software application notes/user guides, users can understand and use modules to design and develop applications quickly.

1.1 Product Outline

The SIM7500A support many air-interface standards, refer to the following table.

Table 1: Module frequency bands (* stands for SIM7500)

Standard	Frequency	SIM7500A
GSM	850MHz	
	900MHz	
	1800M Hz	
	1900M Hz	
WCDMA	B1	
	B2	
	B5	
	B8	
LTE	FDD B1	
	FDD B2	√
	FDD B3	
	FDD B4	√
	FDD B5	
	FDD B7	
	FDD B8	
	FDD B12	√
	FDD B13	
	FDD B18	
	FDD B19	
	FDD B20	
	FDD B26	
	FDD B28	
Category		CAT1
GNSS		√

With a small physical dimension of 24*27*2.75 mm and with the functions integrated, the Module can meet almost any space requirement in users' applications, such as smart phones, PDA's, industrial handhelds, machine-to-machine, vehicle applications, etc.

NOTE

CAT1 or CAT4 correspond to different PN numbers.

1.2 Hardware Interface Overview

The interfaces are described in detail in the next chapters include:

- Power Supply
- USB Interface
- UART Interface
- SIM Interface
- GPIO
- ADC
- Power Output
- Current Sink Source
- PCM Interface
- I2C Interface

1.3 Hardware Block Diagram

The block diagram of the Module is shown in the figure below.

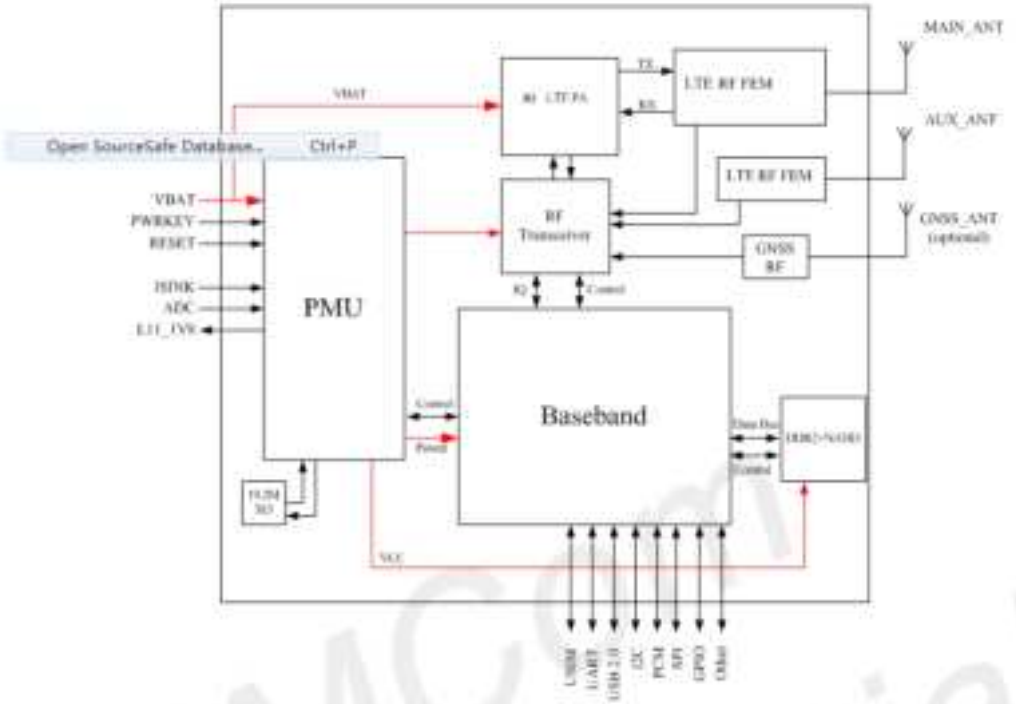

Figure 1: SYS Block Diagram

	TX	RX
LTE		
B2	1850~1910MHz	1930~1990MHz
B4	1710~1755MHz	2110~2155MHZ
B12	699 ~716 MHz	729 ~746 MHz

Figure 1: SIM7500A Block Diagram

1.4 Functional Overview

Table 2: General features

Feature	Implementation
Power supply	Single supply voltage 3.4～4.2V
Power saving	Current in sleep mode : <5mA
Radio frequency bands	Please refer to the table 1
Transmitting power	LTE: Class 3 (23dBm)

Data Transmission Throughput	FDD-LTE CAT 1：10 Mbps (DL), 5 Mbps (UL)
Antenna	LTE main antenna LTE auxiliary antenna GNSS antenna
GNSS	GNSS engine (GPS,GLONASS , BD and QZSS GALILEO) Protocol: NMEA
SMS	MT, MO, CB, Text and PDU mode SMS storage: SIM card or ME(default) Transmission of SMS alternatively over CS or PS.
SIM interface	Support identity card: 1.8V/ 3V
SIM application toolkit	Support SAT class 3, GSM 11.14 Release 98 Support USAT
Phonebook management	Support phonebook types: DC,MC,RC,SM,ME,FD,ON,LD,EN
Audio feature	Support PCM interface Only support PCM master mode and short frame sync, 16-bit linear data formats
UART interface	A full modem serial port by default Baud rate: 300bps to 4Mbps(default:115200bps) Can be used as the AT commands or data stream channel. Support RTS/CTS hardware handshake Multiplex ability according to GSM 07.10 Multiplexer Protocol.
USB	USB 2.0 specification-compliant as a peripheral
Firmware upgrade	Firmware upgrade over USB interface USB 2.0 specification-compliant as a peripheral
Physical characteristics	Weight:4.0 g Size:24*27*2.75mm
Temperature range	Normal operation temperature: 25°C High temperature: 55°C Low temperature -10°C

NOTE

Module is able to make and receive voice calls, data calls, SMS and make WCDMA/HSPA+/LTE traffic in -40℃ ~ +85℃. The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

2 Package Information

2.1 Pin Assignment Overview

All functions of the SIM7500A will be provided through 56 pads that will be connected to the customers' platform. The following Figure is a high-level view of the pin assignment of the SIM7500A.

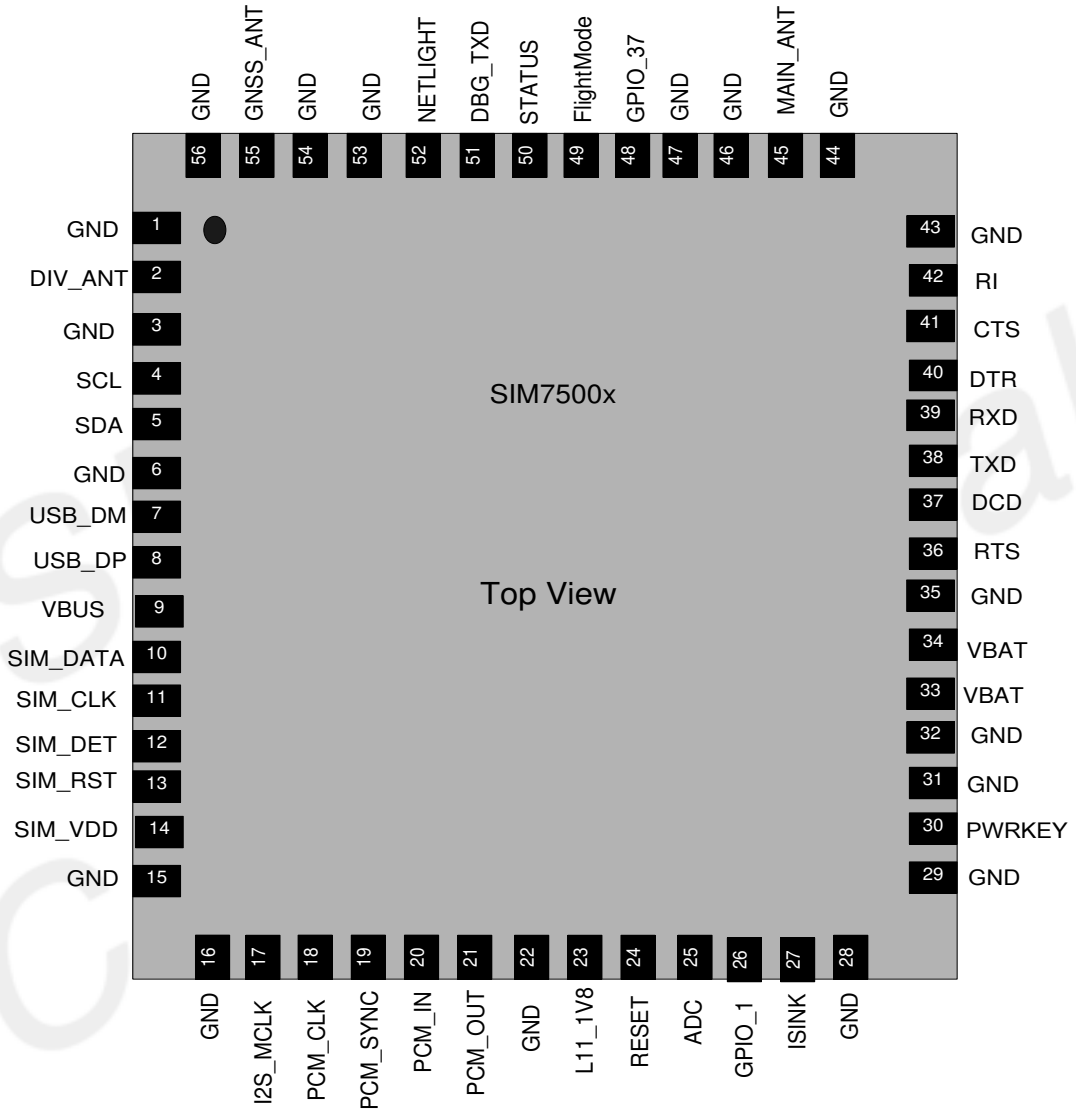

Figure 2: Pin assignment overview

Table 3: Pin Definitions

Pin No.	Pin name	Pin No.	Pin name
1	GND	2	DIV_ANT
3	GND	4	SCL
5	SDA	6	GND
7	USB_DM	8	USB_DP
9	VBUS	10	SIM_DATA
11	SIM_CLK	12	SIM_DET
13	SIM_RST	14	SIM_VDD
15	GND	16	GND
17	I2S_MCLK	18	PCM_CLK
19	PCM_SYNC	20	PCM_IN
21	PCM_OUT	22	GND
23	L11_1V8	24	RESET
25	ADC	26	GPIO_1
27	ISINK	28	GND
29	GND	30	PWRKEY
31	GND	32	GND
33	VBAT	34	VBAT
35	GND	36	RTS
37	DCD	38	TXD
39	RXD	40	DTR
41	CTS	42	RI
43	GND	44	GND
45	MAIN_ANT	46	GND
47	GND	48*	GPIO_37
49	FlightMode	50	STATUS
51	DBG_TXD	52	NETLIGHT
53	GND	54	GND
55	GNSS_ANT	56	GND

NOTE

Before the normal power up, pin48 cannot be pulled up.

2.2 Pin Description

Table 4: IO parameters definition

Pin type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input
DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down

Table 5: Pin Description

Pin name	Pin No.	Default status	Description	Comment
Power supply				
VBAT	33,34	PI	Power supply, voltage range: 3.4～4.2V.	
L11_1V8	23	PO	1.8V output with Max. 50ma current output for external circuit, such as level shift circuit.	If unused, keep it open.
GND	1, 3, 6, 15,16,22,28, 29,31,32,35, 43,44,46,47, 53,54,56		Ground	
System Control				
PWRKEY	30	DI,PU	System power on/off control input, active low.	Default 0.8V
RESET	24	DI, PU	System reset control input, active low.	RESET has been pulled up to 1.8V via a resistor internally.
SIM interface				
SIM_DATA	10	I/O,PU	SIM Card data I/O, which has been pulled up via a 10KR resistor to SIM_VDD internally.	All lines of SIM interface should be protected against
SIM_RST	13	DO	SIM Reset	

SIM_CLK	11	DO	SIM clock	ESD.
SIM_VDD	14	PO	Power output for SIM card, its output Voltage depends on SIM card type automatically. Its output current is up to 50ma.	
USB				
VBUS	9	DI,PD	Valid USB detection input with 3.0～5.25V detection voltage	
USB_DM	7	I/O	Negative line of the differential, bi-directional USB signal.	
USB_DP	8	I/O	Positive line of the differential, bi-directional USB signal.	
UART interface				
RTS	36	DOL	Request to send	If unused, keep them open.
CTS	41	DI,PU	Clear to Send	
RXD	39	DI,PU	Receive Data	
RI	42	DOH	Ring Indicator	
DCD	37	DOH	Carrier detects	
TXD	38	DOH	Transmit Data	
DTR	40	DI,PU	DTE get ready	
I2C interface				
SCL	4	DO	I2C clock output	If unused, keep them open.
SDA	5	I/O	I2C data input/output	
PCM interface				
PCM_OUT	21	DO	PCM data output.	If unused, please keep them open.
PCM_IN	20	DI	PCM data input.	
PCM_SYNC	19	DO	PCM data frame sync signal.	
PCM_CLK	18	DO	PCM data bit clock.	
I2S_MCLK	17	DO	Audio Master clock	
GPIO				
NETLIGHT	52	DO	LED control output as network status indication.	If unused, please keep them open. FlightMode Can't be used when Module is in sleep mode.
STATUS	50	DO	Operating status output. High level: Power on and firmware ready Low level: Power off	
GPIO_1	26	IO	GPIO	
FlightMode	49	DI,PU	Flight Mode control input. High level(or open): Normal Mode Low level: Flight Mode	
SIM_DET	12	IO	Default: GPIO Optional: SIM card detecting input. H: SIM is removed L: SIM is inserted	
GPIO_37	48	IO	Boot configuration input. Module will be forced into USB down load mode by connect 23 pin to VDD_1V8 during power up.	

RF interface				
MAIN _ANT	45	AIO	MAIN antenna soldering pad	
DIV_ANT	2	AI	Auxiliary antenna soldering pad	
GNSS_ANT	55	AI	GNSS antenna soldering pad	
Other interface				
ISINK	27	AI	Ground-referenced current sink.	If unused, please keep them open.
DGB_TXD	51	DO	Use for debug	
ADC	25	AI	Analog-digital converter input	

2.3 Mechanical Information

The following figure shows the package outline drawing of Module.

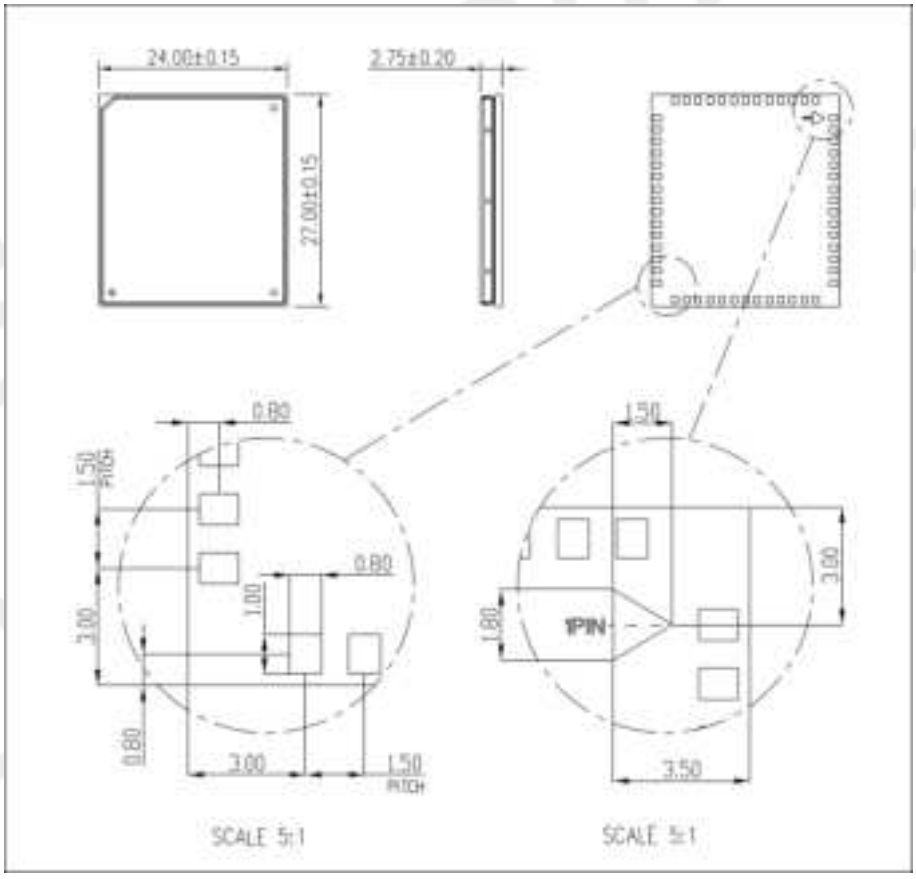

Figure 3: Dimensions (Unit: mm)

2.4 Footprint Recommendation

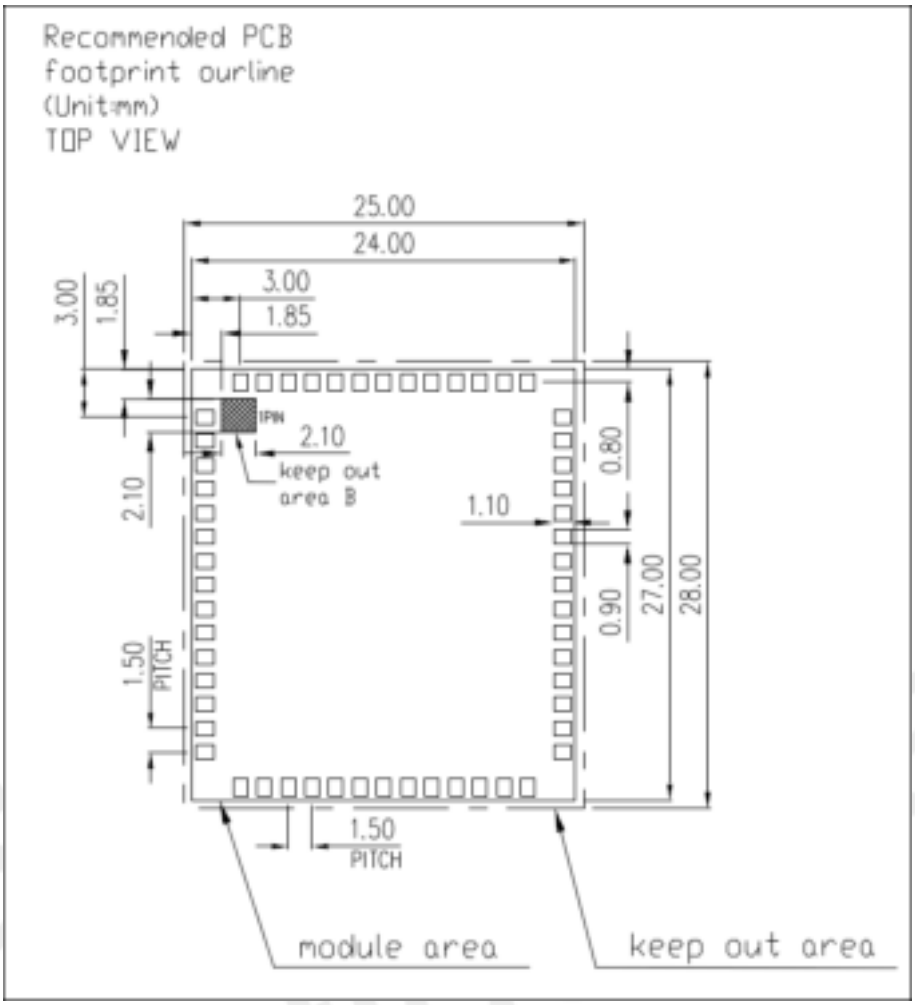

Figure 4: Footprint recommendation (Unit: mm)

3 Interface Application

3.1 Power Supply

On VBAT pads, a ripple current up to 2A typically, may cause voltage drop. Therefore, the power supply for these pads must be able to provide sufficient current up to more than 2A in order to avoid the voltage drop of more than 300mV.

Table 6: VBAT Pins electronic characteristic

Symbol	Parameter	Min	Type	Max	Unit
VBAT	Module power voltage	3.4	3.8	4.2	V
$I_{VBAT(peak)}$	Module power peak current in normal mode.	1.0	-	2	A
$I_{VBAT(average)}$	Module power average current in normal mode	Please refer to the table 34			
$I_{VBAT(sleep)}$	Power supply current in sleep mode				
$I_{VBAT(power-off)}$	Module power current in power off mode.	-	-	20	uA

3.1.1 Power supply Design Guide

Make sure that the voltage on the VBAT pins will never drop below 3.4V.

NOTE

If the power supply for BAT pins can support up to 2A, using a total of more than 220uF capacitors is recommended, or else users must use a total of 1000uF capacitors, in order to avoid the voltage drop of more than 300mV.

Some multi-layer ceramic chip (MLCC) capacitors (0.1/1uF) with low ESR in high frequency band can be used for EMC.

These capacitors should be put as close as possible to VBAT pads. Also, user should keep VBAT trace on the circuit board wider than 2 mm to minimize PCB trace impedance. The following figure shows the recommended circuit.

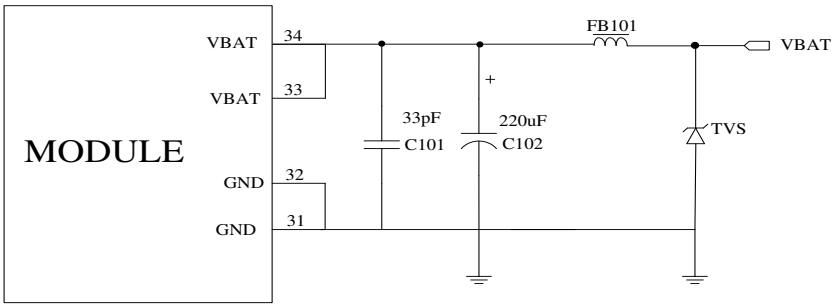

Figure 5: Power supply application circuit

In addition, in order to guard for ESD or surge protection, it is suggested to use a TVS to protect the module.

Table 7: Recommended TVS list

No	Manufacturer	Part Number	Reverse Stand-Off Voltage	Package
1	Js-ele	ESDBW5V0A1	5V	DFN1006-2L
2	Prisem	PESDHC2FD4V5BH	4.5V	DFN1006-2L
3	Way-on	WS05DPF-B	5V	DFN1006-2L
4	Will semi	ESD5611N	5V	DFN1006-2L
5	Will semi	ESD56151W05	5V	SOD-323
6	Way-on	WS4.5DPV	4.5V	DFN1610-2L

3.1.2 Recommended Power Supply Circuit

It is recommended that a switching mode power supply or linear regulator power supply is used. It is important to make sure that all the components used in the power supply circuit can resist a peak current up to 2A.

The following figure shows the linear regulator reference circuit with 5V input and 3.8V output.

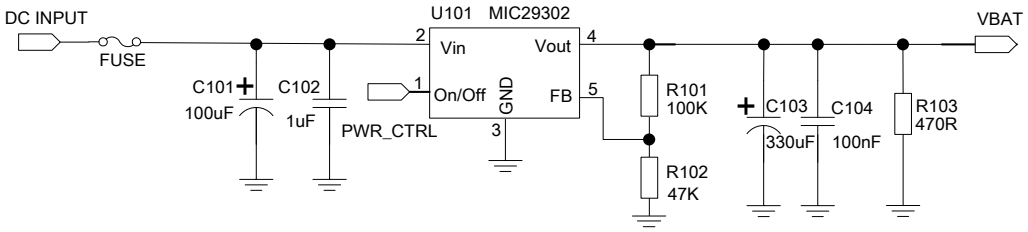

Figure 6: Linear regulator reference circuit

If there is a big voltage difference between input and output for VBAT power supply, or the efficiency is extremely important, then a switching mode power supply will be preferable. The following figure shows the switching mode power supply reference circuit.

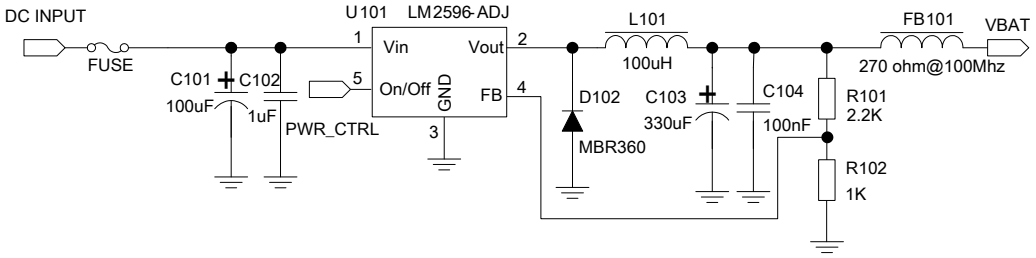

Figure 7: Switching mode power supply reference circuit

NOTE

The Switching Mode power supply solution for VBAT must be chosen carefully against Electro Magnetic Interference and ripple current from depraving RF performance.

3.1.3 Voltage Monitor

To monitor the VBAT voltage, the AT command “AT+CBC” can be used.

For monitoring the VBAT voltage outside or within a special range, the AT command “AT+CVALARM” can be used to enable the under-voltage warning function.

If users need to power off Module, when the VBAT voltage is out of a range, the AT command “AT+CPMVT” can be used to enable under-voltage power-off function.

NOTE

Under-voltage warning function and under-voltage power-off function are disabled by default. For more information about these AT commands, please refer to Document [1].

3.2 Power on/Power off/Reset Function

3.2.1 Power on

Module can be powered on by pulling the PWRKEY pin down to ground.

The PWRKEY pin has been pulled up with a diode to 1.8V internally, so it does not need to be pulled up externally. It is strongly recommended to put a100nF capacitor, an ESD protection diode, close to the PWRKEY pin as it would strongly enhance the ESD performance of PWRKEY pin. Please refer to the following figure for the recommended reference circuit.

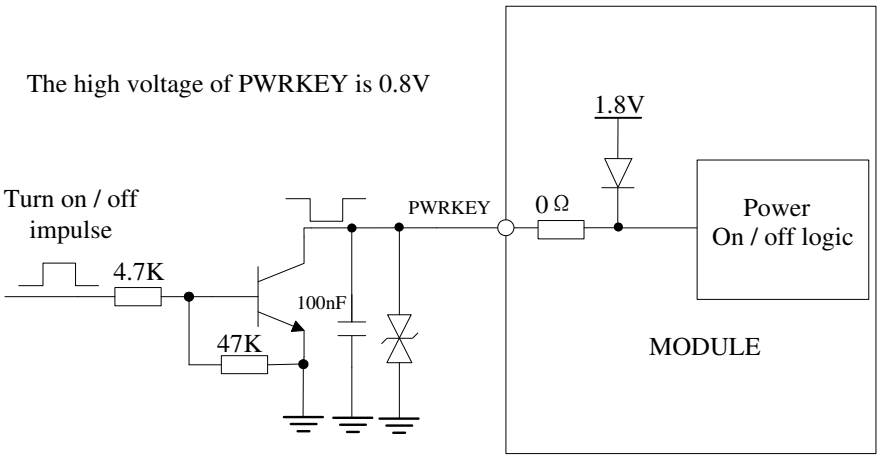

Figure 8: Reference Power on/off Circuit

NOTE

Module could be automatically power on by connecting PWRKEY pin to ground via 0R resistor directly.

The power-on scenarios are illustrated in the following figure.

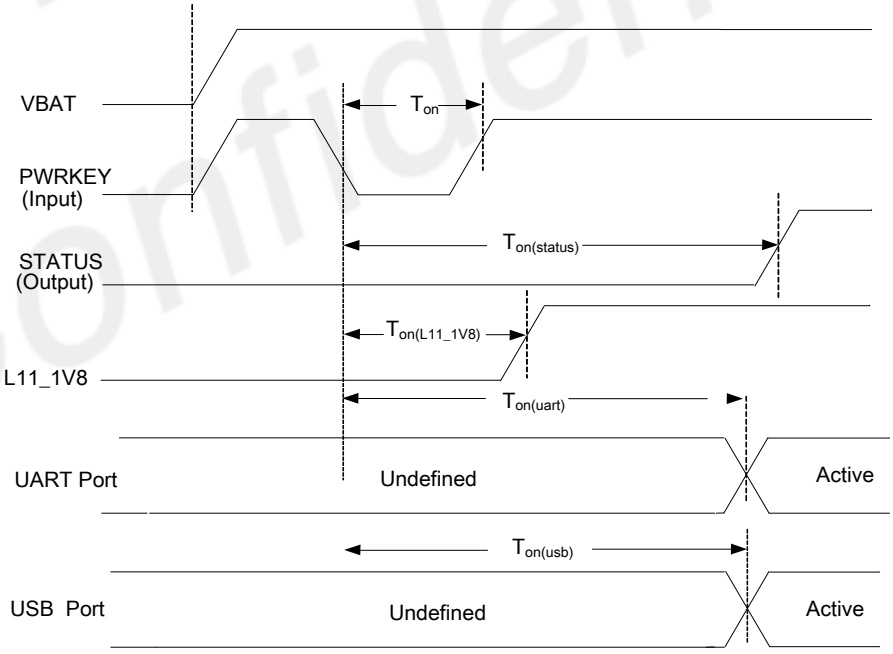

Figure 9: Power on timing sequence

Table 8: Power on timing and Electronic Characteristic

Symbol	Parameter	Min	Type	Max	Unit
T_{on}	The time of active low level impulse of PWRKEY pin to power on module	100	500	-	ms
$T_{on(status)}$	The time from power-on issue to STATUS pin output high level(indicating power up ready)	12	13	-	s
$T_{on(L11\_1V8)}$	The time from power-on issue to L11_1V8 ready	100	-	-	ms
$T_{on(uart)}$	The time from power-on issue to UART port ready	11	12		s
$T_{on(usb)}$	The time from power-on issue to USB port ready	11	12		s
V_{IH}	Input high level voltage on PWRKEY pin	0.6	0.8	1.8	V
V_{IL}	Input low level voltage on PWRKEY pin	-0.3	0	0.5	V

3.2.2 Power off

The following methods can be used to power off Module.

- Method 1: Power off Module by pulling the PWRKEY pin down to ground.
- Method 2: Power off Module by AT command “AT+CPOF”.
- Method 3: Over-voltage or under-voltage automatic power off. The voltage range can be set by AT command “AT+CPMVT”.
- Method 4: Over-temperature or under-temperature automatic power off.

NOTE

If the temperature is outside the range of -30~+80℃, some warning will be reported via AT port. If the temperature is outside the range of -40~+85℃, Module will be powered off automatically.
For details about “AT+CPOF” and “AT+CPMVT”, please refer to Document [1].

These procedures will make modules disconnect from the network and allow the software to enter a safe state and save data before modules are powered off completely.
The power off scenario by pulling down the PWRKEY pin is illustrated in the following figure.

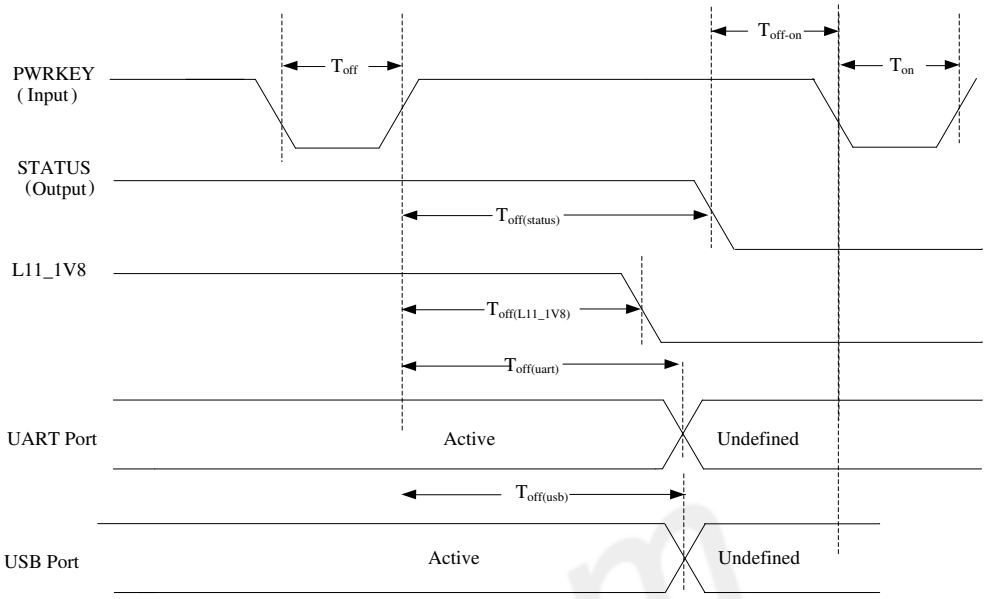

Figure 10: Power off timing sequence

Table 9: Power off timing and Electronic Characteristic

Symbol	Parameter	Time value			Unit
		Min	Type	Max	
Toff	The active low level time pulse on PWRKEY pin to power off module	2.5	--	5.0	s
Toff(status)	The time from power-off issue to STATUS pin output low level(indicating power off)*	25	26	-	s
$T_{off(L11\_1V8)}$	The time from power-off issue to L11_1V8	20	-	-	s
Toff(uart)	The time from power-off issue to UART port off	14	15	-	s
Toff(usb)	The time from power-off issue to USB port off	27	28	-	s
Toff-on	The buffer time from power-off issue to power-on issue	0	-	-	s

NOTE

The STATUS pin can be used to detect whether module is powered on or not. When module has been powered on and firmware goes ready, STATUS will be high level, or else STATUS will still low level.
It is suggested that the host can cut off the power off the module, when the module could not switch off by PWRKEY of RESET interface, customer could cut off the power to restart the module.
If the PWERKY and RESET key works normally, it is not suggested to switch off module by remove the power supply for that might damage the flash.
The power off time may vary for the local net status.

3.2.3 Reset Function

Module can be reset by pulling the RESET pin down to ground.

NOTE

This function is only used as an emergency reset when AT command “AT+CPOF” and the PWRKEY pin all have lost efficacy.

The RESET pin has been pulled up to 1.8V internally, so it does not need to be pulled up externally. It is strongly recommended to put a100nF capacitor and an ESD protection diode close to the RESET pin. Please refer to the following figure for the recommended reference circuit.

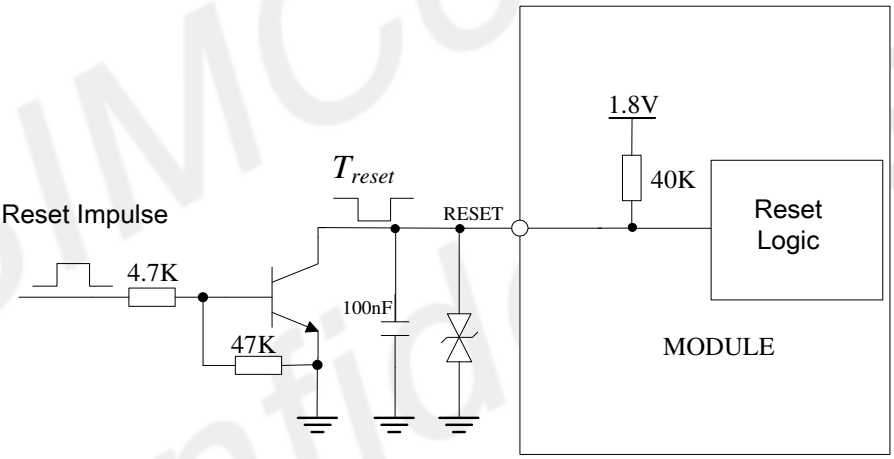

Figure 11: Reference reset circuit

Table 10: RESET pin electronic characteristic

Symbol	Parameter	Min	Type	Max	Unit
T_{reset}	The active low level time impulse on RESET pin to reset module	100			ms
V_{IH}	Input high level voltage	1.17	1.8	2.1	V
V_{IL}	Input low level voltage	-0.3	0	0.8	V

3.3 UART Interface

Module provides a 7-wire UART (universal asynchronous serial transmission) interface as DCE (Data Communication Equipment). AT commands and data transmission can be performed through UART interface.

3.3.1 UART Design Guide

The following figures show the reference design.

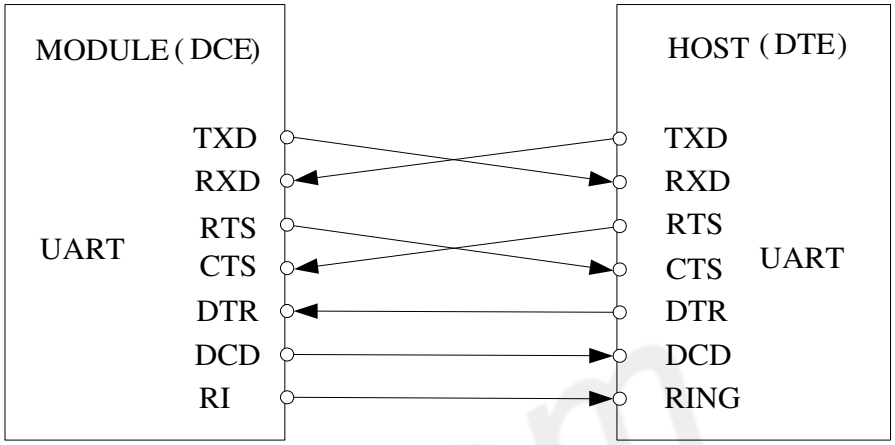

Figure 12: UART Full modem

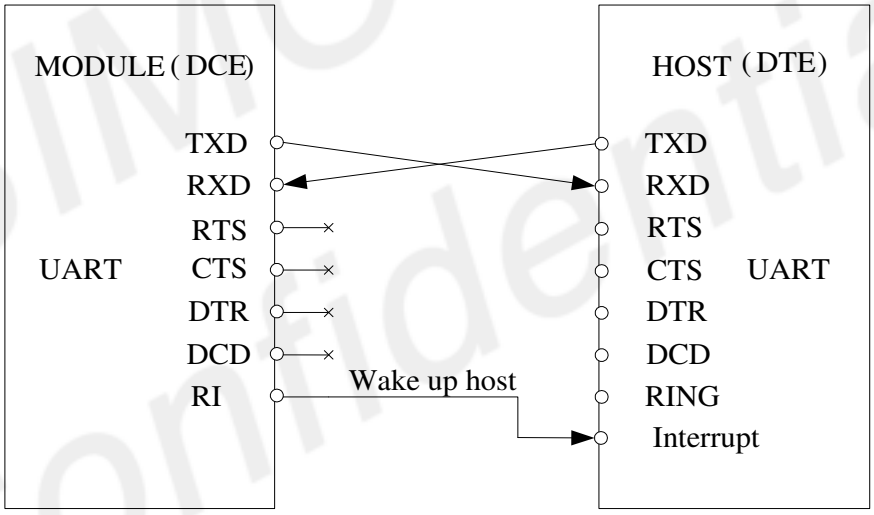

Figure 13: UART Null modem

The Module UART is 1.8V voltage interface. If user's UART application circuit is a 3.3V voltage interface, the level shifter circuits should be used for voltage matching. The TXB0108RGYR provided by Texas Instruments is recommended. The following figure shows the voltage matching reference design.

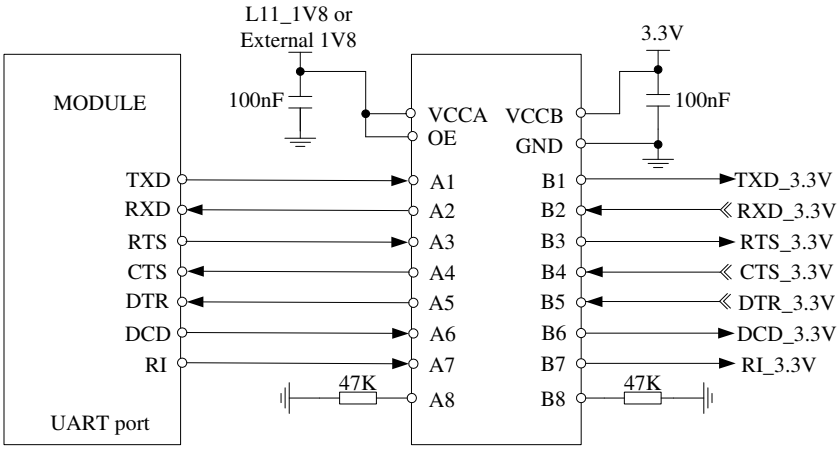

Figure 14: Reference circuit of level shift

To comply with RS-232-C protocol, the RS-232-C level shifter chip should be used to connect Module to the RS-232-C interface, for example SP3238ECA, etc.

NOTE

Module supports the following baud rates: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 3200000, 3686400, 4000000bps. The default band rate is 115200bps.

3.3.2 RI and DTR Behavior

The RI pin can be used to interrupt output signal to inform the host controller such as application CPU.

Normally RI will stay at high level until certain conditions such as receiving SMS, or a URC report come in. It will then change to low level. It will stay low until the host controller clears the interrupted event with "AT+CRIRS" AT command.

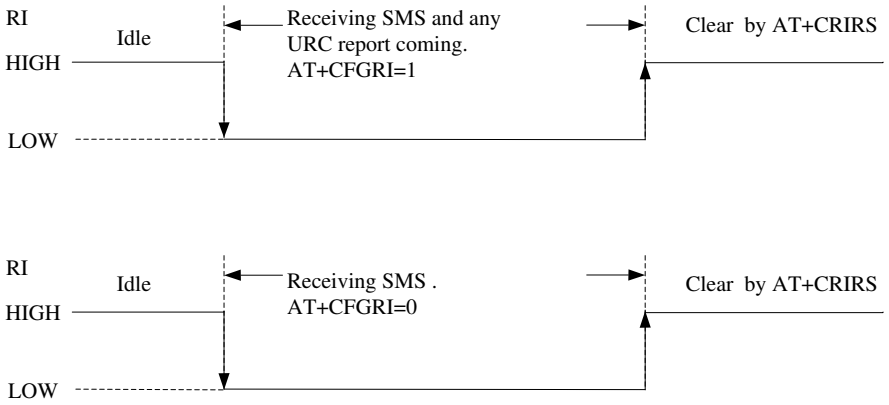

Figure 15: RI behaviour（SMS and URC report）

Normally RI will be kept high until a voice call, then it will output periodic rectangular wave with 5900ms low level and 100ms high level. It will output this kind of periodic rectangular wave until the call is answered or hung up.

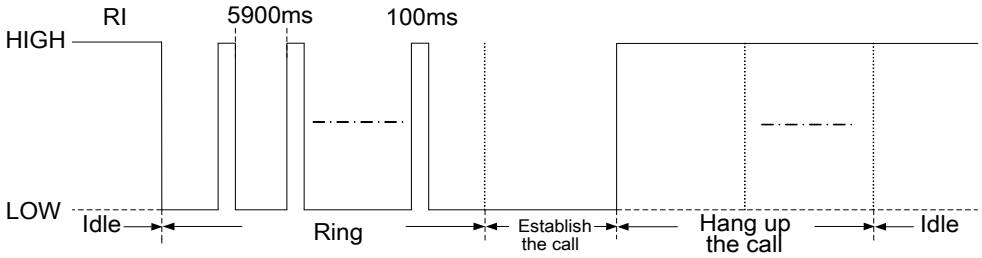

Figure 16: RI behaviour（voice call）

NOTE

For more details of AT commands about UART, please refer to document [1] and [22].

DTR pin can be used to wake Module from sleep. When Module enters sleep mode, pulling down DTR can wake Module.

3.4 USB Interface

The Module contains a USB interface compliant with the USB2.0 specification as a peripheral, but the USB charging function is not supported.

Module can be used as a USB device. Module supports the USB suspend and resume mechanism which can reduce power consumption. If there is no data transmission on the USB bus, Module will enter suspend mode automatically and will be resumed by some events such as voice call, receiving SMS, etc.
The USB interface is a frequency used debug port; it is suggested to reserved test point.

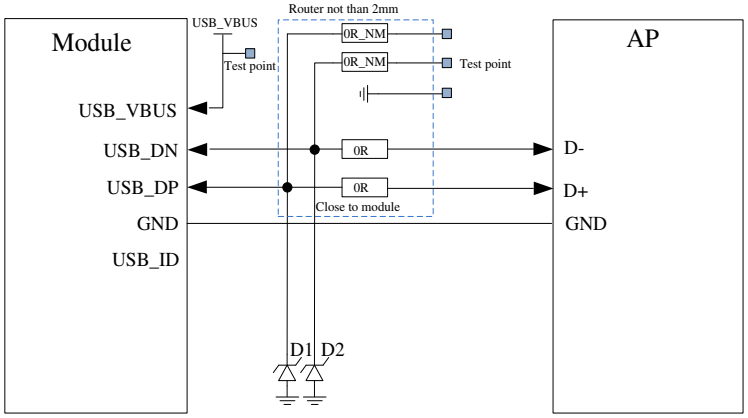

Figure 17: USB reference circuit

Because of the high bit rate on USB bus, more attention should be paid to the influence of the junction capacitance of the ESD component on USB data lines. Typically, the capacitance should be less than 1pF.

It is recommended to use an ESD protection component such as ESD9L5.0ST5G provided by On Semiconductor (www.onsemi.com).

NOTE

1. The USB_DM and USB_DP nets must be traced by 90Ohm+/-10% differential impedance.
2. Must reserve USB interfaces or test points to for software debug.
3. Must reserve pin51(DBG_TXD) and PIN23(L11_1V8) interface or test point to for software debug.

3.5 SIM Interface

Module supports both 1.8V and 3.0V SIM Cards.

Table 11: SIM Electronic characteristic in 1.8V mode (SIM_VDD =1.8V)

Symbol	Parameter	Min	Type	Max	Unit
SIM_VDD	LDO power output voltage	1.75	1.8	1.95	V
V_{IH}	High-level input voltage	0.65*SIM_VDD	-	SIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.35*SIM_VDD	V
V_{OH}	High-level output voltage	SIM_VDD -0.45	-	SIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

Table 12: SIM Electronic characteristic 3.0V mode (SIM_VDD =2.95V)

Symbol	Parameter	Min	Type	Max	Unit
SIM_VDD	LDO power output voltage	2.75	2.95	3.05	V
V_{IH}	High-level input voltage	0.65*SIM_VDD	-	SIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.25*SIM_VDD	V
V_{OH}	High-level output voltage	SIM_VDD -0.45	-	SIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

3.5.1 SIM Application Guide

It is recommended to use an ESD protection component such as ESDA6V1W5 produced by ST (www.st.com) or SMF15C produced by ON SEMI (www.onsemi.com). Note that the SIM peripheral circuit should be close to the SIM card socket. The following figure shows the 8-pin SIM card holder reference circuit.

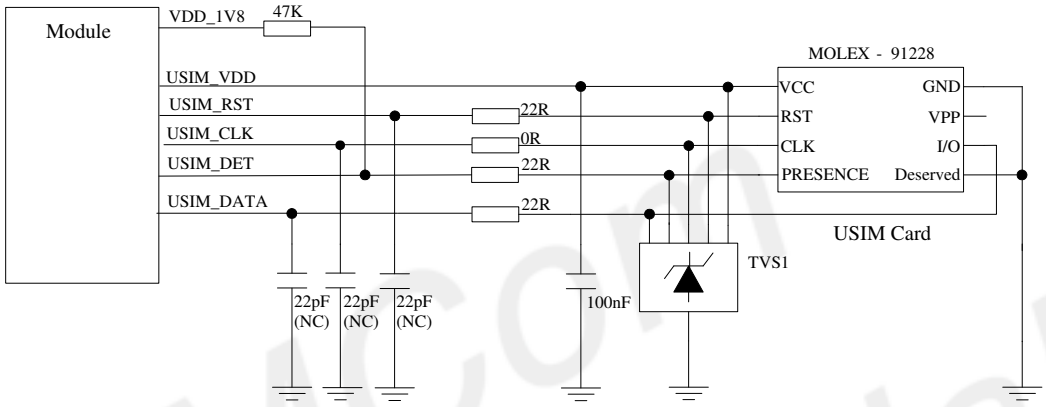

Figure 18: Reference circuit of the 8-pin SIM card holder

The SIM_DET pin is used for detection of the SIM card hot plug in. User can select the 8-pin SIM card holder to implement SIM card detection function.

If the SIM card detection function is not used, user can keep the SIM_DET pin open. The reference circuit of 6-pin SIM card holder is illustrated in the following figure.

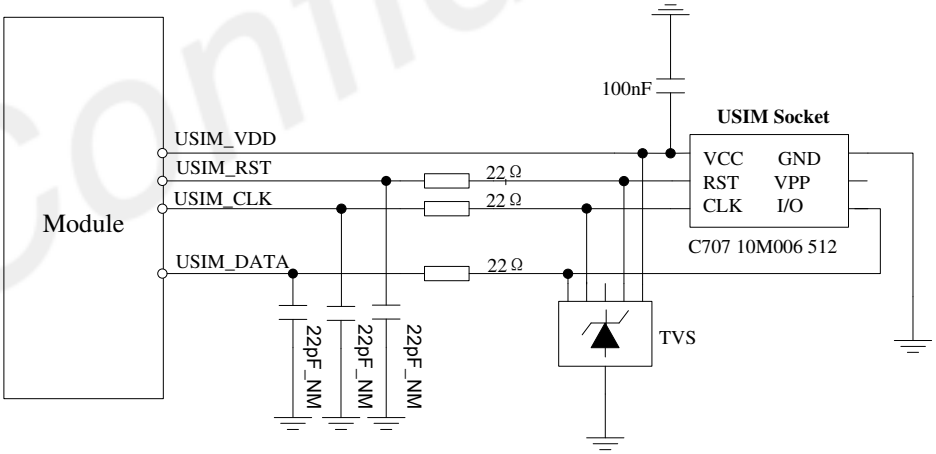

Figure 19: SIM interface reference circuit

NOTE

SIM_DATA has been pulled up with a 10KΩ resistor to SIM_VDD in module. A 100nF capacitor on SIM_VDD is used to reduce interference. For more details of AT commands about SIM, please refer to document [1].

3.5.2 SIM Card Design Guide

SIM card signal could be interferenced by some high frequency signal, it is strongly recommended to follow these guidelines while designing:

- SIM card holder should be far away from main antenna
- SIM traces should keep away from RF lines, VBAT and high-speed signal lines
- The traces should be as short as possible
- Keep SIM card holder's GND connect to main ground directly
- Shielding the SIM card signal by ground well
- Recommended to place a 100nF capacitor on SIM_VDD line and keep close to the SIM card holder
- Add some TVS which parasitic capacitance should not exceed 50pF
- Add 22Ω resistor to (SIM_RST/SIM_CLK/SIM_DATA) signal could enhance ESD protection
- Mount 22pF capacitor to (SIM_RST/SIM_CLK/SIM_DATA) signal if having RF signal interference

3.5.3 Recommended SIM Card Holder

It is recommended to use the 6-pin SIM socket such as C707 10M006 512 produced by Amphenol. User can visit http://www.amphenol.com for more information about the holder.

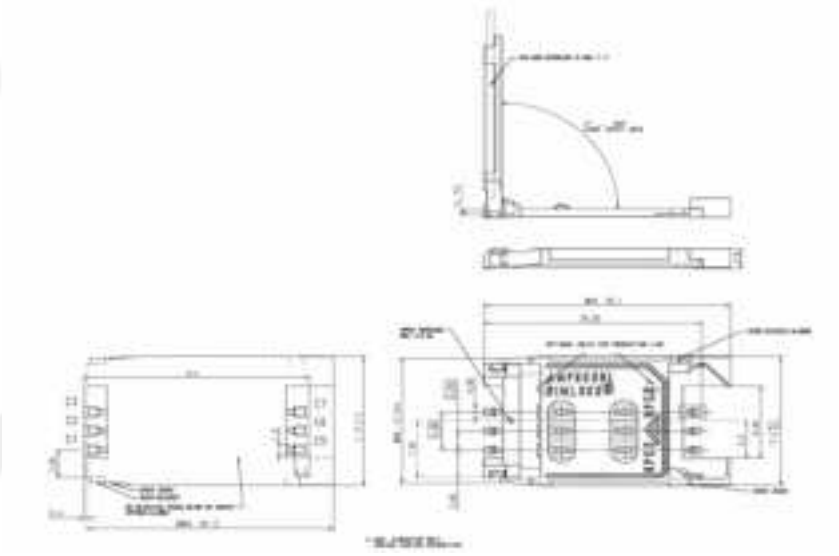

Figure 20: Amphenol SIM card socket

Table 13: Amphenol SIM Socket Pin Description

Pin	Signal	Description
C1	SIM_VDD	SIM Card Power supply.
C2	SIM_RST	SIM Card Reset.
C3	SIM_CLK	SIM Card Clock.
C5	GND	Connect to GND.

C6	VPP	
C7	SIM_DATA	SIM Card data I/O.

3.6 PCM Interface

Module provides a PCM interface for external codec, which can be used inmaster mode with short sync and 16 bits linear format.

Table 14: PCM Format

Characteristics	Specification
Line Interface Format	Linear(Fixed)
Data length	16bits(Fixed)
PCM Clock/Sync Source	Master Mode(Fixed)
PCM Clock Rate	2048 KHz (Fixed)
PCM Sync Format	Short sync(Fixed)
Data Ordering	MSB

NOTE

For more details about PCM AT commands, please refer to document [1].

3.6.1 PCM Timing

Module supports 2.048 MHz PCM data and sync timing for 16 bits linear format codec.

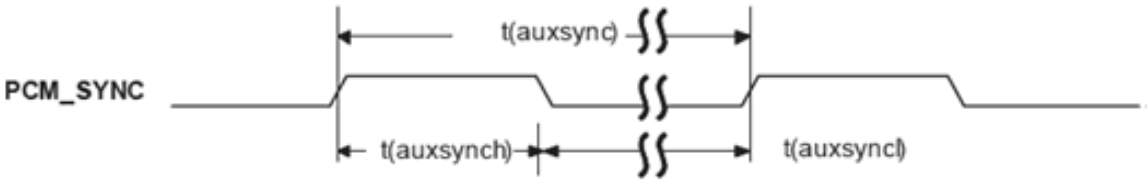

Figure 21: PCM_SYNC timing

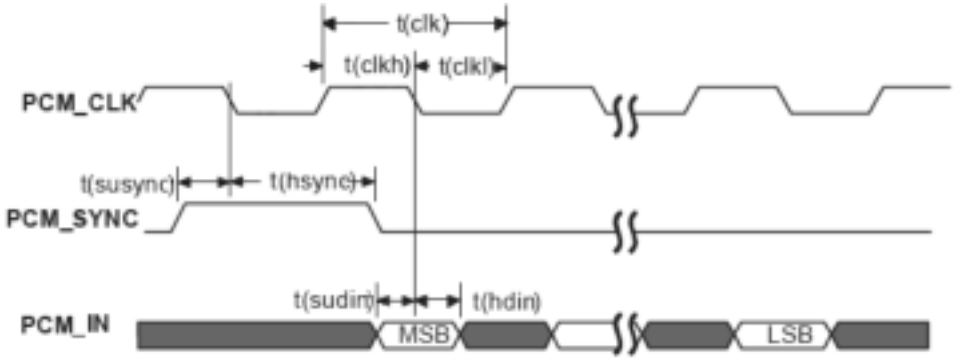

Figure 22: EXT CODEC to MODULE timing

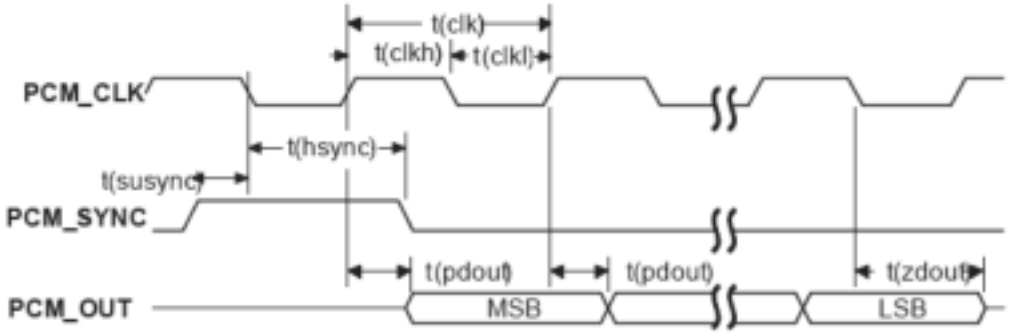

Figure 23: MODULE to EXT CODEC timing

Table 15: PCM Timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
T(sync)	PCM_SYNC cycle time	–	125	–	μs
T(synch)	PCM_SYNC high level time	–	488	–	ns
T(syncl)	PCM_SYNC low level time	–	124.5	–	μs
T(clk)	PCM_CLK cycle time	–	488	–	ns
T(clkh)	PCM_CLK high level time	–	244	–	ns
T(clkl)	PCM_CLK low level time	–	244	–	ns
T(susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	–	122	–	ns
T(hsync)	PCM_SYNC hold time after falling edge of PCM_CLK	–	366	–	ns
T(sudin)	PCM_IN setup time before falling edge of PCM_CLK	60	–	–	ns
T(hdin)	PCM_IN hold time after falling edge of PCM_CLK	60	–	–	ns
T(pdout)	Delay from PCM_CLK rising to PCM_OUT valid	–	–	60	ns

T(zdout)	Delay from PCM_CLK falling to PCM_OUT HIGH-Z	–	–	60	ns

3.6.2 PCM Application Guide

The following figure shows the external codec reference design.

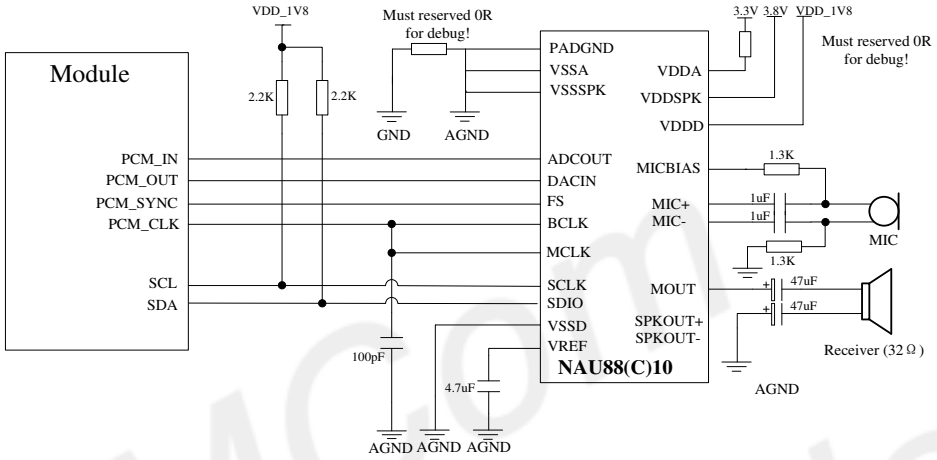

Figure 24: Audio Codec Reference Circuit

NOTE

Module can transmit PCM data by the USB port besides the PCM interface. For more details please refer to documents [1] and [23].

3.7 I2C Interface

Module provides a I2C interface compatible with I2C specification, version 2.1, with clock rate up to 400 kbps. Its operation voltage is 1.8V.

3.7.1 I2C Design Guide

The following figure shows the I2C bus reference design.

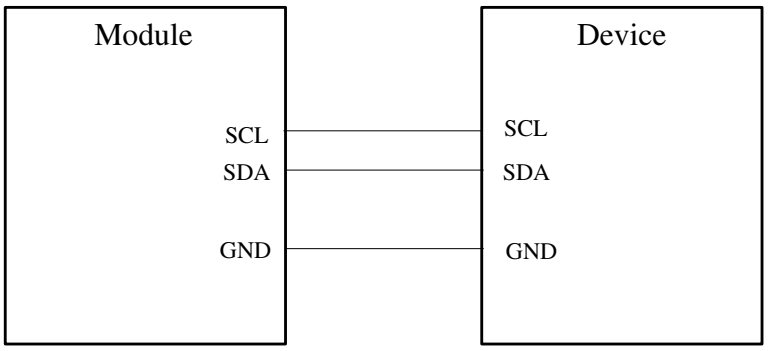

Figure 25: I2C reference circuit

NOTE

SDA and SCLhave pull-up resistors in module. So, 2 external pull up resistors are not needed in application circuit.
"AT+CRIIC and AT+CWIIC" AT commands could be used to read/write register values of the I2C peripheral devices.For more details about AT commands please refer to document [1].

3.8 Network Status

The NETLIGHT pin is used to control Network Status LED, its reference circuit is shown in the following figure.

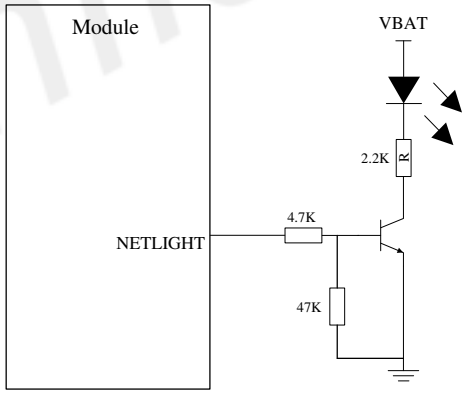

Figure 26: NETLIGHT reference circuit

NOTE

The value of the resistor named "R" depends on the LED characteristic.

Table 16: NETLIGHT pin status

NETLIGHT pin status	Module status
Always On	Searching Network; Call Connect(include VOLTE,SRLTE)
200ms ON, 200ms OFF	Data Transmit; 4G registered;
800ms ON, 800ms OFF	2G/3G registered network
OFF	Power off ;Sleep

NOTE

NETLIGHT output low level as “OFF”, and high level as “ON”.

3.9 Operating Status Indication

The pin50 is for operating status indication of the module. The pin output is high when module is powered on, and output is low when module is powered off.

Table 17: Pin definition of the STATUS

Pin name	Pin number	Description
STATUS	50	Operating status indication

NOTE

For timing about STATUS, please reference to the chapter “3.2 power on/down scenarios”

3.10 Flight Mode Control

The FLIGHTMODE pin can be used to control SIM7500x to enter or exit the Flight mode. In Flight mode, the RF circuit is closed to prevent interference with other equipment’s and minimize current consumption. Bidirectional ESD protection component is suggested to add on FLIGHTMODE pin, its reference circuit is shown in the following figure.

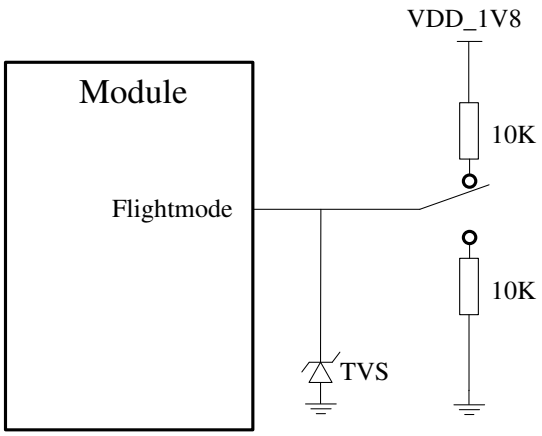

Figure 27: Flight Mode Switch Reference Circuit

Table 18: FLIGHTMODE Pin Status

FLIGHTMODE Pin Status	Module operation
Input Low Level	Flight Mode: RF is closed
Input High Level	AT+CFUN=0: RF is closed AT+CFUN=1:RF is working

NOTE

FlightMode Can't be used when Module is in sleep mode.

3.11 Pin Multiplex Function

Some pins of Module could be used for alternate function besides default function.

Table 19: Pin multiplex function list

Pin Number	Pin Name	Default Function	Alternate Function
4	SCL	SCL	GPIO11
5	SDA	SDA	GPIO10
12	SIM_DET	GPIO34	SIM_DET
18	PCM_CLK	PCM_CLK	GPIO23,SPI_CLK I2C_SCL
19	PCM_SYNC	PCM_SYNC	GPIO20,SPI_MOSI
20	PCM_IN	PCM_IN,	GPIO21,SPI_MISO
21	PCM_OUT	PCM_OUT	GPIO22,SPI_CS_N I2C_SDA

NOTE

For more details of AT commands about GPIO multiplex function, please refer to document [1].

3.12 Other interface

3.12.1 Sink Current Source

The ISINK pin is VBAT tolerant and intended to drive some passive devices such as LCD backlight, white LED, etc. Its output current can be up to 40 mA and be set by the AT command “AT+ CLEDITST”.

Table 20: Sink current electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
V_{ISINK}	Voltage tolerant	0.5	-	VBAT	V
I_{ISINK}	Current tolerant	0	-	40	mA

ISINK is a ground-referenced current sink. The following figure shows its reference circuit.

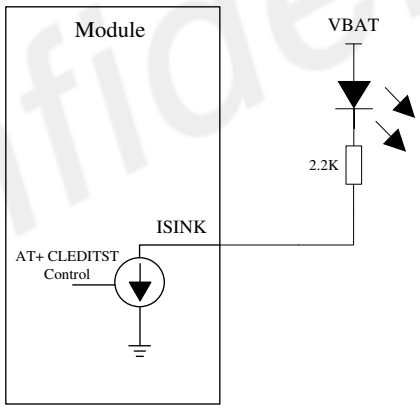

Figure 28: ISINK reference circuit

NOTE

The sinking current can be adjusted to meet the design requirement through the AT command “AT+ CLEDITST =<0>, <value>”.The “value” ranges from 0 to 8, on behalf of the current from 0mA to 40mA by 5mA step.

3.12.2 ADC

Module has 1 dedicated ADC pins named ADC. They are available for digitizing analog signals such as battery voltage and so on. These electronic specifications are shown in the following table.

Table 21: ADC Electronic Characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	–	15	–	Bits
Input Range	0.1		1.7	V
Input serial resistance	1	–	–	MΩ

NOTE

"AT+CADC" can be used to read the voltage of the ADC pins, for more details, please refer to document [1].

4 RF Specifications

4.1 LTE RF Specifications

Table 22: Conducted transmission power

Frequency	Power	Min.
LTE-FDD B2	23dBm +/-2.7dB	<-40dBm
LTE-FDD B4	23dBm +/-2.7dB	<-40dBm
LTE-FDD B12	23dBm +/-2.7dB	<-40dBm

Table 23: Operating frequencies

Frequency	Receiving	Transmission
LTE-FDD B2	1930 ~1990 MHz	1850 ~1910 MHz
LTE-FDD B4	2110~2155 MHz	1710 ~1755 MHz
LTE-FDD B12	729 ~746 MHz	699 ~716 MHz
GPS	1574.4 ～1576.44 MHz	-
GLONASS	1598 ～1606 MHz	-

Table 24: Conducted receive sensitivity

Frequency	Receive sensitivity(Typical)	Receive sensitivity(MAX)
LTE FDD	See table 21.	3GPP

Table 25: Reference sensitivity (QPSK)

E-UTRA band	3GPP standard						Test value@ 10 MHz
	1.4 MHz	3MHz	5MHz	10MHz	15 MHz	20 MHz	
FDD B2	-102.7	-99.7	-98	-95	-93.2	-92	-101
FDD B4	-104.7	-101.7	-100	-97	-95.2	-94	-102
FDD B12	-101.7	-98.7	-97	-94	-	-	-101.5

4.2 LTE Antenna Design Guide

Users should connect antennas to Module's antenna pads through the micro-strip line or other types of RF

trace. The trace impedance must be controlled in 50Ω. SIMCom recommends that the total insertion loss between Module and antenna should meet the following requirements:

Table 26: Recommended Passive Antenna Characteristics

Passive	Recommended standard
Direction	Omnidirectional
Gain	>-3dBi（Avg）
Input impedance	50 ohm
Efficiency	>50%
VSWR	<2

Table 27: Trace Loss

Frequency	Loss
700MHz-960MHz	<0.5dB
1710MHz-2170MHz	<0.9dB
2300MHz-2650MHz	<1.2dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit.

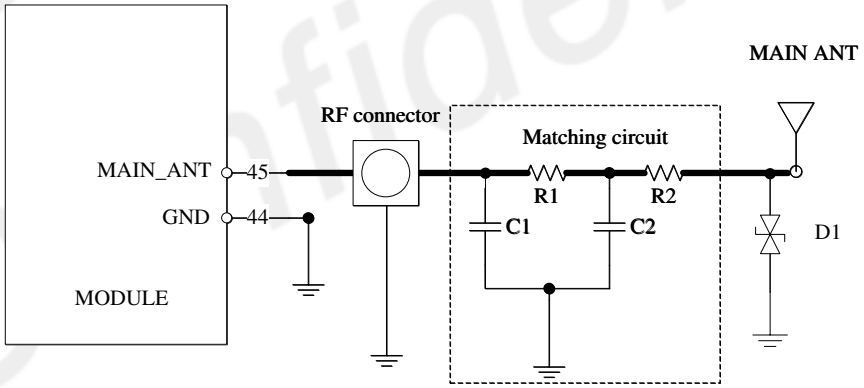

Figure 29: Antenna matching circuit (MAIN_ANT)

In above figure, the components R1,C1,C2 and R2 are used for antenna matching, the value of components can only be achieved after the antenna tuning and usually provided by antenna vendor. By default, the R1, R2 are 0Ω resistors, and the C1, C2 are reserved for tuning. The component D1 is a TVS for ESD protection, and it is optional for users according to application environment.

The RF test connector is used for the conducted RF performance test, and should be placed as close as to the module's MAIN_ANT pin. The traces impedance between Module and antenna must be controlled in 50Ω.

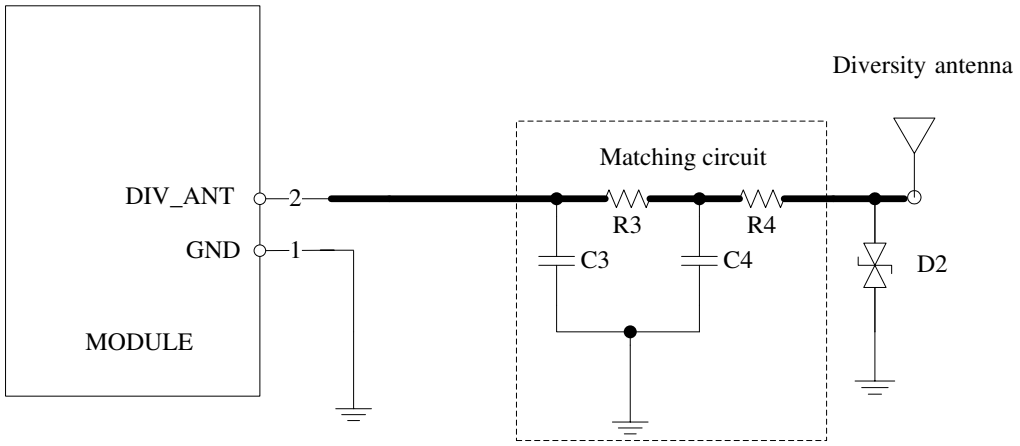

Figure 30: Antenna matching circuit (DIV_ANT)

In above figure, R3, C3, C4 and R4 are used for auxiliary antenna matching. By default, the R3, R4 are 0Ωresistors, and the C3, C4 are reserved for tuning. D2 is a TVS for ESD protection, and it is optional for users according to application environment.
Two TVS are recommended in the table below.

Table 28: Recommended TVS

Package	Part Number	Vender
0201	WE05DGCMS-BH	CYGWAYON
0402	PESD0402-03	PRISEMI
0402	PESD0402-12	PRISEMI

NOTE

SIMCom suggests the LTE auxiliary antenna to be kept on, since there are many high bands in the designing of FDD-LTE. Because of the high insert loss of the RF cable and layout lines, the receiver sensitivity of these bands above will have risk to meet the authentication without the diversity antenna.For more details about auxiliary antenna design notice,please refer to document [24]

4.3 GNSS

SIM7500A merges GNSS satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs well, even in very challenging environmental conditions where conventional GNSS receivers fail, and provides a platform to enable wireless operators to address both location-based services and emergency mandates.

4.3.1 GNSS Technical specification

- Tracking sensitivity: -159 dBm（GPS）/-158 dBm（GLONASS）/-159dBm(BD)
- Cold-start sensitivity: -148 dBm
- Accuracy (Open Sky): 2.5m (CEP50)
- TTFF (Open Sky) : Hot start <1s, Cold start<35s
- Receiver Type: 16-channel, C/A Code
- GPS L1 Frequency: 1575.42±1.023MHz
- GLONASS: 1597.5~1605.8 MHz
- BD: 1559.05~1563.14 MHz
- Update rate: Default 1 Hz
- GNSS data format: NMEA-0183
- GNSS Current consumption : 100mA ((WCDMA/LTE Sleep ,in total on VBAT pins)
- GNSS antenna: Passive/Active antenna

NOTE

If the antenna is active type, the power should be given by main board, because there is no power supply on GPS antenna pad. If the antenna is passive, it is suggested that the external LNA should be used.

4.3.2 GNSS Application Guide

Users can adopt an active antenna or a passive antenna as GNSS signal transceiver. In this document, all GNSS specification mentioned is from passive antenna. The following is the reference circuit.

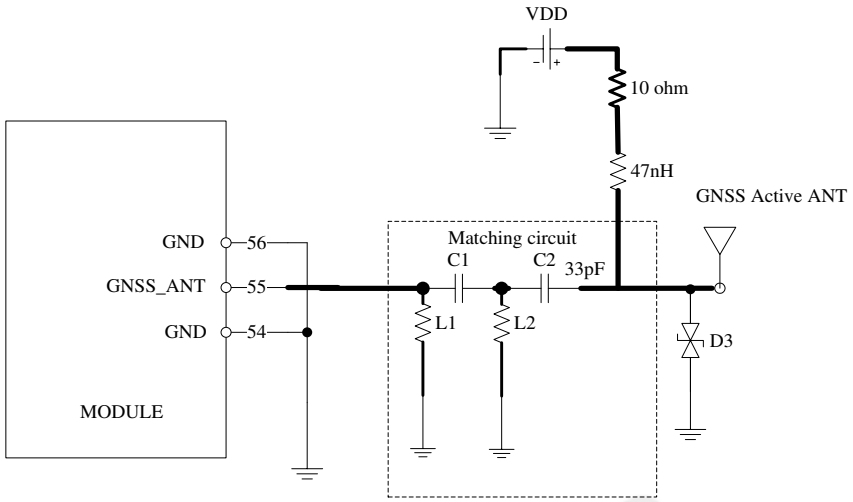

Figure 31: Active antenna circuit

NOTE

If customer need save the power when the GNSS function is disabled, then customer should design a switch circuit to cut off the active antenna power to get a lower power consumption.

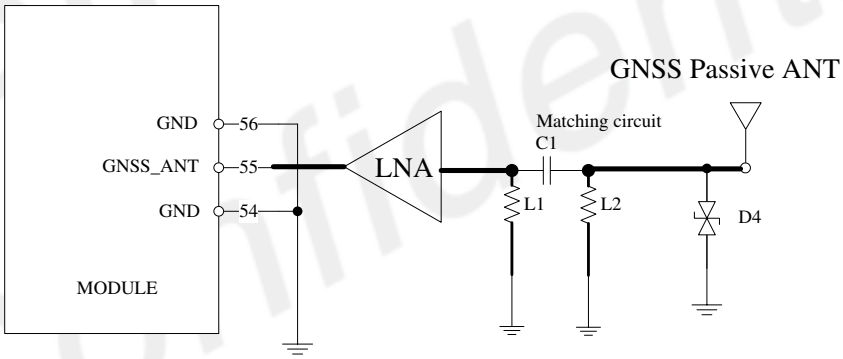

Figure 32: Passive antenna circuit (Default)

In above figures, the components C1 and L1, L2 are used for antenna matching, the values of the components can only be obtained after the antenna tuning and usually provided by antenna vendor. C2 in Figure 29 is used for DC blocking. L3 is the matching component of the external LNA, and the value of L3 is determined by the LNA characteristic and PCB layout. Both VDD of active antenna and V_LNA need external power supplies which should be considered according to active antenna and LNA characteristic. LDO/DCDC is recommended to get lower current consuming by shutting down active antennas and LNA when GNSS is not working.

LNA should apply the following requirements as table 28. LNA is also suggested to put near the passive antenna.

Table 29: LNA requirements

Parameter	Min	Max	Unit
Vdd	1.5	3.3	V
Idd		3	mA
LNA_EN	1.3		V
Gain	14	17	dB
VSWR		2	

GNSS can be used by NMEA port. User can select NMEA as output through UART or USB. NMEA sentences are automatic and no command is provided. NMEA sentences include GSV, GGA, RMC, GSA, and VTG. Before using GNSS, user should configure SIM7500A in proper operating mode by AT command. Please refer to related document for details. SIM7500A can also get position location information through AT directly.

NOTE

GNSS is closed by default, it could be started by AT+CGPS. The AT command has two parameters, the first is on/off, and the second is GNSS mode. Default mode is standalone mode.
AGPS mode needs more support from the mobile telecommunication network. Please refer to document [24] for more details.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of Module are listed in the following table:

Table 30: Absolute maximum ratings

Parameter	Min	Max	Unit
Voltage at VBAT	-0.5	4.7	V
Voltage at VBUS	-0.5	5.5	V
Voltage at digital pins (RESET,SPI,GPIO,I2C,UART,PCM)	-0.3	2.1	V
Voltage at digital pins :SIM	-0.3	3.05	V
Voltage at PWRKEY	-0.3	1.8	V

5.2 Operating Conditions

Table 31: Recommended operating ratings

Parameter	Min	Type	Max	Unit
Voltage at VBAT	3.4	3.8	4.2	V
Voltage at VBUS	3.0	5	5.25	V

Table 32: 1.8V Digital I/O characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.17	1.8	2.1	V
V_{IL}	Low-level input voltage	-0.3	0	0.63	V
V_{OH}	High-level output voltage	1.35	-	1.8	V
V_{OL}	Low-level output voltage	0	-	0.45	V
I_{OH}	High-level output current(no pull down resistor)	-	2		mA
I_{OL}	Low-level output current(no pull up resistor)	-	-2	-	mA
I_{IH}	Input high leakage current (no pull down resistor)	-	-	1	uA
I_{IL}	Input low leakage current(no	-1	-	-	uA

	pull up resistor)

NOTE

These parameters are for digital interface pins, such as SPI, GPIOs (NETLIGHT), I2C, UART, PCM.

The operating temperature of Module is listed in the following table.

Table 33: Operating temperature

Parameter	Min	Type	Max	Unit
Normal operation temperature	-10	25	55	℃

5.3 Operating Mode

5.3.1 Operating Mode Definition

The table below summarizes the various operating modes of Module series products.

Table 34: Operating Mode Definitions

Mode		Function
Normal operation	LTE Sleep	In this case, the current consumption of module will be reduced to the minimal level and the module can still receive paging message and SMS and TCP/UDP.
	LTE Idle	Software is active. Module is registered to the network, and the module is ready to communicate.
	LTE Talk	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences, antenna.
	LTE Standby	Module is ready for data transmission, but no data is currently sent or received. In this case, power consumption depends on network settings.
	LTE transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g. power control level); uplink/downlink data rates, etc.
Minimum functionality mode		AT command “AT+CFUN=0” can be used to set the module to a minimum functionality mode without removing the power

	supply. In this mode, the RF part of the module will not work and the SIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode	AT command “AT+CFUN=4” or pulling down the FLIGHTMODE pin can be used to set the module to flight mode without removing the power supply. In this mode, the RF part of the module will not work but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Power off	Module will go into power off mode by sending the AT command “AT+CPOF” or by pulling down the PWRKEY pin normally. In this mode the power management unit shuts down the power supply and software is not active. The serial port and USB are is not accessible.

5.3.2 Sleep mode

In sleep mode, the current consumption of module will be reduced to the minimal level, and module can still receive paging message, SMS and TCP/UDP.
Several hardware and software conditions must be satisfied together in order to let Module enter into sleep mode:
1. UART condition
2. USB condition
3. Software condition

NOTE

Before designing, pay attention to how to realize sleeping/waking function and refer to Document [25] for more details.

5.3.3 Minimum functionality mode and Flight Mode

Minimum functionality mode ceases a majority function of module, thus minimizing the power consumption. This mode is set by the AT command which provides a choice of the functionality levels.
AT+CFUN=0: Minimum functionality
AT+CFUN=1: Full functionality (Default)
AT+CFUN=4: Flight mode

If Module has been set to minimum functionality mode, the RF function and SIM card function will be closed. In this case, the serial port and USB are still accessible, but RF function and SIM card will be unavailable.

If Module has been set to flight mode, the RF function will be closed. In this case, the serial port and USB are still accessible, but RF function will be unavailable.

When Module is in minimum functionality or flight mode, it can return to full functionality by the AT command "AT+CFUN=1".

5.4 Current Consumption

The current consumption is listed in the table below.

Table 35: Current consumption on VBAT Pins (VBAT=3.8V)

GNSS	
GNSS supply current (AT+CFUN=0,with USB connection)	@-140dBm，Tracking Typical:35mA
LTE Sleep/Idle mode	
LTE supply current (without USB connection)	Sleep mode @DRX=9 Typical: 2.3mA Idle mode @DRX=9 Typical: 17.5mA
LTE Data	
LTE-FDD B2	@5 MHz 22.2dBm Typical: 589mA @10 MHz 22.7dBm Typical: 577mA @20 MHz 22.4dBm Typical: 626mA
LTE-FDD B4	@5 MHz 23.1dBm Typical: 519mA @10 MHz 23.0dBm Typical: 556mA @20 MHz 22.8dBm Typical: 600mA
LTE-FDD B12	@5 MHz 22.7dBm Typical: 516mA @10 MHz 22.9dBm Typical: 512mA

5.5 ESD Notes

Module is sensitive to ESD in the process of storage, transporting and assembling. Especially, Module is mounted on the users' mother board, The ESD components should be placed beside the connectors which human body might touch, such as SIM card holder, audio jacks, switches and keys, etc. The following table shows the Module ESD measurement performance without any external ESD component.

Table 36: The ESD performance measurement table (Temperature: 25℃, Humidity: 45%)

Part	Contact discharge	Air discharge
GND	+/-4K	+/-8K
VBAT	+/-4K	+/-8K
Antenna port	+/-4K	+/-8K
USB	+/-1K	+/-2K
UART	+/-1K	+/-2K
PCM	+/-1K	+/-2K

Other PADs	+/-1K	+/-2K

6 SMT Production Guide

6.1 Top and Bottom View of Module

Figure 33: Top and bottom view of Module

NOTE

The above is the design effect diagram of the module for reference. The actual appearance is subject to the actual product.

6.2 Label Information

Figure 34: Label Information

Table 37: The Description of Label Information

No.	Description
A	LOGO
B	No.1 Pin
C	Project Name
D	Product Code
E	Serial Number
F	International Mobile Equipment Identity
G	QR code
H	Federal Communications Commission

6.3 Typical SMT Reflow Profile

SIMCom provides a typical soldering profile. Therefore the soldering profile shown below is only a generic recommendation and should be adjusted to the specific application and manufacturing constraints.

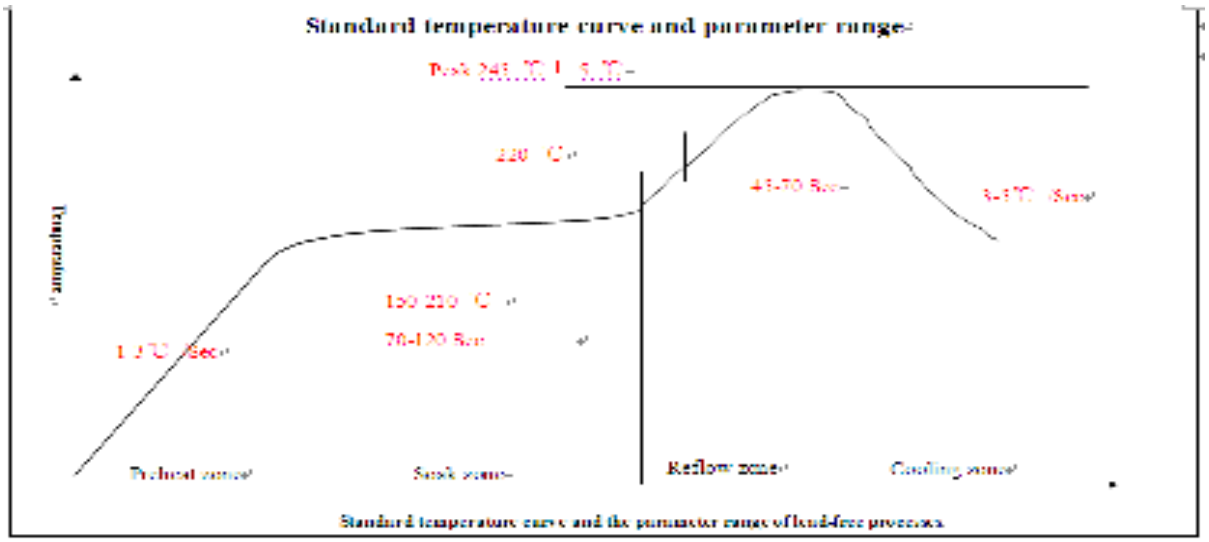

Figure 35: The ramp-soak-spike Reflow Profile of Module

NOTE

For more details about secondary SMT, please refer to the document [21].

6.4 Moisture Sensitivity Level (MSL)

Module is qualified to Moisture Sensitivity Level (MSL) 3 in accordance with JEDEC J-STD-033. If the prescribed time limit is exceeded, users should bake modules for 192 hours in drying equipment (<5% RH) at 40+5/-0°C, or 72 hours at 85+5/-5°C. Note that plastic tray is not heat-resistant, and only can be baked at 45° C.

Table 38: Moisture Sensitivity Level and Floor Life

Moisture Sensitivity Level (MSL)	Floor Life (out of bag) at factory ambient≤30°C/60% RH or as stated
1	Unlimited at ≦30℃/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours

5a	24 hours
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.

NOTE

IPC / JEDEC J-STD-033 standard must be followed for production and storage.

6.5 Stencil Foil Design Recommendation

The recommended thickness of stencil foil is 0.13mm.

7 Packaging

Module support tray packaging.

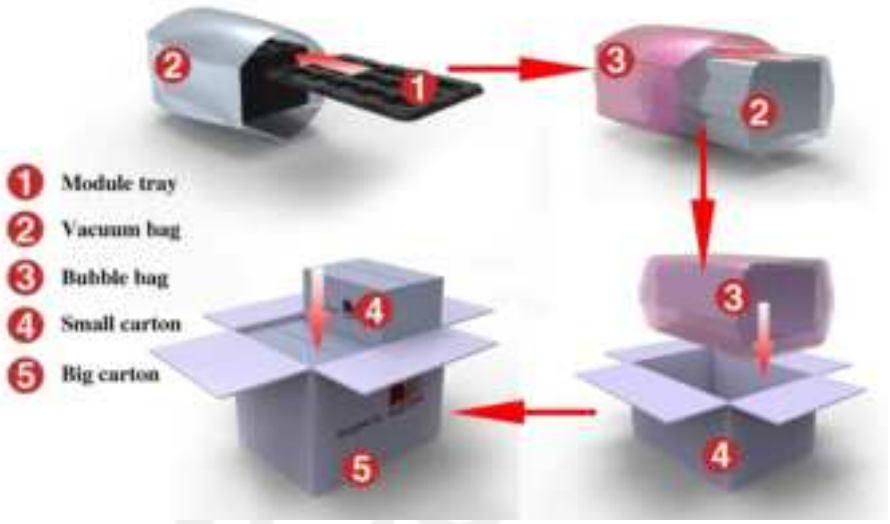

Figure 36: Packaging introduce

Module tray drawing:

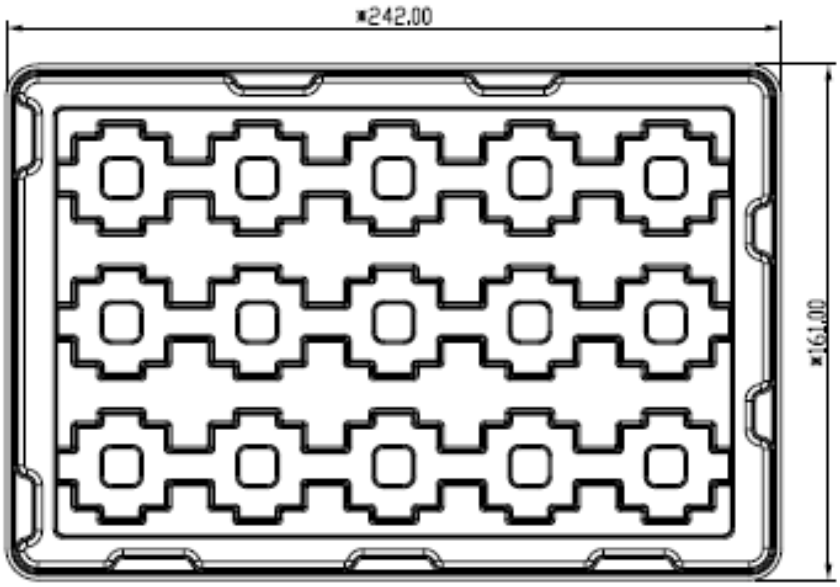

Figure 37: Tray drawing

Table 39: Tray size

Length（±3mm）	Width（±3mm）	Number
242.0	161.0	15

Small carton drawing:

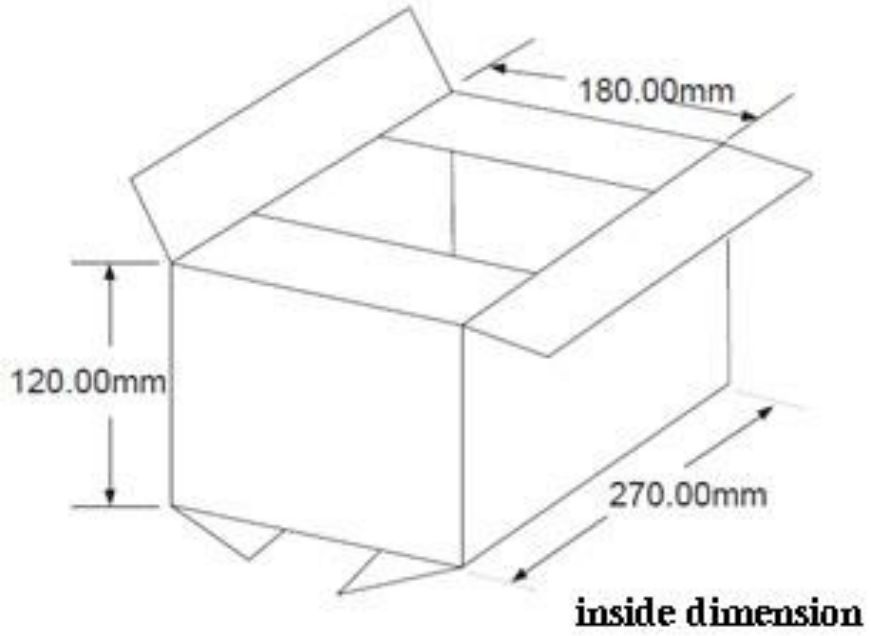

Figure 38: Small carton drawing introduce

Table 40: Small Carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
270	180	120	15*20=300

Big carton drawing:

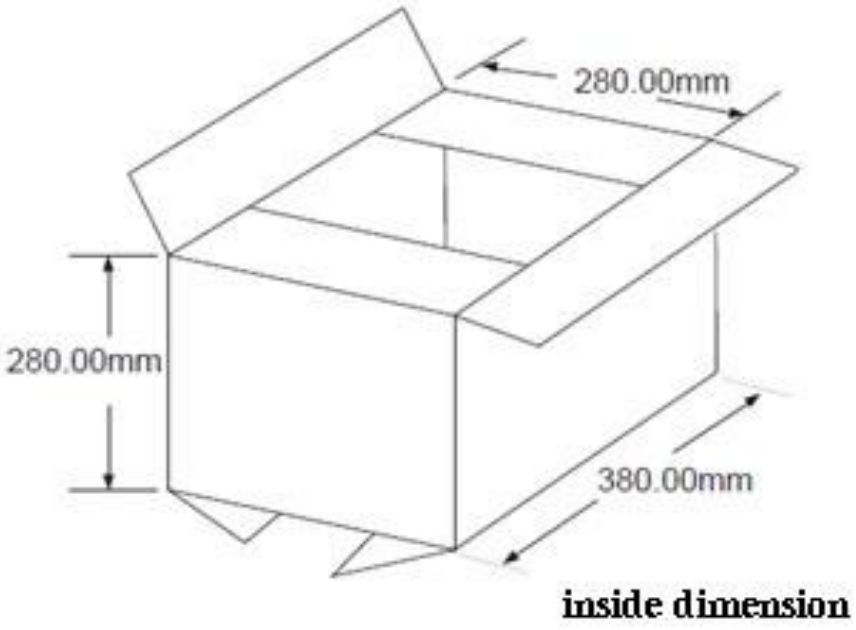

Figure 39: Big carton drawing introduce

Table 41: Big Carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
380	280	280	300*4=1200

8 Notes

This module meets the requirements of FCC part 22/24/27.

The module is a single module.

This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body. "This module is designed to comply with the FCC statement, FCC ID is: 2AJYU-8PYA00A and".

The host system using this module should have label in a visible area indicated the following texts: "Contains FCC ID: 2AJYU-8PYA00A" or “Contains FCC ID: 2AJYU-8PYA00A”.

The module comply with FCC Part 15 Subpart B.

Host manufacturer must perfom test of radiated & conducted emission and spurious emission, etc according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.