iotTech

ITM-D566 User Manual

IEEE 2.4GHz 1T1R Wi-Fi with BLE v5.0 IoT Module Datasheet

V1.0

Revision History

Date	Revision Content	Revised By	Version
2021/05/06	- Initial released (Preliminary)	Issac Chen	0.1
2021/09/03	- Initial released (Preliminary)	Issac Chen	0.2
2022/08/31	- Add packing information	Issac Chen	0.3
2022/09/26	- Add PCB antenna info	Issac Chen	0.4
2022/10/01	- Add BLE and Crystal info.	Issac Chen	0.5
2022/10/06	- Correct GPIOs info.	Issac Chen	0.6
2023/10/27	- Official release	Issac Chen	1.0

Contents

1. General Description

ITM-D566 module features a fully integrated 2.4GHz radio transceiver and baseband processor for Wi-Fi 802.11b and Bluetooth® Smart applications. It can be used as a standalone application-specific communication processor or as a wireless data link in hosted MCU systems where ultra-low power is critical. It supports flexible memory architecture for storing profiles, stacks and custom application codes, and can be updated using Over-The-Air (OTA) technology. Qualified Bluetooth Smart protocol stack and Wi-Fi TCP/IP stack are stored in a dedicated ROM.

ITM-D566 module uses OPULINKS OPL1600 SoC. It is equipped with dual processors, ARM® Cortex®-M0 and M3, for handling different processes. All software runs on the ARM® Cortex®-M0 processor while more intensive application-specific activities run on the ARM® Cortex®-M3 processor. ITM-D566 can be connected to any external MCU through SPI, I2C or UART interfaces and sensors or other devices through GPIOs. The transceiver interfaces directly to the antenna and is fully compliant with the Wi-Fi 802.11b and Bluetooth 5.0 BLE standards. With integrated antenna switch, RF balun, power amplifier (PA) and low noise amplifier (LNA), the OPL1600 allows both Wi-Fi and Bluetooth Smart to minimize PCB design area and external component requirement.

2. Features.

- Processors
  - ARM® Cortex®-M3 Application Processor
  - ARM® Cortex®-M0 Link Controller
- Wi-Fi
  - 802.11b up to 11Mbps
  - Supports STA mode
  - WPA/WPA2 security supported
  - Automatic beacon scanning and discovery
  - Built-in TCP/IP stack
- Bluetooth Smart
  - Compliant with Bluetooth 5.0 BLE specifications
  - Slave mode support
  - All GATT-based profiles supported
  - Built-in BLE stack
- Memories
  - 4Kbit One-Time-Programmable (OTP) memory
  - 384 KB System SRAM
  - 768 KB ROM
  - 8Mbit embedded flash
- HW Crypto Engine
  - AES-128/256 bits Encryption
  - P-192/256 ECDH (Elliptic Curve Diffie-Hellman) Key Generation
  - SHA2
  - TRNG
- Power Management
  - Supports coin cell and alkaline battery
- Clock
  - On-board 22MHz crystal for main clock
  - On-board 32.768kHz crystal for RTC clock
- General purpose, capture and sleep timers

- FW OTA (Over-The-Air) update support
- Digital Interfaces
  - General purpose I/Os: 18
  - One debug UART, and two UARTs with hardware flow control up to 3Mbps
  - One SPI+™ interfaces
  - One I2C bus supporting both master and slave mode
- Analog Interfaces
  - 10-bit Auxiliary ADC with 9 input channels: GPIO2/3/4/5/7/8/9/10/11
  - 6 GPIO pins with 16mA driving capability: GPIO18-23
  - 6 PWMs: GPIO18-23
- Antenna
  - On-board PCB antenna
  - IPEX connector for connecting external antenna
- Current Consumption
  - Deep sleep current ~ 3 uA
  - Timer sleep current ~ 4 uA

3.General Specification

3.1 Voltages

3.1.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.3	3.6	V

Operating temperature	-20°C to 70°C
Storage temperature	-40°C to 85°C

3.1.2 Recommended Operating Ratings

Test conditions: At room temperature				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	2.7	3.3	3.6	V

Test conditions: At operating temperature -20°C ~70°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBAT	2.7	3.3	3.6	V

3.2 Crystal Specification

Parameters	Conditions	Min.	Typ.	Max.	Unit
Nominal Frequency			22		MHz
Load Capacitance			10		pF
Operating Temperature		-20		+75	℃
Frequency Tolerance	25℃±3℃	-10		+10	ppm
Frequency Stability	Operating Temp. Range	-10		+10	ppm
Drive Level				100	uW
ESR				40	ohm

3.3 Wi-Fi RF Specification (RX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2412		2462	MHz
RX Sensitivity	- 1Mbps		-91	-83	dBm
11b @ 8% PER	- 11Mbps		-84	-76	dBm
Maximum Input Level	- 11Mbps	-15			dBm

3.4 Wi-Fi RF Specification (TX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2412		2462	MHz
Output Power	802.11b / 11Mbps	--	11.05	--	dBm
@EVM	802.11b / 11Mbps	--	-25	--	dB

3.5 BLE RF Specification (RX)

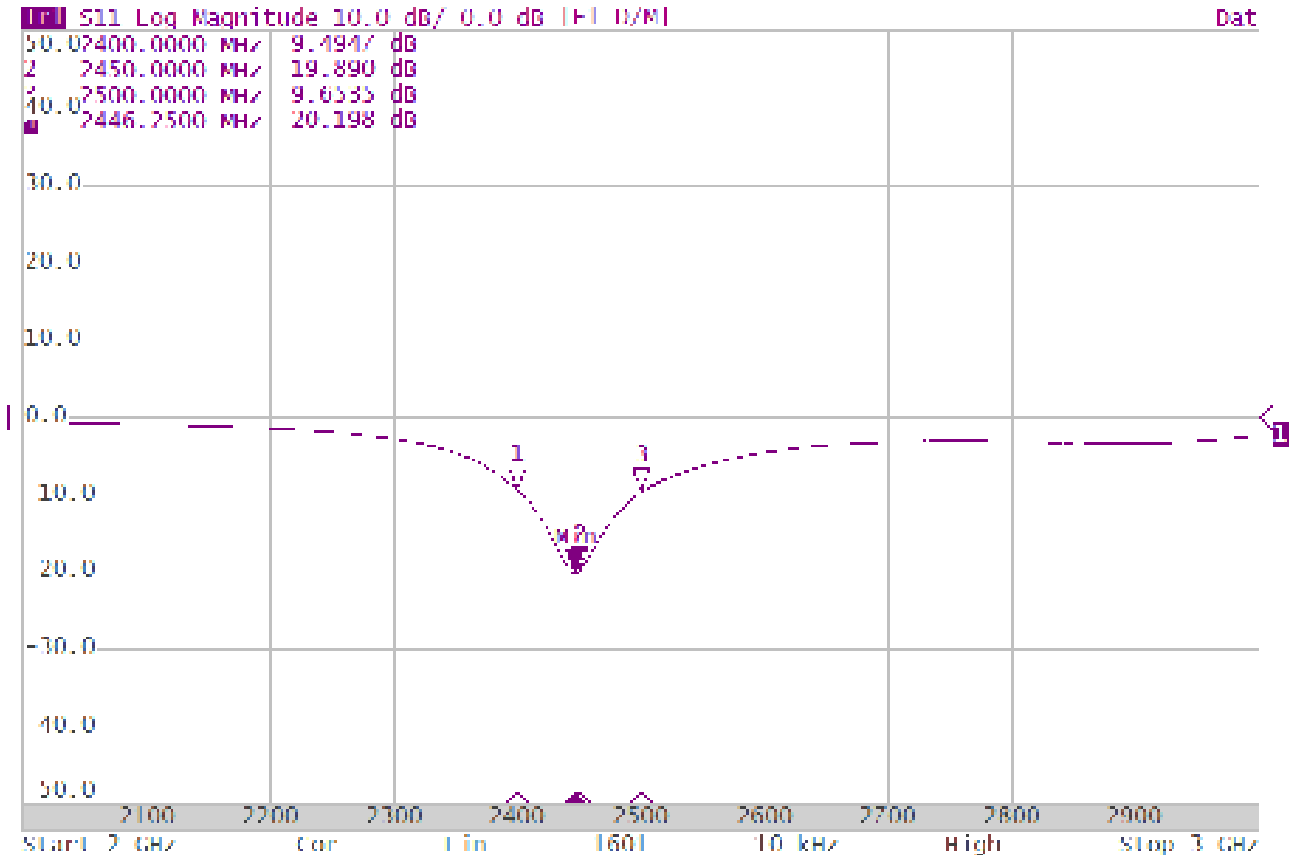
Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
RX Sensitivity	BLE 1M, 0.1% BER			-91	dBm
Maximum Input Power	BLE 1M, 0.1% BER			-20	dBm

3.6 BLE RF Specification (TX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
Output Power		--	0.49	--	dBm
Gain Control Range		--	20	--	dB

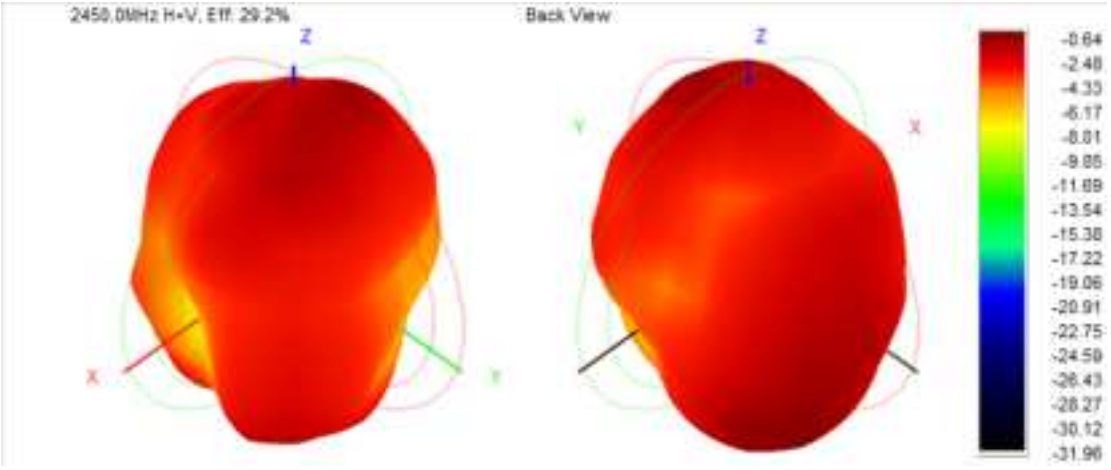
4.Antenna

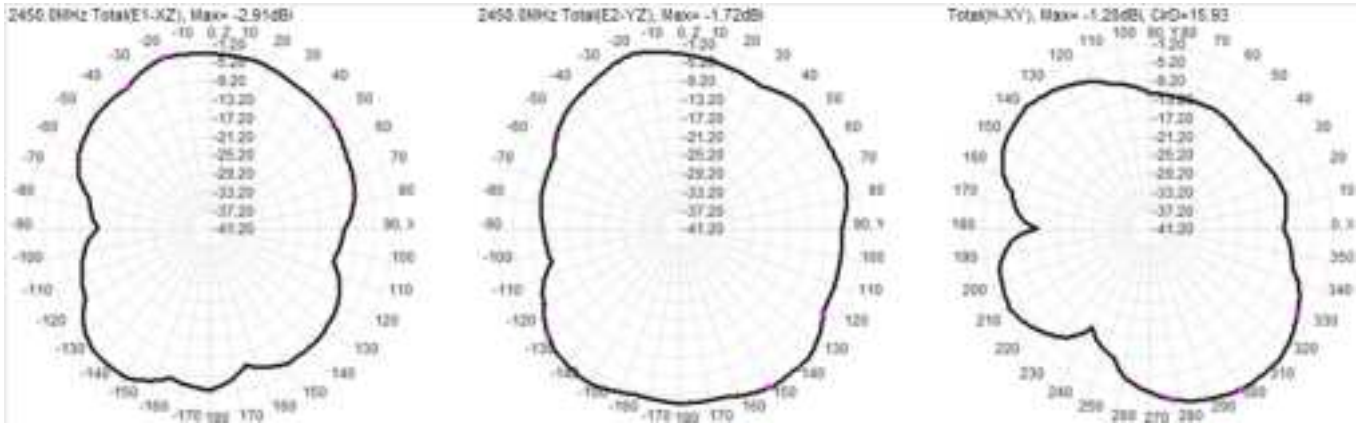
4.1 S11 Parameter



4.2 Gain Pattern

Passive Test (Free Space)

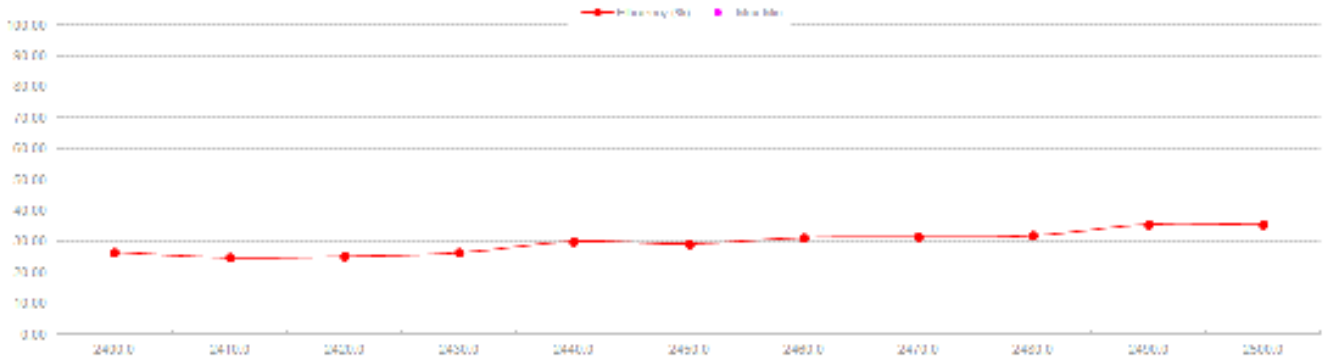




4.3 Efficiency

2400MHz~2500MHz (Average Efficiency = 30%)

Frequency ID	11	12	13	14	15	16	17	18	19	20	21
Frequency (MHz)	2100.0	2110.0	2120.0	2130.0	2140.0	2150.0	2160.0	2170.0	2180.0	2190.0	2500.0
Efficiency (dB)	-5.26	-5.08	-5.07	-5.07	-5.24	-5.15	-5.08	-5.01	-4.97	-4.98	-4.51
Gain (dBi)	-0.30	-0.30	-0.32	-0.27	-0.41	-0.24	-0.16	-0.29	-0.15	0.02	-0.26
Efficiency (%)	29.57	30.89	30.99	30.97	29.96	30.20	31.20	31.19	31.94	31.80	35.41
Directivity (dBi)	5.16	5.38	5.49	5.54	4.79	4.70	4.59	4.50	4.52	4.52	4.24

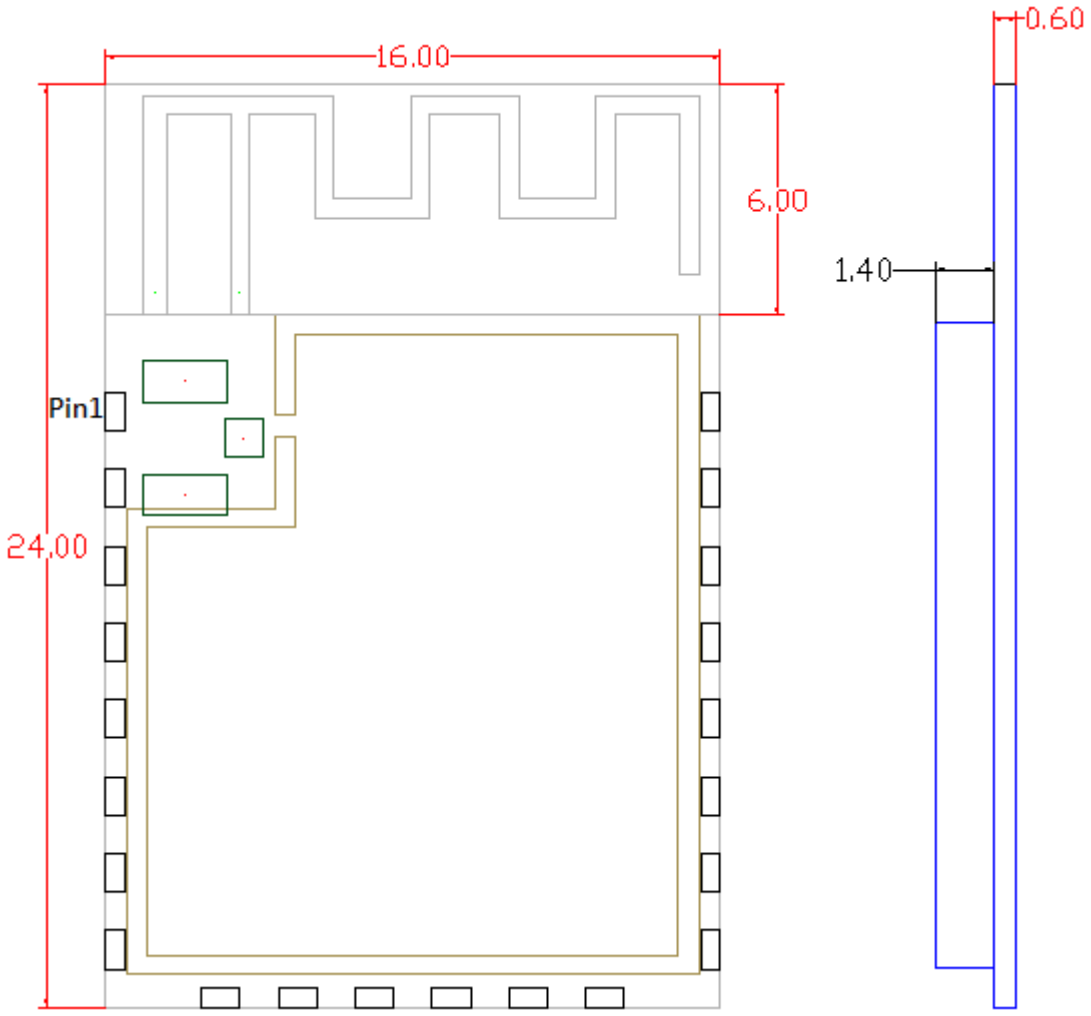


5. Pin Assignments

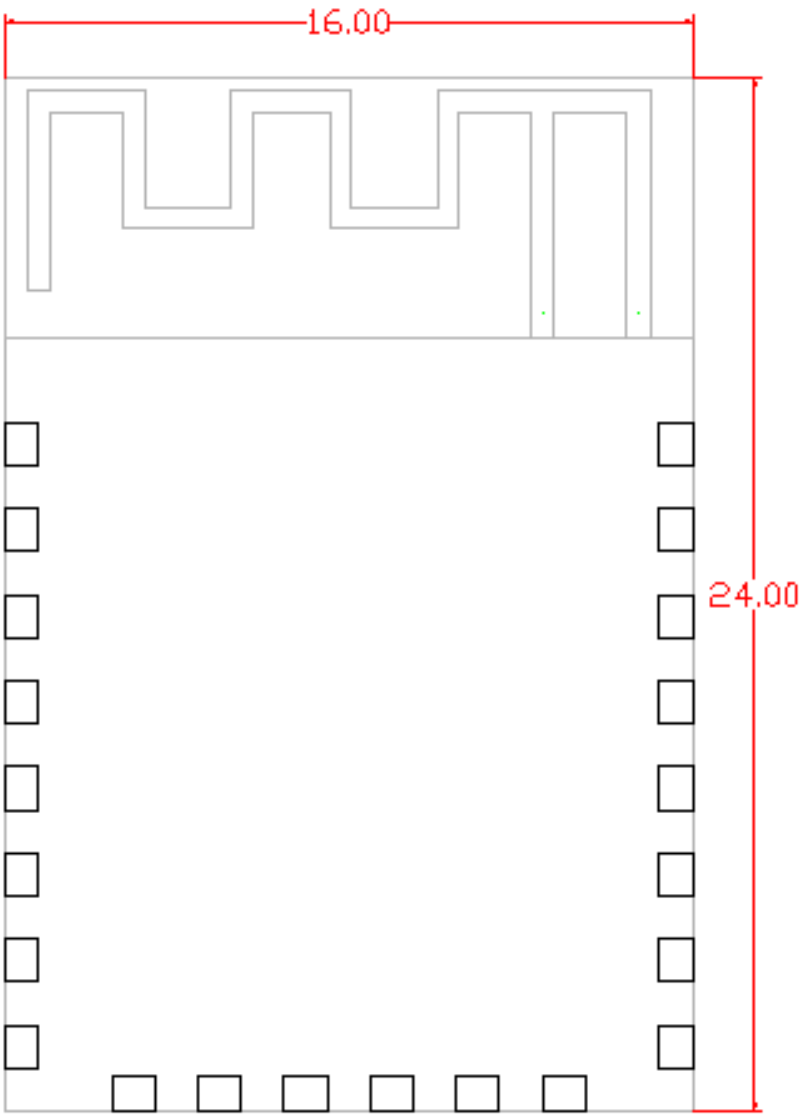
5.1 PCB Pin Outline

< TOP VIEW >

< SIDE VIEW >



< BOTTOM VIEW >



5.2 Pin Definition

Pin No.	Pin-Define	Type	Description
1	RST_N	I	Pull Low to reset whole module Should keep High when operating
2	GPIO5 / ADC5	I/O	General Purpose Input/Output Analog-to-Digital Converter Input
3	RST_N	I	Internal connected with Pin1
4	GPIO7 / ADC7	I/O	General Purpose Input/Output Analog-to-Digital Converter Input
5	GPIO4 / ADC4	I/O	General Purpose Input/Output Analog-to-Digital Converter Input
6	GPIO3 / ADC3 / UART0_RXD	I/O	General Purpose Input/Output Analog-to-Digital Converter Input UART0 Serial Data Receive
7	GPIO2 / ADC2 / UART0_TXD	I/O	General Purpose Input/Output Analog-to-Digital Converter Input UART0 Serial Data Transmit
8	VBAT	P	Main Power Supply Input 3.3V
9	GPIO23 / PWM0	I/O	General Purpose Input/Output PWM Function Output
10	GPIO10 / ADC10 / I2C_SCL	I/O	General Purpose Input/Output Analog-to-Digital Converter Input I2C Clock Signal
11	GPIO11 / ADC11 / I2C_SDA	I/O	General Purpose Input/Output Analog-to-Digital Converter Input I2C Data Signal
12	GPIO12	I/O	General Purpose Input/Output
13	GPIO18 / CS / PWM5	I/O	General Purpose Input/Output SPI CS Signal Pulse-Width Modulated O/P
14	GPIO19 / SPI2_CLK / PWM4	I/O	General Purpose Input/Output SPI2 CLK Signal Pulse-Width Modulated O/P
15	GND	G	Ground
16	GPIO20 / SPI2_MOSI / PWM3	I/O	General Purpose Input/Output SPI2 MOSI Signal Pulse-Width Modulated O/P

17	GPIO0 / Debug_TX	I/O	General Purpose Input/Output UART Serial Data Transmit for debugging
18	GPIO1 / Debug_RX	I/O	General Purpose Input/Output UART Serial Data Receive for debugging
19	GPIO21 / SPI2_MISO / PWM2	I/O	General Purpose Input/Output SPI2 MISO Signal Pulse-Width Modulated O/P
20	GPIO22 / PWM1	I/O	General Purpose Input/Output Pulse-Width Modulated O/P
21	GPIO9 / ADC9 / UART1_RXD	I/O	General Purpose Input/Output Analog-to-Digital Converter Input UART1 Serial Data Receive
22	GPIO8 / ADC8 / UART1_TXD	I/O	General Purpose Input/Output Analog-to-Digital Converter Input UART1 Serial Data Transmit

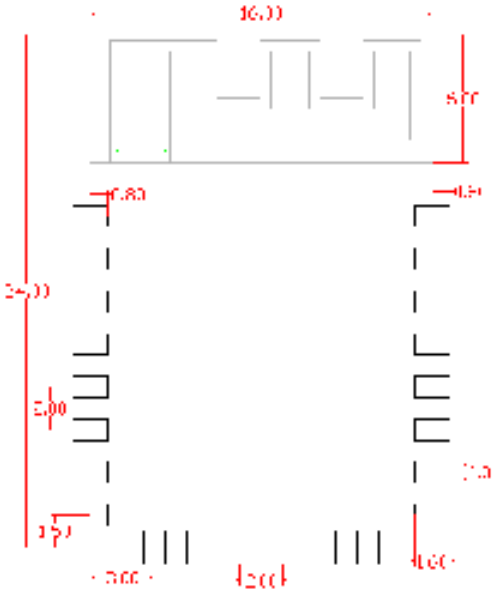
Note: For more details about pin-mux setting, please refer to OPL1600-Datasheet

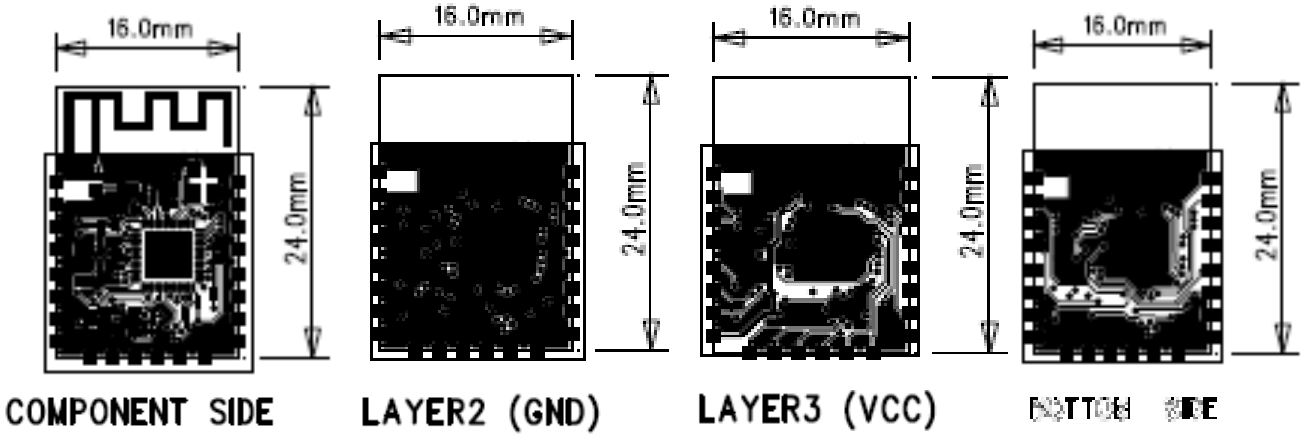
6. Dimensions

6.1 Layout Recommendation

(Unit: mm)

< TOP VIEW >





7. Reference Design

In order to achieve minimal power consumption, users may, under all types of operational modes, control the power modules in the control chip in OPL1600 chip of internal high-performance Buck & LDO DC-DC Converter. The system power, with input of decoupled capacitor from external battery power originated from VDD_BAT (pin 8), reduces noise with in-chip Buck DC-DC Converter, respectively in.

The OPL1600 is divided into four power domains, including analog, Power Management Subsystem (PMS), core, and retention power domains. The retention domain includes SRAM, IOPAD control logic and register files.

The analog and core domains can be powered off, and the retention domain power reduced to retention voltage to minimize the current of SRAM during the sleep mode. The sleep mode wakeup event can come from external event GPIOs and internal timer event.In addition, the OPL1600 can be put into lowest power consumption mode by driving EN pin to ground.

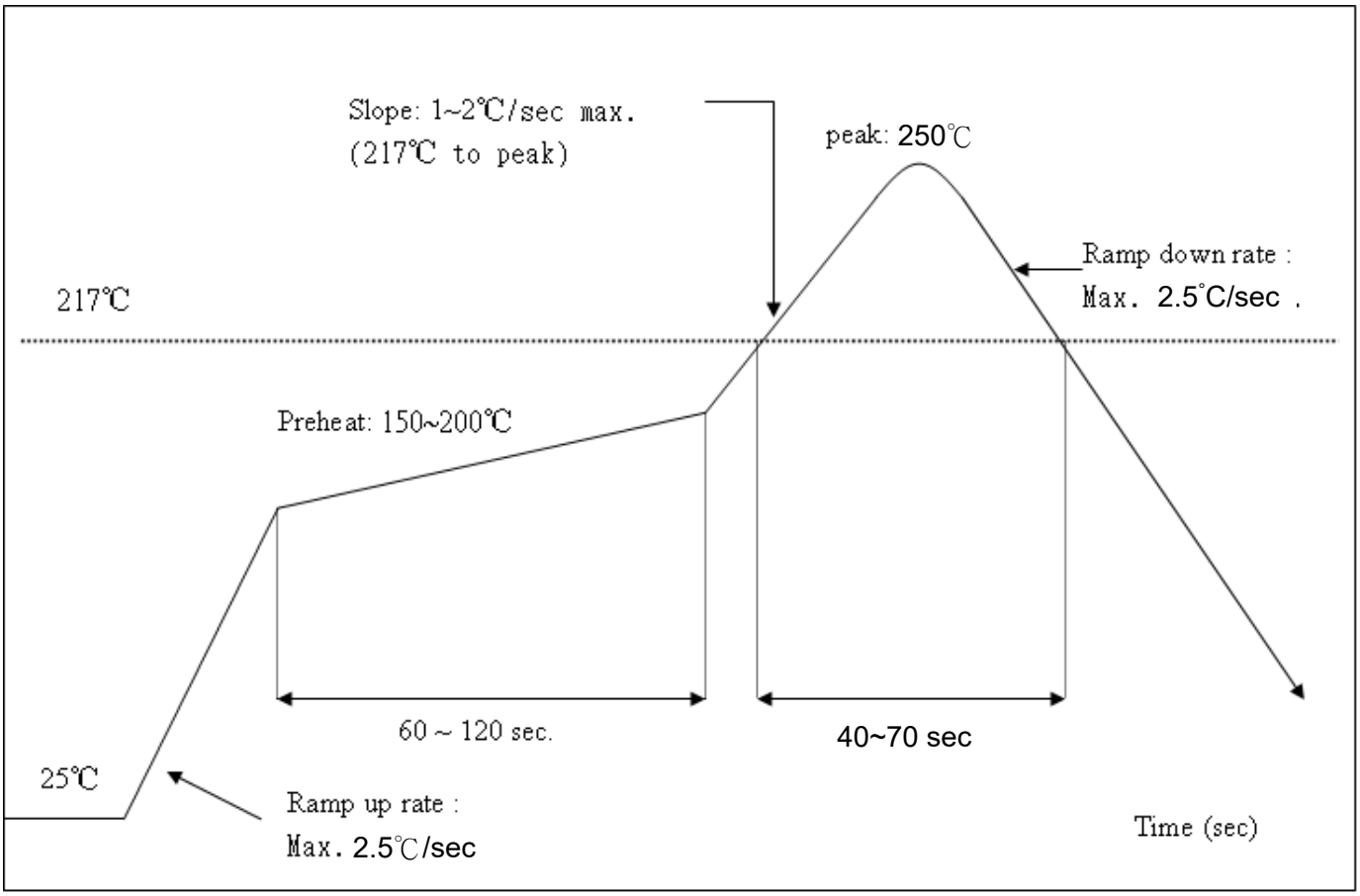
PWR_EN is used to control some basic analog bias blocks. Pull this pin low can minimize the leakage current. To avoid race condition and make sure power up sequence is normal, PWR_EN must not rise with VBAT at the same time. A simple RC circuit connect to VBAT can provide enough delay if PWR_EN is not controlled separately.

8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



9. Software Introduction

9.1 Software Architecture

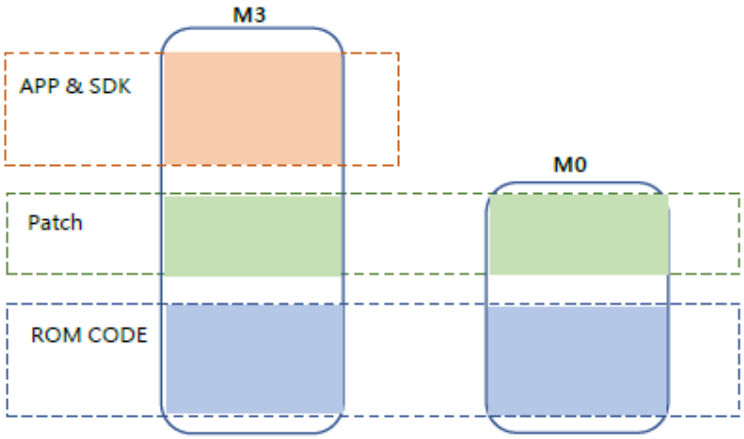


Figure 1: The Relationship Between User APP & ROM CODE and Patch

Relationship between APP & ROM Code & Patch

OPL1000 consists of two MCU's of ARM Cortex M3 and Cortex M0. The so-called OPL1000 APP Development refers to the application procedure for development users on M3 MCU of OPL1000. The initial M3, M0 firmware of OPL1000 is comprised in the Chip as ROM CODE. Furthermore, as functions expand and bugs resolved, OPL1000 also provides firmware patch of M3 and M0. Therefore, the development of user APP is completed based on the foundation of ROM code and firmware patch. Their relationship can be demonstrated with Figure 1.

The M0 Patch is sent out via Opulinks in the format of binary files. M3 Patch is provided in the format for lib documents, as the user APP and SDK source code from Opulinks are used as Keil C project for coding, therefore, the generated M3 bin document include M3 Firmware Patch, SDK and user APP application procedure. Ultimately, M0 Patch Bin documents and M3 Bin documents are combined and then downloaded to external Flash, and after OPL1000 is powered up, M3/M0 Bin documents in the Flash is loaded into RAM to execute. The overall process can be shown with Figure 2.

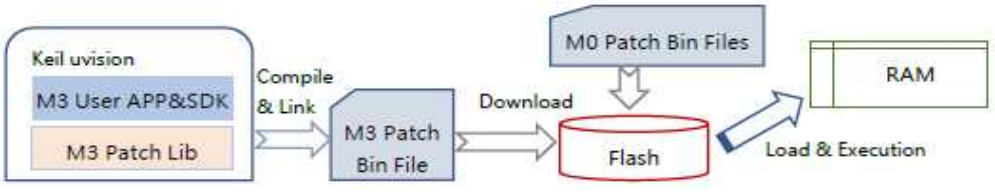


Figure 2: Compiling of User APP & Patch, Loading Process (without OTA Function)

The two types of Bin documents, supported by OPL1000, are "Pure Bin" documents as shown in Figure 2, as M3 bin document coded with users' procedure, then combined with M0 bin document in generating opl1000.bin file. This file stored in Flash 0x0000 position, neither including OTA loader, nor supporting OTA (Over-The-Air Download) function, and the other is called "OTA Image" document which is based on "Pure Bin" document, with messages such as OTA Loader and Bin Header, etc. included, in generating firmware documents that support OTA download, with the document generated by using

download tool named as “opl1000_ota.bin”. In order to understand the structure of OTA Image document, we need to first understand the working process of OPL1000 OTA upgrade firmware. When OPL1000 firmware supports OTA download for upgrade, there are two firmware maintained in Flash, as shown in Table 1,as the first OTA Bin file and the second OTA Bin file are placed in 0x00005000 and 0x0003E000 locations respectively, with the maximum size of 228K Bytes. At the locations of 0x00003000 and 0x00004000 there are Header message of the first and the second OTA bin. Header messages include the chip type, version message, firmware calibration and firmware size and Header Calibration, etc., of OTA Bin Firmware. The first OTA bin file and the second OTA bin use ping-pong switch method to execute upgrade. For example, when the currently executing firmware corresponding to the first OTA Bin document, then the firmware (and its Header message) downloaded through OTA download would be placed in the second OTA Bin document location (firmware in 0x0003E000, and header in 0x00004000). If the currently executing firmware corresponding to the second OTA Bin document, then the newly downloaded upgrade firmware would be placed in the first OTA Bin document location (firmware in 0x00005000, and header in 0x00003000) .
Please note that there are two premises for OPL1000 firmware supporting OTA download that firstly, being structured on opl1000_ota.bin, and the other being OTA Bin document supporting the function of obtaining firmware through BLE or WIFI. Regarding user APP coding that supports OTA function, download process is shown in Figure 3, as it includes two-time Pack combination functions. One is to combine user APP bin document and M0 bin document as opl1000.bin. The second is to combine opl1000.bin, OTA loader and the Header message of opl1000.bin, in forming opl1000_ota.bin document.

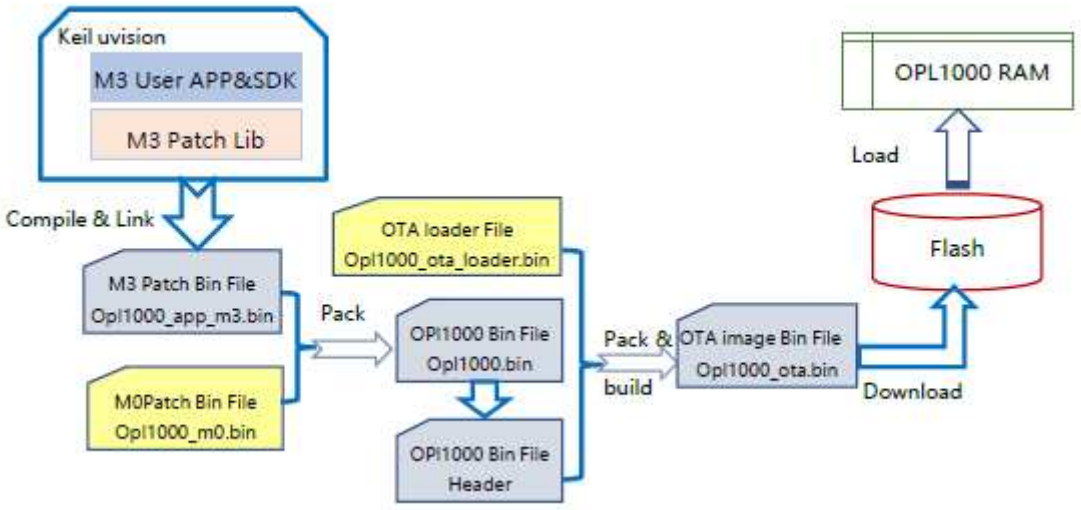


Figure 3: Coding of User APP & Patch, Loading Process (Supporting OTA Function)

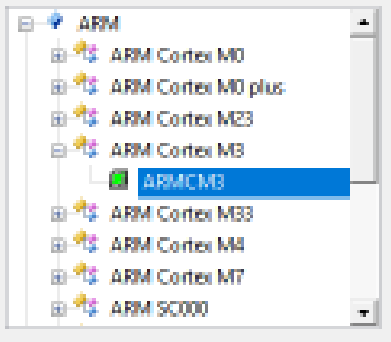
9-2 SDK Environment Setup

When users develop APP, it is recommended to develop with the Keil uVision 5 IDE tool. This chapter introduces the Keil uVision-based user APP project configuration method, and combines the hello_world demonstration project to briefly explain the project configuration, document structure, and RTOS usage, etc.

A. Keil uVision Project Setup
Open hello_world demonstration project.
Path: DK\APS_PATCH\examples\get_started\hello_world

Click the button, “ ”, with the following set-up.
Device, by default select ARMCM3, and for new project, users should be aware of the selection of this setting.

Figure 7: Device Selection



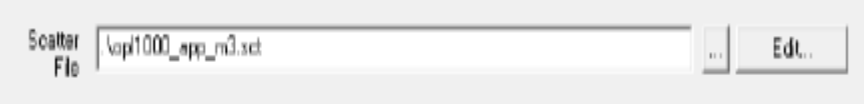
1. Target page sets up the address of size of the ROM address and the RAM address.

Table 6: Address Table

Type	Initialization Address	SIZE
IROM1	0x0	0xC0000
IRAM1	0x400000	0x50000

2. Linker label does not need to select “use Memory layout From Target Dialog” option. Scatter File document needs to be set up, as shown in Figure 8. By clicking button, this Scatter File can be opened up.

Figure 8: Scatter File



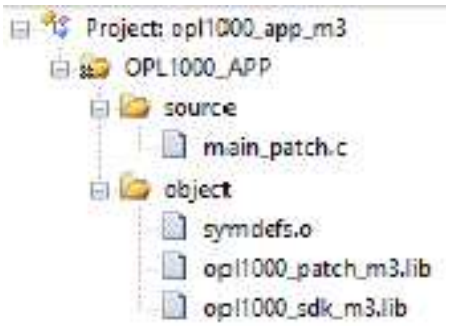
3. Debug label does not select “Load Application at Startup” option, but the content of “initialization File” needs to be set up, as shown in Figure 9, and if there is need to understand the content of “ini” further, click “ ”, and open “ini” document.
Figure 9: debug Setup

Note: In view of the importance of "ini" between patch code and ROM code, it is recommended NOT to modify the content of this document; otherwise it may result in abnormal operation of the codes.

9.3 Project Preview

By using the example of "hello world", Kei project set-up method was outlined, and this chapter willbe devoted to introduce the code structure of "hello_world" project. One basic project at least
includes these documents such as "main_patch.c", "sysdefs.o" , "opl1000_patch_m3.lib", and "opl1000_sdk_m3.lib".

Figure 10: hello world Project Source Code Strucure



Amongst those, "main_patch.c" is project demonstration code, and "sysdefs.o", "opl1000_patch_m3.lib" and "opl1000_sdk_m3.lib' are stored documents.
Address of folder for "opl1000_patch_m3.lib"& "opl1000_sdk_m3.lib":
SDK\APS\targets\opl1000\Output\Objects
If users need to newly build their own project, please add documents based on addresses outlined above.

9.4 Main Function Entrance

Open up “main_patch.c” document, and jump to “_Patcch_EntryPoint(void)” function.

```
static void __Patch_EntryPoint(void)
{
    // don't remove this code
    SysInit_EntryPoint();
    // update the flash layout
    MwFim_FlashLayoutUpdate = Main_FlashLayoutUpdate;
    // application init
    Sys_AppInit = Main_AppInit_patch;
}
```

As the SysInit_EntryPoint() function has been implemented in ROM. This function is only called to implement initialization, so the function should not be modified or move. Then as the code redefines the “Sys_AppInit” entry to the “Main_AppInit_patch” function, “Sys_AppInit” is the main function entry reserved by the SDK for software development on the user-end, and after mapping the entry function of “Sys_AppInit”, all APP initializations, such as peripheral initialization, creation of multitasking, etc. are all created internally in the mapping function of Main_AppInit_patch.

9.5 Log Output Setup

When users are developing APP, there are two types of debug message output.

(1) Internal log of user APP
(2) OPL1000 SDK firmware log

Log debugging print-out information is instrumental for users to check whether the application execution process and results are normal. The firmware log can help users quickly locate and analyze firmware module execution status, such as the operation of the ble and wifi protocol stacks.
In order to avoid excessive log output information that is not constructive for APP debugging, SDK only keeps the user log message output, and closes the internal log information output inside the firmware. If users need to manage log output mechanism, there are three methods:

(1) APS serial-port tracer command

After command is input, APS serial-port lists out all of missions that are currently carried out.

Figure 11:TRACER Command

```
Tracer Mode       [1]     0:disable/1:normal/2:print directly
Display Task Name [0]     0:disable/1:enable
Priority          [-2]    osPriorityIdle(-3) ~ osPriorityRealtime(3)
StackSize         [128]   number of uint_32
Queue Number      [128]   max number of log
Queue Size        [80]    max length of log
Log Level         [0x00:None/0x01:Low/0x02:Med/0x04:High/0x07:All]

Default Level for App Tasks      [0x07]

Index                 Name: Level
---------------------------------- Internal Tasks (Start from Index 0)
[ 0]              opl_isr_: 0x00
[ 1]              opl_diag: 0x00
[ 2]          opl_wifi_mac: 0x07
[ 3]        opl_supplicant: 0x00
[ 4]        opl_controller: 0x07
[ 5]                opl_le: 0x00
[ 6]        opl_event_loop: 0x07
[ 7]             opl_tcpip: 0x00
[ 8]              opl_ping: 0x00
[ 9]             opl_iperf: 0x00
[10]             opl_agent: 0x00
[11]       opl_at_wifi_app: 0x00
[12]                opl_at: 0x00
[13]        opl_at_tx_data: 0x00
[14]          opl_at_sock_: 0x00
[15]       opl_at_sockserv: 0x00
---------------------------------- App Tasks (Start from Index 32)
```

The user-created tasks are listed in the Start of App Tasks project, and with the example of user_app_demo task, it is created by users in the main procedure with index of 32, while 0x07 denotes
that printing all the logs of the task, so if users need to close the log output of the task. , command of “Tracer level 32 0x00” can be input in APS serial-port, which can also be applied in the log management of other tasks.
Note: The premise for using this method is that the user needs to enable the input function of the APS
serial-port when the main program is initialized, otherwise the input becomes invalid.
At the same time, when the configuration loses power, it needs to be reconfigured when it is powered on next.

```
#include "hal_dbg_uart_patch.h"
static void Main_AppInit_patch(void)
{

    Hal_DbgUart_RxIntEn(1); // APS uart rx enable

}
```

(2) Using log output provided by SDK to configure API management task log API relevant content configured by log output is as follows:

```
extern T_TracerLogLevelSetFp tracer_log_level_set_ext;
int tracer_log_level_set_ext(uint8_t bIdx, uint8_t bLevel);
```

"tracer_log_level_set_ext" function entry parameters are defined in Table 7.

Table 7: tracer_log_level_set_ext Function Entry Parameter Definition

Parameter	Value	Description
bIdx	0 ~ TRACER_TASK_IDX_MAX	Internal module index number
bLevel	LOG_ALL_LEVEL	Print all log
	LOG_NONE_LEVEL	Close log

The method users through API enable internal log of firmware:

```
tracer_log_level_set_ext (2, LOG_ALL_LEVEL); // here 2->opl_wifi_mac
```

(3) Multi-task log management

If there needs to be differentiated management towards log output of multiple tasks, the structure, "g_taTracerExtTaskInfoBodyExt", of "msg_patch.c"needs to be edited. Adding user-defined tasks.

```
T_TracerTaskInfo g_taTracerExtTaskInfoBody[TRACER_EXT_TASK_NUM_MAX] =
{
    {"demo_app1", LOG_ALL_LEVEL, 0, 0 },
    {"demo_app2", LOG_ALL_LEVEL, 0, 0},
    {"",  LOG_NONE_LEVEL, 0, 0},
};
```

The name of task, created for users by demo_app1 and demo_app2, can be configured and defined as:

```
#define LOG_HIGH_LEVEL    0x04
#define LOG_MED_LEVEL     0x02
#define LOG_LOW_LEVEL     0x01
#define LOG_NONE_LEVEL    0x00
#define LOG_ALL_LEVEL     (LOG_HIGH_LEVEL | LOG_MED_LEVEL | LOG_LOW_LEVEL)
```

The log management of users' other tasks is added to the structure in the manner as outlined above.

If needed to know more about the Log configuration, please refer to the log configuration demonstration with the directory of "SDK\APS_PATCH\examples\get_started\log"

10.Appendix

Compliance with

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C has been investigated. It is applicable to the modular transmitter

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions (example, uses another antenna) for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

This module is single modular.

Not applicable.

2.5 Trace antenna designs

Not applicable.

2.6 RF exposure considerations

This modular transmitter should be used in the mobile conditions and 20cm from a person's body, the host product manufacture should be put those information in the end-product manual to the end users. If RF exposure statement and use conditions are not provided, then the host product manufacture is required to take responsibility of the module through a change in FCC ID(new application)

2.7 Antennas

This radio transmitter FCC ID : 2AWP5WMD566 and has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Manufacturer	Part No.	Antenna Type	Maximum antenna gain
IOTTECH	ITM-D566	PCB Antenna	-0.27 dBi for 2.4GHz

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID: 2AWP5WMD566.

2.9 Information on test modes and additional testing requirements

Host manufacturer which install this modular with limit modular approval should perform the test of radiated emission and spurious emission according to FCC part 15 :15.212 requirement, only if the test result comply with FCC part 15.212 requirement, then the host can be sold legally.When testing host product, the host manufacture should follow FCC KDB Publication 996369 D01 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B.

Federal Communications Commission (FCC) Statement

15.21

You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b) for Class B Device (usual)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: To assure continued compliance, any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. (Example - use only shielded interface cables when connecting to computer or peripheral devices).

End Product Labeling

This transmitter module is authorized only for use in devices where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in visible area with the following: "Contains FCC ID: 2AWP5WMD566"

End Product Manual Information

The user manual for end users must include the following information in a prominent location "IMPORTANT NOTE: To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter." This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions (1) This device may not cause harmful interference and (2) This device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

This devisees intended only for OEM integrators under the following conditions: The antenna must be installed such that 20 cm is maintained between the antenna and users. As long as a condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral

requirements, etc.).

NCC警語：

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使
用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。低功率射頻器材之
使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善
至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。
低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

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