Datasheet

RM126x LoRaWAN™ Module

Part Numbers: RM126x (RM1261 and RM1262)

Version 1.1

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
0.1	17 May 2023	Preliminary Release	Raj Khatri Dave Drogowski	Senthooran Ragavan
0.2	29 Sept 2023	Replaced “MCU” with SoC” where applicable. Replaced “microcontroller” to SoC” in Figure 4	Raj Khatri Dave Drogowski	Senthooran Ragavan
0.3	20 Oct 2023	Updated Sleep currents in Table 8 of section 3.3.4 LoRa Power Consumption.	Greg Leach Dave Drogowski	Senthooran Ragavan
0.4	23 Oct 2023	Updated orientation for MOSI/MISO signals and pad for BUSY signal in Block Diagram and Pin-out	Raj Khatri Dave Drogowski	Senthooran Ragavan
1.0	24 Oct 2023	Initial Release	Various	Senthooran Ragavan
1.1	31 Oct 2023	Added Note 6 for EFR32 Soc GPIO (PB01) control of RF switch (ANT_SW) pin.	Raj Khatri Greg Leach, Dave Drogowski	Senthooran Ragavan

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1 Overview and Key Features

This Datasheet describes both the RM1261 and RM1262. The differences are outlined in the radio specifications.

The Laird Connectivity RM126x series of modules (RM1261 and RM1262), is based on **Silicon Labs EFR32 series SoC** and the **Semtech SX1261** / **SX1262 radio.** They provide a low power, long range solution for you to easily develop your LoRaWAN™ application. The RM126x supports LoRaWAN classes A, B and C for secure, scalable, and bi-directional communication and leverages the advantages of Silicon Labs hardware, software, and tools. The Laird Connectivity RM126x module also includes a **LoRa Point to Point (LoRa P2P)** capability which enables you to create your own private ultra-long range radio network between two RM126x modules.

The RM126x series modules are small form factor PCB modules with a built in MHF4 connector, TCXO and a DC-DC converter.

Note: This information in this document is subject to change. For full documentation, technical drawings, software downloads and more visit the RM126x page at: www.lairdconnect.com/rm126x-series

1.1 Features and Benefits

- Designed to operate in both hosted and hostless modes:
  - **Hosted Mode**: When connected to an external MCU, the RM126x can be simply and easily programmed with our AT command set.
  - **Hostless Mode**: Utilizing the powerful Cortex-M33 core which includes 512kB flash and 32K of RAM. Full support is offered by Silabs' Simplicity Studio for development purposes with a range of sample applications we offer to simplify your development.
- **Designed for IoT Devices:** Small 14mm x 13mm PCB module for smaller end device design.
- **Based on the EFR32 series SoC:** First LoRaWAN module based on Silicon Labs SoC, following Silicon Labs tools for development.
- **Powerful Core Cortex-M33**: 512 kB Flash, 32 kB RAM
- **Many interfaces**: GPIO, I2C, UART, SPI, Analog, Freq, PWM
- **Ultra-low power consumption**: Years of use on a single battery
- **Broad regulatory region support**:
  - RM1261 – Europe, UK, Taiwan, Japan, India
  - RM1262 – USA, Canada, Australia, New Zealand
- **LoRa P2P** Communication: create your own proprietary radio.
- **Certifications**: FCC, ISED, EU, UKCA, NCC, AS/NZS, MIC, IN
- **Lora Alliance** certified
- **Fully featured development kits:** Everything needed to start your LoRaWAN device development.
- **Fast time-to-market**

1.2 Application Areas

- Public or private networks
- Irrigation/Agriculture
- Parking
- Lighting
- Asset tracking
- Tank monitoring
- Smart Home – smoke alarms, heating,
- Access control – security
- Industrial automation – factory
- Any long range, battery powered sensor application

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2 SPECIFICATIONS

Table 1: Specifications

Categories	Feature	Implementation	
LoRaWAN Wireless Specification	Specification	LoRaWAN 1.04 (End Device) LoRa MAC Class A, B and C	
	LoRaWAN Regional Parameters specification	LoRaWAN RP002-1.0.3 LoRaWAN Regional Parameters	
	RF connector	MHF4	
	Frequency	863-870MHz	
		902-928MHz	
	Maximum Transmit Power Setting (conducted)	Upto 22dBm	RM1262 (see Note1)
		Upto 14dBm/15dBm	RM1261 (see Note1)
	Minimum Transmit Power Setting (conducted)	-9.0dBm RM1262 -17dBm RM1261	
	Receive Sensitivity	-125.6dBm (SF7, LoRa 125kHz, 903.0MHz) -139.2dBm (SF12, LoRa 125kHz, 863.1MHz) -122.7dBm (SF7, LoRa 250kHz, 869.9MHz) -130.8dBm (SF12, LoRa 500kHz, 923.3MHz) -109 dBm (FSK 50kbps, TBD MHz)	
	Modulation, Bandwidth, data rates (as per RP002-1.0.3)	LoRa – Chirp Spread Spectrum and FSK 50kps LoRa 125kHz, LoRa 250kHz, LoRa 500kHz, FSK 50kbps	
	TCXO High Accuracy	32MHz ±1ppm (at 25°C) Stable Frequency over temperature and duration of the LoRa, FSK packet (longest packet is 2793.5ms)	
	Link Budget (RM1262) Link Budget (RM1261)	183.2dB @ LoRa 125kHz, SF12, 22dBm TX power 153.2dB @ LoRa 125kHz, SF12, 14dBm TX power	
	Range	Up to 15 km in free space	
LoRa Point to Point (LoRa P2P)	Specification	Supports Unicast or Broadcast with nodes up to 64 devices per network.	
Host Interface and Peripherals	Total	16 GPIOs: SWD (3 pins), EUART (4pins), Boot pin (1 pin), GPIO, I2C, UART, SPI, Analog, Freq, PWM (8 pins)	
	UART	TX, RX, CTS, RTS DCD, RI, DTR, DSR, CTS, RTS (Note1) Default 115200, n, 8, 1 From 9,600 to 1,000,000 bps	
	GPIO	Up to 8 With configurable I/O direction, pull-up/pull-down Default Silabs “Disabled input” at application start-up (AT FW)	

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Categories	Feature	Implementation
	ADC	One 12-bit channel (including ADC reference) 12-bit resolution 1.21V internal reference or external reference VDD
	PWM or FREQ output	PWM output on up to three GPIO output pins (in AT firmware):
		PWM output duty cycle: 0%-100%
		PWM output frequency: 10kHz
		FREQ output on up to one GPIO output pins (in AT firmware):
		FREQ output frequency: 0 MHz-1 MHz (50% duty cycle)
	I2C	Upto 2xI2C interface (100 kbps, 400kbps, 1Mbps)
	SPI	Upto 2xSPI Master interface (1Mbps)
	BOOT pin (for AT firmware)	BOOT pin High (default, pull-up 44KOhms): start application BOOT pin Low (externally): enter Bootloader
	SWD interface	1 x 3 pins Programming firmware (preferred)
Software	Programming or upgrade (via SWD 2-pin interface)	Hosted: AT Command set Hostless: C development using Silicon Labs Simplicity Studio
Supply Voltage	Operating Voltage (Internally regulated DCDC or LDO)	RM1261: 2.0V-3.6V 14dBm
		RM1262: 3.0V-3.6V 22dBm (22dBm – 2dB)
		2.7V 20dBm
		2.4V 19dBm (22dBm – 3dB)
		2.0V 16dBm (22dBm – 6dB)
LoRa Power Consumption	Peak TX current	RM1262 LoRa TX 915MHz: 107mA 22dBm RM1262 LoRa TX 915MHz: 50.7mA 14dBm RM1261 LoRa TX 915MHz: 25.0mA 14dBm
	Peak RX current	RM1262 LoRa Receive: 8.1mA (LoRa); 7.6mA (FSK) RM1261 LoRa Receive: 8.1mA (LoRa); 7.6mA (FSK)
	Sleep current	RM1262/ RM1261 Sleep: 2.6uA (EM2, Full RAM retention, RTC(LXFO)) RM1262/ RM1261 Sleep: 2.2uA (EM3, Full RAM retention, RTC(ULFRCO)) RM1262/ RM1261 Sleep: 2.1uA (EM2, Full RAM retention, RTC(LFXO), no SoC Radio RAM retention, BURTC enabled)
Antenna Options	LoRa (External)	Dipole antenna with up to 2.0 dBi (868MHz). Dipole antenna with up to 2.2 dBi (915MHz). Some with MHF4 (IPEX) connector or RP-SMA connector
Physical	Dimensions	14 mm x 13 mm x 2 mm
	Weight	0.9 grams
Environmental	Operating	-40˚C to +85˚C
	Storage	-40˚C to +85˚C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	1-Year Warranty

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Categories	Feature	Implementation
Development Tools	Development Kit	Development Kits: DVK-RM1261 (453-00140-K1), DVK-RM1262 (453-00139-K1) and Free Software Tools
Approvals	LoRa Alliance	LoRaWAN Alliance End Node Certified
	Radio Regulatory	RM1262: FCC, ISED, AS/NZS RM1261: EU, UKCA, NCC(Taiwan), MIC(Japan), IN(India)

Note 1: It is mandatory to use the correct RF registers to set RF TX power based on country radio regulatory requirements. For details, see Mandatory FW Requirements Related to Hardware.

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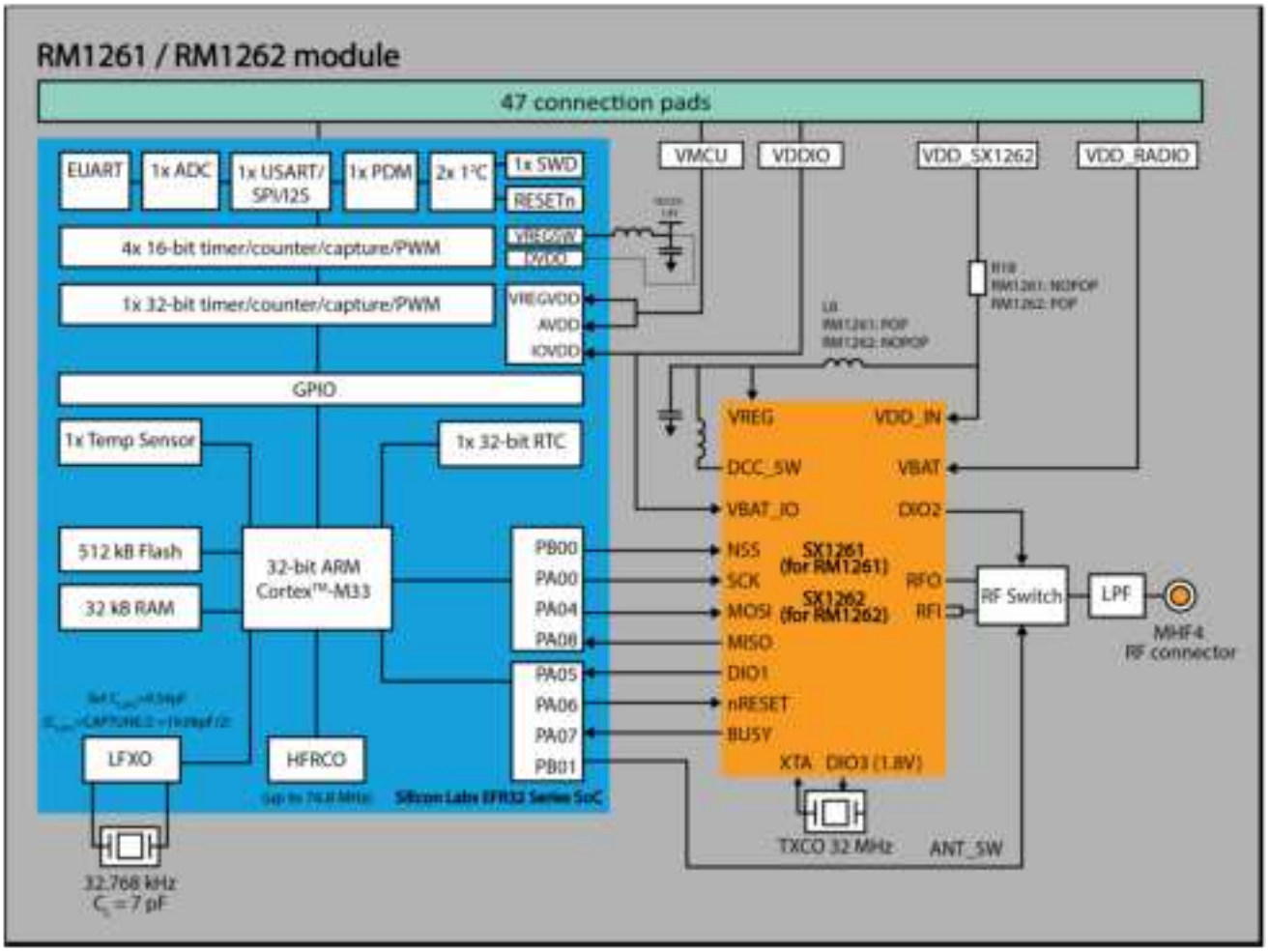
3 HARDWARE SPECIFICATIONS

3.1 Block Diagram and Pin-out



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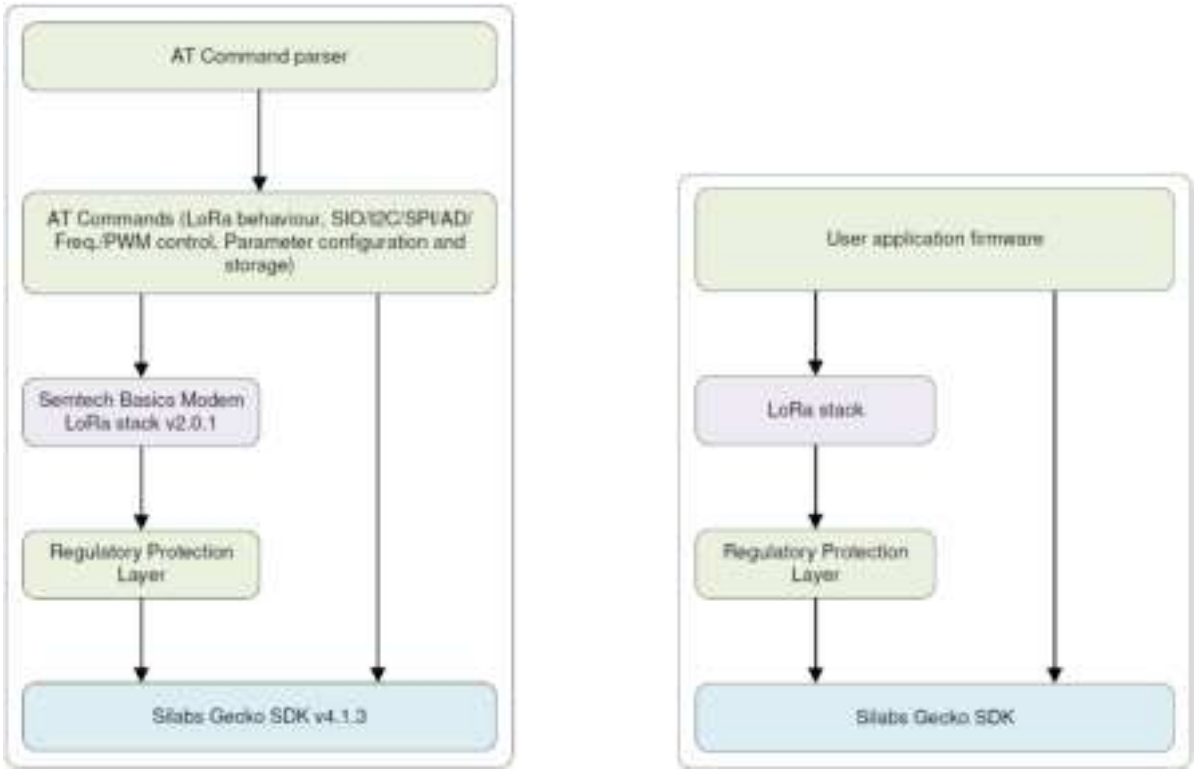

When using AT firmware **When NOT using AT firmware – Native C development**

Figure 1: Functional HW and FW block diagram for RM126x series AT modules

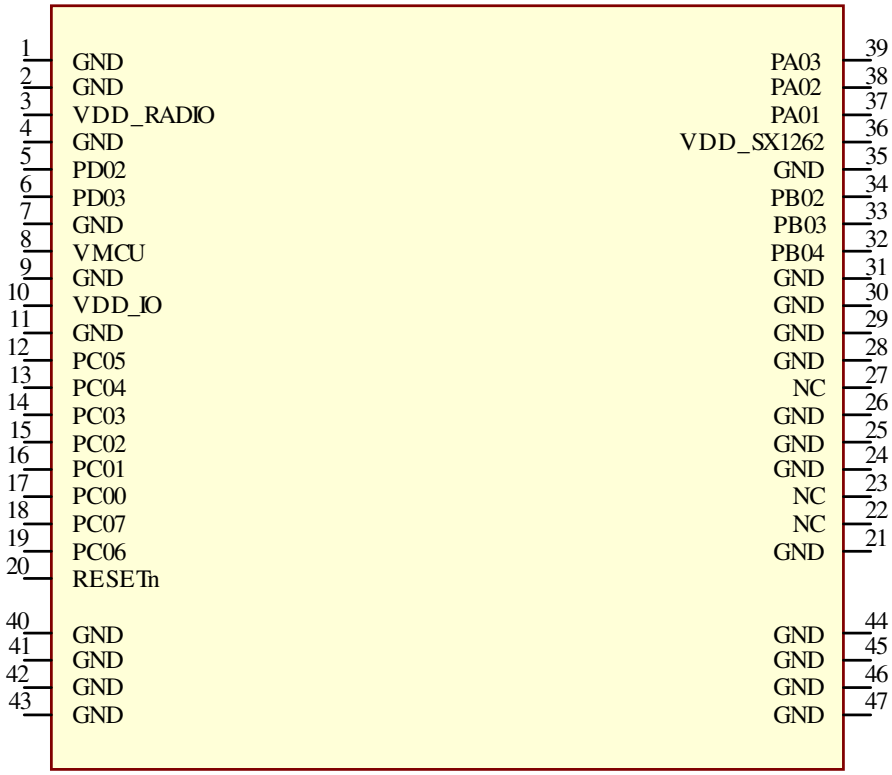

Figure 2: RM1261 and RM1262 module pin-out (top view)

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3.2 Pin Definitions

Table 2: Pin definitions

Pin #	Pin name and Port	Pin Name when using AT Firmware (NOTE1 for IO state)	Pin Name When using Custom FW / Native C development)	EFR32 SoC pin #	EFR32 SoC pin name	Comment
1	GND	-	-	-	-	-
2	GND	-	-	-	-	-
3	VDD_RADIO	-	-	-	-	MUST connect to same external supply as VMCU, VDD_IO, VDD_SX1262.
4	GND	-	-	-	-	-
5	PD02	SIO07/I2C1/AN/ FREQ/PWM/SPI_CIPO	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	38	PD02	MIKROE_SPI_MISO on DVK-RM126x
6	PD03	SIO06/I2C1/AN/ FREQ/PWM/SPI_COPI	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	37	PD03	MIKROE_SPI_MOSI on DVK-RM126x
7	GND	-	-	-		-
8	VMCU	-	-	32 35	VREGVDD, AVDD	MUST connect to same external supply as VDD_RADIO, VDD_IO, VDD_SX1262.
9	GND	-	-	-	-	-
10	VDD_IO	-	-	36	IOVDD	MUST connect to same external supply as VDD_RADIO, VMCU, VDD_SX1262.
11	GND	-	-	-	-	-
12	PC05	SIO05 /I2C1/AN/ FREQ/PWM	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	6	PC05/	LED0 on DVK-RM126x or MIKROE_INT on DVK-RM126x
13	PC04	SIO04/I2C1/AN/ FREQ/PWM	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	5	PC04	MIKROE_PWM on DVK-RM126x
14	PC03	SIO03 /I2C1/AN/ FREQ/PWM	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	4	PC03	MIKROE_RST on DVK-RM126x
15	PC02	SIO02/I2C1/AN/ FREQ/PWM	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	3	PC02	MIKROE_ANALOG on DVK-RM126x
16	PC01	SIO01/I2C1/AN/ FREQ/PWM	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0	2	PC01	MIKROE_SPI_CS on DVK-RM126x
17	PC00	SIO00/I2C1/AN/ FREQ/PWM/SPI_CLK	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	1	PC00	MIKROE_SPI_SCK on DVK-RM126x
18	PC07	EUART_TX	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0.PDM	8	PC07	Output, Set high in FW
19	PC06	BOOT	I2C0/I2C1/AN/ FREQ/PWM/EUART0/USART0/PDM	7	PC06	Input, default pull high (not enter BOOT mode). BOOT or BUTTON0 on DVK-RM126x. 1Mohm pull on DVK-126X
20	RESETn	RESETn	RESETn	11	RESETn	System Reset (Active low). 1.8V IO voltage only. Internally pulled-up to 1.8V.

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Pin #	Pin name and Port	Pin Name when using AT Firmware (NOTE1 for IO state)	Pin Name When using Custom FW / Native C development)	EFR32 SoC pin #	EFR32 SoC pin name	Comment
21	GND	-	-	-	-	-
22	NC	-	-	-	-	DO NOT CONNECT
23	NC	-	-	-	-	DO NOT CONNECT
24	GND	-	-	-	-	-
25	GND	-	-	-	-	-
26	GND	-	-	-	-	-
27	NC	-	-	-	-	DO NOT CONNECT Reserved for future. RF pad active on future RF pad variant.
28	GND	-	-	-	-	-
29	GND	-	-	-	-	-
30	GND	-	-	-	-	-
31	GND	-	-	-	-	-
32	PB04	EUART_CTS	I2C0/AN/FREQ/PWM/ EUART0/USART0/USART1/PDM	15	PB04	Input, pull-down in AT FW
33	PB03	EUART_RX	I2C0/AN/FREQ/PWM/ EUART0/USART0/USART1/PDM	17	PB03	Input, pullup in AT FW
34	PB02	EUART_RTS	I2C0/AN/FREQ/PWM/ EUART0/USART0/USART1/PDM	18	PB02	Output Set low in AT FW
35	GND	-	-	-	-	-
36	VDD_SX1262	-	-	-	-	VDD_SX1262: RM1262: Lora Radio only. 3.3V minimum to achieve 22dBm. VDD_SX1262: NC on RM1261. MUST connect to same external supply as VDD_RADIO, VMCU, VDD_IO.
37	PA01	SWCLK	I2C0/AN/FREQ/PWM/ EUART0/USART0/USART1/SWCLK/PDM	22	PA01	-
38	PA02	SWDIO	I2C0/AN/FREQ/PWM/ EUART0/USART0/USART1/SWDIO/PDM	23	PA02	-
39	PA03	SWO	I2C0/AN/FREQ/PWM/ EUART0/USART0/USART1/SWO/PDM	24	PA03	-
40	GND	-	-	-	-	-
41	GND	-	-	-	-	-
42	GND	-	-	-	-	-
43	GND	-	-	-	-	-
44	GND	-	-	-	-	-
45	GND	-	-	-	-	-
46	GND	-	-	-	-	-
47	GND	-	-	-	-	-

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Note 1: Apart from EUART, BOOT, when using AT firmware, most of the SIO GPIO pins are input and EFR32BG22 pin configuration “DISABLED” by default. “DISABLED” disables the pin, reducing the power consumption to a minimum. When the input drivers are disabled, the pin can be used as connection for an analog module.

Avoid floating inputs, which can also cause current consumption in low power mode (e.g. Sleep) to drift with time.

When using AT firmware, BOOT pin is default high (internally).

When using AT firmware, EUART, has below IO direction and state:
- EUART_TX, PC07 is an output, set high (in AT firmware).
- EUART_RTS, PB02 is an output, set low (in AT firmware).
- EUART_RX, PB03 is an input, set with internal pull-up (in AT firmware).
- EUART_CTS, PB04 is an input, set with internal pull-down (in AT firmware).

For Native C development, to learn which GPIO ports provide access to every peripheral, consult Analog Peripheral Connectivity and Digital Peripheral Connectivity in the EFR32BG22 datasheet.

Note 2: All pins (SIO, AN, EUART, SWD) I/O voltage tracks VDD.

Note 3: 2-pin Serial Wire Debug (SWD) Programming/Debug Interface, pin38 (PA02, SWDIO) and pin37 (PA01, SWDCLK) used for upgrading firmware with Silabs Simplicity Studio SWD programmer via the Mini Simplicity connector. Using this 2-pin Serial Wire SWD Programming/Debug Interface requires on customers host PCB a header connector, refer to Two-pin Serial-Wire Debug (SWD) Programming/Debug Interface for details **of connector and wiring.**

Note 4: Pull the RESETn pin (pin 20) low for minimum 100 ns to reset the module. RESETn pin has a pull-up internally (to an internal 1.8V). RESETn pin should not exceed 1.8V.

Note 5: When I2C interface is selected, pull-up resistors on I2C SDA and I2C SCL MUST be connected externally as per I2C standard.

Note 6: EFR32 Soc GPIO (PB01) control of RF switch (ANT_SW).

Mode (SX1261 or SX1262 radio)	EFR32 series SoC GPIO PB01 state driving RF switch (ANT_SW) pin. PB01 is configured as Push Pull output. PB01 initialised to output low to put RF switch in disabled state.
RF transmit	Output High
RF receive	Output High
Standby	Output High
Sleep	Output Low

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3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage (Table 3).

Table 3: Maximum Current Ratings

Parameter	Minimum	Maximum	Unit
Voltage at VDD_RADIO	-0.5	3.9	V
Voltage at VDD_SX1262	-0.5	3.9 (Note 1)	V
Voltage at VDD_VMCU	-0.3	3.8	
Voltage at VDD_IO	-0.3	3.8	V
Voltage ramp rate on any supply pin		1.0	V / us
Voltage at GND pin		0	V
DC voltage on any GPIO pin	-0.3	VDD_IO+0.3	V
DC voltage in RESETn pin	-0.3	3.8(Note 2)	V
Total current into VDD_VMCU		200	mA
Current per I/O pin (sink or source)		50	mA
Current for all I/O pins (sink or source)		200	mA
RF Input level	10		dBm
Storage temperature	-40	+85	ºC
Moisture Sensitivity Level (MSL)		MSL4	
ESD (as per EN301-489)			
Conductive coupling		4	kV
Air coupling		8	kV

Note 1: VDD_SX1262 pin is only for RM1262. VDD_SX1262 pin on RM1261 is no connect or can be connected (as it is not used in the RM1261 module).

Note 2: RESETn pin has a pull-up internally (to an internal 1.8V). For minimum leakage, RESETn should not exceed 1.8V.

3.3.2 Recommended Operating Parameters

Table 4: Power Supply Operating Parameters

Parameter	Min	Typ	Max	Unit
Voltage at supply pins VDD_RADIO, VDD_VMCU, VDD_IO, VDD_SX1262 (Note 1). (With DCDC in EFR32 in regulation with EFR32 Iload=5mA limit, (Note 2).	2.0	3.3	3.7	V
Voltage at supply pins VDD_RADIO, VDD_VMCU, VDD_IO, VDD_SX1262(NOTE1). (With DCDC in EFR32 in bypass).	2.0	3.3	3.7	V
VCC Maximum ripple or noise (Note 3)			TBD	mV
Operating Temperature Range	-40	-	+85	ºC
RF input power			0	dBm

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Parameter	Min	Typ	Max	Unit
Maximum allowed RF TX power per country		As per radio certifications (Section 5.4)		dBm

Note 1: VDD_SX1262 pin is only for RM1262: To achieve RM1262 full RF TX power of 22dBm, requires minimum 3.3V on pin VDD_SX1262. Other VDD pins MUST be at same voltage as that on VDD_SX1262 pin.

VDD_SX1262 pin on RM1261: is no connect on the RM1261 or can be connected (as it is not used in the RM1261 module). Other VDD pins MUST be at same voltage.

Note 2: EFR32 DCDC in regulation (in AT Firmware) and with EFR32 Iload=5mA limit**.** If Iload more than 5mA, the supply voltage minimum needs to be 2.2V.

Note 3: The maximum VDD ripple or noise (at any frequency) that does not disturb the radio.

Table 5: Signal Levels for GPIO (SIO) Interface and RESETn

Parameter	Minimum	Typical	Maximum	Unit
Input high voltage (any GPIO), V_{IH}	0.7*VDD	-	VDD	V
Input high voltage (RESETn), V_{IH} (Note1)	0.7*1.8V	-	1.8	V
Input low voltage (any GPIO), V_{IL}	-	-	0.3VDD	V
Input low voltage (RESETn), V_{IL} (Note1)	-	-	1.8	V
Hysteresis of input voltage (any GPIO), V_{HYS}	0.05*VDD	-	-	
Hysteresis of input voltage (RESETn), V_{HYS}	0.05*1.8	-	-	
Output high voltage, V_{OH}		-		
source 20mA, VDD=3.0V	0.8*VDD		-	V
source 8mA, VDD=2.0V	0.6*VDD		-	V
Output low voltage, V_{OL}				
source 20mA, VDD=3.0V	-	-	0.2*VDD	V
source 8mA, VDD=2.0V	-	-	0.4*VDD	V
GPIO rise time, T_{GPIO_RISE}				
VDD=3.0V, C_{LOAD}=50pF, SLEWRATE=4, 10% to 90%	-	8.4	-	ns
VDD=2.0V, C_{LOAD}=50pF, SLEWRATE=4, 10% to 90%	-	13	-	ns
GPIO fall time, T_{GPIO_FALL}				
VDD=3.0V, C_{LOAD}=50pF, SLEWRATE=4, 90% to 10%	-	7.1	-	ns
VDD=2.0V, C_{LOAD}=50pF, SLEWRATE=4, 90% to 10%	-	11.9	-	ns
Pull up/ down resistance, V_{PULL} (Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0).	35	44	55	kΩ
Pull up/ down resistance, V_{PULL} (RESETn pin. Pull-up to 1.8V) (Note 2)	35	44	55	kΩ
Maximum filtered gltch width, V_{GF} (MODE = INPUT, DOUT = 1)	-	27	-	ns
RESETn low time to ensure pin reset, T_{RESET}	100	-	-	ns

Note 1: GPIO input thresholds are proportional to VDD pin. RESETn input threshold proportional to internal 1.8V.

Note 2: GPIO pull-ups connect to VDD supply, pull-downs connect to VSS. RESETn pull-ups connect to internal 1.8V.

Table 6: SIO pin alternative function AIN (ADC) specification

Parameter	Minimum	Typical	Maximum	Unit

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Main analog supply, V_{IN_MAX} (Note 1)	2		VDD	V
Full-Scale Voltage, V_{FS}	-	V_{REF} /Gain	-	-
Input Measurement Range				
Differential Mode - Plus and Minus inputs	-V_{FS-}	-	+V_{FS}	V
Single Ended Mode - One input tied to ground	0	-	V_{FS}	
Input Sampling Capacitance, C_S				
Analog Gain =1x	-	1.8	-	pF
Analog Gain =2x	-	3.6	-	pF
Analog Gain =4x	-	7.2	-	pF
Analog Gain =0.5x	-	0.9	-	pF
ADC clock frequency, f_{CLK}	-	-	10	MHz
Current from supply continuous operation, I_{ADC_CONT}				
Normal Mode, 1 Msps, OSR=2, fCLK =10 MHz	-	290	385	uA
Current in Standby mode. ADC is not functional but can wake up in 1us, I_{STBY}				
Normal Mode	-	16	-	uA
ADC Startup Time, $T_{startup}$				
From power down state	-	5	-	us
From Standby state	-	1	-	us
ADC Resolution	-	12	-	bits
External reference voltage range, V_{EVREF}	2	-	VDD	V
Internal reference voltage range, V_{IREF}	-	1.21	-	V

3.3.3 BOOT pin (for AT firmware)

For RM126x loaded with AT firmware, the BOOT pin is used to determine when execution of the bootloader is required. Upon reset, execution of the bootloader begins. The state of the BOOT pin is read immediately upon start-up of the bootloader. If LOW, execution of the bootloader continues, facilitating firmware update via the EUART. If the BOOT pin is HIGH, the bootloader will stop execution and pass control to the main application firmware.

Table 7: BOOT pin

Signal Name	Pin #	I/O	Comments
PC06/BOOT	19	I	Input with active low logic. Operating mode selected by BOOT pin status (at power up): If externally held Low (0V), enters BOOT mode; If High (VDD), enter application (default).

3.3.4 LoRa Power Consumption

VDD 3.3V with both DCDC on (in SX126x and EFR32) and 25°C, see Table 8).

Table 8: Power consumption

Parameter	Min	Typical						Max	Unit
		928	915	902	870	868	863		MHz
RM1262:									
RM1262 RF TX power at setting @22dBm		20.7	21.1	21.4		Note2			dBm
RM1262 Peak current at setting @22dBm		106	109	111		Note2			mA
RM1262 RF TX power at setting @14dBm						Note2			dBm
RM1262 Peak current at setting @14dBm						Note2			mA

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Parameter	Min	Typical						Max	Unit
		928	915	902	870	868	863		MHz
RM1261:									
RM1261 RF TX power at setting @15dBm									dBm
RM1261 Peak current at setting @15dBm									mA
RM1261 RF TX power at setting @14dBm		13.7	13.8	13.9	13.9	14.0	14.0		dBm
RM1261 Peak current at setting @14dBm		28.3	28.8	29.0	29.4	29.5	29.5		mA
RM1261 RF TX power at setting @13dBm									dBm
RM1261 Peak current at setting @13dBm									mA
RM1261 RF TX power at setting @12dBm									dBm
RM1261 Peak TX current at setting @12dBm									mA

RM1261 AND RM1262:	Min	Typical	Max	Unit
Peak current, RF RX Mode				
RX boosted, FSK, includes, EFR32 (peripherals disabled) current.		7.6		mA
RX boosted, LoRa, includes, EFR32 (peripherals disabled) current.		8.1		mA
Sleep (Note 2)				
RM1262/ RM1261 Sleep: 2.6uA (EM2, Full RAM retention, RTC(LXFO))		2.6		uA
RM1262/ RM1261 Sleep: 2.2uA (EM3, Full RAM retention, RTC(ULFRCO))		2.2		uA
RM1262/ RM1261 Sleep: 2.1uA (EM2, Full RAM retention, RTC(LFXO), no SoC Radio RAM retention, BURTC enabled) - used in AT firmware.		2.1		uA

Note 1: Peak currents measured with RM126x radio test firmware, EUART open. Receive “RX Boosted” refers to SX126x radio which can operate in RX boosted gain setup or in RX power saving gain setup. In RX power saving gain, the radio will consume less power at small cost in RX sensitivity. In RX Boosted gain, the radio will consume more power to improve the RX sensitivity (this is preferred and default).

Note2: RM1262 HW RF tuned and capable of operating in both 902-928MHz, 863-870MHz, but RM1262 not certified for the 863-870MHz band and certified for 902-928MHz band countries (USA, Canada, Australia, New Zealand).

RM1261 HW RF tuned and capable of operating in both 902-928MHz, 863-870MHz, but RM1261 is certified for both 902-928MHz (Taiwan, Japan) and 863-870MHz band (India, CE, UKCA) countries.

Note 3: Sleep mode current assumes SX126x in SLEEP mode with warm start, config retained.

Note 4: For asynchronous interface like the EUART (asynchronous as the other end can communicate at any time), the EUART (on RM126x) must kept resulting in the base current consumption.

For synchronous interface like the I2C or SPI (when RM126x side is the master), the interface can be closed and opened only when needed resulting in current saving (no base current consumption penalty). There’s a similar argument for ADC (open ADC when needed).

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3.4 RF Specifications

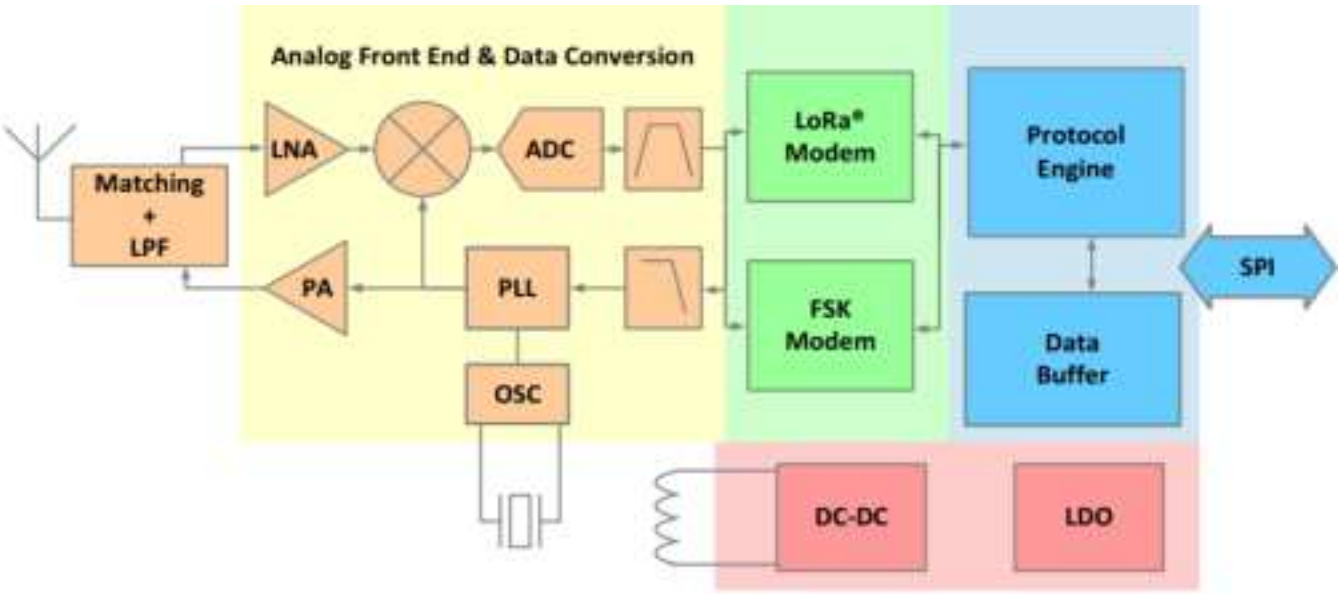

Figure 3: SX126X Block Diagram (from SX1261/SX1262 Datasheet)

The RM126x (RM1261 / RM1262) module uses SX1261 /SX1262 LoRa transceivers capable of low power operation in the case of RM126x operated in 863-870 and 902-928MHz frequency bands. The radio comprises four main blocks:-

- **RF front end**: RF transmit and receive chains (including channel filters) interface to digital blocks. The last stage of transmit chain is different between SX1261 and SX1262. The (RM1261) SX1261 transceiver capable of outputting 14/15dBm maximum RF TX output power under DCDC convertor or LDO supply. The (RM1262) SX1262 transceiver capable of RF TX power of 22dBm under external supply (3.3V minimum to get 22dBm). The rest of the SX1262 powered by DCDC or LDO.
- **Digital Modem**: A range of modulations are available but the RM126x is designed and certified for:
  - LoRa 125kHz
  - LoRa 250kHz
  - LoRa 500kHz
  - FSK 50kbps
  - LR-FHSS (Long Range FHSS) Transmit mode - **not currently certified for the RM126x**

  as per the LoRaWAN RP002-1.0.3 LoRaWAN Regional Parameters specification and per countries radio regulatory certified.
- **Digital Interface and Control**: this comprises all payload data and protocol processing as well as access to configuration of the radio via the SPI interface.
- **Power Distribution**: two forms of voltage regulation, DC-DC or linear regulator LDO, are available depending upon the design priorities of the application.

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3.4.1 LoRa / FSK RF Transmit Power

Table 9: LoRa / FSK RF Transmit Power

Part	Maximum RF TX power conducted at MHF4 RF connector Typical	Conditions All VDD pins	Comment
RM1261	14/15dBm	2V to 3.6V	RF Transmit programmable 14dBm down to -17dBm in 1dB step.
RM1262	22dBm	3.3V to 3.6V. (3.3V min. for 22dBm).	RF Transmit programmable 22dBm down to -9dBm in 1dB step.
	22dBm – 2dB	2.7V	
	22dBm – 3dB	2.4V	
	22dBm – 6dB	2.0V	

The actual maximum RF TX power achieved per country radio regulatory certification are shown in Mandatory FW Requirements Related to Hardware.

- **SX126x Errata:** In AT firmware, all errata workarounds are implemented as per the SX1261/SX1262 Datasheet. For example, "Better Resistance of the SX1262 TX to Antenna Mismatch," if not patched, would result in 5dB to 6dB lower RF TX power due to antenna mismatch.

3.4.2 External antenna

The RM1261 supports a range of external antennas with up to peak antenna gain of 2.0dBi (863-879MHz). The RM1262 supports range of external antennas with up to peak antenna gain of 2.2dBi (902-928MHz). For more information, see 6.4 LoRa External Antenna Integration with RM126x.

3.4.3 32MHz TCXO LoRa SX126x radio clock

The LoRaWAN radio (SX1261 / SX1261) uses very accurate 32MHz TCXO (±1ppm at 25°C) which additionally reduces the frequency drift within a LoRa packet (longest LoRa packet is 2793.5ms) due to the temperature rise due to the RF power amplifier.

3.4.4 LoRa / FSK RF Receive Sensitivity vs Data Rate

Table 10 tabulates typical LoRaWAN RF receive sensitivity as a function of the LoRa data rate. The data rate is determined by the combination of bandwidth and spreading factor of the incoming LoRa signal. The data rates in the table are the LoRaWAN data rates used by the gateway when transmitting to the end device.

Table 10: Receive sensitivity vs LoRa or FSK data rate

	DR	Bit Rate [Bits/s]	BW [kHz]	SF	Conducted Rx Sensitivity [dBm]
RM126x1	8	980	500	12	-130.8
	13	21900	500	7	TBD
	0	250	125	12	-139.2
	5	5470	125	7	-125.6
	6	11000	250	7	-122.7
	7	50000	FSK	-	-109.0

Note the following:

- DR = LoRaWAN data rate
- Bit rate is the effective over the air bit rate
- BW is the bandwidth of the incoming LoRa transmission
- SF is the Spreading Factor of the incoming LoRa transmission

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4 EFR32 SoC Peripherals

The major RM126x series module functional blocks (peripherals inside EFR32) are shown in Figure 4.

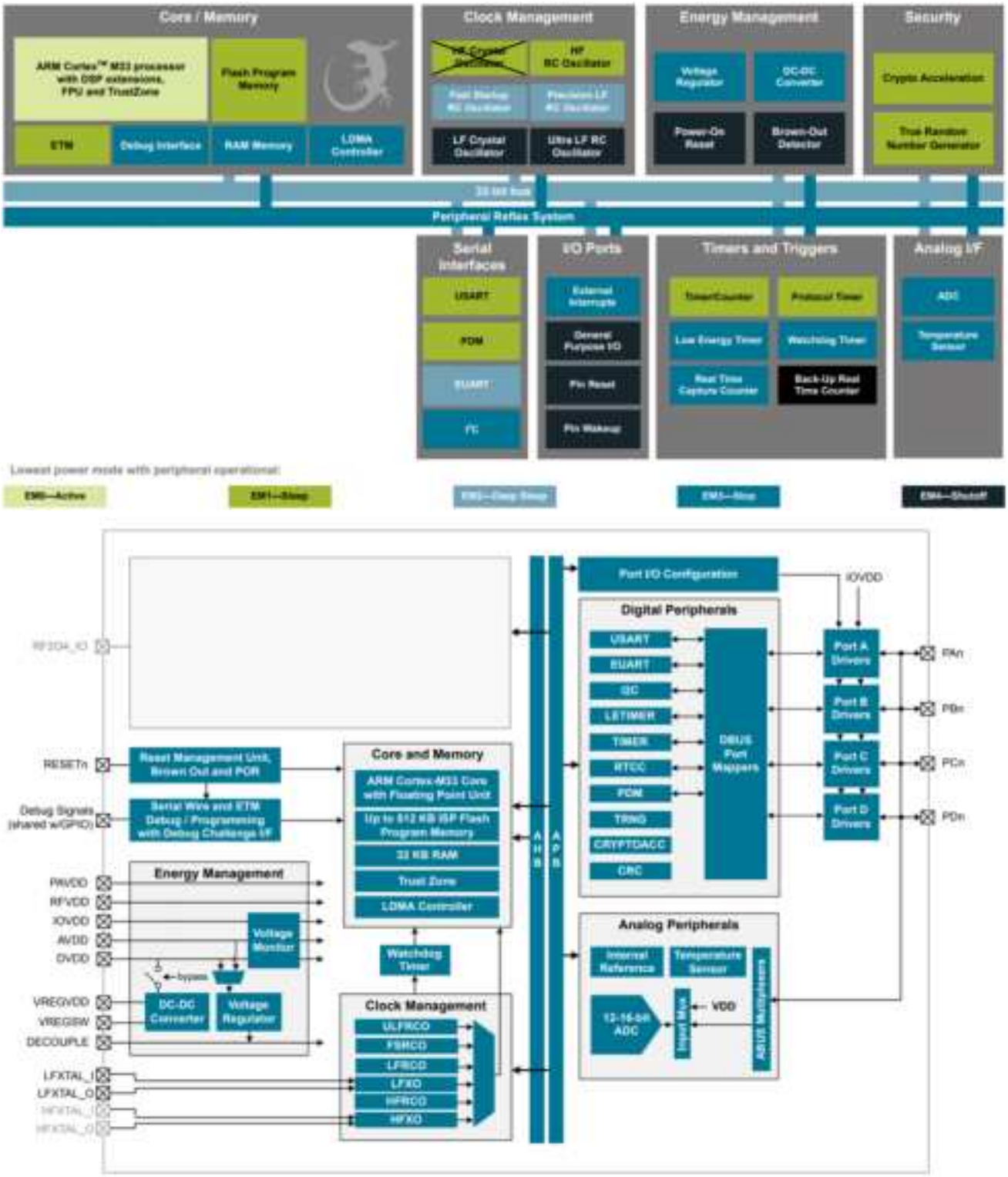

Figure 4: EFR32BG22 SoC peripherals and block diagram (from EFR32 datasheet)

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The available SoC peripherals include:

- ADC: 12-bit@1 Msps, 16-bit@76.9 ksps
- TBD x GPIO with output state retention and asynchronous interrupts
- 4 x 16-bit Timers/Counters with 3 compare/capture/PWM
- 1 x 32-bit Timers/Counters with 3 compare/capture/PWM
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- 2 x USART (UART/SPI/SmartCards(ISO7816)/IrDA/I2S)
- 1 x EUART (UART/IrDA)
- 2 x I2C peripheral interface with SMBus support
- Digital microphone interface (PDM)
- Die temperature sensor with ±1.5°C accuracy after single-point calibration
- 12 Channel Peripheral Reflex System

For details on their electrical performance, consult the relevant portions of Section 4 in the EFR32BG22 datasheet.

To learn which GPIO ports provide access to every peripheral, consult Analog Peripheral Connectivity and Digital Peripheral Connectivity in the EFR32BG22 datasheet.

4.1 Power Management (includes brown-out and power on reset)

Flexible Energy Management System:

- Five energy modules from EM0 to EM4 provide flexibility between higher performance and low power System Sleep /Deep Sleep modes
- Power DCDC or DCDC bypass control
- Voltage monitoring and brow out detection (Brownout Reset)
- Automatic voltage scaling for additional energy savings
- State retention
- Open/Close peripherals (UART, SPI, I2C, SIO's/GPIO's and ADC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption.
- Pin wake-up system from deep sleep
- Ultra efficient Power-on Reset (POR) and Brown-Out Detector (BOD).
- 2V to 3.65V supply range.

4.2 Clocks

4.2.1 76.8MHz HFRCO EFR32 SoC high frequency RC oscillator clock

The EFR32 SoC integrated high speed RC oscillator (HFRCO) is used for the RM126x module. The HFRCO employs fast startup at minimal energy consumption combined with wide frequency range from 1MHz to 76.8MHz.

4.2.2 32.768kHz LFXO EFR32 SoC low frequency crystal oscillator clock

The EFR32 SoC uses a high accuracy LXFO (+/-20 ppm at 25°C) 7pF load capacitor 32.768 kHz crystal (tuning fork) oscillator circuit. It provides an accurate protocol timing and helps with radio power consumption in the system sleep mode. The EFR32 LXFO block provides the load capacitance (EFR32 CAPTUNE) for the 32.768 kHz crystal (which is 7pF load capacitance tuning fork) to create the oscillator circuit. The RM126x optimised value (to account for PCB parasitics) for CAPTUNE is 19.08pF, which is equal to 32.668kHz crystal seeing 9.54pF (C_{LXFO}=CAPTUNE/2).

The EFR32 SoC LFRCO 32.768kHz RC oscillator is not used by the RM126x module as it has lower accuracy of ±500 ppm.

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4.3 General Purpose I/O, ADC and PWM/FREQ

4.3.1 GPIO

All SIO pins are configurable and can be accessed individually. Each has the following user configured features:

- Input/output direction (or tristate [reset state])
- More advanced configurations including open-drain and glitch-filtering can be configured for each individual GPIO pin
- All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.
- A few GPIOs also have EM4 wake functionality/EM4 IO retention (output enable, output value, pull enable, pull direction)

GPIO	Alternative Function		
PC00	GPIO.EM4WU6	GPIO.THMSW_EN	
PC05	GPIO.EM4WU7		
PC07	GPIO.EM4WU8		
PB03	GPIO.EM4WU4		
PA01	GPIO.SWCLK		
PA02	GPIO.SWDIO		
PA03	GPIO.SWV (this is SWO)	GPIO.TDO	GPIO.TRACEDA-TA0
PD02	GPIO.EM4WU9		

- Output drive strength (8mA)
- Internal pull-up and pull-down resistors (44kOhms typical) or no pull-up/down
- All GPIO pins are selectable as interrupts in EM0 and EM1
- All PA and PB GPIO pins are also selectable as interrupts down to EM2 and EM3
- All EM4 wake-up pins are also available as interrupts in EM0/1/2/3

4.3.2 Timer / Counter and PWM

The TIMER (Timer/Counter) is not configurable with AT.

The TIMER (Timer/Counter) keeps track of timing and counts events, generates output waveforms, and triggers timed actions in other peripherals.

The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes:

- **Capture mode**: The counter state is stored in a buffer at a selected input event.
- **Compare mode**: The channel output reflects the comparison of the counter to a programmed threshold value.
- **PWM mode**: The TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition, some timers offer dead-time insertion for motor control applications.

Refer to the EFR32BG22 datasheet to determine the capabilities (capture/compare channel count, width, and DTI) of each timer instance.

Refer to the EFR32BG22 datasheet also for Low Energy Timer (LETIMER), Real Time Clock with Capture (RTCC), Back-up Real Time Counter (BURTC), Watchdog Timer (WDOG).

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4.4 Communications and other Digital peripherals

4.4.1 EUART Interface

The Enhanced Universal Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485 and IrDA support. In EM0 and EM1 the EUART provides a high-speed, buffered communication interface.

Two-way hardware flow control is implemented by EUART_RTS and EUART_CTS. EUART_RTS is an output and EUART_CTS is an input. Both are active low.

These signals operate according to normal industry convention. EUART_RX, EUART_TX, EUART_CTS, EUART_RTS are all CMOS logic levels that track VDD. For example, when RX and TX are idle they sit at a high logic level (VDD). Conversely for handshaking pins CTS, RTS at 0 V is treated as an assertion.

The module communicates with the customer application using the following signals (Figure 5):

- Port /TXD of the application sends data to the module's EUART_RX signal line
- Port /RXD of the application receives data from the module's EUART_TX signal line

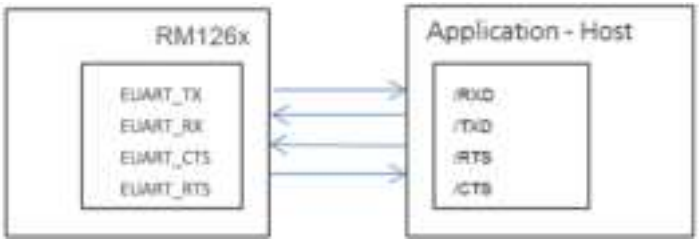

Figure 5: EUART Signals

Some serial implementations link CTS and RTS to remove the need for handshaking. Laird does not recommend linking CTS and RTS other than for testing and prototyping. If these pins are linked and the host sends data at the point that the RM126x deasserts its RTS signal, then there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This will drop the connection and may require a power cycle to reset the module. Laird Connectivity recommends that the correct CTS/RTS handshaking protocol be adhered to for proper operation.

Table 11: EUART Interface (on DVK-RM126x)

Pin #	Pin name	Pin Name when using AT Firmware	I/O State	Pin Name when customers using own FW - Native C development
18	PC07	EUART_TX	Output, set high	I2C0/I2C1/AN/FREQ/PWM/EUART0/USART0/PDM
32	PB04	EUART_CTS	Input, pull-down	I2C0/AN/FREQ/PWM/EUART0/USART0/USART1/PDM
33	PB03	EUART_RX	Input, pull-up	I2C0/AN/FREQ/PWM/EUART0/USART0/USART1/PDM
34	PB02	EUART_RTS	Output, set low	I2C0/AN/FREQ/PWM/EUART0/USART0/USART1/PDM

The EUART interface is also used to interface with host microcontroller.

Alternatively, on the same pins USART0 can be used (instead of SPI) for interfacing to host (with customers own firmware).

4.4.2 SPI Bus (alternative USART0)

The SPI interface is an alternate function on any SIO pins.

The module is a master device that uses terminals SPI_CIPO, SPI_COPI and SPI_CLK (also called SPI_MISO, SPI_MOSI, SPI_CLK). SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping.

The SPI interface enables full duplex synchronous communication between devices. It supports a three-wire (SPI_CIPO, SPI_COPI and SPI_CLK) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals are necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double buffered.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

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Table 12: SPI interface (on DVK-RM126x)

Pin #	Pin name	Pin Name when using AT Firmware	IO state when SPI	Pin Name when customers using own FW - Native C development	Comment
5	PD02	SIO07/I2C1/AN/FREQ/PWM/ **SPI_CIPO**	**Input**	I2C0/I2C1/AN/FREQ/PWM/EUART0/USART0/ PDM	MIKROE_SPI_MISO on DVK-RM126x
6	PD03	SIO06/I2C1/AN/FREQ/PWM/ **SPI_COPI**	**Output**	I2C0/I2C1/AN/FREQ/PWM/EUART0/USART0/ PDM	MIKROE_SPI_MOSI on DVK-RM126x
17	PC00	SIO00/I2C1/AN/FREQ/PWM/ **SPI_CLK**	**Output**	I2C0/I2C1/AN/FREQ/PWM/EUART0/USART0/ PDM	MIKROE_SPI_SCK on DVK-RM126x
16	PC01	SIO01/I2C1/AN/FREQ/PWM	**Output**	I2C0/I2C1/AN/FREQ/PWM/EUART0/USART0/ PDM	MIKROE_SPI_CS on DVK-RM126x

When customer using own firmware, these SPI bus pins alternatively can be used for bringing out USART0 or I2C0.

USART0 Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I2S

4.4.3 I2C Interface

The I2C interface is an alternate function on any SIO pins.

The I2C module provides an interface between the host MCU and a serial I2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode (100kbps), fast-mode (400kbps) and fast-mode plus (1Mbps) speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Note that not all instances of I2C are available in all energy modes.

The two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and an I2C interface allows multiple masters and slaves to communicate over a shared wired-OR type bus consisting of two lines which normally sit at VDD. As a true multi-leader bus it includes collision detection and arbitration to resolve situations where multiple leaders transmit data at the same time without data loss. The SCL is the clock line which is always sourced by the master and SDA is a bi-directional data line which can be driven by any device on the bus.

Each device on the bus is addressable by a unique address, and an I2C leader can address all the devices on the bus, including other leaders.

Both the bus lines are open-drain. The maximum value of the pull-up resistor can be calculated as a function of the maximal rise-time tr for the given bus speed, and the estimated bus capacitance Cb as shown in I2C pull-up resistor equation:

Rp(max) = tr /(0.8473 x Cb)

The maximal rise times for 100 kHz, 400 kHz and 1 MHz I2C are 1 µs, 300 ns and 120 ns respectively.

Note: The GPIO slew rate control should be set for the desired slew rate.

Note: If VDD drops below the voltage on SCL and SDA lines, the host MCU could become back powered and pull the SCL and SDA lines low.

IMPORTANT: It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.

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Table 13: I2C Interface (on DVK-RM126x)

Pin #	Pin name	Pin Name when using AT Firmware	I/O State	Pin Name when customers using own FW - Native C development	Comment
5	PD02	SIO07/**I2C1**/AN/FREQ/PWM/SPI_CIPO	I/O	I2C0/I2C1/AN/FREQ/PWM/EUART0/ USART0/PDM	MIKROE_I2C_SCL on DVK-RM126x
6	PD03	SIO06/**I2C1**/AN/FREQ/PWM/SPI_COPI	I/O	I2C0/I2C1/AN/FREQ/PWM/EUART0/ USART0/PDM	MIKROE_I2C_SDA on DVK-RM126x

4.4.4 Pulse Density Modulation (PDM) interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

4.5 Analog

4.5.1 Incremental Analog to Digital Convertor (IADC)

The ADC is an alternate function on any SIO pins, configurable.

The ADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style convertors. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

4.5.1.1 Incremental Analog To Digital Convertor (IADC)

Table 14: Analog interface (on DVK-RM126x)

Pin #	Pin name	Pin Name when using AT Firmware	I/O State	Pin Name when customers using own FW - Native C development	Comment
15	PC02	SIO02/I2C1/**AN**/FREQ/PWM	I	I2C0/I2C1/AN/FREQ/PWM/EUART0/USART0/PDM	MIKROE_ANALOG on DVK-RM126x

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used, positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins.

Table 16: ABUS Routing Table

Peripheral	Signal	GPIO port PA		GPIO port PB		GPIO port PC		GPIO port PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

4.5.2 Temperature Sense

Die temperature sensor with +/-1.5 degree C accuracy after single-point calibration.

For details on their electrical performance, consult the relevant portions of Section 4 in the EFR32BG22 datasheet.

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4.6 nRESET Pin

Table 15: nRESET pin

Pin #	Pin name	Pin Name when using AT Firmware	I/O State	Pin Name when customers using own FW	Comment
20	RESETn	RESETn	Input, pull-up	RESETn	System Reset (Active low). 1.8V IO voltage only. Internally pulled to 1.8V. Pull the RESETn pin low for minimum 100nS in order for the RM126x to reset.

4.7 Two-pin Serial-Wire Debug (SWD) Programming/Debug Interface

The EFR32xG22 devices include hardware debug support through a 2-pin serial-wire debug (SWD) interface. There is also Serial Wire Viewer (SWO or SWV) pin which can be used to output profiling information, data trace and software-generated messages.

Pin #	Pin name	Pin Name when using AT Firmware	I/O State	Pin Name when customers using own FW	Comment
37	PA01	SWCLK	Input, pull-down	I2C0/AN/FREQ/PWM/EUART0/USART0/USART1/SWCLK/PDM	
38	PA02	SWDIO	Input/ Output, pull-up	I2C0/AN/FREQ/PWM/EUART0/USART0/USART1/SWDIO/PDM	
39	PA03	SWO		I2C0/AN/FREQ/PWM/EUART0/USART0/USART1/SWO/PDM	

Serial Wire Clock Input and Test Clock Input (SWCLKTCK) (SWCLK): This pin is enabled after power-up and has a built-in pull-down.

Serial Wire Data Input/Output and Test Mode Select Input (SWDIOTMS) (SWDIO): This pin is enabled after power-up and has a built-in pull-up.

Serial Wire Viewer (SWV): This pin is disabled after reset.

The EFR32xG22 also has JTAG interface.

The connector for the (2-Wire SWD Programming/Debug Interface) MPN is as follows:

Reference	Value	Description	Manufacturer part number, Manufacturer
P201 Note1	N146-T-10-2-56-H0	CON, SMT, Header, 2x5, Pitch 1.27mm, Vertical, 2 rows	N146-T-10-2-56-H0, Kingmate or any equivalent

Note 1: Reference the RM126x development board schematic. Figure 6 shows the wiring for the 2-Wire SWD Programming/Debug Interface connector and RM126x module 2-Wire SWD Programming/Debug Interface pins.

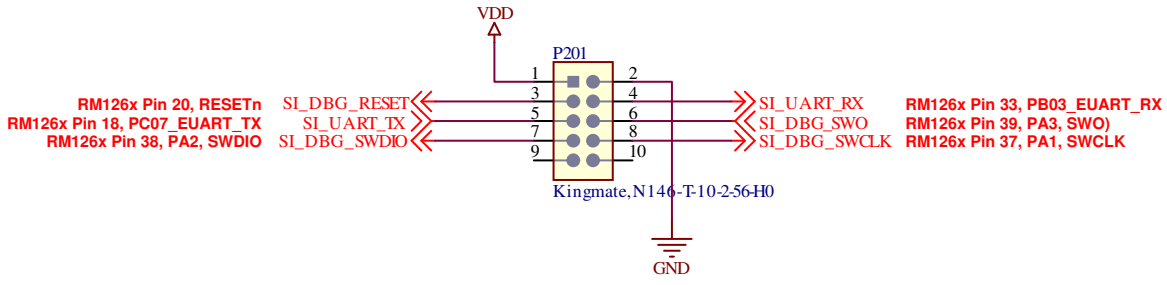

Figure 6: Wiring for 2-Pin SWD Programming/Debug Interface connector to SWD Programming/Debug interface on RM126x module

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5 PROGRAMMABILITY

5.1 AT Application firmware

The RM126x family of modules ship with a factory programmed Bootloader and AT Interface application firmware image. Updates to the AT Interface application are signed to prevent malicious updates. The update files are provided by Laird Connectivity and must be programmed via the factory programmed Bootloader. The Bootloader implements Silabs' BGAPI protocol, which is further described in the Silabs Application Note **AN1086**. A UART DFU application is provided by Laird Connectivity at **[link needed]** to facilitate update of the module firmware via a Windows based host PC.

The AT Application firmware incorporates the following elements.

- **AT Command parser** – This is the interface to the host that processes incoming AT commands and sends response details to the host.
- **AT commands** – These are the individual AT command handlers.
- **Semtech Basics Modem Lora Stack** – This is the Semtech LoRa stack used to interact with the LoRaWAN. The stack has been tailored for the RM126x module by Laird Connectivity. The original version is provided by Semtech via a **Github** page.
- **Regulatory Protection Layer** – This is the RM126x bespoke driver layer for the RM126x module to ensure radio regulatory requirements are complied with. This will prevent network server requested transmit powers or frequencies violating regulatory stipulated limits.
- **Silabs Gecko SDK v4.1.3** – This is Silabs Gecko SDK used for interacting with the underlying EFR32 SoC.

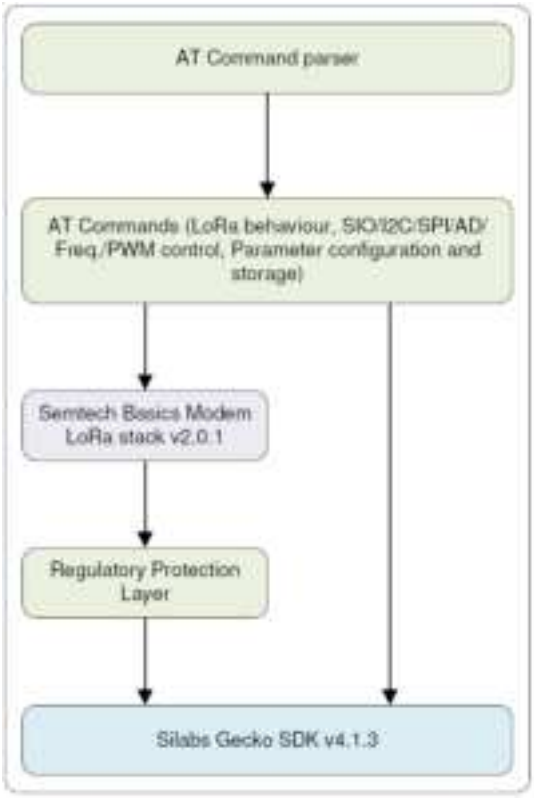

Figure 7: Firmware block diagram - AT firmware

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5.2 Native C Development

The RM126x family of modules can also be programmed with bespoke customer applications. In this case, the part must first be erased. This will remove the factory programmed Bootloader and AT Interface application images and disable readback protection of the part.

Silabs' Simplicity Studio and Gecko SDK can then be used to implement an end user specific Bootloader and Application image. SWD is recommended for debug and programming during development, and a bespoke Bootloader for field upgrade once the application is finalized and released.

When implementing a LoRaWAN based application, the RM126x **Regulatory Protection Layer MUST be used by the end user application to ensure RM126x radio regulatory compliance**. This is provided by Laird Connectivity, in addition to sample applications, at www.lairdconnect.com/rm126x-series. All code is provided in a Silabs Gecko SDK extension. These are further described in the Silabs Gecko SDK Extensions User Guide **UG520**.

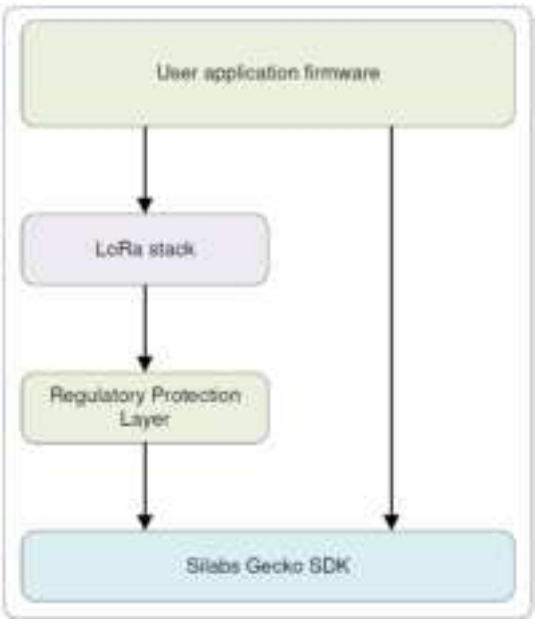

Figure 8: Firmware block diagram - native C development

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5.3 Mandatory FW Requirements Related to Hardware

To be within the certified RM126x radio regulatory per country the below sections cover maximum RF TX power achieved and the frequency band (start and stop channel) allowed (passed) per country and the associated RF TX power register values (paDutyCycle, hpMax, Value in SetTxParams), RampTime register value and some others registers related to TCXO, LNA etc… These are what is referred to as the radio's "Regulatory Protection Layer" in Programmability section.

5.4 Certified Max RF TX power and Frequency Bands per Country

Table 16 shows the maximum radio regulatory certified RF TX power and frequency band (TX and RX) (first and last channel (center frequency) per country and supported LoRaWAN regional parameters supported per country.

Note: Countries are color-coded for easier identification between Table 16, Table 17, and Table 18.

Table 16: Max RF TX Power and frequency bands per country

Part	Regulatory Country see NOTE1	LoRaWAN Regional Parameters	Certified Frequency band		Certified Max. Conducted TX power setting	Max. Certified Peak Antenna Gain
			Frequency band (channel centre)	Modulation		
RM1262	FCC(USA) / ISED(Canada)	US902-928	902.3-914.9MHz 903.0-914.2MHz	LoRa 125kHz LoRa 500kHz	22dBm	2.2dBi peak
RM1262	AUSTRALIA	AU15-928 as Main	915.2-927.8MHz 915.9-927.1MHz	LoRa 125kHz LoRa 500kHz	22dBm	2.2dBi peak
RM1262	AUSTRALIA	AS923 as alternative	915.2-927.8MHz 915.3-927.7MHz 915.2-927.8MHz	LoRa 125kHz LoRa 250kHz FSK 50kbps	22dBm	2.2dBi peak
RM1262	NEW ZEALAND	AS923 as Main	915.6-927.6MHz 915.9-927.7MHz 915.6-927.8MHz	LoRa 125kHz LoRa 250kHz FSK 50kbps	14dBm	2.2dBi peak
RM1262	NEW ZEALAND	AU15-928 as Alternative	915.6-927.6MHz 920.7-925.5MHz	LoRa 125kHz LoRa 500kHz	14dBm	2.2dBi peak
RM1261	TAIWAN (NCC)	AS923	920.2-924.8MHz 920.3-924.7MHz 920.2-924.8MHz	LoRa 125kHz LoRa 250kHz FSK 50kbps	14dBm	2.2dBi peak
RM1261	JAPAN (MIC)	AS923 with LBT	920.6-923.4MHz 920.7-923.3MHz 920.6-923.4MHz	LoRa 125kHz LoRa 250kHz FSK 50kbps	12dBm	2.2dBi peak
RM1261	INDIA	IN865-867	865.0625-867.9375MHz	LoRa 125kHz FSK 50kbps	13dBm	2.0dBi peak
RM1261	EU (CE), UKCA	EU863-868 per sub-band	**H1.3**			2.0dBi peak
			863.1-864.9MHz	LoRa 125kHz, FSK 50kbps	13dBm, 0.1%	
			863.2-864.8MHz	LoRa 250kHz		
			H1.4			
			865.1-867.9MHz	LoRa 125kHz, FSK 50kbps	13dBm, 1%	
			865.2-867.8MHz	LoRa 250kHz		
			H1.5			
			868.1-868.5MHz	LoRa 125kHz, FSK 50kbps	13dBm, 1%	
			868.2-868.4MHz	LoRa 250kHz		
			H1.6			

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Part	Regulatory Country see NOTE1	LoRaWAN Regional Parameters	Certified Frequency band		Certified Max. Conducted TX power setting	Max. Certified Peak Antenna Gain
			Frequency band (channel centre)	Modulation		
			868.8-869.1MHz	LoRa 125kHz, FSK 50kbps	13dBm, 0.1%	
			868.9-869MHz	LoRa 250kHz		
			H1.7			
			869.5-869.55MHz	LoRa 125kHz, FSK 50kbps	15dBm, 10%	
			H1.9			
			869.8-869.9MHz	LoRa 125kHz, FSK 50kbps	13dBm, 1%	

NOTE1: USA(FCC), Canada (ISED) – RM1262 declared as FHSS for LoRa 125kHz. DTS for LoRa 500kHz.
Australia, New Zealand – RM1262 declared as DTS.
Taiwan (NCC) - RM1261 declared as FHSS.
Japan - is Listen Before Talk for Japan. RM1261 declared as DTS.
India - RM1261 declared as DTS.
CE, UKCA - is Duty cycle limit control per sub-band. RM1261 declared as DTS.

The maximum RF TX power radio power table (and associated mandatory RF TX power register settings) and RampTime settings used for RM1261 and RM1262 (certifications and optimal performance) are shown in table xyz and zyx. These table also show the lower RF TX power in 1dB steps from maximum to minimum.

Table 17: RM1261 Radio RF TX power table registers values and RampTime value

Radio regulatory country and maximum	Part	Output Power	paDutyCycle	hpMax	deviceSel	paLut	Value in SetTxParams	RampTime
CE and UKCA (sub-band H1.7 only) maximum	RM1261	15dBm	0x05	0x00	0x01	0x01	14dBm	10us
Taiwan NCC maximum	RM1261	14dBm	0x04	0x00	0x01	0x01	14dBm	10us
India, CE and UKCA (sub-band H1.3, H1.4, H1.5, H1.6, H1.9) maximum	RM1261	13dBm	0x03	0x00	0x01	0x01	14dBm	10us
Japan maximum	RM1261	12dBm	0x05	0x00	0x01	0x01	12dBm	10us
	RM1261	11dBm	0x02	0x00	0x01	0x01	14dBm	10us
	RM1261	10dBm	0x01	0x00	0x01	0x01	14dBm	10us
	RM1261	9dBm	0x01	0x00	0x01	0x01	13dBm	10us
	RM1261	8dBm	0x00	0x00	0x01	0x01	13dBm	10us
	RM1261	7dBm	0x00	0x00	0x01	0x01	12dBm	10us
	RM1261	6dBm	0x01	0x00	0x01	0x01	9dBm	10us
	RM1261	5dBm	0x01	0x00	0x01	0x01	8dBm	10us
	RM1261	4dBm	0x00	0x00	0x01	0x01	8dBm	10us
	RM1261	3dBm	0x00	0x00	0x01	0x01	7dBm	10us
	RM1261	2dBm	0x00	0x00	0x01	0x01	6dBm	10us
	RM1261	1dBm	0x00	0x00	0x01	0x01	5dBm	10us
	RM1261	0dBm	0x01	0x00	0x01	0x01	2dBm	10us
	RM1261	-1dBm	0x01	0x00	0x01	0x01	1dBm	10us
	RM1261	-2dBm	0x00	0x00	0x01	0x01	1dBm	10us

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Radio regulatory country and maximum	Part	Output Power	paDutyCycle	hpMax	deviceSel	paLut	Value in SetTxParams	RampTime
	RM1261	-3dBm	0x01	0x00	0x01	0x01	-1dBm	10us
	RM1261	-4dBm	0x01	0x00	0x01	0x01	-2dBm	10us
	RM1261	-5dBm	0x01	0x00	0x01	0x01	-3dBm	10us
	RM1261	-6dBm	0x01	0x00	0x01	0x01	-4dBm	10us
	RM1261	-7dBm	0x02	0x00	0x01	0x01	-6dBm	10us
	RM1261	-8dBm	0x02	0x00	0x01	0x01	-7dBm	10us
	RM1261	-9dBm	0x02	0x00	0x01	0x01	-8dBm	10us
	RM1261	-10dBm	0x00	0x00	0x01	0x01	-7dBm	10us
	RM1261	-11dBm	0x00	0x00	0x01	0x01	-8dBm	10us
	RM1261	-12dBm	0x00	0x00	0x01	0x01	-9dBm	10us
	RM1261	-13dBm	0x03	0x00	0x01	0x01	-13dBm	10us
	RM1261	-14dBm	0x03	0x00	0x01	0x01	-11dBm	10us
	RM1261	-15dBm	0x03	0x00	0x01	0x01	-15dBm	10us
	RM1261	-16dBm	0x00	0x00	0x01	0x01	-14dBm	10us
	RM1261	-17dBm	0x00	0x00	0x01	0x01	-15dBm	10us

Table 18: Certified RM1262 Radio RF TX power table registers values and RampTime value

Radio regulatory country and maximum	Part	Output Power	paDutyCycle	hpMax	deviceSel	paLut	Value in SetTxParams	RampTime
USA(FCC), Canada(ISED), Australia	RM1262	22dBm	0x04	0x07	0x00	0x01	22dBm	10us
	RM1262	21dBm	0x03	0x07	0x00	0x01	22dBm	10us
	RM1262	20dBm	0x03	0x06	0x00	0x01	22dBm	10us
	RM1262	19dBm	0x04	0x04	0x00	0x01	22dBm	10us
	RM1262	18dBm	0x01	0x05	0x00	0x01	22dBm	10us
	RM1262	17dBm	0x00	0x05	0x00	0x01	22dBm	10us
	RM1262	16dBm	0x02	0x03	0x00	0x01	22dBm	10us
	RM1262	15dBm	0x01	0x03	0x00	0x01	22dBm	10us
New Zealand maximum	RM1262	14dBm	0x03	0x02	0x00	0x01	22dBm	10us
	RM1262	13dBm	0x02	0x02	0x00	0x01	22dBm	10us
	RM1262	12dBm	0x01	0x02	0x00	0x01	22dBm	10us
	RM1262	11dBm	0x00	0x02	0x00	0x01	22dBm	10us
	RM1262	10dBm	0x04	0x01	0x00	0x01	22dBm	10us
	RM1262	9dBm	0x03	0x01	0x00	0x01	22dBm	10us
	RM1262	8dBm	0x02	0x01	0x00	0x01	22dBm	10us
	RM1262	7dBm	0x01	0x01	0x00	0x01	22dBm	10us

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Radio regulatory country and maximum	Part	Output Power	paDutyCycle	hpMax	deviceSel	paLut	Value in SetTxParams	RampTime
	RM1262	6dBm	0x00	0x01	0x00	0x01	22dBm	10us
	RM1262	5dBm	0x00	0x02	0x00	0x01	18dBm	10us
	RM1262	4dBm	0x00	0x01	0x00	0x01	21dBm	10us
	RM1262	3dBm	0x01	0x01	0x00	0x01	20dBm	10us
	RM1262	2dBm	0x02	0x01	0x00	0x01	19dBm	10us
	RM1262	1dBm	0x00	0x01	0x00	0x01	20dBm	10us
	RM1262	0dBm	0x01	0x01	0x00	0x01	14dBm	10us
	RM1262	-1dBm	0x00	0x01	0x00	0x01	15dBm	10us
	RM1262	-2dBm	0x00	0x01	0x00	0x01	12dBm	10us
	RM1262	-3dBm	0x03	0x01	0x00	0x01	8dBm	10us
	RM1262	-4dBm	0x00	0x01	0x00	0x01	10dBm	10us
	RM1262	-5dBm	0x00	0x01	0x00	0x01	8dBm	10us
	RM1262	-6dBm	0x01	0x01	0x00	0x01	7dBm	10us
	RM1262	-7dBm	0x00	0x01	0x00	0x01	7dBm	10us
	RM1262	-8dBm	0x01	0x01	0x00	0x01	4dBm	10us
	RM1262	-9dBm	0x01	0x01	0x00	0x01	3dBm	10us

5.5 Other Mandatory Radio Settings (Sx126x)

RM126x SX126x register name	RM126x Default Mandatory register value	Notes
Lna_cap_tune_n Register Address 0x08E3 Bits [3:0]	b'100' / 0x4 / 0.2pF	
Lna_cap_tune_p Register Address 0x08E4 Bits [7:4]	b'100 0000' / 0x40 / 0.2pF	
Tcxo_voltage	1.8V	WARNING: LoRa radio may not start or be out of specification if tcxo_voltage less than 1.8V is set.
Tcxo_delay	5ms	

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5.6 EFR32 Low Frequency crystal oscillator (LXFO) settings

See section 32.768kHz LFXO EFR32 SoC low frequency crystal oscillator clock, the mandatory LXFO register settings are shown below in table 19.

Table 19: Mandatory LXFO register settings

RM126x EFR32 SoC LXFO register name	RM126x Default Mandatory LXFO register value	Notes
GAIN	1	Mandatory
CAPTUNE	19.08pF	Mandatory RM126x optimised value (to account for PCB parasitics) for CAPTUNE is 19.08pF which is equal to 32.668kHz crystal seeing 9.54pF (C_{LXFO}=CAPTUNE/2).
HIGH AMPLITUDE	0	Default, See section 4.11.2 Low Frequency Crystal Oscillator https://www.silabs.com/documents/public/data-sheets/efr32bg22-datasheet.pdf
AGC	1	Default, See section 4.11.2 Low Frequency Crystal Oscillator https://www.silabs.com/documents/public/data-sheets/efr32bg22-datasheet.pdf
STARTUP DELAY	7	Default, 7=32k cycles. See section 4.11.2 Low Frequency Crystal Oscillator https://www.silabs.com/documents/public/data-sheets/efr32bg22-datasheet.pdf

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6 Hardware Integration Suggestions

6.1 Reference Diagrams

6.1.1 RM126x with EUART Host

The RM126x can be controlled over the EUART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below.

For BOOT pin (for AT firmware only), see 3.3.3 BOOT pin.

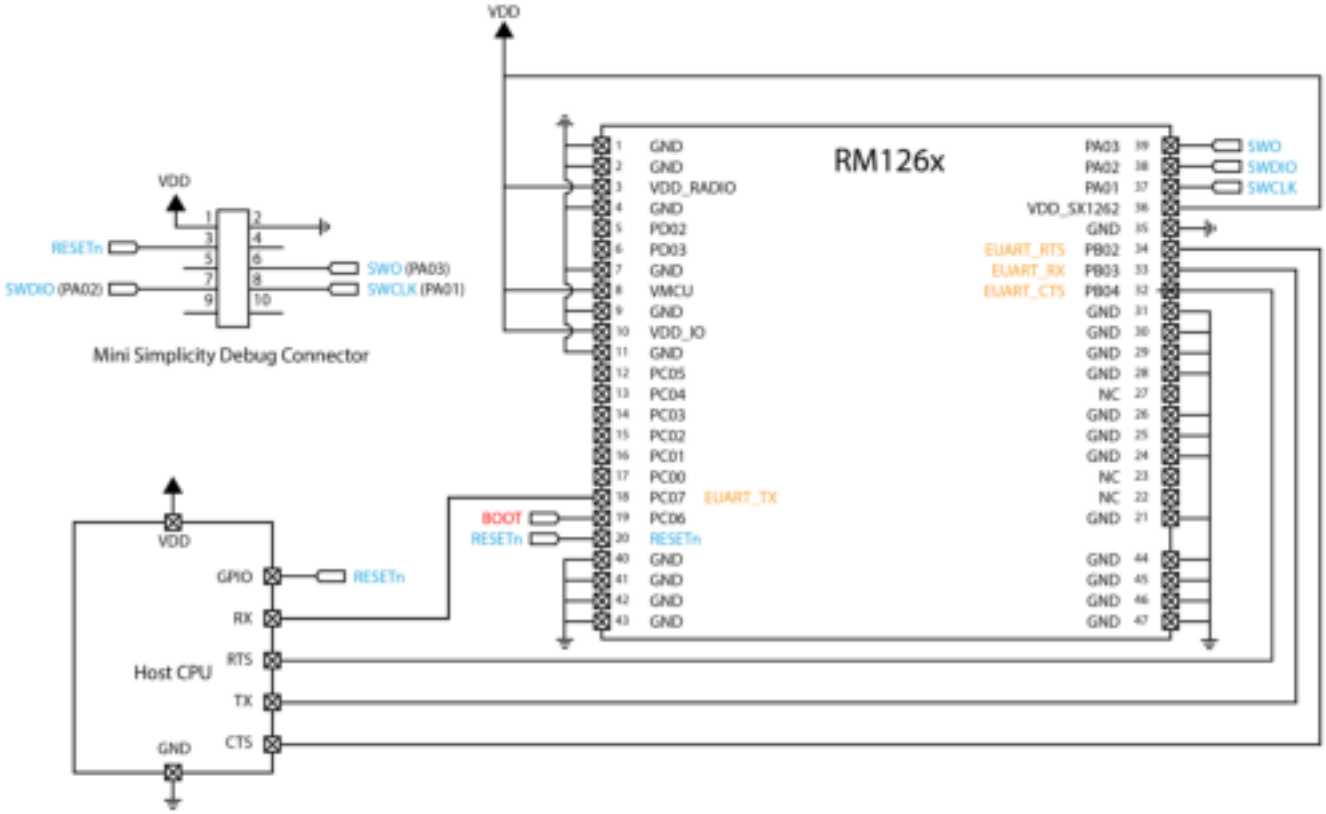

Figure 9: EUART Host Configuration

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6.1.2 RM126x standalone host-less

The RM126x can be used in a stand-alone configuration without an external host processor with firmware written by customer. Typical power supply and programming/debug interface connections are shown in the figure below.

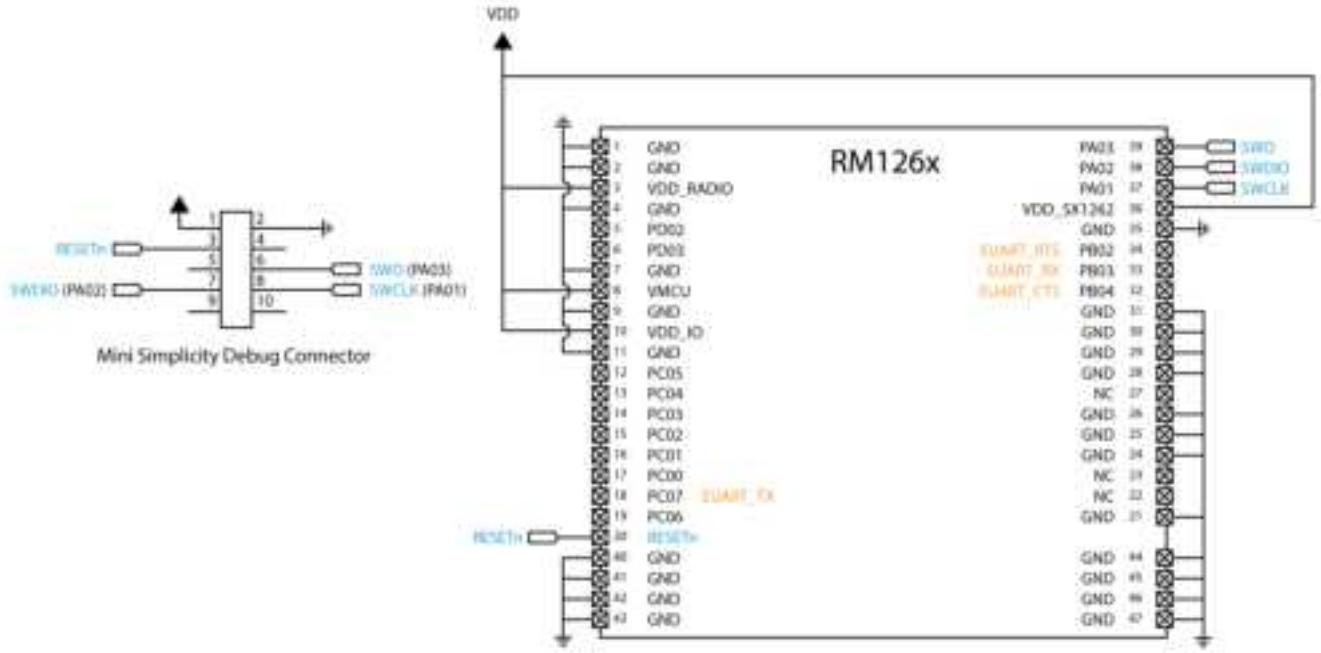

Figure 10: Standalone hostless configuration

6.2 Circuit

The RM126x-series module is easy to integrate requiring no external components on the customer's board apart from those required by customer for development and in customers end application.

Checklist (for Schematic):

- **VDD_RADIO, VDD_IO, VMCU, VDD_SX1262**

  RM1261: connect same external supply (2V-3.6V) voltage to RM161 pins VDD_RADIO, VDD_IO, VMCU. VDD_SX1262 can be left unconnected or can be connected to same external voltage (as internally not connected).

  RM1262: connect same external supply (2V-3.6V) voltage to RM161 pins VDD_RADIO, VDD_IO, VMCU, VDD_SX1262. If require RM1262 full RF TX power of 22dBm, then voltage MUST be 3.3V minimum (to 3.6V maximum).

  The module VDD pins should be chosen to optimize either range or power consumption and must be within the valid operating range and noise/ripple specification of RM126x. RM126x VDD pins should be tied together and decoupling capacitors for filtering should be added close to the module VDD pins for purpose of filtering noise/ripple from the customer host power supply. Upon application of power, the internal power-on reset ensures module starts correctly.

- **RESETn**

  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VDD pins. RESETn pin is pulled up to internal 1.8V. Therefore, RESETn pin input maximum is 1.8V only.

- **AN (ADC) and SIO pin IO voltage levels**

  RM126x SIO operating voltage levels are from 0V to VDD. Ensure input voltage levels into SIO do not exceed VDD also (if VDD source is a battery whose voltage will drop). Ensure ADC pin maximum input voltage for damage is not violated.

- **AN (ADC) impedance and external voltage divider setup**
  If one wanted to measure with ADC, a voltage higher than 3.6V then one can connect a high impedance voltage divider to lower the voltage to the ADC input pin. Other methods are to use a voltage buffer or FET transistor in conjunction with a low resistance voltage divider.
  Two-pin SWD Programming/Debug Interface

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Add 2-pin SWD Programming/Debug Interface as detailed in Two-pin Serial-Wire Debug (SWD) Programming/Debug Interface.

Required for upgrading firmware.

- **EUART**
  The EUART is required for customers host to use AT firmware. Add connector to allow UART to be interfaced to PC (via UART–RS232 or UART-USB). Cannot upgrade AT firmware via EUART.
- **EUART_RX and EUART_CTS**
  PB03 EUART_RX is an input, set with internal pull-up.
- PB04 EUART_CTS is an input, set with internal pull-down. This pull-down ensures the default state of the EUART_CTS will be asserted which means can send data out of the EUART_TX line. In the case when EUART_CTS is not connected (which we do not recommend).
- **BOOT pin (for AT firmware only)**
  BOOT pin is internally pulled-up to VDD (by default). Can be externally held high or low to select between the two RM126x modes at power-up:
  - Bootloader mode (BOOT pin held at 0V).
  - Application mode (BOOT pin held at VDD, default).
- Make provision to allow operation in the required mode. Add jumper to allow BOOT pin to be held high or low (via 10K resistor) OR driven by host GPIO.
- **I2C**
  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the RM126x module and MUST be provided external to the module as per I2C standard, see I2C Interface.
- **SPI / USART0**
  Implement SPI chip select using any unused SIO pin then SPI_CS is controlled allowing multi-dropping.
- **SIO pin direction**
  RM126x modules shipped from production loaded with AT firmware, all SIO pins with default Silabs “Disabled input”, see Pin Definitions Table 2. Change the direction of any SIO pin that is required to be an output in your design. This was done to avoid floating inputs (which can also cause current consumption in low power modes (e.g. Sleep) to drift with time.

6.3 PCB Layout on Host PCB – General

Checklist (for PCB):

- MUST locate RM126x module close to the edge of PCB (preferred for a radio for good floor planning)
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on the top layer can be flooded with copper but place GND vias regularly to connect copper flood to inner GND plane. If GND flood copper exists on the top PCB layer (under of the RM126x module), then connect with GND vias to inner GND plane and ensure that it is covered with solder mask.
- Route traces to avoid noise being picked up on supply pins, AIN (analogue) and GPIO (digital) traces.
- Ensure no exposed copper beneath the module (refer to land pattern of RM126x development board).
- An example is shown in Figure 11.

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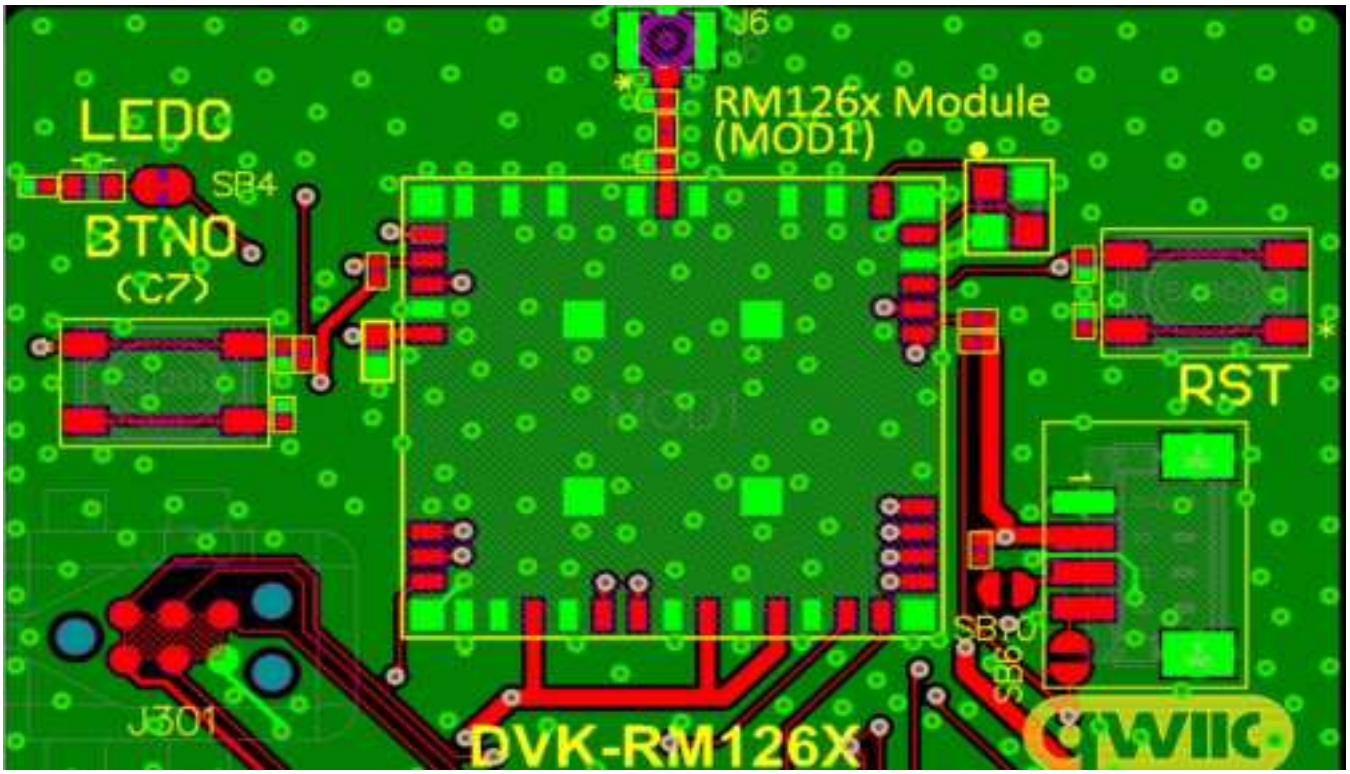

Figure 11: RM126x module PCB placement and grounding (shown in green) on DVK-RM126x PCB (part of DVK-RM126x PCB with RM126x module shown only) with RM126x module placed near the edge.

6.3.1 External Antenna Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40mm top/bottom and 30mm left or right.
- Metal close to the RM126x antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. How much; that is entirely system dependent which means some testing by customer required (in their host application).
- Anything metal closer than 20mm will start to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that the customer tests the Range with mock-up (or actual prototype) of the product to assess effects of enclosure height (and material whether metal or plastic).

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6.4 LoRa External Antenna Integration with RM126x

Please refer to the regulatory sections for details of use of RM126x with external antennas.

The RM126x has been designed to operate with the below external antennas (with a maximum gain of 2dBi for 868MHz band and 2.2dBi for 915MHz band). The required antenna impedance is 50 ohms. See Table 20.

Table 20: LoRa External antennas for the RM126x

Manufacturer	Manufacturer Part Number	Model	Dimension (mm)	Weight	Operating Temperature	Type	Connector	Peak Gain (dBi)	Frequency (MHz)
Embedded Antenna Design (EAD)	**FBKR35301-RS-KR**	BKR915	221 x 13	-	-	Dipole	RP-SMA	2.0	902-928
Chang Hong Information	**GSM-8696-2**	GSM-8696-2	200 x 13.7 x 13.7	30g	-	Dipole	RP-SMA	2.0	860-960
Linx	**ANT-916-OC-LG-RPS**	OC-LG Series	193.5 x 5.3 x 10	-	-20 to +85 °C	Dipole	RP-SMA	2.2	895-935
Linx	**ANT-868-OC-LG-RPS**	OC-LG Series	193.5 x 5.3 x 10	15g	-20 to +85 °C	Dipole	RP-SMA	0.4	862-876
Laird Connectivity	**EFB8555A3S-15MH4L**	800FlexPIFA	88 x 40 x 6.2	13g	-40 to +85 °C	PIFA	IPEX MHF4L	-1.1	863-870
Laird Connectivity	**EFB9020A3S-15MH4L**	900FlexPIFA	88 x 40 x 6.2	11g	-40 to +85 °C	PIFA	IPEX MHF4L	-0.1	902-928
Laird Connectivity	**EFG8555A3S-15MH4L**	i-800FlexPIFA	88 x 40 x 6.2	18g	-40 to +85 °C	PIFA	IPEX MHF4L	-0.4	863-870
Laird Connectivity	**EFG9020A3S-15MH4L**	i-900FlexPIFA	88 x 40 x 6.2	17g	-40 to +85 °C	PIFA	IPEX MHF4L	0.5	902-928
Laird Connectivity	**EFH8631A3S-10MH4L**	868/915MHz FlexDIPOLE	75.8 x 13.75 x 0.1	-	-40 to +85 °C	Flexible Planar Dipole	IPEX MHF4L	1.9	863-870
								2.4	902-928

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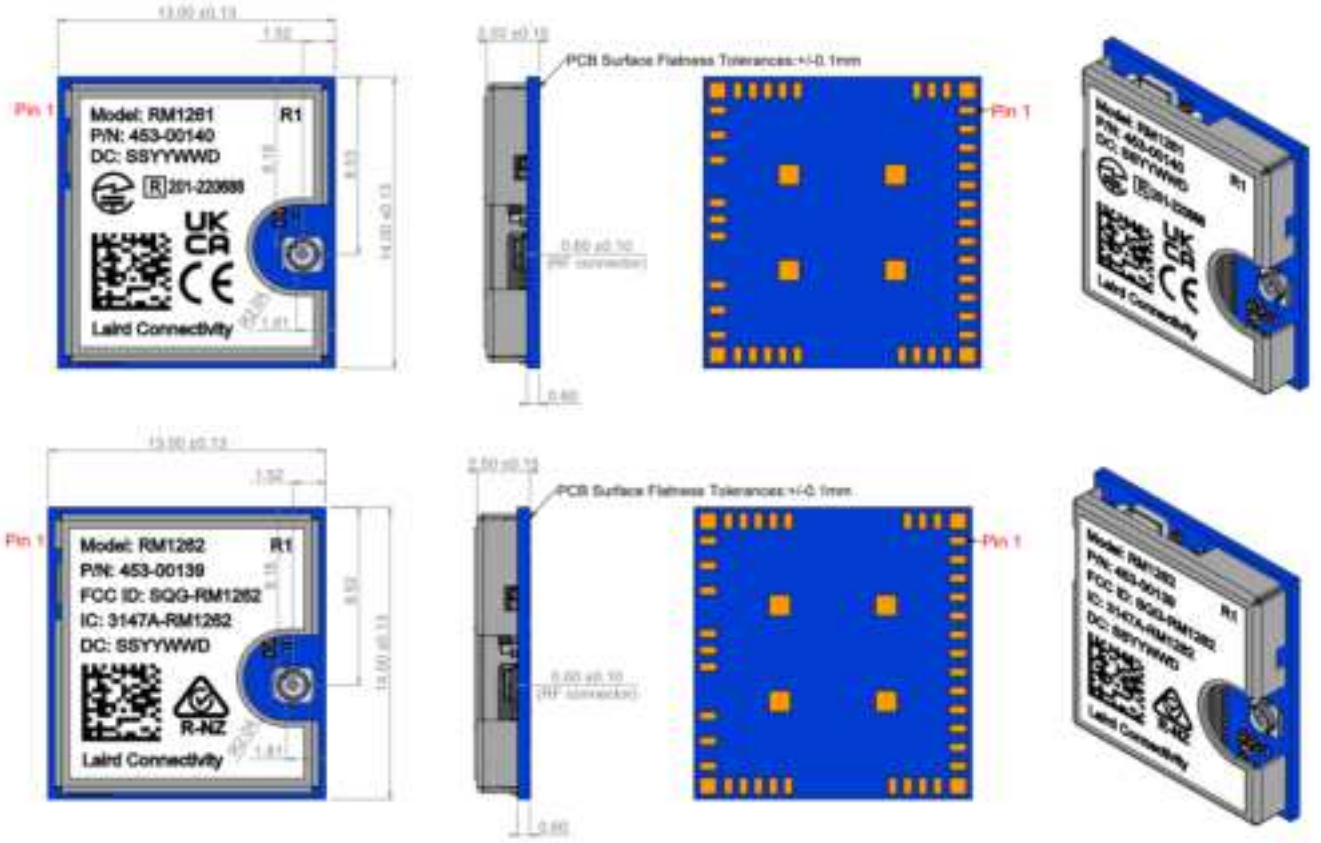
7 MECHANICAL DETAILS

7.1 RM126x Mechanical Details



Note: Dimensions in mm.

Center of RF shield can opening (over MHF4 RF connector) is located 1.52 mm horizontally and 8.53 mm vertically from top right hand corner of module.

Figure 12: RM126x Mechanical drawings

Development Kit Schematics can be found in the Documentation tab of the RM126x product page:
https://www.lairdconnect.com/wireless-modules/lorawan-modules-solutions/rm126x-ultra-low-power-lorawan-a-b-c-module

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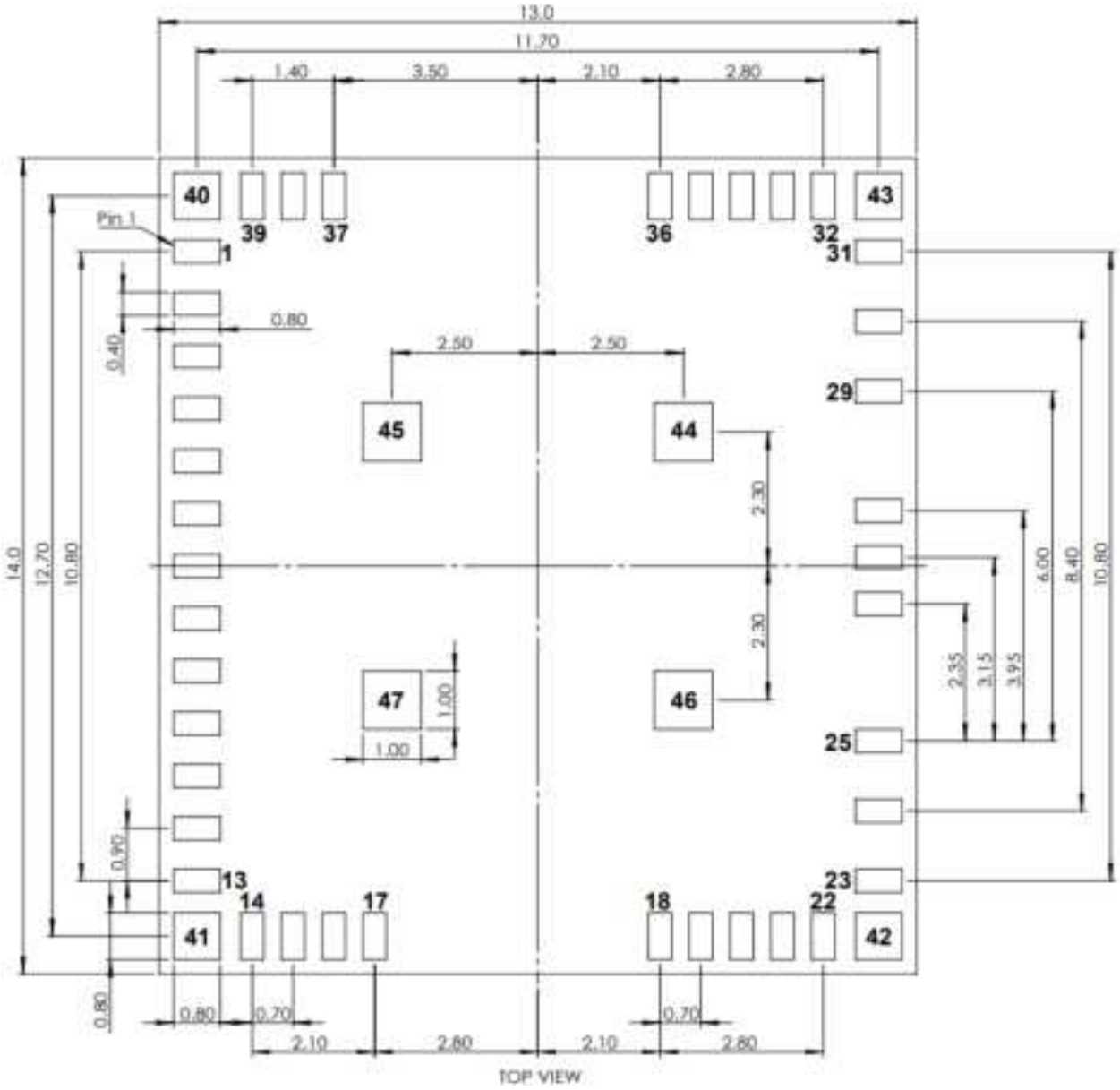
7.2 Host PCB Land Pattern for RM126x



SCH symbols (Altium format) and PCB footprints (DXF and Altium) format can be found on RM126x product page https://www.lairdconnect.com/wireless-modules/lorawan-modules-solutions/rm126x-ultra-low-power-lorawan-a-b-c-module

Notes:
1. RM126x development board has an RM126x placed on the edge of the PCB board (see section Host PCB Land Pattern for RM126x. This was used for module development and external antenna performance evaluation.
2. Ensure no exposed copper under module on host PCB.
3. The user may modify the PCB land pattern dimensions based on their experience and / or process capability.

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8 APPLICATION NOTE FOR SURFACE MOUNT MODULES

8.1 Introduction

Laird Connectivity's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the User Manual. This Application Note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of a number of commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

8.2 Shipping

There are 1,000 x RM126x modules taped in a reel (and packaged in a pizza box) and five boxes per carton (5000 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels.

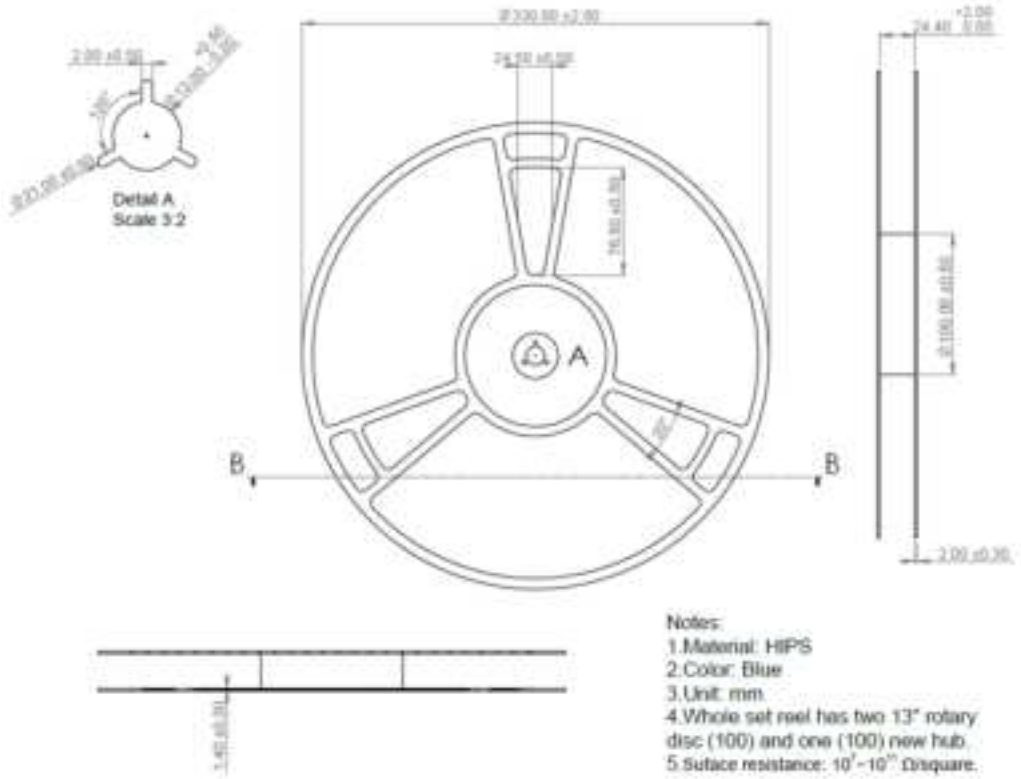

Figure 13 Reel Specifications

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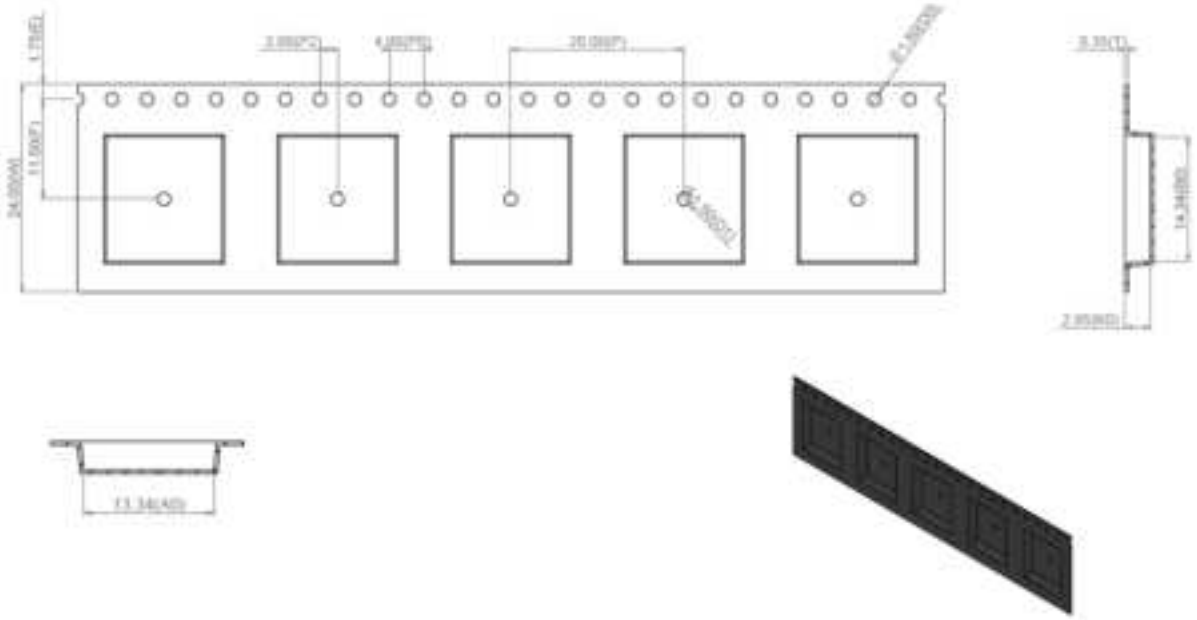

Figure 14: RM126x Carrier Tape Specifications

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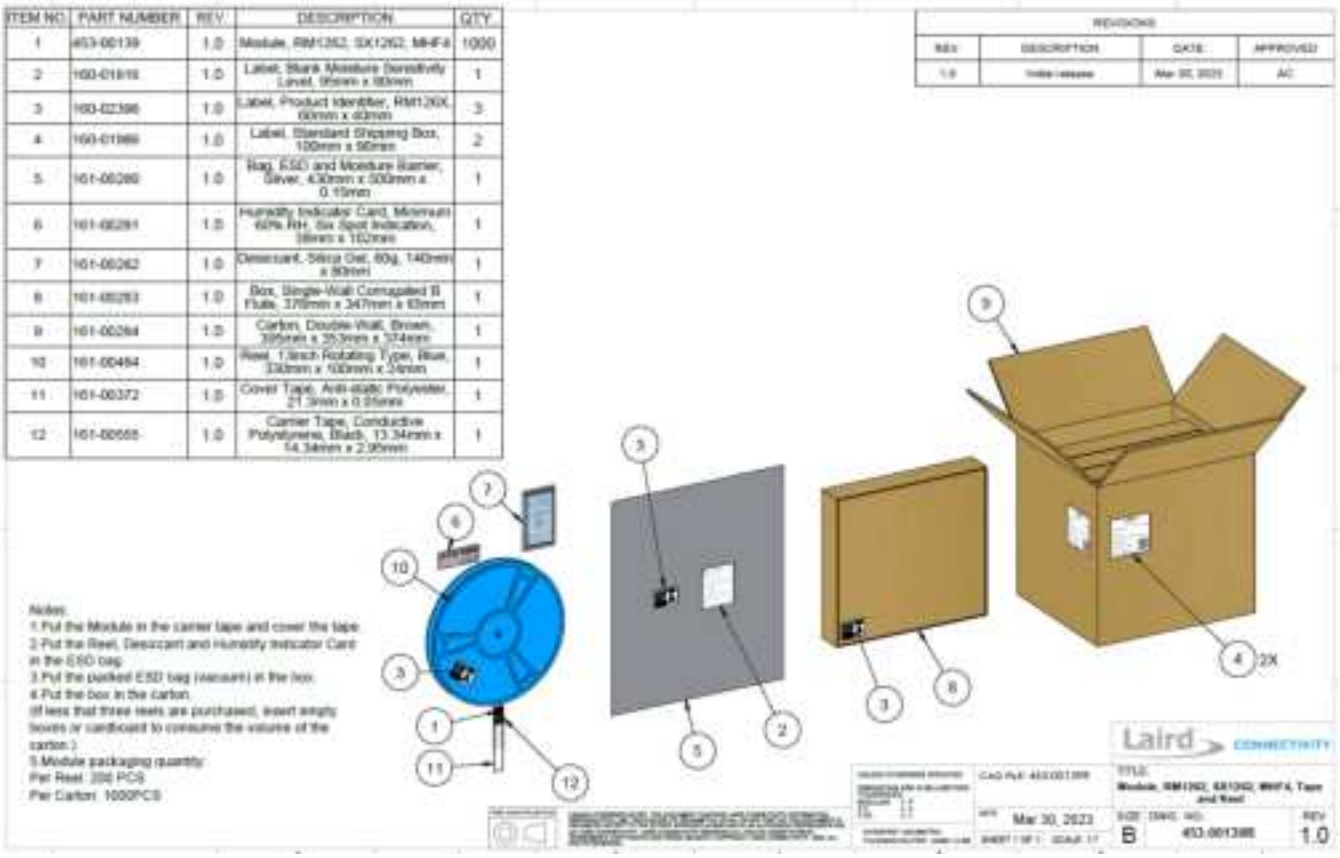
9 Carton Contents and Packaging Process

9.1 Carton Contents and Packaging Process



ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00139	1.0	Module, RM1262, SX1262, MHF4	1000
2	100-01818	1.0	Label, Blank Moisture Sensitivity Level, 95mm x 60mm	1
3	100-02398	1.0	Label, Product Identifier, RM126X, 60mm x 40mm	3
4	100-01988	1.0	Label, Standard Shipping Box, 100mm x 95mm	2
5	101-00280	1.0	Bag, ESD and Moisture Barrier, Silver, 430mm x 508mm x 0.15mm	1
6	101-00281	1.0	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
7	101-00282	1.0	Desiccant, 5Wgt Gel, 60g, 140mm x 90mm	1
8	101-00283	1.0	Box, Single-Wall Corrugated B Flute, 378mm x 347mm x 63mm	1
9	101-00284	1.0	Carton, Double-Wall, Brown, 395mm x 353mm x 374mm	1
10	101-00464	1.0	Reel, 13inch Rotating Type, Blue, 330mm x 100mm x 24mm	1
11	101-00372	1.0	Cover Tape, Anti-static Polyester, 21.3mm x 0.05mm	1
12	101-00555	1.0	Carrier Tape, Conductive Polystyrene, Black, 13.34mm x 14.34mm x 2.95mm	1

REV	DESCRIPTION	DATE	APPROVED
1.0	Initial release	Mar 30, 2023	AC

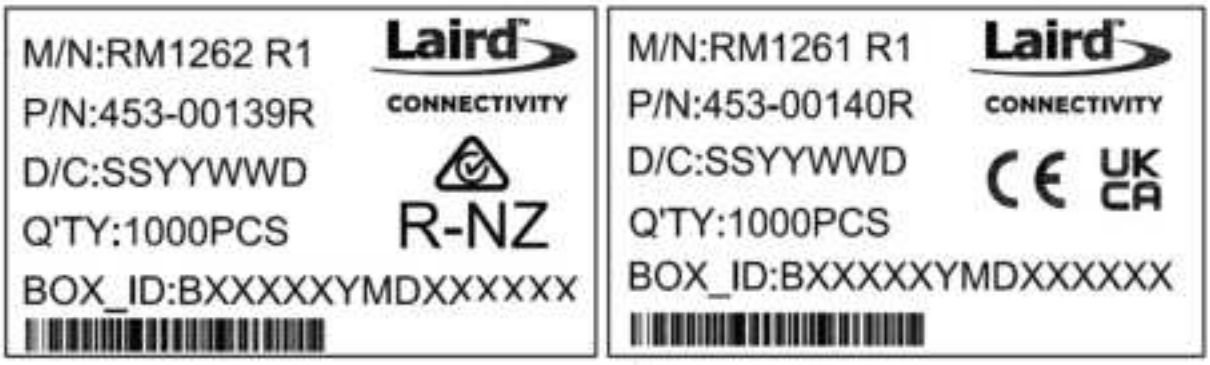
Notes:
1. Put the Module in the carrier tape and cover the tape.
2. Put the Reel, Desiccant and Humidity Indicator Card in the ESD bag.
3. Put the packed ESD bag (vacuum) in the box.
4. Put the box in the carton.
(If less that three reels are purchased, insert empty boxes or cardboard to consume the volume of the carton.)
5. Module packaging quantity:
Per Reel: 200 PCS
Per Carton: 1000PCS

Laird CONNECTIVITY
Mar 30, 2023
B
453-00139
1.0

Figure 15 RM126x carton contents and packaging process

9.2 Labelling

The following are placed on the reel, anti-static bag, and the pizza box.



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The following package labels are placed on both sides of the master carton.

10 Soldering Recommendations

10.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

10.2 Recommended Reflow Profile for lead Free Solder Paste

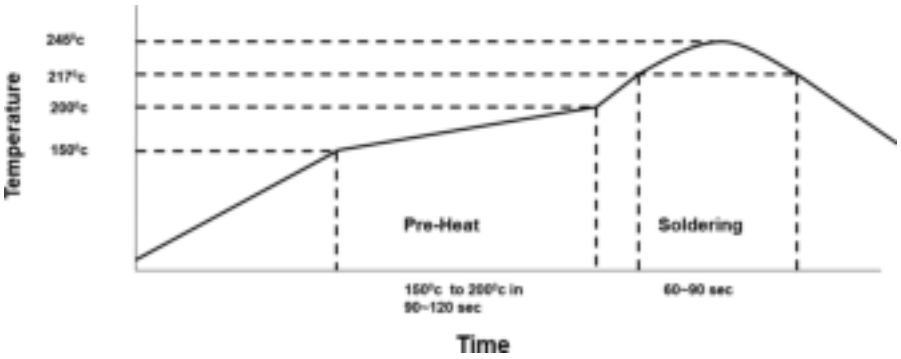

Figure 16: Recommended Reflow Profile

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11 MISCELLANEOUS

11.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

11.2 Rework

The RM126x module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions terminate warranty coverage.

11.3 Handling and Storage

11.3.1 Handling

The RM126x module contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

11.3.2 Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

11.3.3 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX. Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

11.3.4 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

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12 Reliability Test

The RM126x modules were tested for reliability, and the test items and the corresponding standards are shown in Table 38.

12.1 Climatic and Dynamic

The RM126x module went through the below reliability tests and passed.

Table 38: RM126x Reliability Test Items and Standards

Test Item	Standard	Specification		Test Result
Thermal Shock	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	1. Temperature:	-40 ~ 85℃	Pass
		2. Ramp time:	Less than 10 seconds.	
		3. Dwell Time:	10 minutes	
		4. Number of Cycles:	500 times	
Vibration Non-operating Unpackaged device	JEDEC 22-B103B (2016)	1. Vibration Wave Form:	Sine Waveform	Pass
		2. Vibration frequency / Displacement:	20-80 Hz/1.5mm	
		3. Vibration frequency / Acceleration:	80-2000 Hz/20g	
		4. Cycle Time:	4 min/cycle	
		5. Number of Cycles:	4 cycle/axis	
		6. Vibration Axes：	X, Y and Z (Rotate each axis on vertical vibration table)	
Mechanical Shock Non-operating Unpackaged device	JEDEC 22-B110B.01 (2019)	1. Pulse shape:	Half-sine waveform	Pass
		2. Impact acceleration:	1500 g	
		3. Pulse duration:	0.5 ms	
		4. Number of shocks:	30 shocks (5 shocks for each face)	
		5. Orientation:	Bottom, top, left, right, front and rear faces	

Before and after the testing, visual inspection showed no physical defect on samples.

After Vibration test and Mechanical Shock testing, the samples were functionally tested, and all samples functioned as normal. Then after Thermal shock test, the samples were functionally tested, and all samples functioned as normal.

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12.2 Reliability MTBF Prediction

Test Item	Specification	Standard
Mean Time Between Failure (MTBF)	1. Normal Operating Temperature:45 ℃ 2. High Temperature: 85 ℃	Telcordia SR-332 Issue 3

Laird Part Number	Environment	Test Result 45 ℃ (Hours)
453-00139R	Ground, Fixed, Uncontrolled	3,814,794
453-00139C	Ground, Mobile	1,907,397
453-00140R	Ground, Fixed, Uncontrolled	3,803,987
453-00140C	Ground, Mobile	1,901,993
Laird Part Number	**Environment**	**Test Result 85 ℃ (Hours)**
453-00139R	Ground, Fixed, Uncontrolled	711,487
453-00139C	Ground, Mobile	355,744
453-00140R	Ground, Fixed, Uncontrolled	710,797
453-00140C	Ground, Mobile	355,399

13 REGULATORY

Note: For complete regulatory information, refer to the RM126x Regulatory Information document which is also available from the RM126x product page at www.lairdconnect.com/rm126x-series.

The RM1261 / RM1262 holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC) – *RM1262 only*	SQG-RM1262
EU – *RM1261 only*	N/A
UKCA – *RM1261 only*	N/A
Canada (ISED) – *RM1262 only*	3147A-RM1262
Taiwan (NCC) – *RM1261 only*	TBD
Australia – *RM1262 only*	N/A
New Zealand – *RM1262 only*	N/A
India – *RM1261 only*	TBD
Japan – *RM1261 only*	201-220688

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14 Ordering Information

Part Number	Description
453-00139R	Module, RM126x, SX1262, MHF4 - Tape / Reel packaging version
453-00139C	Module, RM126x, SX1262, MHF4 – Cut Tape packaging
453-00139-K1	Development Kit, RM126x, SX1262, MHF4
453-00140R	Module, RM126x, SX1261, MHF4 - Tape / Reel packaging version
453-00140C	Module, RM126x, SX1261,MHF4 – Cut tape packaging
453-00140-K1	Development Kit, RM126x, SX1261,MHF4

15 LoRaWAN Alliance END Node Qualification

15.1 Overview

The RM1261 and RM1262 modules are listed on the LoRaWAN Alliance End Node website as qualified End Products.

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16 Additional Information

Please contact your local sales representative or our support team for further assistance:

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Website	www.lairdconnect.com/
Technical Support	www.lairdconnect.com/resources/support
Sales Contact	www.lairdconnect.com/contact

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