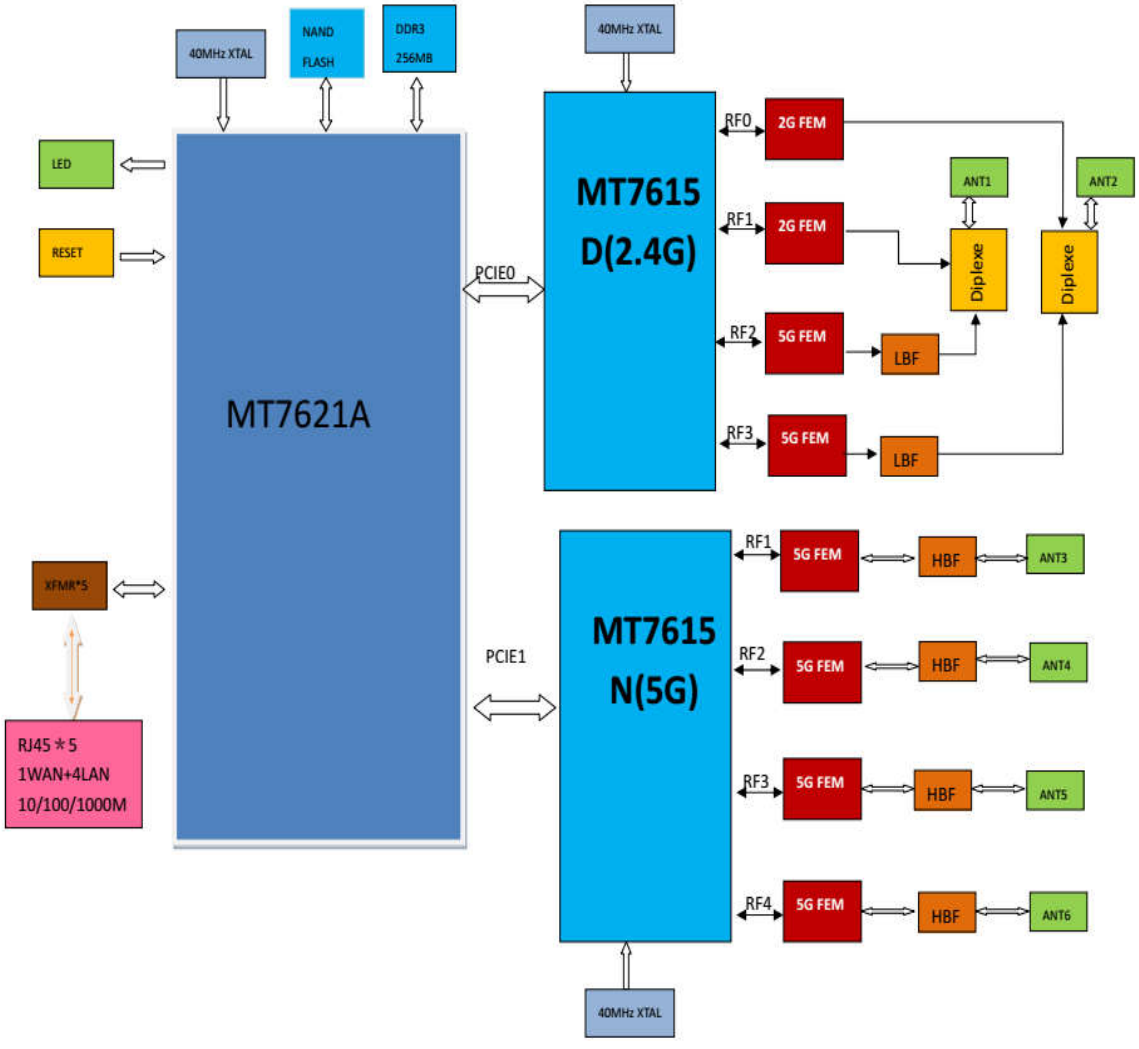
Module Number	DIR-3060
Product Type	4 LAN+1 WAN+2.4G 2T2R+5G Low Band 2T2R+5G High Band 4T4R +WPS+RESET+POWER

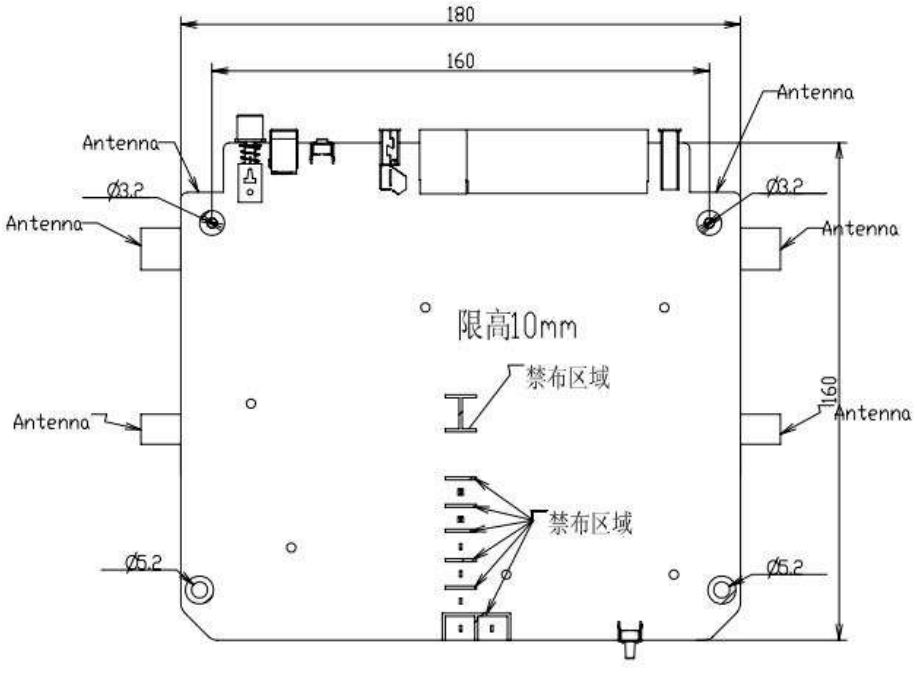
Revision History

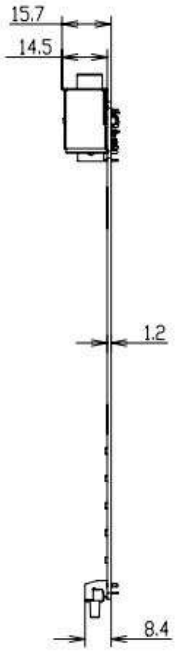
Version	Description	Designer	Date
0.1	Initial release	liuying	2017/03/09

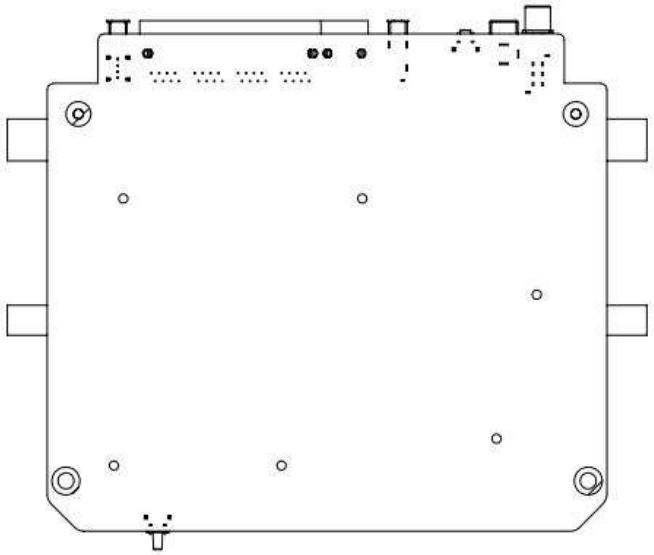
T&W ELECTRONICS	DIR-3060			
	Cover			
Size: B	Document Number:	Design By: Liuying	Review By:	Rev: 0.1
Date:		Sheet 1 of 23		



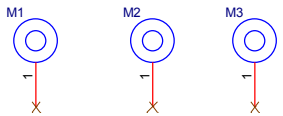
T&W ELECTRONICS	DIR-3060			
	Block Diagram			
Size: C	Document Number:	Design By: liuying	Review By:	Rev: 0.1
Date:		Sheet 2 of 23		







FILDMARK/fildmc_40/C40S120
FILDMARK/fildmc_40/C40S120
FILDMARK/fildmc_40/C40S120
FILDMARK/fildmc_40/C40S120



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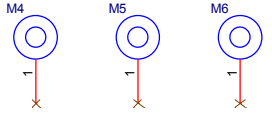
FILDMARK/fildmc_40/C40S120
FILDMARK/fildmc_40/C40S120



T&W ELECTRONICS	DIR-3060			
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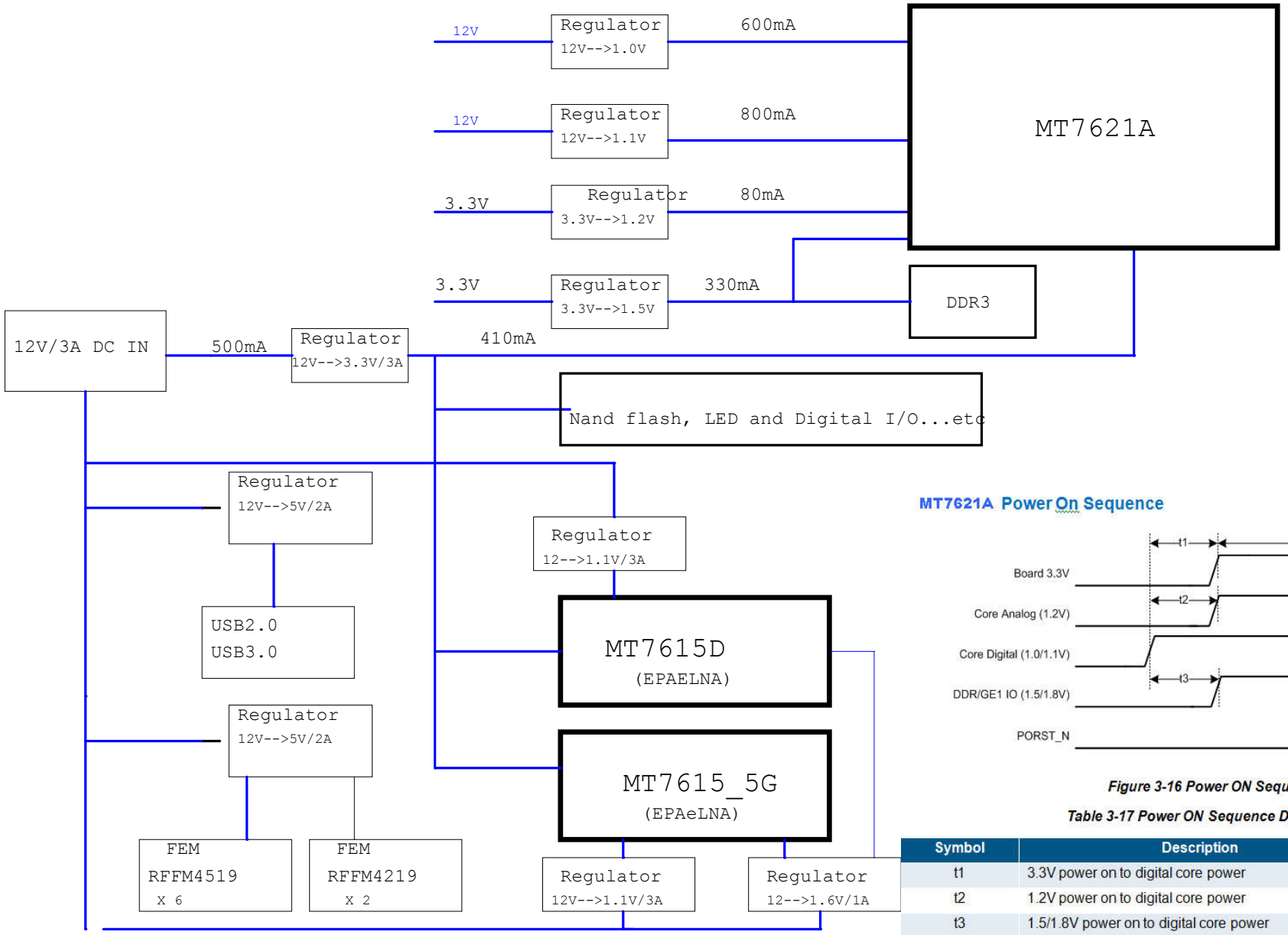
Size: B	Document Number:	Design By: liuying	Review By:	Rev: 0.1
Date: JAN. 28, 2013		Sheet 3 of 23		



MT7621A Power On Sequence

Figure 3-16 Power ON Sequence

Table 3-17 Power ON Sequence Diagram Key

Symbol	Description	Min	Max	Unit
t1	3.3V power on to digital core power	1	-	ms
t2	1.2V power on to digital core power	1	-	ms
t3	1.5/1.8V power on to digital core power	1	-	ms
t4	3.3V power on to PORST_N de-assertion	100	-	ms

Current= 300mA

Please reomve all components in this block for ac1900

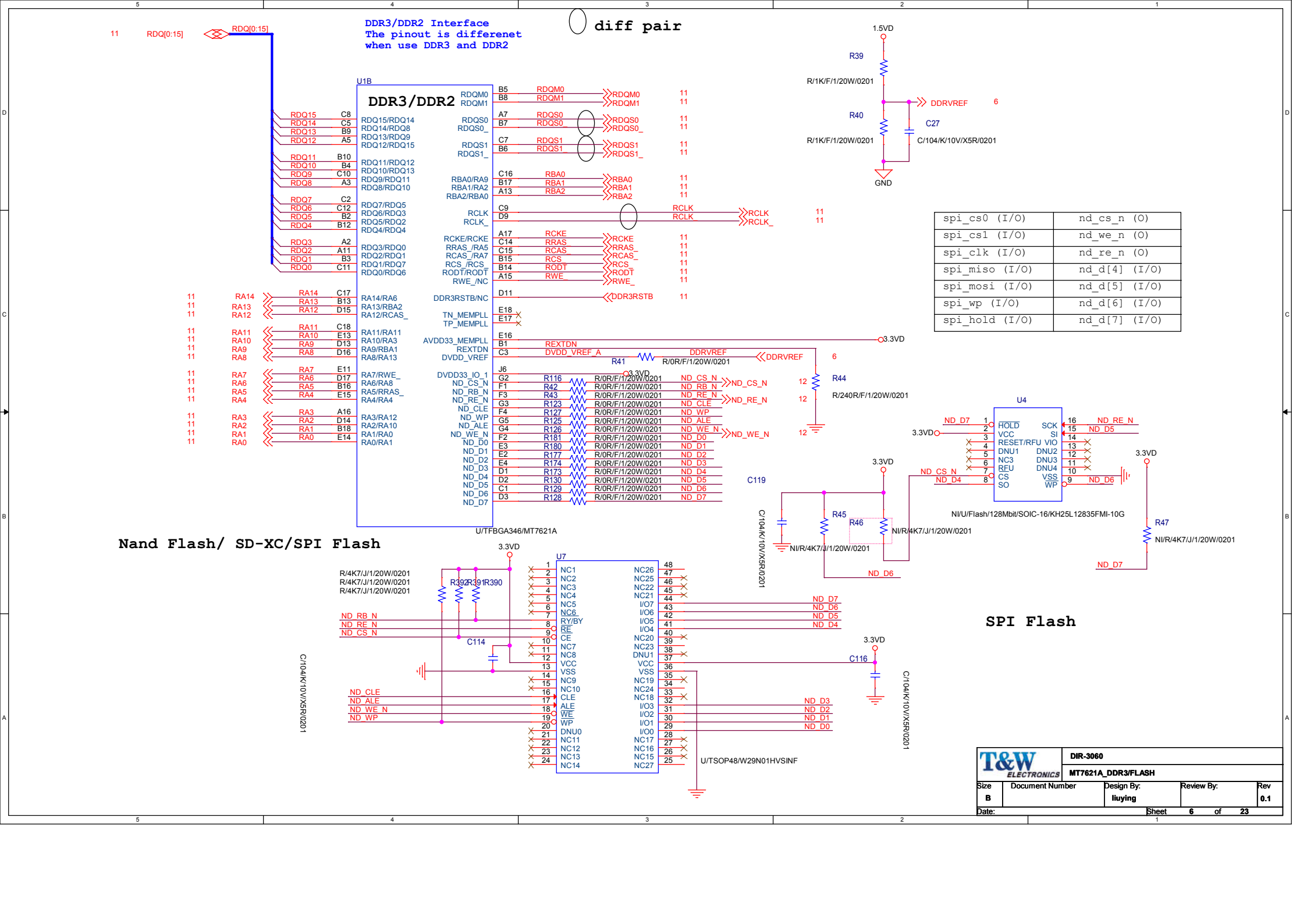
USB

PCIe

diff pair

Console

T&W ELECTRONICS	DIR-3060	
	MT7621A_INTERFACE	
Size: C	Document Number:	Design By: liuying
Review By:	Rev: 0.1	
Date:	Sheet 5 of 23	


DDR3/DDR2 Interface
The pinout is differenet
when use DDR3 and DDR2
diff pair
U1B
DDR3/DDR2
U/TFBGA346/MT7621A
Nand Flash/ SD-XC/SPI Flash
1.5VD
R39
R/1K/F/1/20W/0201
DDRVREF
R40
C27
C/104/K/10V/X5R/0201
GND
spi_cs0 (I/O)
spi_cs1 (I/O)
spi_clk (I/O)
spi_miso (I/O)
spi_mosi (I/O)
spi_wp (I/O)
spi_hold (I/O)
nd_cs_n (O)
nd_we_n (O)
nd_re_n (O)
nd_d[4] (I/O)
nd_d[5] (I/O)
nd_d[6] (I/O)
nd_d[7] (I/O)
3.3VD
R41
R0R/F/1/20W/0201
R44
R/240R/F/1/20W/0201
U4
NI/U/Flash/128Mbit/SOIC-16/KH25L12835FMI-10G
C119
C/104/K/10V/X5R/0201
R45
R46
NI/R/4K7/J/1/20W/0201
R47
U7
U/TSOP48/W29N01HVSINF
R/4K7/J/1/20W/0201
C114
C116
SPI Flash
T&W ELECTRONICS
DIR-3060
MT7621A_DDR3/FLASH
Size B
Document Number
Design By: liuying
Review By:
Rev 0.1
Date:
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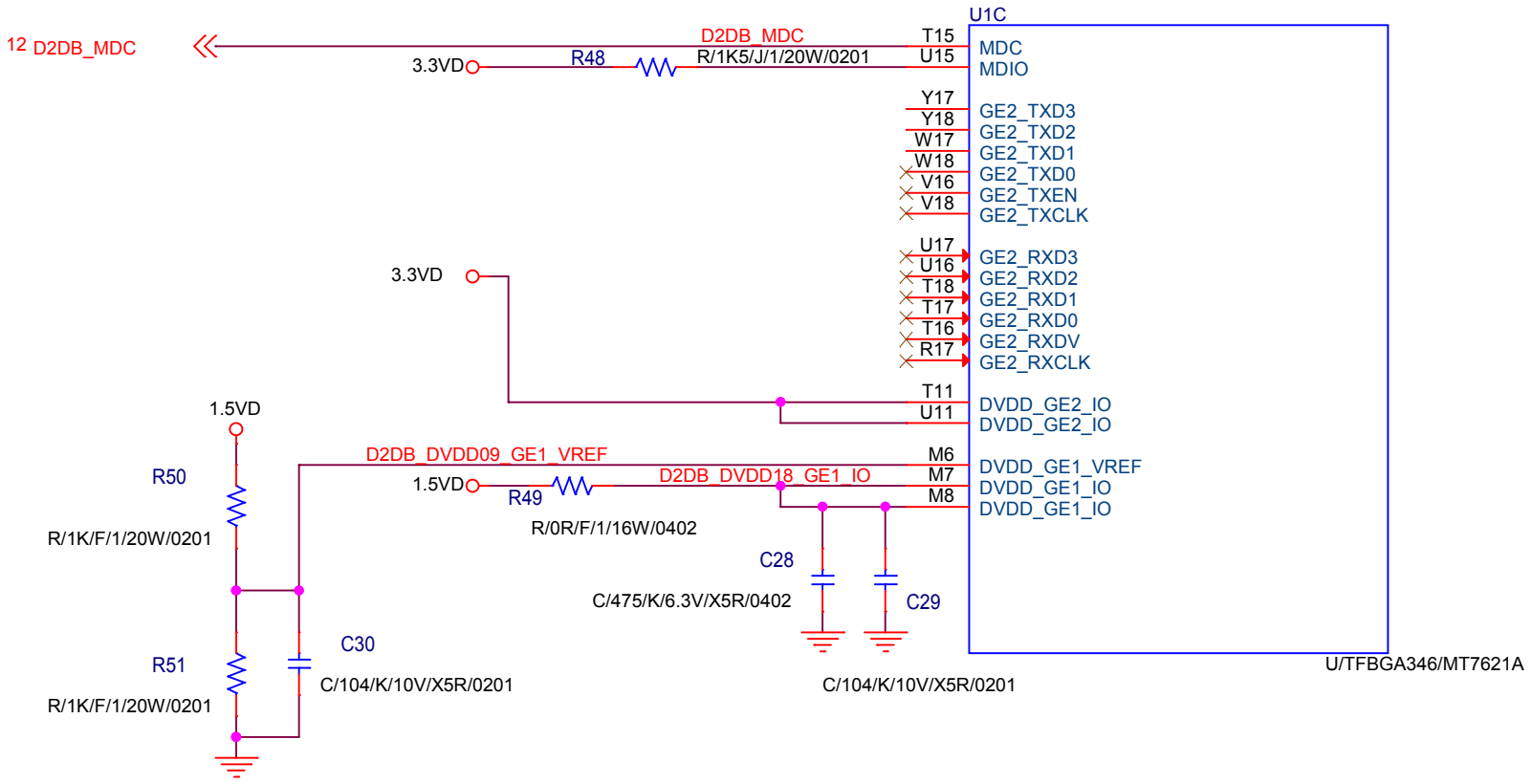
RGMII Interface



T&W ELECTRONICS	DIR-3060			
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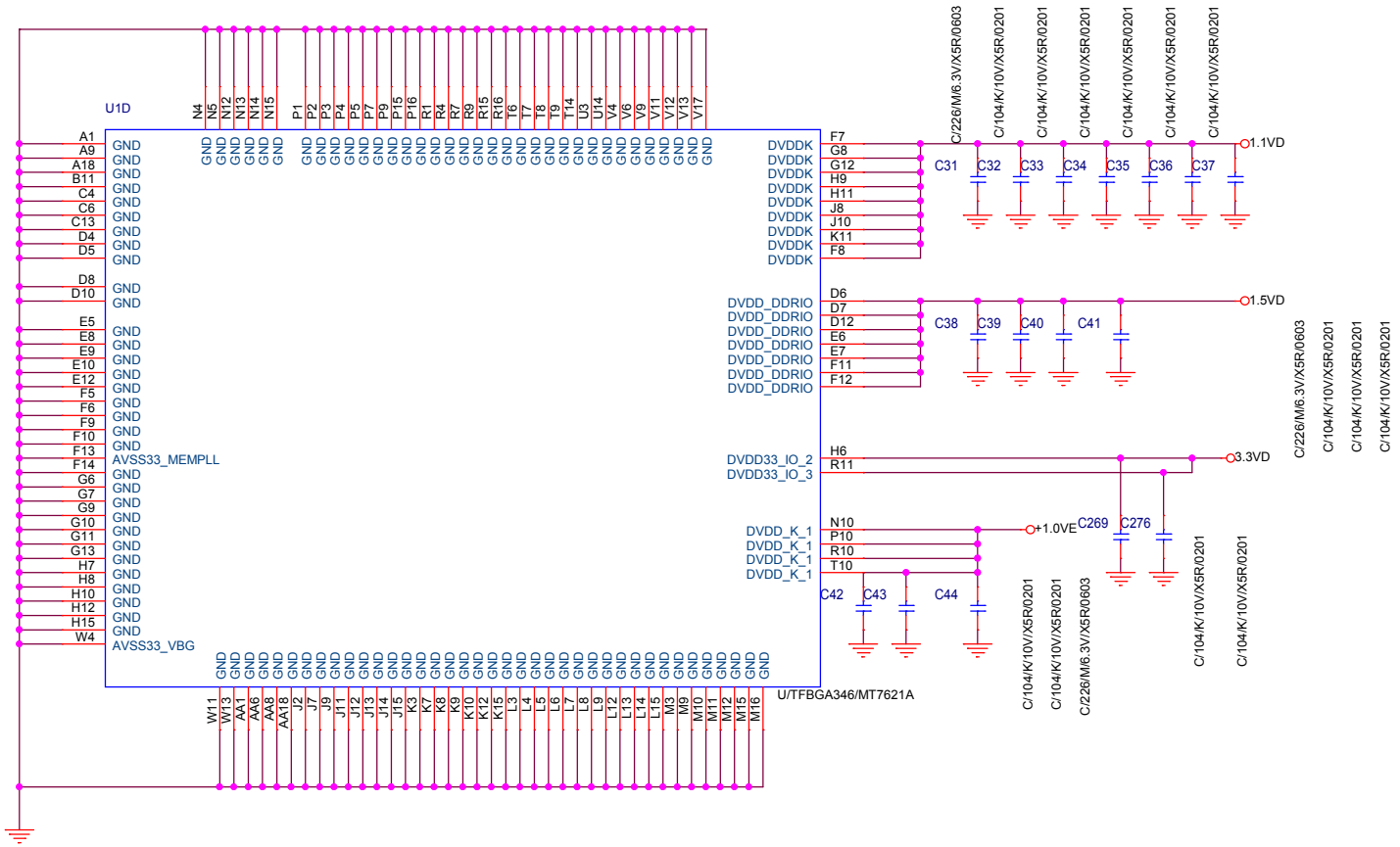
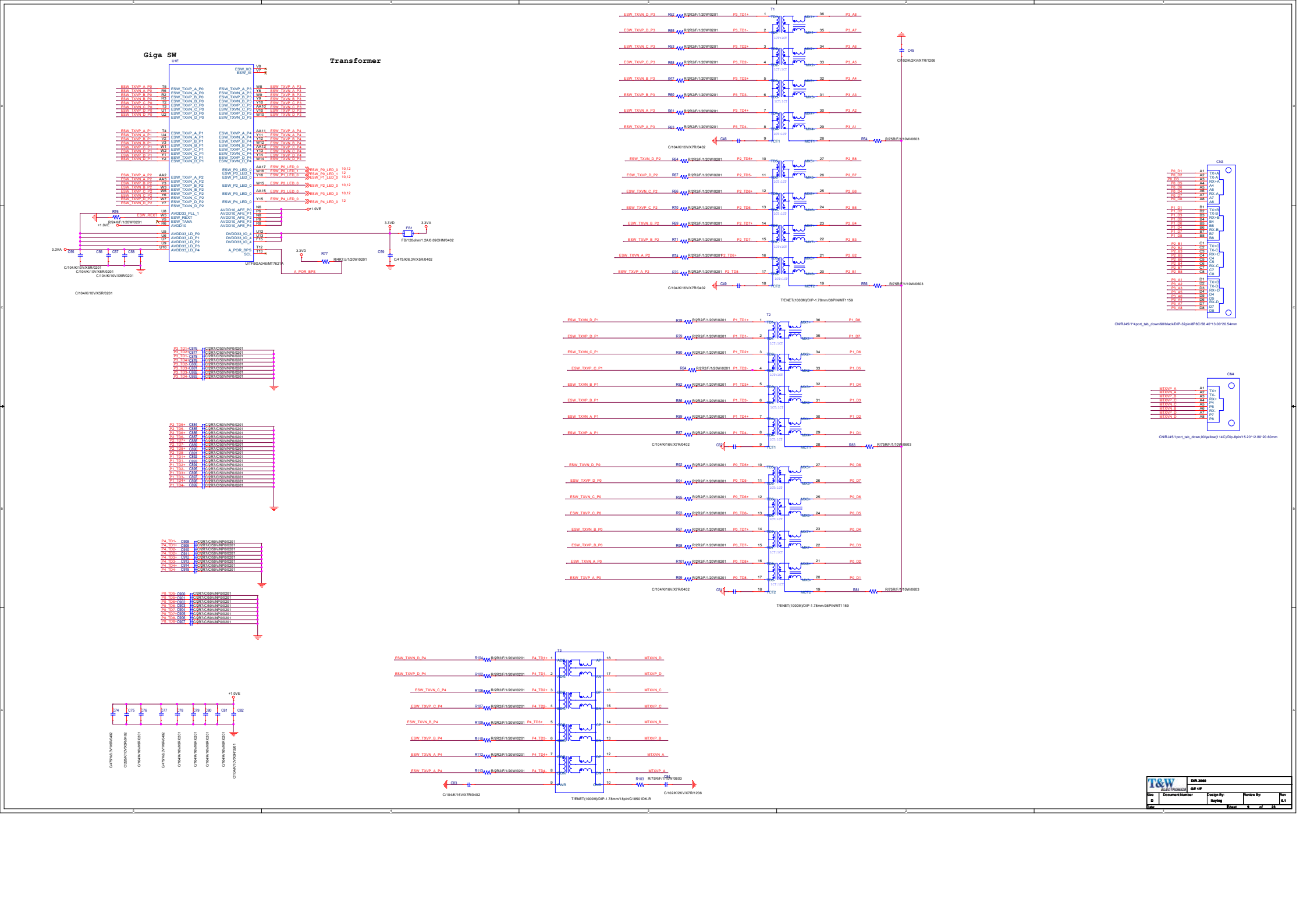
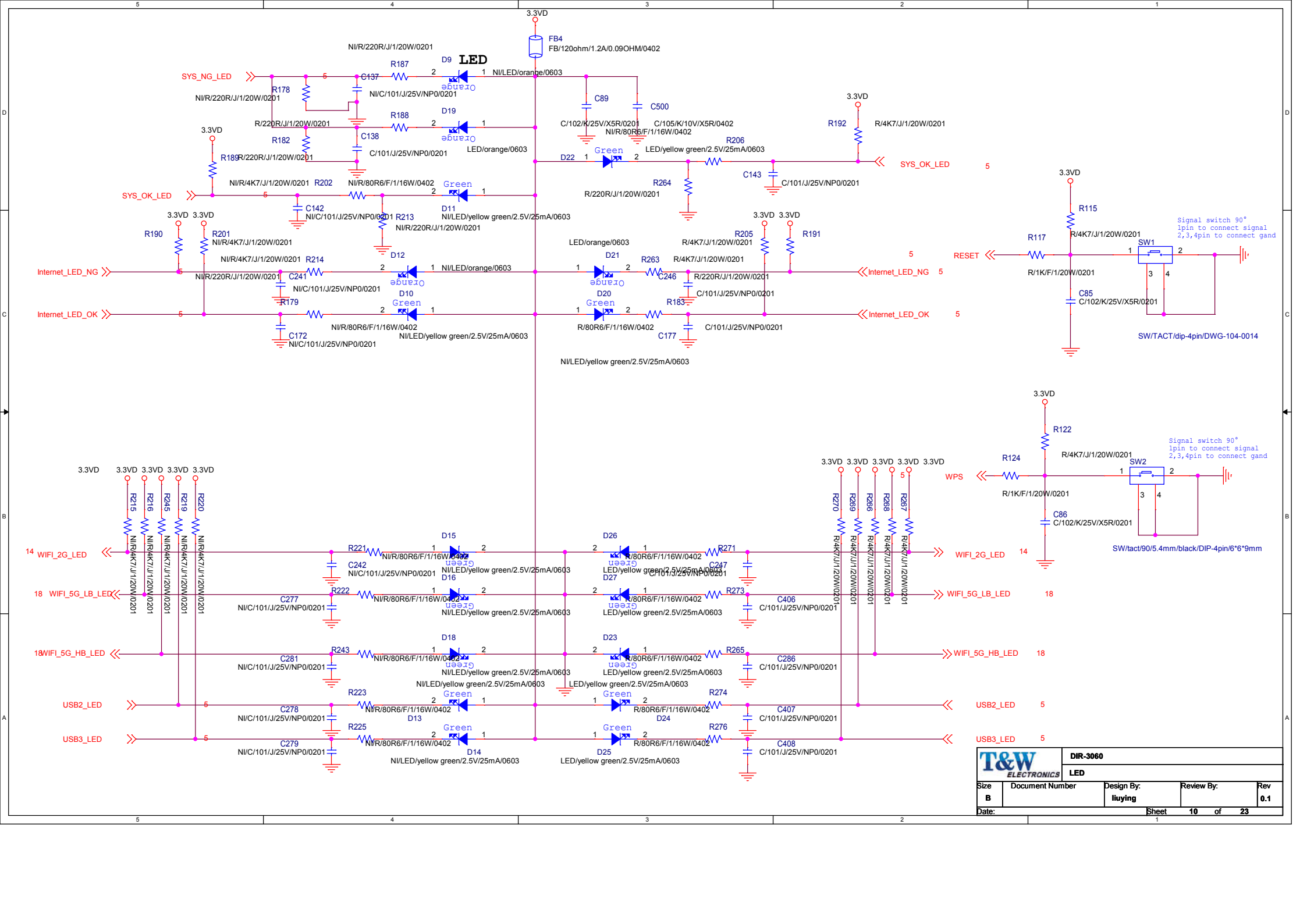
Size: A	Document Number:	Design By: liuying	Review By:	Rev: 0.1
Date:		Sheet 7 of 23		

MT7621 Power



T&W ELECTRONICS	DIR-3060			
	CPU_POWER			
Size: B	Document Number	Design By: liuying	Review By:	Rev: 0.1
Date:		Sheet 8 of 23		


Giga SW
Transformer
U1E
U1TFBGA346/MT7621A
T1
T2
T3
T:ENET(1000M)/DIP-1.78mm/36PIN/MT1159
T:ENET(1000M)/DIP-1.78mm/18pin/G18501DK-R
CN3
CN4
CN/RJ45/1*4port_tab_down/90/black/DIP-32pin/8P8C/58.40*13.00*20.54mm
CN/RJ45/1port_tab_down,90/yellow(114C)/Dip-8pin/15.20*12.80*20.60mm
C/104K/16V/X7R/0402
C/102K/2KV/X7R/1206
C/104K/10V/X5R/0201
C/475K/6.3V/X5R/0402
FB/120ohm/1.2A/0.09OHM/0402
R/240K/F/1/20W/0201
R/4K7/J/1/20W/0201
R/75R/F/1/10W/0603
C/2R7/C/50V/NP0/0201
A_POR_BPS
Date:
Sheet 9 of 23


3.3VD
FB4
FB/120ohm/1.2A/0.09OHM/0402
LED
D9
R187
NI/R/220R/J/1/20W/0201
NI/LED/orange/0603
SYS_NG_LED
C137
NI/C/101/J/25V/NP0/0201
R178
NI/R/220R/J/1/20W/0201
R188
D19
R/220R/J/1/20W/0201
C138
C/101/J/25V/NP0/0201
R182
R189
R/220R/J/1/20W/0201
LED/orange/0603
C89
C500
C/102/K/25V/X5R/0201
C/105/K/10V/X5R/0402
NI/R/80R6/F/1/16W/0402
R192
R/4K7/J/1/20W/0201
R206
LED/yellow green/2.5V/25mA/0603
D22
R264
R/220R/J/1/20W/0201
C143
C/101/J/25V/NP0/0201
SYS_OK_LED
NI/R/4K7/J/1/20W/0201
R202
NI/R/80R6/F/1/16W/0402
C142
NI/C/101/J/25V/NP0/0201
R213
NI/R/220R/J/1/20W/0201
D11
NI/LED/yellow green/2.5V/25mA/0603
R190
R201
NI/R/4K7/J/1/20W/0201
R214
Internet_LED_NG
Internet_LED_OK
C241
NI/C/101/J/25V/NP0/0201
R179
C172
NI/C/101/J/25V/NP0/0201
D12
D10
NI/LED/orange/0603
NI/LED/yellow green/2.5V/25mA/0603
LED/orange/0603
D21
D20
R263
C246
R/220R/J/1/20W/0201
C/101/J/25V/NP0/0201
R205
R191
R183
R/80R6/F/1/16W/0402
C177
C/101/J/25V/NP0/0201
NI/LED/yellow green/2.5V/25mA/0603
RESET
R115
R117
R/1K/F/1/20W/0201
SW1
C85
C/102/K/25V/X5R/0201
Signal switch 90° 1pin to connect signal 2,3,4pin to connect gand
SW/TACT/dip-4pin/DWG-104-0014
WPS
R122
R124
R/1K/F/1/20W/0201
SW2
C86
C/102/K/25V/X5R/0201
SW/tact/90/5.4mm/black/DIP-4pin/6*6*9mm
R215
R216
R245
R219
R220
R/4K7/J/1/20W/0201
WIFI_2G_LED
WIFI_5G_LB_LED
WIFI_5G_HB_LED
USB2_LED
USB3_LED
R221
R222
R243
R223
R225
D15
D16
D18
D13
D14
R/80R6/F/1/16W/0402
NI/LED/yellow green/2.5V/25mA/0603
C242
C277
C281
C278
C279
NI/C/101/J/25V/NP0/0201
D26
D27
D23
D24
D25
LED/yellow green/2.5V/25mA/0603
R271
R273
R265
R274
R276
C247
C406
C286
C407
C408
C/101/J/25V/NP0/0201
R270
R269
R266
R268
R267
T&W ELECTRONICS
DIR-3060
LED
Size
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Document Number
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liuying
Review By:
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Date:
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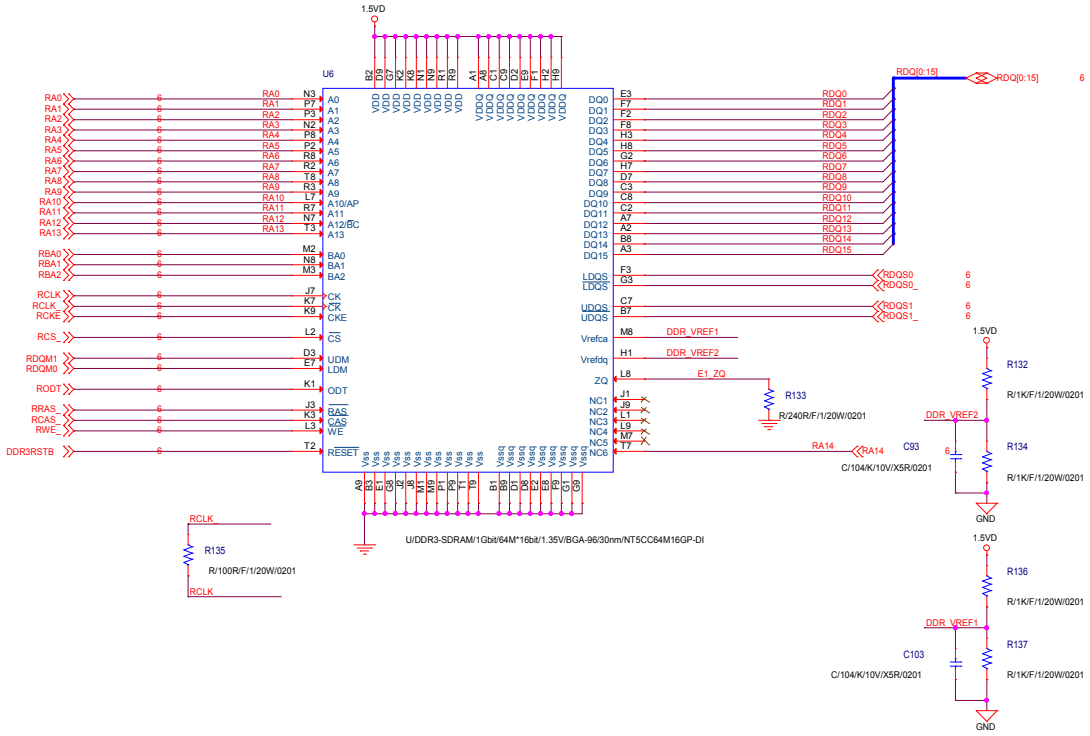
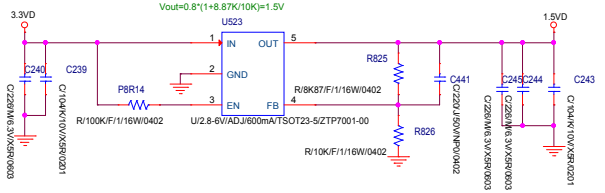
10
of
23

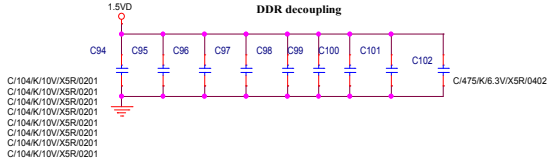


3.3V to 1.5V LDO Converter

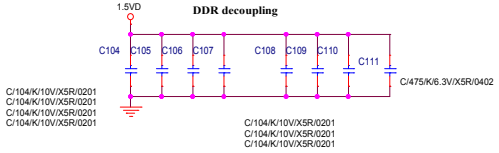
1.5V/500mA Max.



DDR decoupling



DDR decoupling



T&W ELECTRONICS	DIR-3060			
	DDR3			
Size: C	Document Number:	Design By: liuying	Review By:	Rev: 0.1
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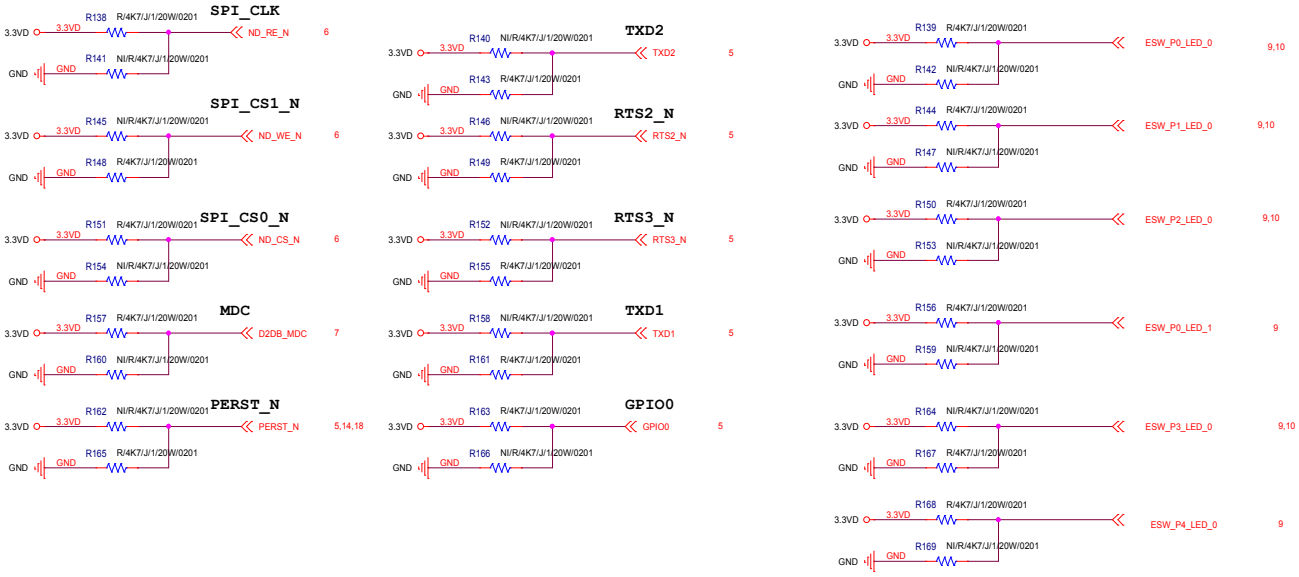
Boot Strapping

Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	 **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock **0001: Normal / Boot from ROM (NAND page 2k+64 bytes)** 0010: Normal / Boot from SPI 3-byte address 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

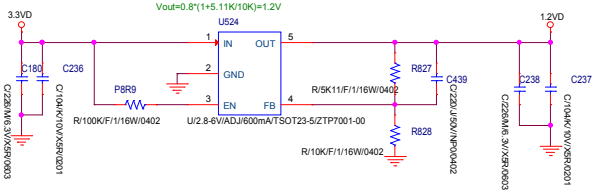


T&W ELECTRONICS	DIR-3060		
	Config		
Size: C	Document Number:	Design By: liuying	Review By:
Rev: 0.1			
Date:	Sheet 12 of 23		

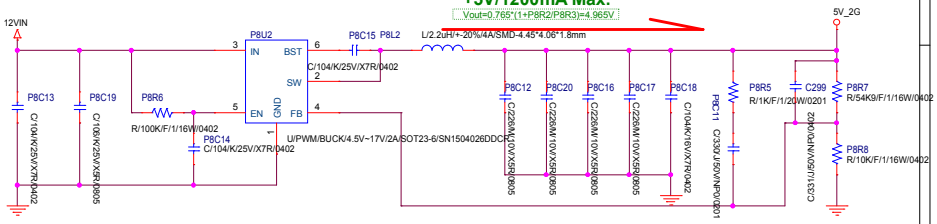
3.3V to 1.2V DC-DC Converter

For USB/PCIe PHY Power (1.2V)

1.2V/300mA Max.



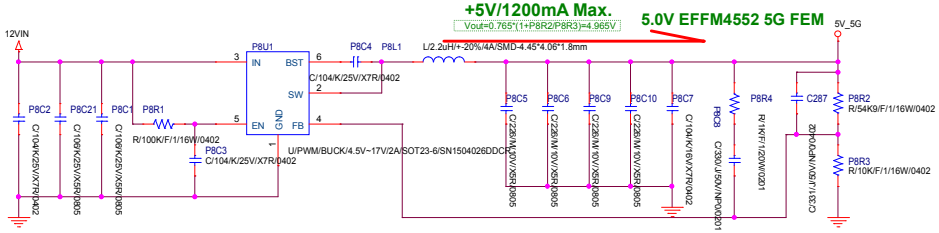
+5V/1200mA Max.



Vout

+5V/1200mA Max.

5.0V EFFM4552 5G FEM

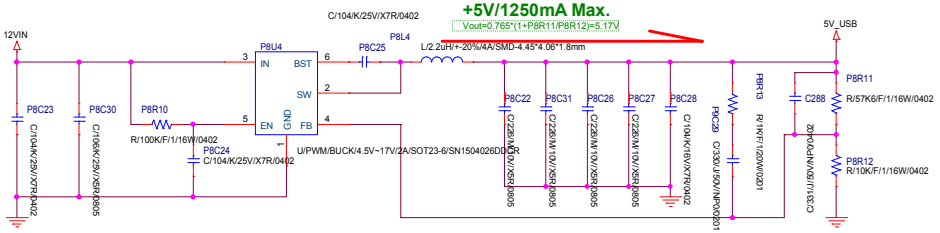


12V to 5V_EFM DC-DC Converter

Please reomve all components in this block
for ac1900

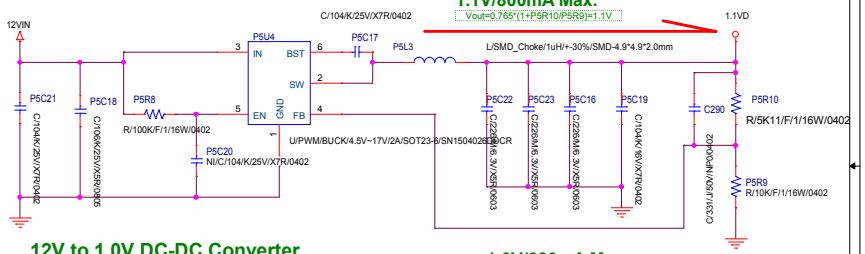
12V to 5V_USB DC-DC Converter

5.0V USB2.0&USB3.0



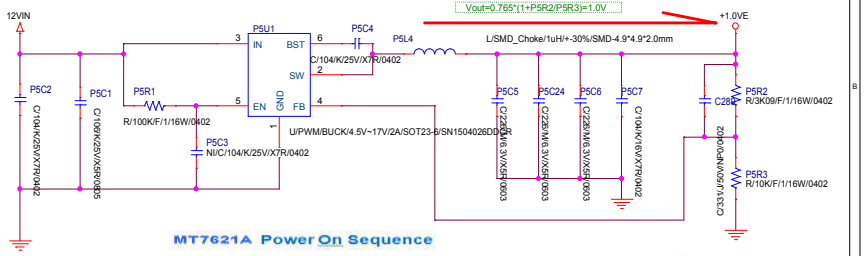
12V to 1.1V DC-DC Converter

1.1V/800mA Max.



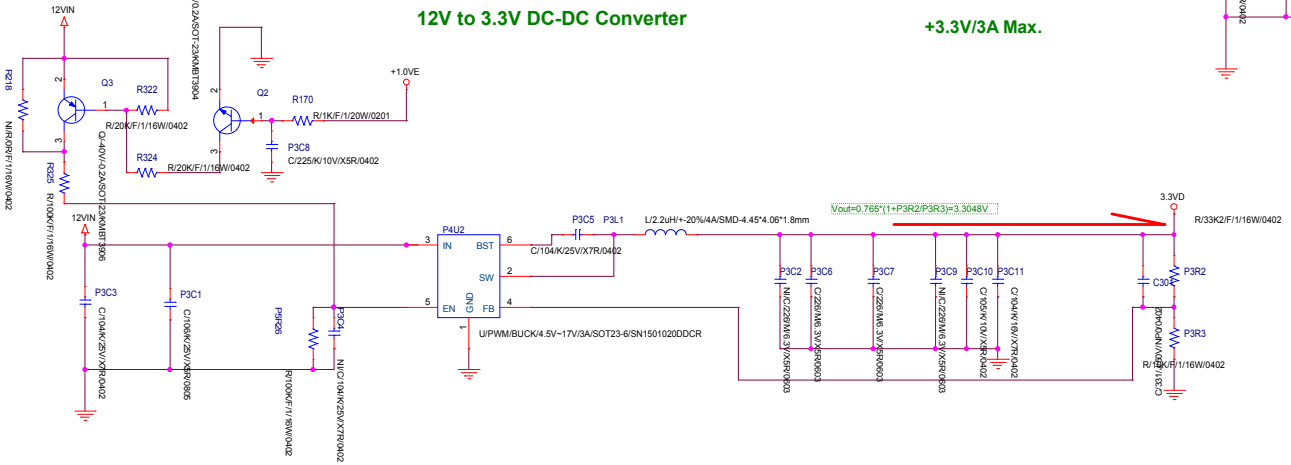
12V to 1.0V DC-DC Converter

1.0V/600mA Max.



12V to 3.3V DC-DC Converter

+3.3V/3A Max.



MT7621A Power On Sequence

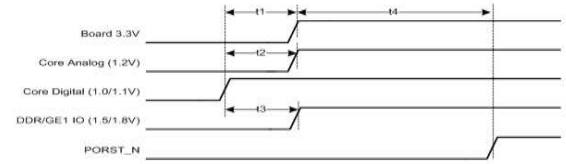


Figure 3-16 Power ON Sequence

Table 3-17 Power ON Sequence Diagram Key

Symbol	Description	Min	Max	Unit
t1	3.3V power on to digital core power	1	-	ms
t2	1.2V power on to digital core power	1	-	ms
t3	1.5/1.8V power on to digital core power	1	-	ms
t4	3.3V power on to PORST_N de-assertion	100	-	ms

T&W ELECTRONICS	DIR-3060			
	POWER			
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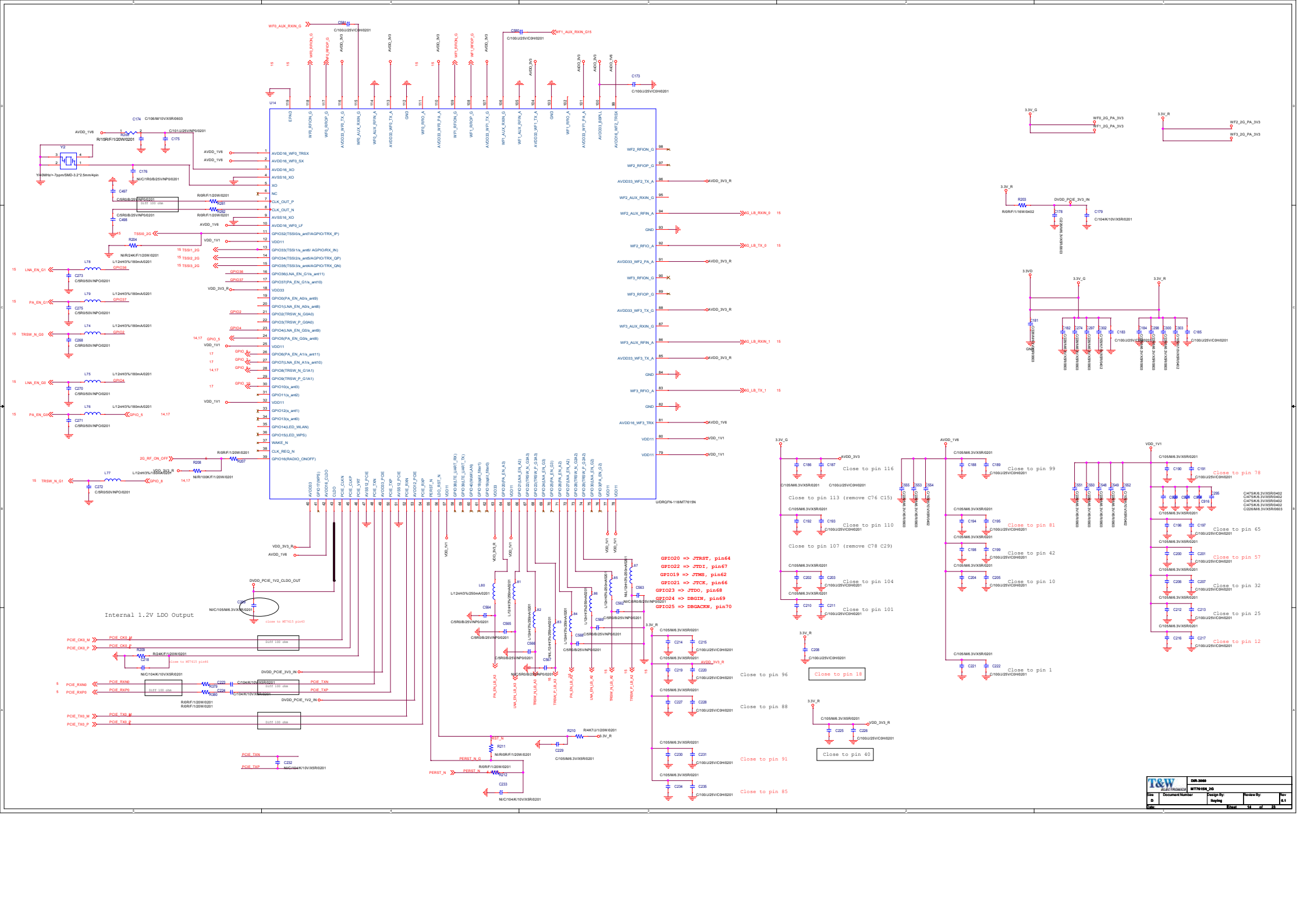
U14
MT7615N
U/DRQFN-118/MT7615N
Internal 1.2V LDO Output
close to MT7615 pin43
GPIO20 => JTRST, pin64
GPIO22 => JTDI, pin67
GPIO19 => JTMS, pin62
GPIO21 => JTCK, pin66
GPIO23 => JTDO, pin68
GPIO24 => DBGIN, pin69
GPIO25 => DBGACKN, pin70
Close to pin 116
Close to pin 113 (remove C76 C15)
Close to pin 110
Close to pin 107 (remove C78 C29)
Close to pin 96
Close to pin 88
Close to pin 91
Close to pin 85
Close to pin 99
Close to pin 81
Close to pin 42
Close to pin 104
Close to pin 10
Close to pin 101
Close to pin 1
Close to pin 18
Close to pin 40
Close to pin 78
Close to pin 65
Close to pin 57
Close to pin 32
Close to pin 25
Close to pin 12
Y1 40MHz/+-7ppm/SMD-3.2*2.5mm/4pin
Diff 100 ohm
T&W
DIR-3060
MT7615N_2G
Design By: liuying
Review By:
Rev 0.1
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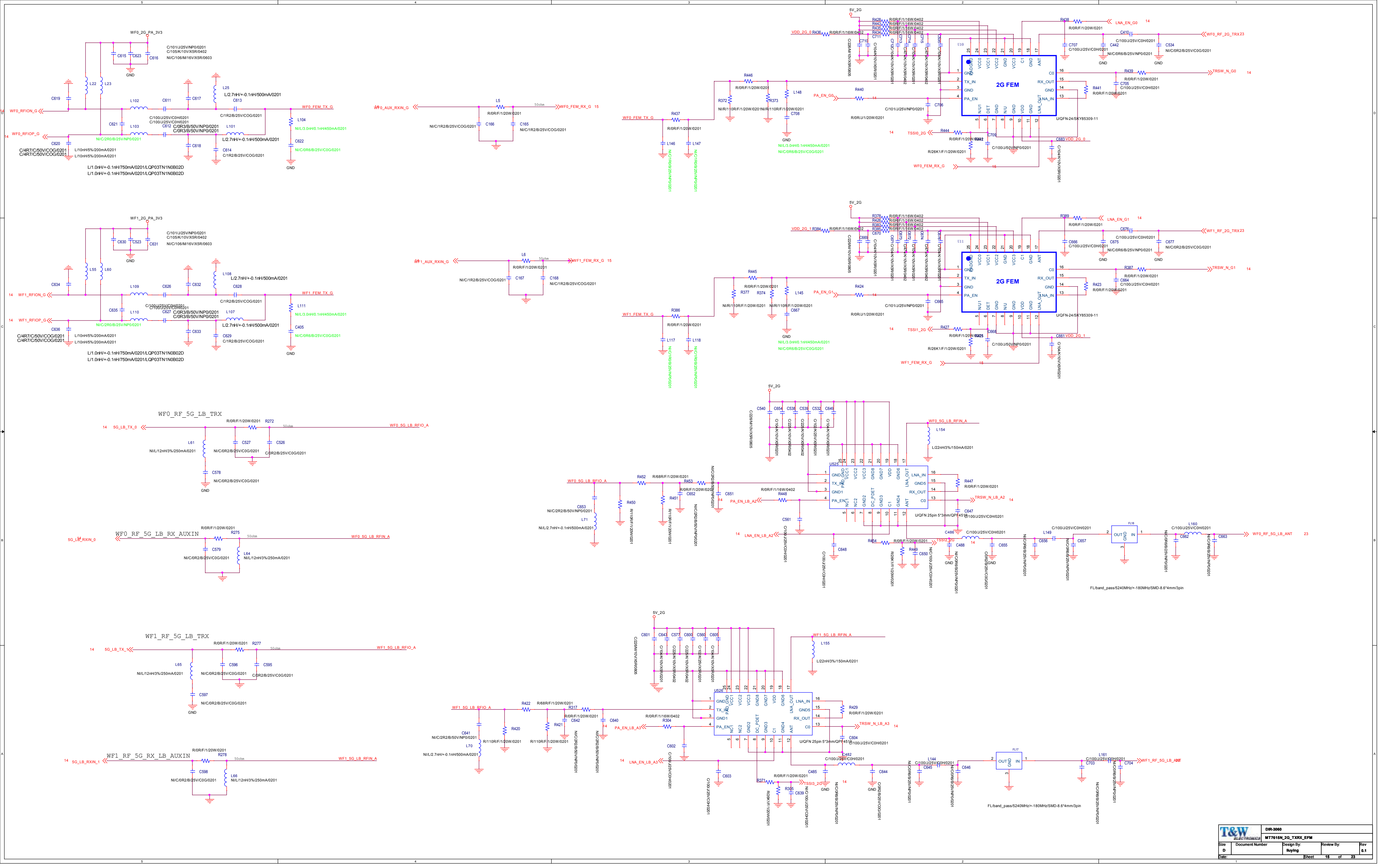

WF0_2G_PA_3V3
WF1_2G_PA_3V3
WF0_RFIOP_G
WF0_RFION_G
WF1_RFION_G
WF1_RFIOP_G
WF0_FEM_TX_G
WF1_FEM_TX_G
WF0_AUX_RXIN_G
WF1_AUX_RXIN_G
WF0_FEM_RX_G
WF1_FEM_RX_G
5V_2G
VDD_2G_0
VDD_2G_1
2G FEM
U/QFN-24/SKY85309-11
LNA_EN_G0
LNA_EN_G1
WF0_RF_2G_TRX23
WF1_RF_2G_TRX23
TRSW_N_G0
TRSW_N_G1
PA_EN_G0
PA_EN_G1
TSSI0_2G
TSSI1_2G
WF0_RF_5G_LB_TRX
WF0_RF_5G_LB_RX_AUXIN
WF1_RF_5G_LB_TRX
WF1_RF_5G_LB_RX_AUXIN
5G_LB_TX_0
5G_LB_TX_1
5G_LB_RXIN_0
5G_LB_RXIN_1
WF0_5G_LB_RFIO_A
WF1_5G_LB_RFIO_A
WF0_5G_LB_RFIN_A
WF1_5G_LB_RFIN_A
WF0_RF_5G_LB_ANT
WF1_RF_5G_LB_ANT
PA_EN_LB_A2
PA_EN_LB_A3
LNA_EN_LB_A2
LNA_EN_LB_A3
TRSW_N_LB_A2
TRSW_N_LB_A3
TSSI2_2G
TSSI3_2G
U/QFN 25pin 5*3mm/QPF4518
FL/band_pass/5240MHz/+-180MHz/SMD-8.6*4mm/3pin
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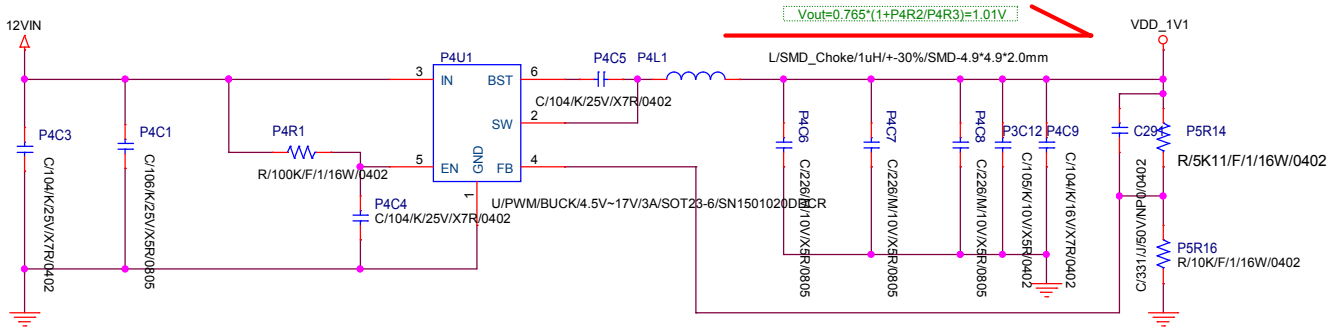
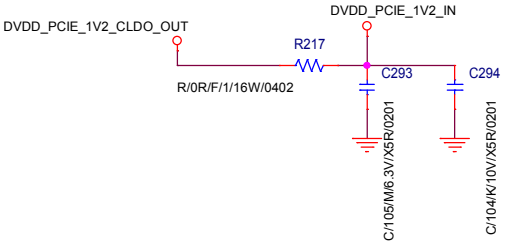
12V to 1.1V DC-DC Converter

1.1V MT7615E Core

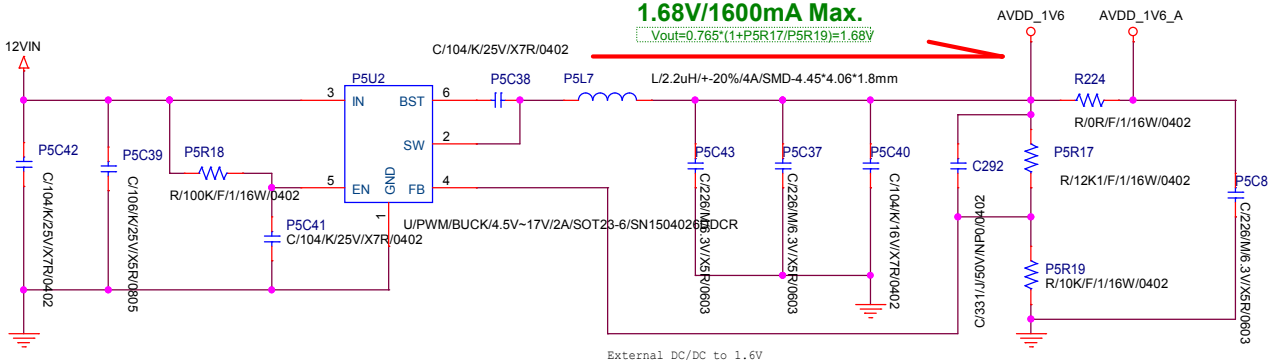
J17 1.15V source from external DC/DC converter
J25 1.15V source from power supply
(pin 1 need to connect to power supply equipment)

1.1V/3000mA Max.





1.68V/1600mA Max.



T&W ELECTRONICS	DIR-3060			
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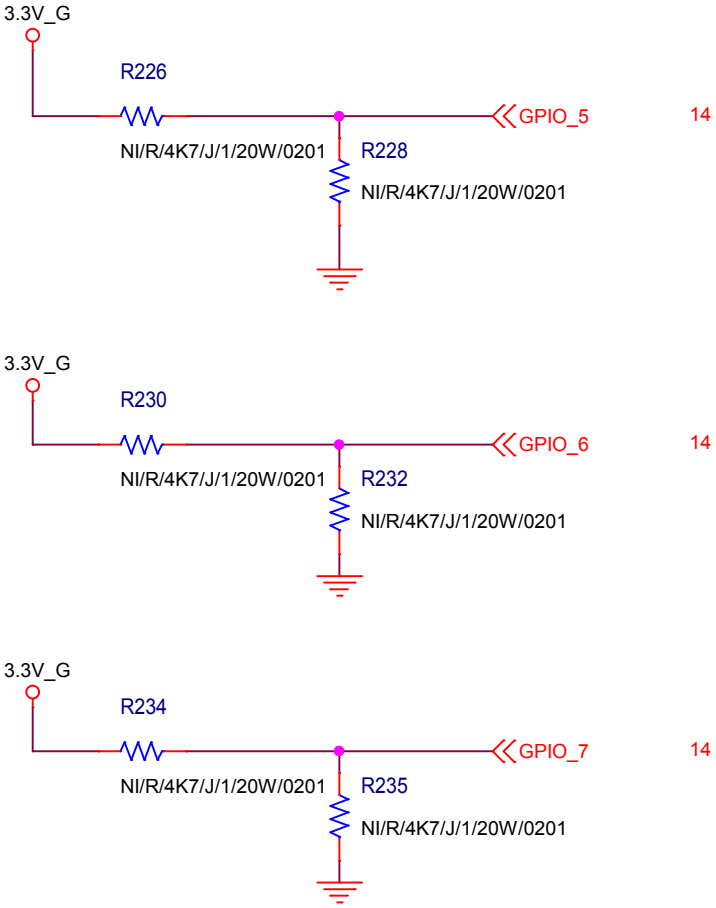

T&W ELECTRONICS	DIR-3060			
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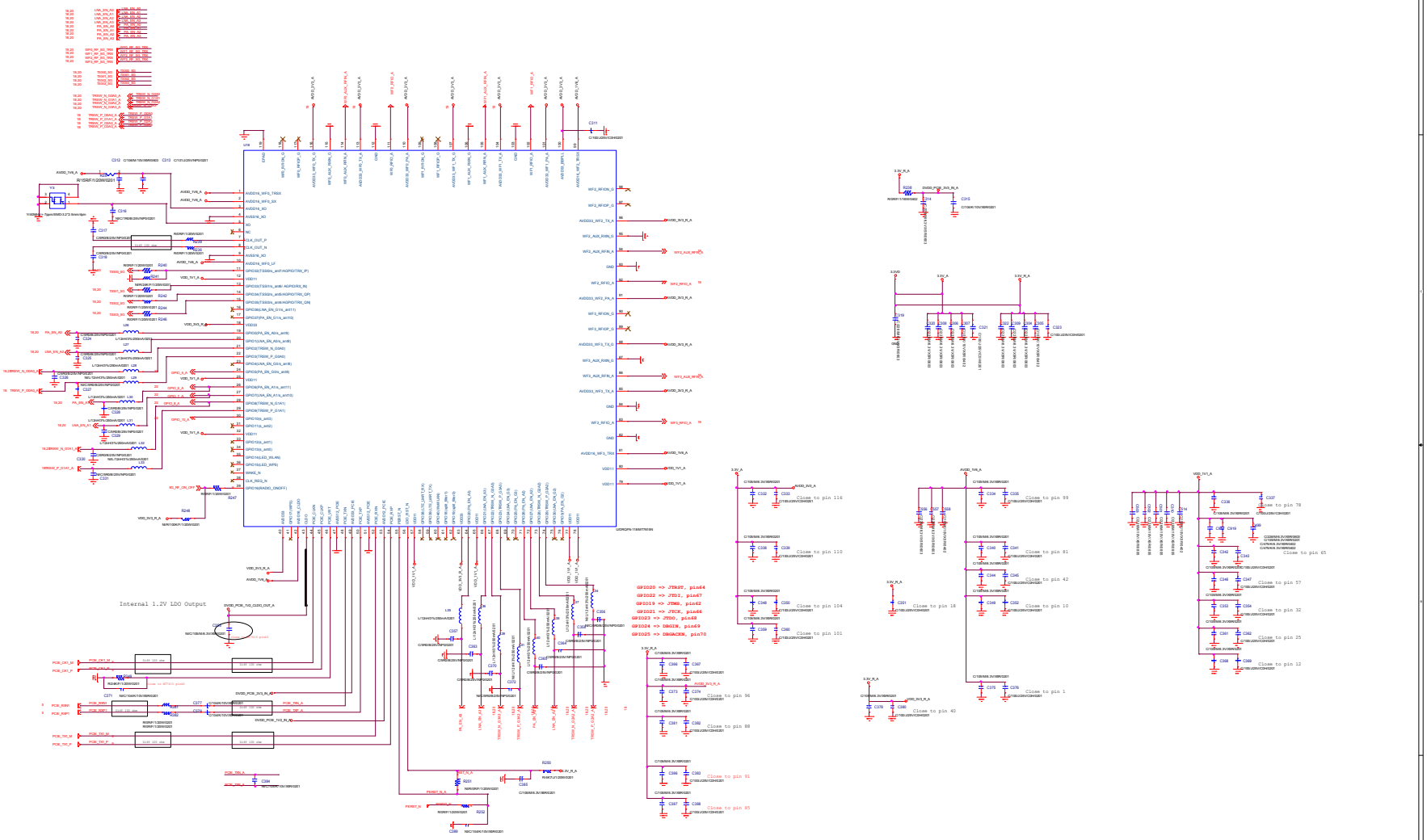
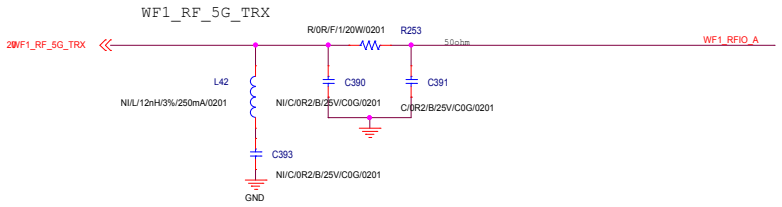
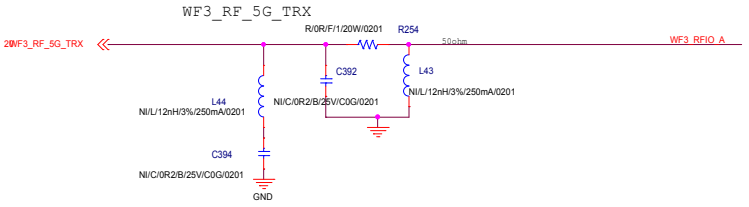
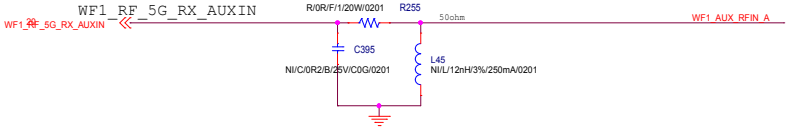
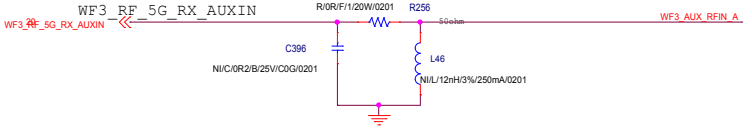
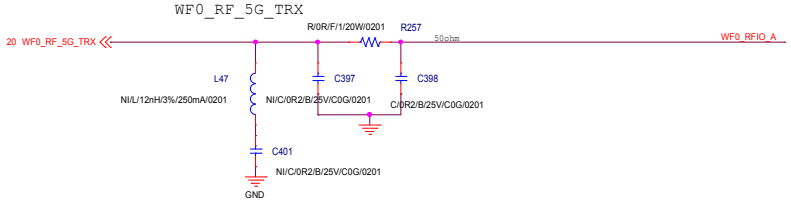

GP1020 => JTRST, pin64
GP1022 => JTDI, pin67
GP1019 => JTMS, pin62
GP1021 => JTCK, pin66
GP1023 => JTDO, pin68
GP1024 => BBGEN, pin69
GP1025 => BBGACKM, pin70
Internal 1.2V LDO Output
Close to pin 116
Close to pin 110
Close to pin 104
Close to pin 101
Close to pin 96
Close to pin 88
Close to pin 91
Close to pin 85
Close to pin 99
Close to pin 81
Close to pin 42
Close to pin 18
Close to pin 10
Close to pin 1
Close to pin 40
Close to pin 78
Close to pin 65
Close to pin 57
Close to pin 32
Close to pin 25
Close to pin 12

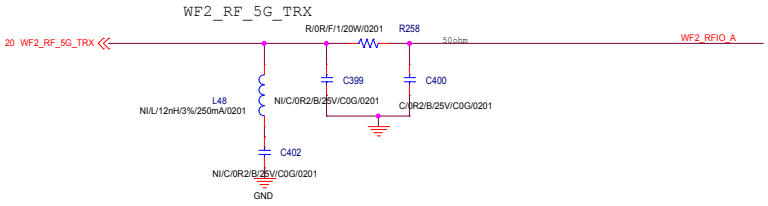


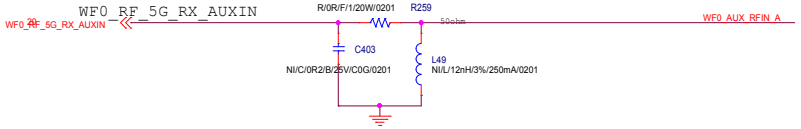


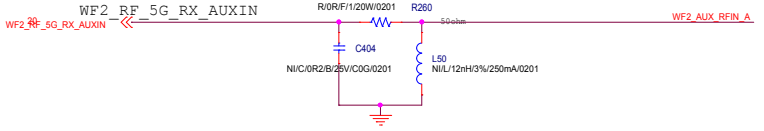


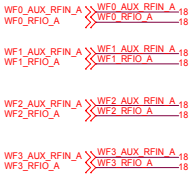












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	5G_TXRX			
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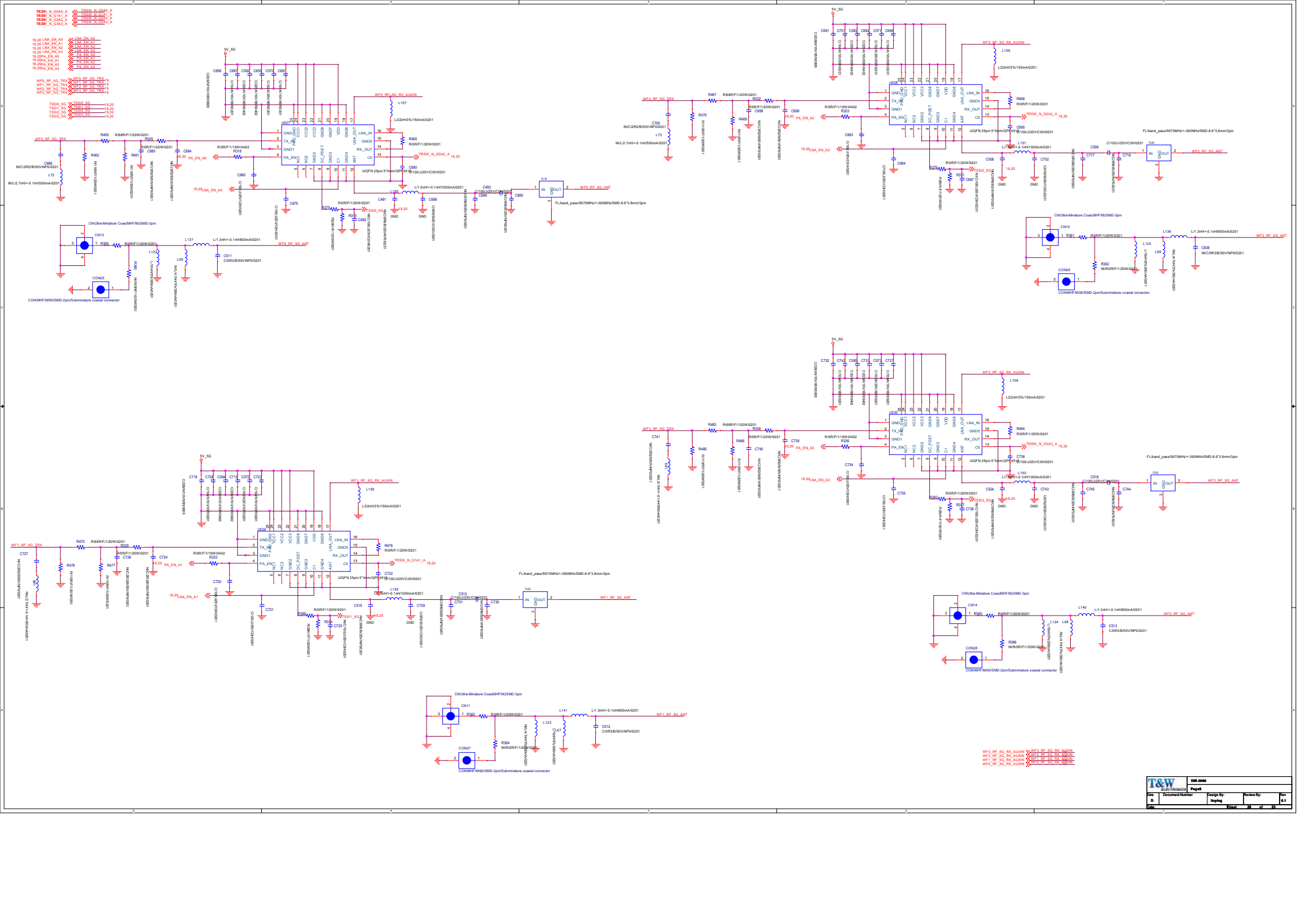

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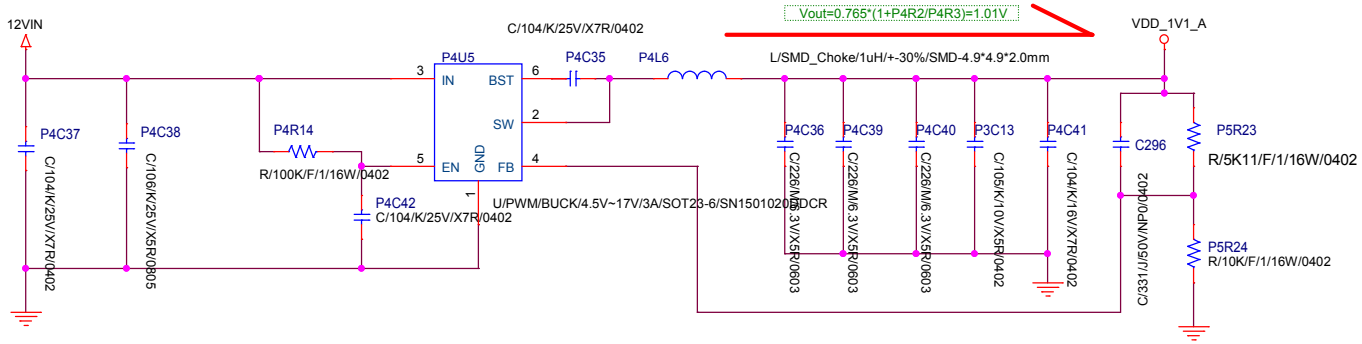
J17 1.15V source from external DC/DC converter
J25 1.15V source from power supply
(pin 1 need to connect to power supply equipment)

12V to 1.1V DC-DC Converter

1.1V MT7615E Core

1.1V/3000mA Max.



$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.

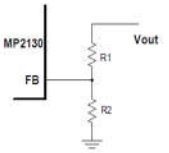
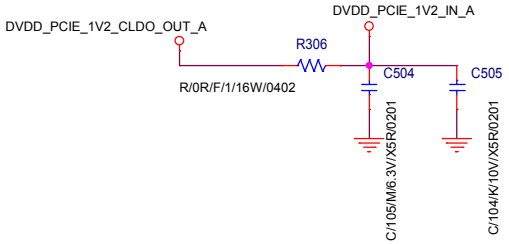


Figure 2— Feedback Network



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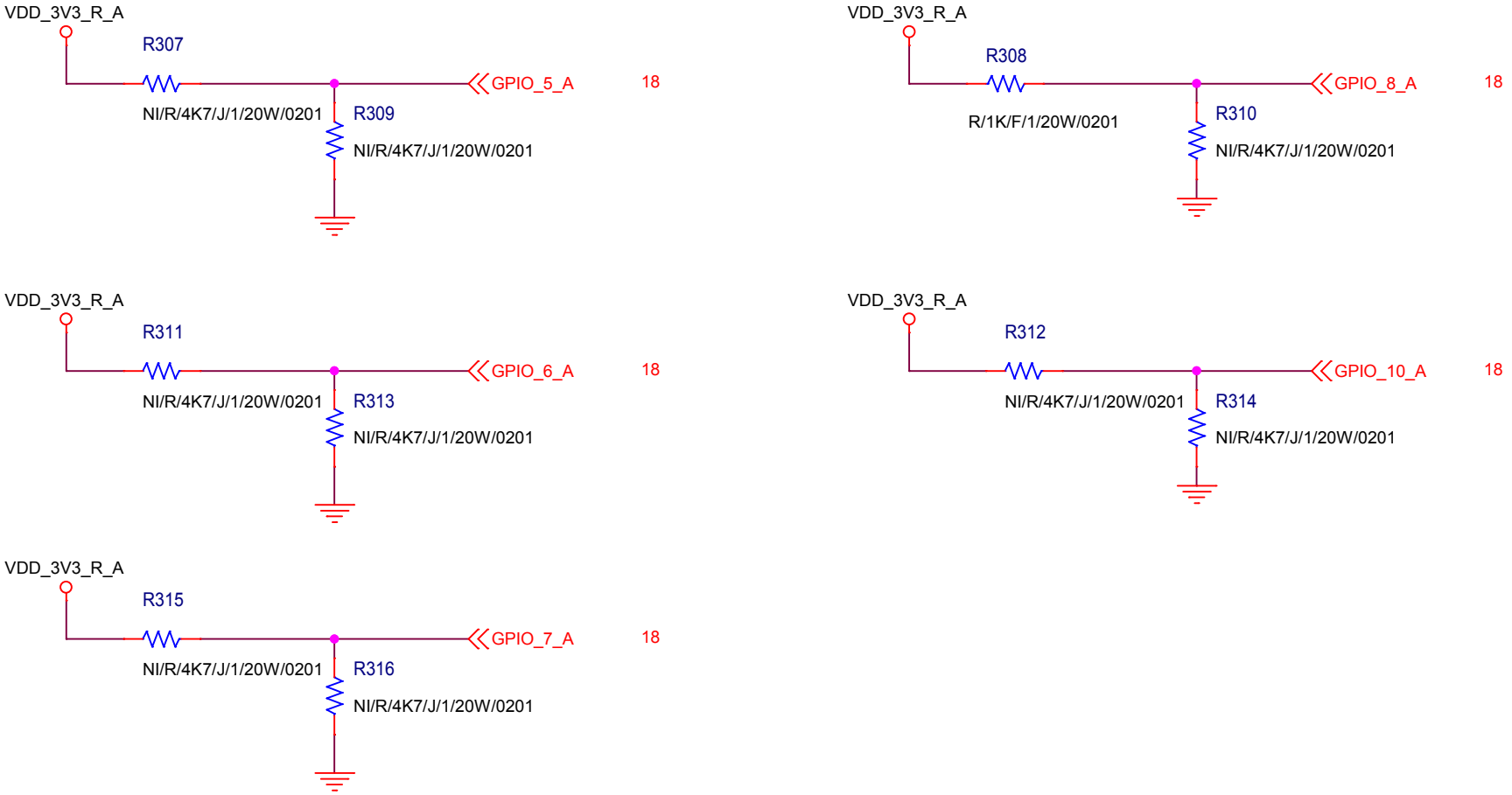

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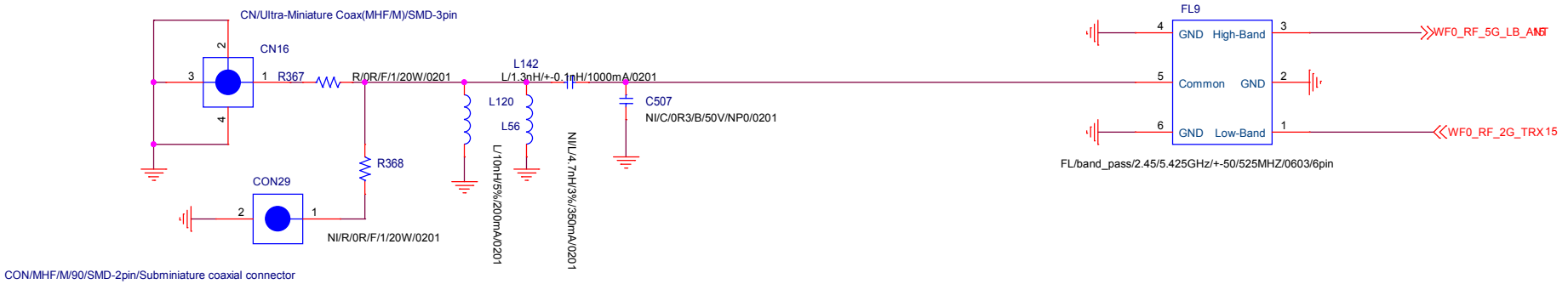

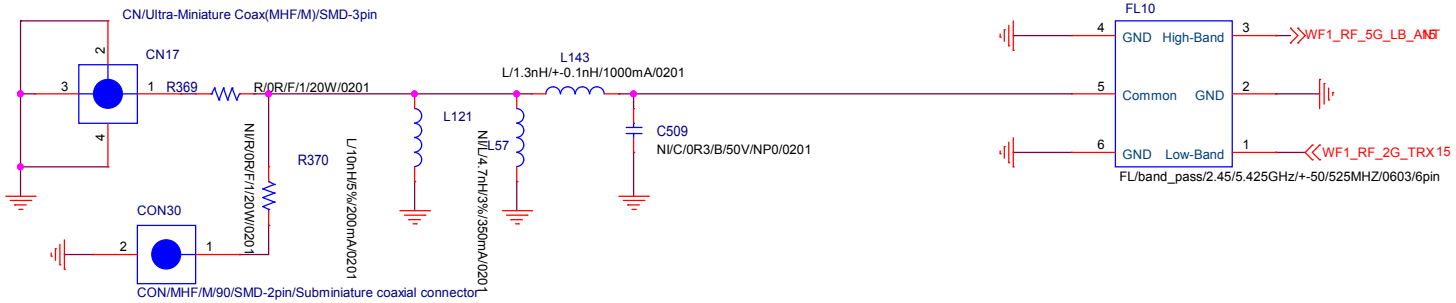

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