

7.THEORY OF OPERATION

Circuit Compositions and Operation Theory

The basic explanation for the circuit composition the board controlling the analog circuit parts and the digital circuit parts.

Receiver

Transmission parts are composed in the double conversion system, which has the 1st IF Frequency of 21.7 MHz and 2nd IF Frequency of 450 kHz. With the saw filter, which has an excellent band characteristic and sharp characteristic, the 2 poles MCF used in the 1st IF, and the sensitivity repression is reduced for the more stable reception.

RF Frontend

The signal received by the antenna will be transmitted to the band pass filter through the antenna switching circuit consisted of CT1, CT2, LT1, CT3 and LR1. The front RF amplifier transistor QR1 consists of the saw filter and input/output band pass filter.

Saw filter has the bandwidth of approximately 6 MHz, primarily diminishes the other signal rather than the 1st IF image and other signal within the reception band and amplifies only the necessary signal within the RF.

1st Mixer

The receiver signal which has been amplified in the RF fronted is provided to the base of the 1st mixer QR2. The 1st L/O signal provide from the VCO is supplied to the emitter of QR2 and converted to the 1st IF 21.7 MHz.

1st IF Filter and 1st IF Amplifier

The signal converted by QR2 to 21.7 MHz, the 1st frequency, change its impedance through CR8, LR6 and then is infused to the fundamental MCF which has the center frequency of 21.7 MHz and the width of +/-3.75 kHz.

Here, the signal reduces the image and other unwanted signal for the 2nd IF. Then the signal is infused to the IC3. The IC3 which functions as the 2nd mixer, the 2nd IF amplifier, and the FM detector, RSSI, PREMIC, compander, PLL circuit.

2nd Mixer, and IF, FM Detector

The receiver IF signal of 21.7 MHz, which has been infused to IC3 is mixed with the 2nd L/O signal of 21.250MHz, and converted to 450 kHz, the 2nd IF frequency. The receiver signal converted to the 2nd IF frequency passed through the F3, the ceramic filter of 450 kHz again. After the limiting inside the IC3 and the FM demodulating by the quadrature detector inside the IC3, the signal offers the output through the 21th pin of IC3.

The 2nd L/O signal of 21.250MHz, which infused to the IC3 filters and uses directly the crystal of 21.250 MHz. The squelch circuit is composed to detect the noised from the received signal demodulate in the 31th pin of the IC3. For this purpose, the noise filter is using the OP amplifier inside the IC3.

Transmitter

The transmission parts of the HH-200 are designed to amplify the RF signal oscillated and modulated by the synthesizer to approximately 2 W by the power transistor of QT3.

TX Power (QT3)

The transmitted signal of approximately 2 W, combined at the driver TR is supplied to the gate of the QT3 amplifier. The transmitted signal amplified to 2W here passes the TX LPF of the 2nd characteristic of the LT5, CT6, LT3, LT2, and RX/TX switching takes place by the DT1. After this, the signal is provided to the antenna the TX LPF of the 1st characteristics, consisted of the LT1, CT2.

Frequency Synthesizer

Voltage Control Oscillator (VCO)

The VCO oscillates 165.0500 MHz to 163.2750 MHz under the transmission condition and 134.3500 MHz to 141.5750 MHz under the reception condition. The VCO consists of the clip oscillator of the QV3, and contains the oscillator frequency of approximately 21.7MHz during the transmission/reception conversion. That is since the VCO should oscillate relatively low frequency during reception compared to transmission, the DV2 is directly biased by the QV2.

Therefore as a result, the CV21 is added in parallel to the resonance circuit of the VCO to oscillate a low frequency. During transmission, a relatively high frequency should be oscillating compared to reception. Therefore, the DV2 is adversely biased by the QV2, and as a result, the CV21, which is added unparallel to the circuit of the VCO is removed to oscillate the desired transmission frequency.

The IC11 PLL IC controls the VCO in order to oscillate the accurate frequency. The output frequency of the VCO is supplied to the 44th pin of IC3. At the IC3, TCXO(21.250MHz) by the TCXO-1 is compared to the output frequency of the VCO.

The VCO is controlled the loop filter consisted of the RL2, RL3, RL4 and the CL1 in order to oscillate the stable frequency wanted for the radio.

The VCO controlled voltage which has passed the loop filter is supplies to the DV1 varactor diode, and the VCO oscillate the PLL programmed frequency by the capacity variation in the DV1. In addition, the LV1 on the VCO circuit function as frequency for the VCO to be properly controlled.

RX/TX Buffer Amplifier (QF1)

The RF signal oscillate at the VCO is provide to the QF1 RX 1st mixer through the QF1 during the reception, and is provide to the QT2 power driver amplifier through the QT3 during the transmission.

PLL Frequency Synthesizer (AN 6311)

The PLL synthesizer of the signal loop PLL circuit with the reference of 6.25 kHz. The IC3 includes all the function such as the reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider.

At the reference oscillator, the 21.250 MHz TCXO of the TCXO is connected to the pin 52,53 of the IC3 to oscillate the frequency of 21.250MHz. The TCXO (21.250MHz) is the temperature compensation circuit to maintain the frequency within the allowable error range even under a low temperature of -20°C.

The phase detector sends out the output power to the loop filter through 44 pin of the IC3. IF the oscillation frequency of the VCO is low compared to the referenced frequency, the phase detector sends out the output power in positive pulse. If the oscillation frequency of the VCO is high, phase detector send out can maintain the frequency set.

The programmable divider maintains the desired frequency with control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below:

$N = \text{VCO oscillation frequency} / \text{reference frequency}$

If the desired frequency is 156.050 MHz

$N = 156.050 \text{ MHz} / 0.00625 \text{ MHz} = 24968$