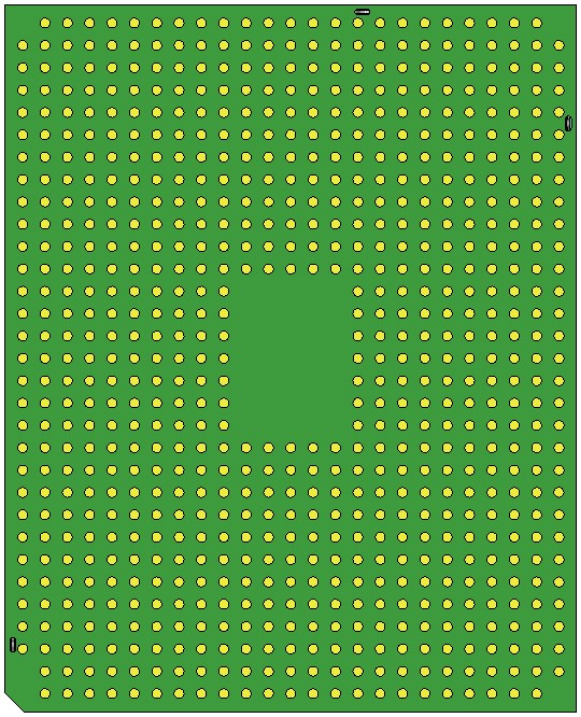

User Manual

Product Name: IMQC

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Revision: 1.0

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Revision History

Rev. #	Author	Summary of Changes	Date
0.1	WNC	First release	2021/10/11
0.2	WNC	Added SMT recommendation	2021/10/12
0.3	WNC	Added module test recommendation after reflow	2021/11/17
0.4	WNC	1. Update module test recommendation after reflow 2. Add GPS external circuit 3. Antennas map table update	2021/11/22
0.5	WNC	Update Steel Stencil Design	2021/11/22
0.6	WNC	Update Module test---RF Function Check	2021/11/23
0.7	WNC	Add note for USB2.0 interface is recommended to bring out on main board to proceed with module test	2021/11/23
0.8	WNC	Update LTE/5G Conducted Sensitivity	2022/01/03
0.9	WNC	Update design guide chapter	2022/02/25
1.0	WNC	Rearrange the Chapter order. Update Antenna Mapping	2022/03/08
1.1	WNC	Add section 4.4.4 : Antenna gain limits	2022/03/28

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Contents

1. Introduction

IMQC is a 5G NR BGA module support NSA and SA modes. It consists of processors with integrated LTE and 5G modems capable of supporting 5G Sub6-GHz radio. The key radio features of IMQC are the ULCA of LTE and Sub6-GHz, detail is described in the RF section. IMQC also supports dual-connectivity framework of the 3GPP standard Release 16.

IMQC is designed with flexibility and scalability in order to provide the unifying connectivity platform for three main categories of 5G services: enhanced mobile broadband, mission-critical control, and massive Internet of Things – each driving a very diverse set of requirements.

The module is able to support a variety of services including wide coverage, high throughput, enhanced capacity and low latency. It also support wide range of devices including low-data rate sensors at 10s of kbps to new immersive mobile experiences at multi-Gbps.

In addition to supporting a wide range of services, it supports a wide array of spectrum available across regulatory standards and spectrum including low-bands below 1 GHz, and mid-high/UHB bands between 1.7 GHz and 4.2 GHz, which will open up vast amount of bandwidths for extreme data rates and capacity that were previously not usable for wide-area mobile communications.

This document consists of several technical sections including, Electrical Specifications, RF Specifications, Power, SW Features and Tools, SW Guideline, Mechanical concept, Thermal considerations, Regulatory Compliance and Certification, Environmental Requirements, Packaging and Safety Recommendation.

1.1. RF band support

This section lists the main features and functions that the IMQC module supports in the table.

IMQC module overview

Module	5G	LTE	GNSS	Temperature Grade
IMQC	v	v	v	Consumer

1.“ √ ” indicates supporting. “ × ” indicates not supporting.

1.2. Features

Feature Lists:

- 5G bands/modes
  - 5GNR, NSA/SA, FR1
  - n77 (DL 4x4 MIMO, UL 2x2 MIMO, 8Rx, SRS)
  - n2, n30, n66 (DL 4x4 MIMO)
  - n5, n12 (DL 2x2 MIMO)
- LTE bands/modes:
  - LTE DL CAT 20, UL CAT 18
  - B2/30/66 (DL 4x4 MIMO)
  - B5/12/29 (DL 2x2 MIMO)
  - B14 (DL 2x2 MIMO)
- HPUE (PC2) for n77 (TDD)
- GNSS L1/L5
- Compliant with 3GPP release 16
- Application CPU: Quad ARM Cortex-A55 operating up to 2.0GHz
- Modem: Qualcomm SDX65 modem
- Linux OS
- Memory size: 4Gb LPDDR4X SDRAM and 4Gb NAND Flash (can be extended to 8Gb+8Gb)
- Power management systems
- Interfaces
  - RESET_N X1
  - PMIC ADC X 1
  - Clock_32.768K X 1

- PCIE GEN3 2-Lane X 1
- USB 3.1 & USB 2.0 X1
- GPIO x 25
- I2S/PCM x 1
- SDIO x1
- Debug_UART x1
- UARTx2
- RFFE X3
- I2C X1
- SPI x 1
- SIM x 1
- JTAG X 1
- GNSS L1 /L5

1.3. Connection Interface

The IMQC module is LGA device. All electrical connections are made though the 735 pads on the bottom side of a PCB.

1.4. Environmental Specifications and Certifications

1.4.1 Environmental Specifications

The environmental specifications for both operating and storage conditions are defined in the Table below.

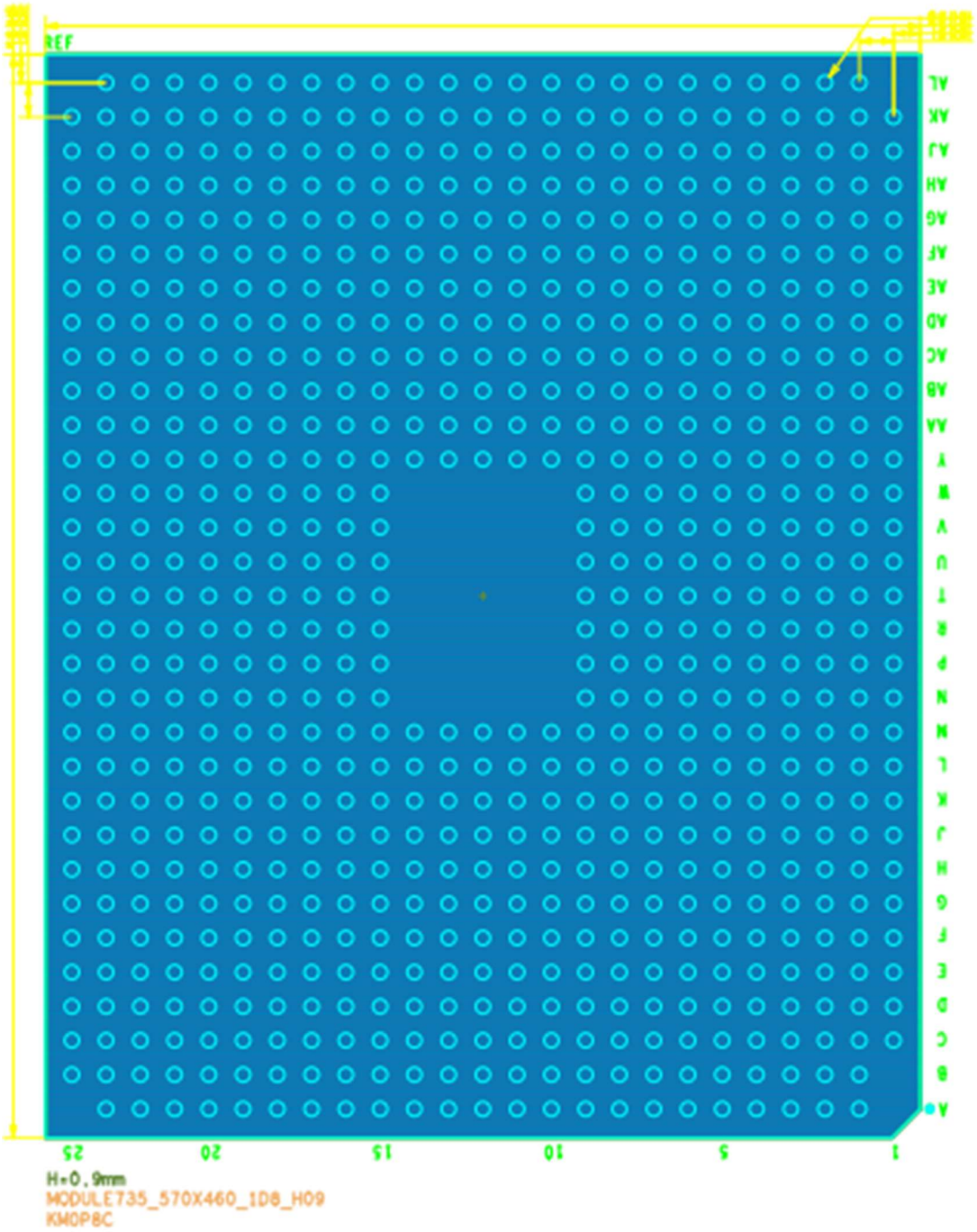
Condition	Temperature Range	Remark
Normal operating temperature range	–15 °C to 55°C	Fully functional and in compliance with 3GPP specifications
Extended operating temperature range	–40 °C to 85°C	RF performance may be affected outside the normal range, but the module will still function.
Storage	–40 °C to 85 °C	

Note: All temperatures above refer to ambient temperatures.

2. Pin Definitions

2.1. LGA Module Pin Diagram

The IMQC LGA module pin layout is illustrated below.



LGA pad diagram (top view)

2.2. LGA Module Pin Definitions

I/O type description:

- AO: Analog Output
- AI: Analog Input
- AIO: Analog bi-direction
- DO: Digital Output
- DI: Digital Input
- DIO: Digital bi-direction
- P: Power
- PI: Power input
- PO: Power output
- GND
- NC

Table 2-1 Pin Interface Family

Signal							
Power On Trigger , Reset, Force Download					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
1	G5	CBL_PWR_N(PMX65_GPIO3)	Power On	DI	1.7	1.8	1.95
2	A6	KPD_PWR_N	Power On	DI	1.7	1.8	1.95
3	F2	RESET_N	Reset input	DI	1.7	1.8	1.95
4	J19	FORCED_USB_BOOT	Force Download	DI	1.7	1.8	1.95
5	D3	FAULT_N	PMIC_Fault	DIO	1.7	1.8	1.95
PCIE and Control Signal					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
6	N25	PCIE_WAKE_N	PCIE	DIO	1.62	1.8	1.98
7	M25	PCIE_CLK_REQ_N	PCIE	DIO	1.62	1.8	1.98
8	L25	PCIE_RST_N	PCIE	DIO	1.62	1.8	1.98
9	C11	PCIE_REFCLK_M	PCIE	AIO		Note1	

10	C10	PCIE_REFCLK_P	PCIE	AIO		Note1	
11	B9	PCIE_RX0_M	PCIE	AIO		Note1	
12	B8	PCIE_RX0_P	PCIE	AIO		Note1	
13	A9	PCIE_RX1_M	PCIE	AIO		Note1	
14	A8	PCIE_RX1_P	PCIE	AIO		Note1	
15	A13	PCIE_TX0_M	PCIE	AIO		Note1	
16	A12	PCIE_TX0_P	PCIE	AIO		Note1	
17	B13	PCIE_TX1_M	PCIE	AIO		Note1	
18	B12	PCIE_TX1_P	PCIE	AIO		Note1	
USB3.1 & USB2.0					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
19	B17	USB_SS_RX_M	USB 3.1	AIO		Note2	
20	B16	USB_SS_RX_P	USB 3.1	AIO		Note2	
21	A19	USB_SS_TX_M	USB 3.1	AIO		Note2	
22	A18	USB_SS_TX_P	USB 3.1	AIO		Note2	
23	B21	USBC_HS_D_M	USB 2.0	AIO		Note2	
24	B20	USBC_HS_D_P	USB 2.0	AIO		Note2	
UART and I2C					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
25	E25	I2C_SDA(GPIO_10)	I2C0	DIO	1.62	1.8	1.98
26	D25	I2C_SCL(GPIO_11)	I2C0	DIO	1.62	1.8	1.98
27	K19	UART1_TX(GPIO_48)	UART1	DIO	1.62	1.8	1.98
28	K20	UART1_RX(GPIO_49)	UART1	DIO	1.62	1.8	1.98
29	G7	UART0_TX(GPIO_63)	UART0	DIO	1.62	1.8	1.98
30	F8	UART0_RX(GPIO_64)	UART0	DIO	1.62	1.8	1.98
31	F7	UART0_CTS/I2C_SDA(GPIO_65)	UART0/I2C1	DIO	1.62	1.8	1.98
32	E8	UART0_RFR/I2C_SCL(GPIO_66)	UART0/I2C1	DIO	1.62	1.8	1.98
SPI					Voltage Level (V)		

Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
33	J10	SPI_MOSI(GPIO_04)	SPI0	DIO	1.62	1.8	1.98
34	J9	SPI_MISO(GPIO_05)	SPI0	DIO	1.62	1.8	1.98
35	J8	SPI_CS_N(GPIO_06)	SPI0	DIO	1.62	1.8	1.98
36	J7	SPI_CLK(GPIO_07)	SPI0	DIO	1.62	1.8	1.98
37	J25	SLIC_SPI_MOSI(GPIO_16)	SPI1	DIO	1.62	1.8	1.98
38	H25	SLIC_SPI_MISO(GPIO_17)	SPI1	DIO	1.62	1.8	1.98
39	K25	SLIC_SPI_CS(GPIO_18)	SPI1	DIO	1.62	1.8	1.98
40	G25	SLIC_SPI_CLK(GPIO_19)	SPI1	DIO	1.62	1.8	1.98
I2S or PCM					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
41	H22	I2S_MCLK(GPIO_62)	I2S	DIO	1.62	1.8	1.98
42	H23	PCM_SYNC/I2S_WS(GPIO_12)	I2S/PCM	DIO	1.62	1.8	1.98
43	J23	PCM_RX_IN/I2S_Data0(GPIO_13)	I2S/PCM	DIO	1.62	1.8	1.98
44	K23	PCM_TX_OUT/I2S_Data1(GPIO_14)	I2S/PCM	DIO	1.62	1.8	1.98
45	G23	PCM_PCLK/I2S_SCK(GPIO_15)	I2S/PCM	DIO	1.62	1.8	1.98
RFFE					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
46	G12	RFFE0_DATA(GPIO_36)	REFE0	DIO	1.62	1.8	1.98
47	G11	RFFE0_CLK(GPIO_37)	REFE0	DIO	1.62	1.8	1.98
48	H12	RFFE1_DATA(GPIO_38)	REFE1	DIO	1.62	1.8	1.98
49	H11	RFFE1_CLK(GPIO_39)	REFE1	DIO	1.62	1.8	1.98
50	E11	RFFE3_DATA(GPIO_27)	REFE3	DIO	1.62	1.8	1.98
51	F11	RFFE3_CLK(GPIO_26)	REFE3	DIO	1.62	1.8	1.98
SIM					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.

52	C6	UIM1_DATA(GPIO_67)	SIM1	DIO	1.7	1.8	1.98
53	C5	UIM1_PRESENT(GPIO_68)	SIM1	DIO	1.7	1.8	1.98
54	C4	UIM1_RESET(GPIO_69)	SIM1	DIO	1.7	1.8	1.98
55	C3	UIM1_CLK(GPIO_70)	SIM1	DIO	1.7	1.8	1.98
56	B4	NC40					
57	A5	NC41					
58	A4	NC42					
59	A3	NC43					
SDIO Interface(Note5)					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
60	F25	RESOUT_N	Reset Output	DO	1.62	1.8	1.98
61	A22	SDC_CLK	SDIO	DO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
62	C24	SDC_CMD	SDIO	DO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
63	D22	SDC_DATA_0	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
64	C22	SDC_DATA_1	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
65	C23	SDC_DATA_2	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
66	D23	SDC_DATA_3	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
67	C25	SDC_DATA_4(GPIO_98)	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
68	A23	SDC_DATA_5(GPIO_99)	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6

69	B23	SDC_DATA_6(GPIO_100)	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
70	B24	SDC_DATA_7(GPIO_101)	SDIO	DIO	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
JTAG					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
71	G8	JTAG_SRST_N	JTAG	DI	1.62	1.8	1.98
72	E10	JTAG_TCK	JTAG	DI	1.62	1.8	1.98
73	E9	JTAG_TDI	JTAG	DI	1.62	1.8	1.98
74	F9	JTAG_TDO	JTAG	DO	1.62	1.8	1.98
75	G9	JTAG_TMS	JTAG	DI	1.62	1.8	1.98
76	F10	JTAG_TRST_N	JTAG	DI	1.62	1.8	1.98
DBI interface and Control Signal					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
77	E21	NC19					
78	F22	NC20					
79	E22	NC21					
80	F20	NC22					
81	F21	NC23					
82	D21	NC24					
83	G20	NC25					
84	E20	NC26					
85	F24	NC27					
86	G21	NC28					
87	D24	NC29					
88	G22	NC30					
89	F23	NC31					

90	E23	NC32					
91	E24	NC33					
Debug UART					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
92	D15	DBG_UART_TX(GPIO_8)	DB UART	DO	1.62	1.8	1.98
93	C15	DBG_UART_RX(GPIO_9)	DB UART	DI	1.62	1.8	1.98
GPIO					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
94	L4	NC1					
95	H7	NC2					
96	F4	NC3					
97	E3	NC4					
98	H5	NC5					
99	H6	NC6					
100	K4	NC7					
101	K5	NC8					
102	F1	NC9					
103	C7	NC10					
104	G4	NC11					
105	E4	NC12					
106	F3	NC13					
107	E1	NC14					
108	J6	NC15					
109	G3	NC16					
110	G2	NC17					
111	G1	NC18					
112	G13	GPIO_31	SDX65_GPIO	DIO	1.62	1.8	1.98

113	J13	GPIO_32	SDX65_GPIO	DIO	1.62	1.8	1.98
114	H9	NC34					
115	F12	NC35					
116	H10	NC36					
117	D13	GPIO_44	SDX65_GPIO	DIO	1.62	1.8	1.98
118	D14	GPIO_45	SDX65_GPIO	DIO	1.62	1.8	1.98
119	J22	GPIO_47	SDX65_GPIO	DIO	1.62	1.8	1.98
120	H21	NC37					
121	H20	NC38					
122	H19	NC39					
123	J5	GPIO_80	SDX65_GPIO	DIO	1.62	1.8	1.98
124	L5	GPIO_81	SDX65_GPIO	DIO	1.62	1.8	1.98
125	J4	GPIO_82	SDX65_GPIO	DIO	1.62	1.8	1.98
126	H4	GPIO_83	SDX65_GPIO	DIO	1.62	1.8	1.98
127	P24	GPIO_86	SDX65_GPIO	DIO	1.62	1.8	1.98
128	K18	GPIO_87	SDX65_GPIO	DIO	1.62	1.8	1.98
129	D12	GPIO_88	SDX65_GPIO	DIO	1.62	1.8	1.98
130	E12	GPIO_91	SDX65_GPIO	DIO	1.62	1.8	1.98
131	H13	GPIO_92	SDX65_GPIO	DIO	1.62	1.8	1.98
132	J14	GPIO_93	SDX65_GPIO	DIO	1.62	1.8	1.98
133	J21	GPIO_94	SDX65_GPIO	DIO	1.62	1.8	1.98
134	K21	GPIO_95	SDX65_GPIO	DIO	1.62	1.8	1.98
135	H14	GPIO_96	SDX65_GPIO	DIO	1.62	1.8	1.98
136	J15	GPIO_97	SDX65_GPIO	DIO	1.62	1.8	1.98
137	K24	GPIO_102	SDX65_GPIO	DIO	1.62	1.8	1.98
138	J20	GPIO_104	SDX65_GPIO	DIO	1.62	1.8	1.98
139	R24	GPIO_103	SDX65_GPIO	DIO	1.62	1.8	1.98
140	K22	GPIO_105	SDX65_GPIO	DIO	1.62	1.8	1.98

141	H24	GPIO_106	SDX65_GPIO	DIO	1.62	1.8	1.98
142	J24	GPIO_107	SDX65_GPIO	DIO	1.62	1.8	1.98
Clock and charger configure					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
143	B3	RFCLK3	WLAN Clock	AO	1.02	1.05	1.08
144	E2	PMK_Sleep_Clk	32.768KHz Clock	AO	1.62	1.8	1.98
145	D1	SPMI_CLK(Note4)	SPMI_CLK	DIO	1.62	1.8	1.98
146	D2	SPMI_DATA(Note4)	SPMI_Data	DIO	1.62	1.8	1.98
147	D8	PMX_AMUX5(Note3)	Set Charger configure	AI	0	-	1.875
PMX65_ADC					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
148	D7	PMX_AMUX6	PMIC_ADC	AI	0	-	1.875
RF (Antenna Port)					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
149	AL11	ANT0	RF	AIO			
150	AL13	ANT1	RF	AIO			
151	AL17	ANT2	RF	AIO			
152	AL15	ANT3	RF	AIO			
153	AL19	ANT4	RF	AIO			
154	AJ25	ANT5	RF	AIO			
155	AL23	ANT6	RF	AIO			
156	AL21	ANT7	RF	AIO			
157	W25	ANT12	RF	AIO			
158	U25	ANT13	RF	AIO			
GPS_L1/L5 EN					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.

159	P25	GNSS_ELNA_L1_EN/UART1_CTS (GPIO_22)	GPS_L1_En	DO	1.62	1.8	1.98
160	R25	GNSS_ELNA_L5_EN/UART1_RFR (GPIO_23)	GPS_L5_En	DO	1.62	1.8	1.98

Note1: Refer to section 2.5 PCIE standard for more electronic characteristics.

Note2: Refer to section 2.4 USB standard for more electronic characteristics.

Note3: PMX_AMUX5 pin is used for external charge configuration, there is a default 26.7kohm pull down resistor connected to PMX_AMUX5 pin in the module and configure to no charger function, so PMX_AMUX5 is recommend to keep floating.

Note4: SPMI_CLK/ SPMI_DATA pin are interface between the Module and external charger chip, the module configure to no charger function, so SPMI_CLK/ SPMI_DATA is recommend to keep floating.

Note5: SDIO IO Interface (exception RESOUT_N pin) can provide two types of voltages (1.8V/2.95V), refer to JESD84-B51---Embedded Multi-Media Card (eMMC) Electrical Standard (5.1).

Power (Please refer to Sec2.2)							
System Power					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
161	L3	VPH_PWR	System Power	P	3.3	3.8	4.3
162	L2	VPH_PWR	System Power	P	3.3	3.8	4.3
163	L1	VPH_PWR	System Power	P	3.3	3.8	4.3
164	K3	VPH_PWR	System Power	P	3.3	3.8	4.3
165	K2	VPH_PWR	System Power	P	3.3	3.8	4.3
166	K1	VPH_PWR	System Power	P	3.3	3.8	4.3
167	J3	VPH_PWR	System Power	P	3.3	3.8	4.3
168	J2	VPH_PWR	System Power	P	3.3	3.8	4.3
169	J1	VPH_PWR	System Power	P	3.3	3.8	4.3
170	H3	VPH_PWR	System Power	P	3.3	3.8	4.3
171	H2	VPH_PWR	System Power	P	3.3	3.8	4.3

172	H1	VPH_PWR	System Power	P	3.3	3.8	4.3
173	M1	VREG_DBB1_3P3	System Voltage	P	VPH_PWR / EXT_3V3		
174	M2	VREG_DBB1_3P3	System Voltage	P	VPH_PWR / EXT_3V3		
175	N5	VPH_PWRS	RF Power	P	3.3	3.8	4.3
176	M5	VPH_PWRS	RF Power	P	3.3	3.8	4.3
177	P6	VPH_PWRS	RF Power	P	3.3	3.8	4.3
178	N6	VPH_PWRS	RF Power	P	3.3	3.8	4.3
179	M6	VPH_PWRS	RF Power	P	3.3	3.8	4.3
180	L6	VPH_PWRS	RF Power	P	3.3	3.8	4.3
181	P7	VPH_PWRS	RF Power	P	3.3	3.8	4.3
182	N7	VPH_PWRS	RF Power	P	3.3	3.8	4.3
183	M7	VPH_PWRS	RF Power	P	3.3	3.8	4.3
184	L7	VPH_PWRS	RF Power	P	3.3	3.8	4.3
VBUS					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
185	H8	VBUS_DET	USB_VBUS	P	4.75	5	5.25
SDIO_IO Power					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
186	C18	VREG_LDO_SDC(Note6)	SDIO IO Voltage	P	1.7/ 2.7	1.8/ 2.95	1.95/ 3.6
SIMVCC1					Voltage Level (V)		
Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
187	B6	SIMVCC1(VREG_L11_1P8)	SIM1 Power	P	1.7	1.8	1.98
188	B5	NC44					
Output Voltage					Voltage Level (V)		

Pin Count	Pin Number	Pin Name	Function	Type	Min.	Typ.	Max.
189	D5	VREG_S4_1P9	Output Voltage 1V9	P	1.824	1.88	2
190	D4	VREG_S4_1P9	Output Voltage 1V9	P	1.824	1.88	2
191	K7	VREG_L6_1P8	Output Voltage 1V8	P	1.62	1.8	1.98
192	C2	VREG_1P8_SYS	Output Voltage 1V8	P	1.7	1.8	1.95
193	E7	VREG_L10_3P1	Output Voltage 3V1	P	3	3.088	3.1

Note6: VREG_LDO_SDC is for SDIO Supply IO voltage, it can provide two types of voltages (1.8V/2.95V), refer to JESD84-B51---Embedded Multi-Media Card (eMMC) Electrical Standard (5.1).

GND	
GND	
Pin Count	Pin Number
194~ 735	AH25,AG25,AF25,AE25,AD25,AC25,AB25,AA25,Y25,V25,T25,B25,AK14,AJ14,AH14,AG14,AF14,AE14,AD14,AC14,AB14,AA14,Y14,L14,K14,G14,F14,E14,B14,AK19,AJ19,AH19,AG19,AF19,AE19,AD19,AC19,AB19,AA19,Y19,W19,V19,U19,T19,R19,P19,N19,M19,L19,M24,N24,N23,G19,F19,E19,D19,C19,B19,AK8,AJ8,AH8,AG8,AF8,AE8,AD8,AC8,AB8,AA8,Y8,W8,V8,U8,T8,R8,P8,N8,M8,L8,C8,B2,AK22,AJ22,AH22,AG22,AF22,AE22,AD22,AC22,AB22,AA22,Y22,W22,V22,U22,T22,R22,P22,N22,G24,B22,D20,AK11,AJ11,AH11,AG11,AF11,AE11,AD11,AC11,AB11,AA11,Y11,L11,K11,J11,N1,P1,A15,B11,AK16,AJ16,AH16,AG16,AF16,AE16,AD16,AC16,AB16,AA16,Y16,W16,V16,U16,T16,R16,P16,N16,M16,L16,K16,J16,H16,G16,F16,E16,D16,C16,A16,AK5,AJ5,AH5,AG5,AF5,AE5,AD5,AC5,AB5,AA5,Y5,W5,V5,U5,T5,R5,P5,R2,P2,F5,E5,AK24,AJ24,AH24,AG24,AF24,AE24,AD24,AC24,AB24,AA24,Y24,W24,V24,U24,T24,A24,AK13,AJ13,AH13,AG13,AF13,AE13,AD13,AC13,AB13,AA13,Y13,L13,K13,T2,F13,E13,C13,A11,AK18,AJ18,AH18,AG18,AF18,AE18,AD18,AC18,AB18,AA18,Y18,W18,V18,U18,T18,R18,P18,N18,M18,L18,M23,J18,H18,G18,F18,E18,D18,B18,AK7,AJ7,AH7,AG7,AF7,AE7,AD7,AC7,AB7,AA7,Y7,W7,V7,U7,T7,R7,N3,K6,K8,K9,B7,AK21,AJ21,AH21,AG21,AF21,AE21,AD21,AC21,AB21,AA21,Y21,W21,V21,U21,T21,R21,P21,N21,M21,L21,M22,L23,R23,C21,A21,AK10,AJ10,AH10,AG10,AF10,AE10,AD10,AC10,AB10,AA10,Y10,L10,K10,G10,D10,B10,AK15,AJ15,AH15,AG15,AF15,AE15,AD15,AC15,AB15,AA15,Y15,W10,V10,U10,T10,R10,P10,N10,M10,L15,K15,H15,G15,F15,E15,B15,AK4,AJ4,AH4,AG4,AF4,AE4,AD4,AC4,AB4,AA4,Y4,W4,V4,U4,T4,R4,P4,N4,M4,AJ1,AH1,AG1,AF1,AE1,AD1,AC1,AB1,AA1,Y1,W1,V1,U1,T1,D11,C1,AK2,AJ2,AH2,AG2,AF2,AE2,AD2,AC2,AB2,AA2,Y2,W2,V2,U2,C14,A2,AK3,AJ3,AH3,AG3,AF3,AE3,AD3,AC3,AB3,AA3,Y3,W3,V3,U3,T3,M3,AK23,AJ2	

	3,AH23,AG23,AF23,AE23,AD23,AC23,AB23,AA23,Y23,W23,V23,U23,T23,AK12,AJ12,AH12,AG12,AF12,AE12,AD12,AC12,AB12,AA12,Y12,L12,K12,J12,R1,A14,C12,A10,AK17,AJ17,AH17,AG17,AF17,AE17,AD17,AC17,AB17,AA17,Y17,W17,V17,U17,T17,R17,P17,N17,M17,L17,K17,J17,H17,G17,F17,E17,D17,C17,A17,AK6,AJ6,AH6,AG6,AF6,AE6,AD6,AC6,AB6,AA6,Y6,W6,V6,U6,T6,R6,N2,R3,P3,G6,F6,E6,D6,AK20,AJ20,AH20,AG20,AF20,AE20,AD20,AC20,AB20,AA20,Y20,W20,V20,U20,T20,R20,P20,N20,M20,L20,L24,L22,P23,C20,A20,AK9,AJ9,AH9,AG9,AF9,AE9,AD9,AC9,AB9,AA9,Y9,W9,V9,U9,T9,R9,P9,N9,M9,L9,D9,C9,A7,M11,M12,M13,M14,M15,AK1,AK25,AL2,AL3,AL4,AL5,AL6,AL7,AL8,AL9,AL10,AL12,AL14,AL16,AL18,AL20,AL22,AL24

3. Electrical Specifications

3.1. Power supply

The IMQC module receives and supplies power with the following potentials:

Pin name	Pin Number	Description	Type	Input range(V)		
				Min.	Typ.	Max.
VPH_PWR	L3,L2,L1,K3,K2,K1,J3,J2 ,J1,H3,H2,H1	System Power	PI	3.3	3.8	4.3
VPH_PWRS	N5,M5,P6,N6,M6,L6,P7 ,N7,M7,L7	RF Power	PI	3.3	3.8	4.3
VREG_DBB1_3P3	M1,M2	System Voltage	PI	3.3	3.8	4.3
VREG_LDO_SDC	C18	SDIO IO Voltage	PI	1.7	1.8	1.95
VBUS_DET	H8	VUSB Detection	PI	4.75	5	5.25
VREG_S4_1P9	D5,D4	Output Voltage 1V9	PO	1.824	1.88	2
VREG_1P8_SYS	C2	Output Voltage 1V8	PO	1.7	1.8	1.95
VREG_L10_3P1	E7	Output Voltage 3V1	PO	3	3.088	3.1
VREG_L6_1P8	K7	IO Voltage	PO	1.62	1.8	1.98

SIMVCC1	B6	SIM1 Power	PO	1.7	1.8	1.98

4. RF Specifications

4.1. LTE Conducted Power

LTE Conducted Power

Band	Items	Parameter	Unit	Design Target
Band 2	Max. TX Power	20MHz 1RB/QPSK	dBm	23
Band 5	Max. TX Power	20MHz 1RB/QPSK	dBm	23
Band 12	Max. TX Power	20MHz 1RB/QPSK	dBm	23
Band 14	Max. TX Power	20MHz 1RB/QPSK	dBm	23
Band 30	Max. TX Power	20MHz 1RB/QPSK	dBm	22
Band 66	Max. TX Power	20MHz 1RB/QPSK	dBm	23

LTE B2,5,12,14,66 Tolerance: +/- 2.7 dB

LTE B30 Tolerance: +/- 1.5 dB

4.2. 5G Conducted Power

5G Conducted Power

Band	Items	Parameter	Unit	Design Target
n2	Max. TX Power	DFT-s-OFDM QPSK	dBm	23
n5	Max. TX Power	DFT-s-OFDM QPSK	dBm	23
n12	Max. TX Power	DFT-s-OFDM QPSK	dBm	23
n30	Max. TX Power	DFT-s-OFDM QPSK	dBm	22
n66	Max. TX Power	DFT-s-OFDM QPSK	dBm	23
n77	Max. TX Power	DFT-s-OFDM QPSK	dBm	25

n2, n5, n12, n66 Tolerance: +/- 2.7 dB

n30, n77 Tolerance: +/- 1.5 dB

4.3. LTE/5G Conducted Sensitivity

Minimum Conductive Sensitivity

Band	RX0	RX1	RX2	RX3	RX4	RX5	RX6	RX7
LTE B2	-93.3	-93.3	-93.3	-93.3	-93.3			
LTE B5	-91.3	-91.3						
LTE B12	-90.3	-90.3						
LTE B14	-90.3	-90.3						
LTE B29	-91	-91						
LTE B30	-92.3		-92.3	-92.3	-92.3			
LTE B66	-92.8	-92.8	-92.8	-92.8	-92.8			
Sub 6G n77	-92.6	-92.6	-92.6	-92.6	-92.6	-92.6	-92.6	-92.6

Condition:

LTE: QPSK/BW 10MHz with Full RBs

Sub 6G: QPSK/BW 10MHz/SCS 30kHz

4.4. Antennas Map

4.4.1 LTE

Band	Uplink (UL) MHz	Downlink (DL) MHz	ANT0		ANT1		ANT2	ANT3	ANT4	ANT5	ANT6	ANT7	ANT12	ANT13
			Pin AL11		Pin AL13		Pin AL17	Pin AL15	Pin AL19	Pin AJ25	Pin AL23	Pin AL21	Pin W25	Pin U25
			TX0	RX0	TX1	RX1	RX2	RX3	RX4	RX5	RX6	RX7	GPS RX	GPS RX
B29	N/A	717-728		V		V								
B12	699-716	729-746	V	V		V								
B14	788-798	758-768	V	V		V								
B5	824-849	869-894	V	V		V								
B66	1710-1780	2110-2200	V[1]	V[1]	V	V	V	V	V[1]					
B2	1850-1910	1930-1990	V[2]	V[2]	V	V	V	V	V[2]					
B30	2305-2315	2350-2360			V	V	V	V	V					

4.4.2 5G

Band	Uplink (UL) MHz	Downlink (DL) MHz	ANT0		ANT1		ANT2	ANT3	ANT4	ANT5	ANT6	ANT7	ANT12	ANT13
			Pin AL11		Pin AL13		Pin AL17	Pin AL15	Pin AL19	Pin AJ25	Pin AL23	Pin AL21	Pin W25	Pin U25
			TX0	RX0	TX1	RX1	RX2	RX3	RX4	RX5	RX6	RX7	GPS RX	GPS RX
n12	699-716	729-746	V	V		V								
n5	824-849	869-894	V	V		V								
n66	1710-1780	2110-2200	V[3]	V[3]	V	V	V	V	V[3]					
n2	1850-1910	1930-1990	V[4]	V[4]	V	V	V	V	V[4]					
n30	2305-2315	2350-2360			V	V	V	V	V					
n77	3300-4200		V[5,6]	V	V[5,6]	V	V[6]	V[6]	V[6]	V[6]	V[6]	V[6]		

4.4.3 GPS

Band	Downlink (DL) MHz	ANT12	ANT13
		Pin W25	Pin U25
		GPS RX	GPS RX
GPS_L1	1575.42	V	
GPS_L5	1176.45		V

Note1: LTE B66 Tx/Rx works on ANT0 instead of ANT4 as the CA ENDC combos include

LTE B66/LTE B2 transmit simultaneously or

LTE B66/LTE B30 transmit simultaneously or

LTE B66/5G n2 transmit simultaneously or

LTE B66/5G n30 transmit simultaneously.

Note2: LTE B2 Tx/Rx works on ANT0 instead of ANT4 as the CA ENDC combos include

LTE B2/LTE B30 transmit simultaneously or

LTE B2/5G n30 transmit simultaneously or

LTE B2/LTE B66 transmit simultaneously or

LTE B2/ 5G n66 transmit simultaneously.

Note3: 5G n66 Tx/Rx works on ANT0 instead of ANT4 as the CA ENDC combos include

5G n66/LTE B2 transmit simultaneously or

5G n66/LTE B30 transmit simultaneously or

5G n66/5G n30 transmit simultaneously.

Note4: 5G n2 Tx/Rx works on ANT0 instead of ANT4 as the CA ENDC combos include

5G n2/LTE B30 transmit simultaneously.

Note5: Uplink MIMO is supported for 5G n77 and its combined power can be up to PC1.5.

Note6: n77 SRS function work on ANT0~ANT7.

Note7: The cells highlighted with color are single band default antenna.

4.4.4 Antenna gain Limits

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss is a mobile-only exposure condition must not exceed the limits below.

Band	Frequency (MHz)	Max Antenna Gain(dBi)
LTE Band 2	1850~1910	**7.3**
LTE Band 5	824~849	**8.7**
LTE Band 12	699~716	**7.9**
LTE Band 14	788~798	**8.5**
LTE Band 30	2305~2315	**0.5**
LTE Band 66	1710~1780	**4.3**
LTE CA Band 5B	824~849	**8.7**
5G NR n2	1850~1910	**7.3**
5G NR n5	824~849	**8.7**
5G NR n12	699~716	**7.9**
5G NR n30	2305~2315	**0.5**
5G NR n66	1710~1780	**4.3**
5G NR n77	3450~3550 3700~3980	**3.5**

5. Software Interface

5.1. USB Interface

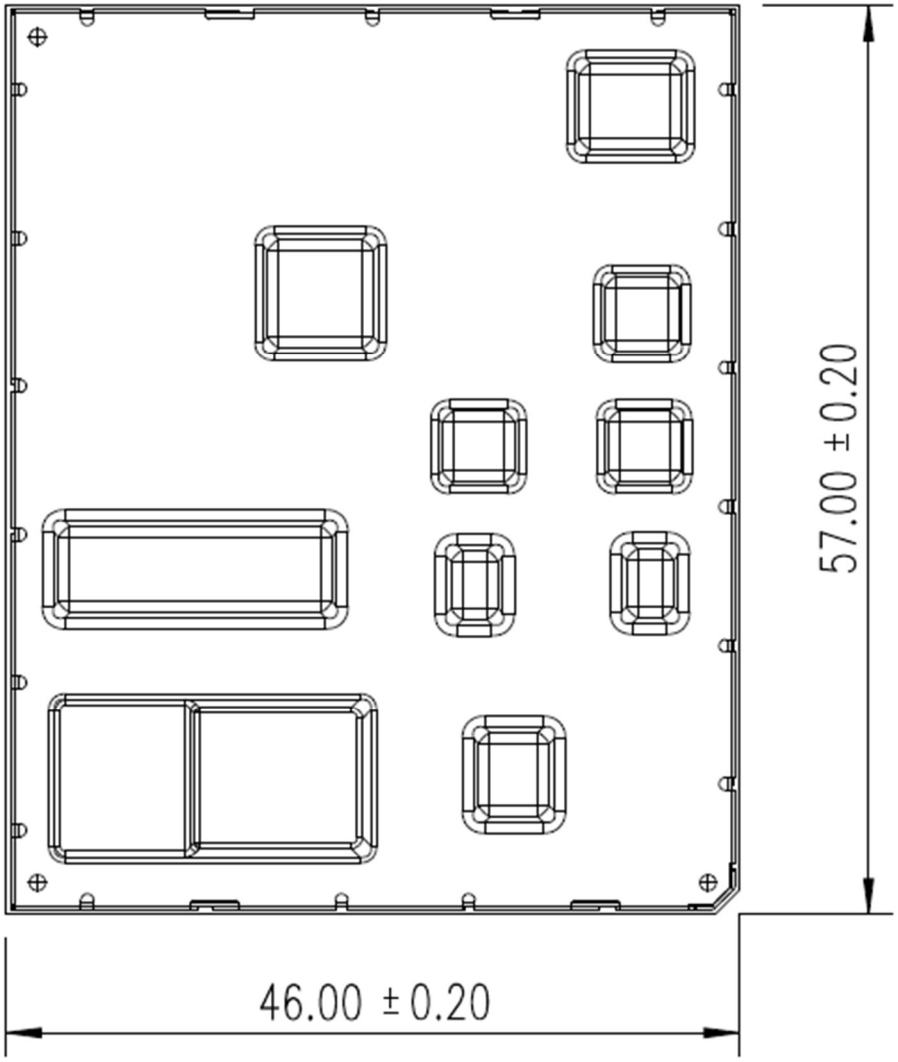
The IMQC module supports 3GPP's standard AT commands and proprietary AT commands.

6. Mechanical and Miscellaneous

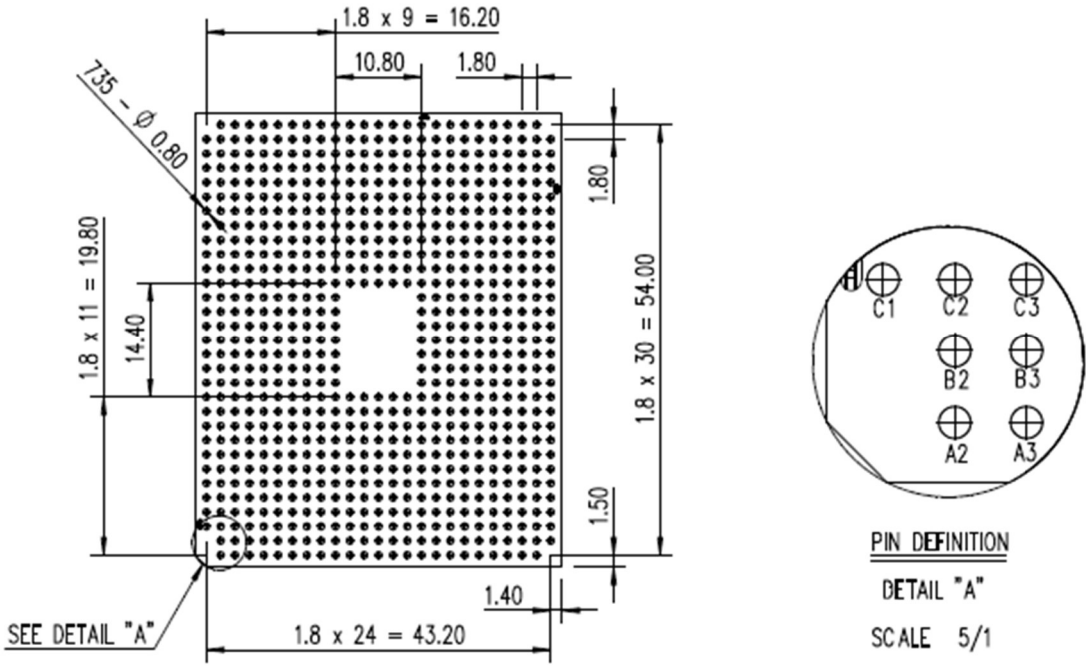
6.1. PCBA Form Factor

The dimensions of IMQC module as below:

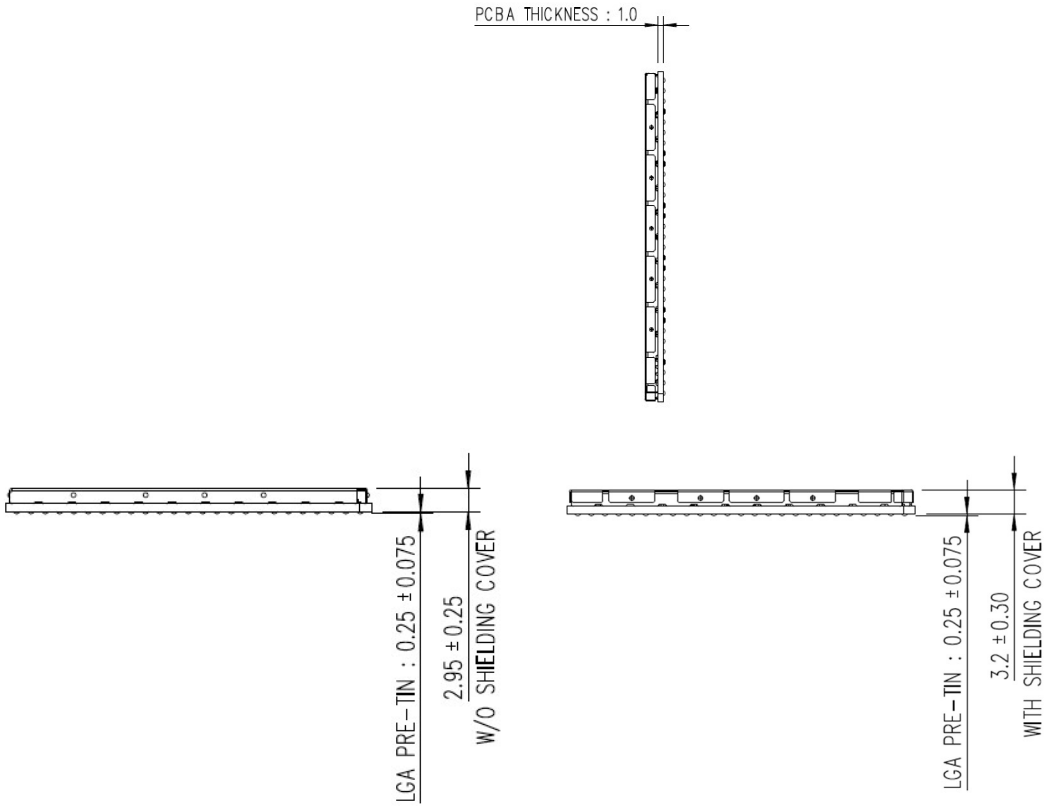
57mm (typ.) x 46 mm (typ.) x 3.2mm (typ.)



Module with shielding cover (Top side)



Module LGA (Bottom side)



Module Thickness

7. Design Guide

7.1. Power Supply

Pin name	Pin Number	Description	Type	Input range(V)		
				Min.	Typ.	Max.
VPH_PWR	L3,L2,L1,K3,K2,K1,J3,J2 ,J1,H3,H2,H1	System Power	PI	3.3	3.8	4.3

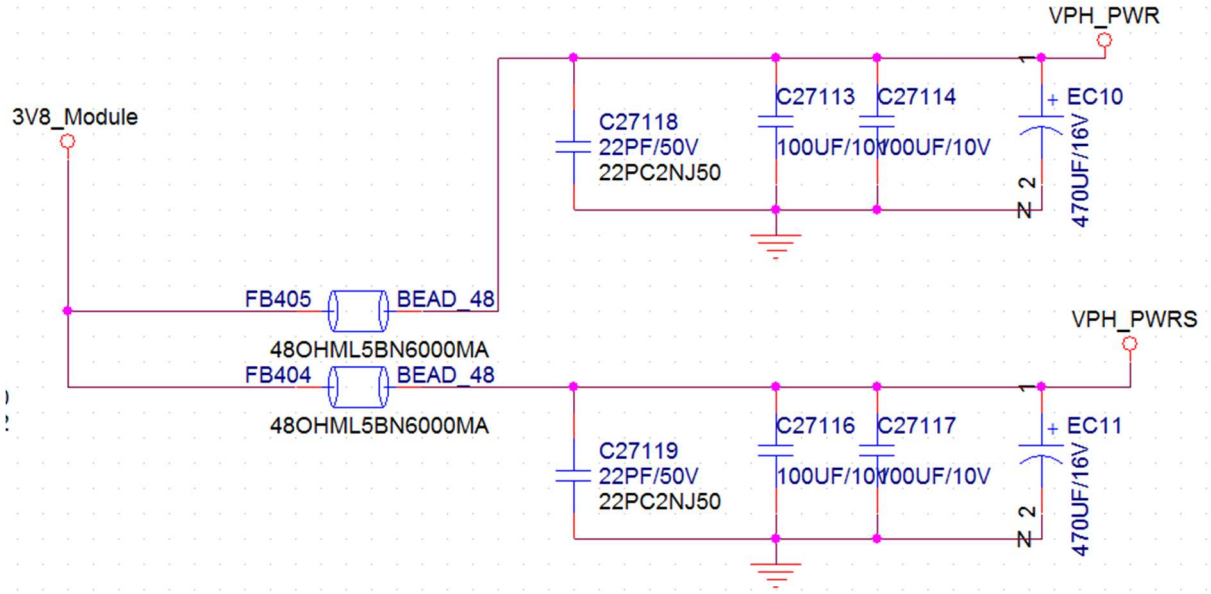
The Main Power input for this 5G module is VPH_PWR which supplies the PMIC inside the module. The PMIC converts different power rails for different functions, respectively.

Pin name	Pin Number	Description	Type	Input range(V)		
				Min.	Typ.	Max.
VPH_PWRS	N5,M5,P6,N6,M6,L6,P7 ,N7,M7,L7	RF Power	PI	3.3	3.8	4.3

The Main RF Power input for this 5G module is VPH_PWRS which supplies the ET chip inside the module.

Schematic suggestion:

To ensure that the voltage drop of VPH_PWR/ VPH_PWRS will not affect system performance, it's recommended to follow the capacitance that's a total of more than 400uF. These capacitors are required to place near VPH_PWR/ VPH_PWRS pins as close as possible.



Net name	Current Value
VPH_PWR	1.5A
VPH_PWRS	1.5A
VREG_DBB1_3P3	1600mA
VREG_LDO_SDC	200mA
VBUS_DET	500mA
VREG_L6_1P8	600mA
SIMVCC1(VREG_L11_1P8)	150mA

7.2. RF Connector

IMQC provides 10 RF pads; developers can connect them via 50 Ω traces to the main board.

ANT0 (Pin AL11): UHB_ANT0, MHB_TX1/RX1, LB_TX0/RX0

ANT1 (Pin AL13): UHB_ANT1, MHB_TX0/RX0, LB_TX1/RX1

ANT2 (Pin AL17): UHB_ANT2, MHB_RX2

ANT3 (Pin AL15): UHB_ANT3, MHB_RX3

ANT4 (Pin AL19): UHB_RX4, MHB_RX4

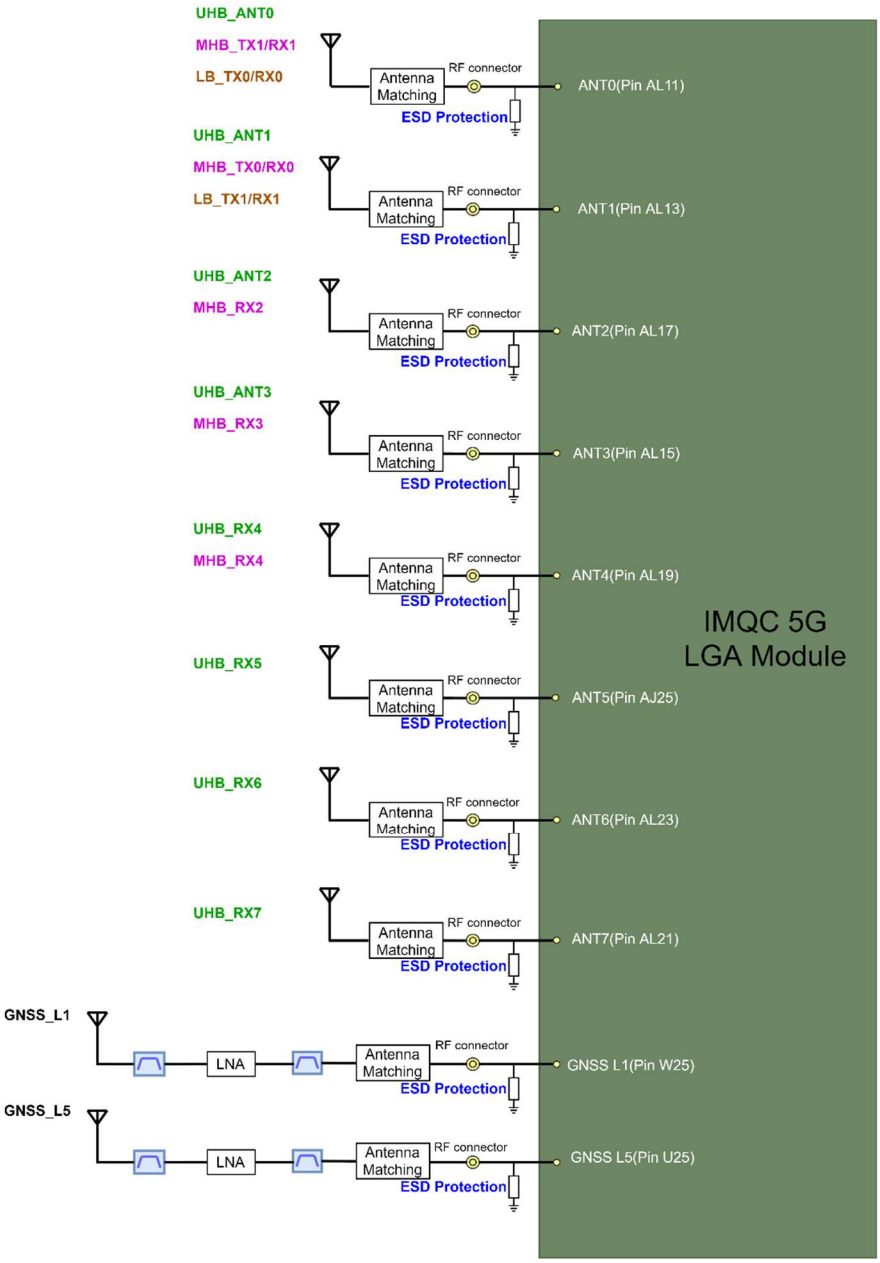
ANT5 (Pin AJ25): UHB_RX5

ANT6 (Pin AL23): UHB_RX6

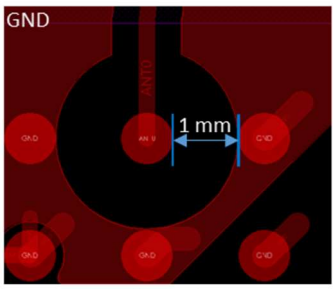
ANT7 (Pin AL21): UHB_RX7

ANT12 (Pin W25): GNSS_L1

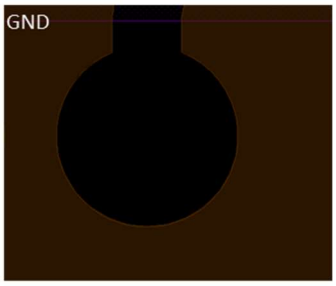
ANT13 (Pin U25): GNSS_L5



We recommend that no grounds are present under the surface of IMQC's RF pads on Layer1. Details are shown in the below Figure. Layer2 has the same keep-out size as Layer1. Layer3 are as reference GND.



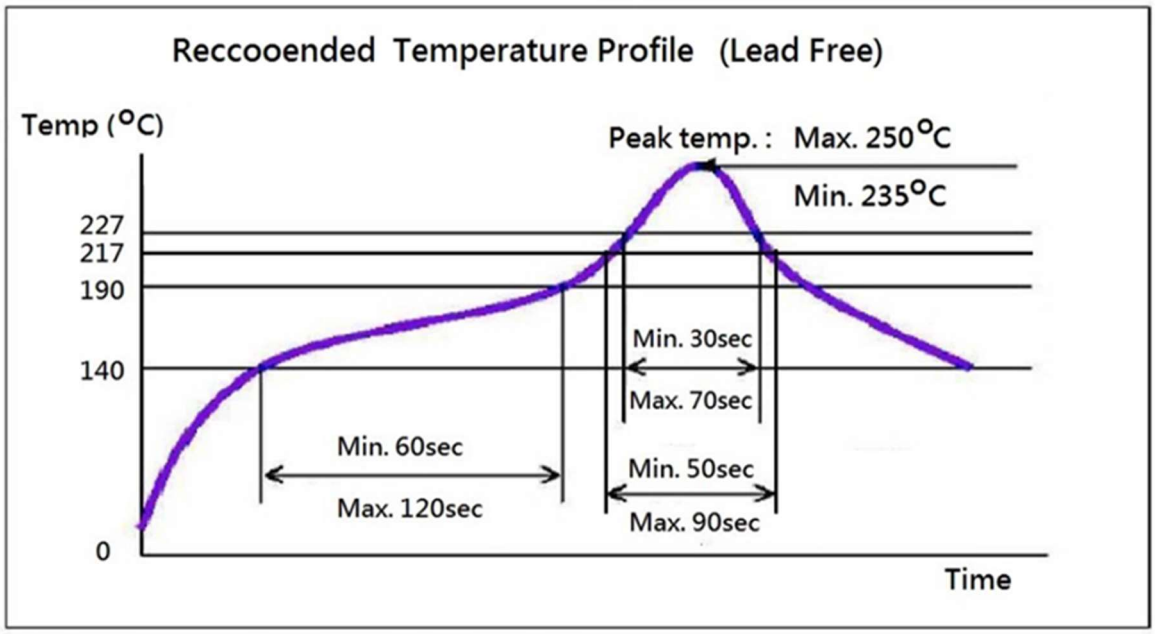
Layer 1



Layer 2

Layer 3

7.3. Reflow Profile



Peak Temperature : 235°C ~ 250°C
Reflow Zone (above 217°C) : 50 ~ 90 sec. (SAC305)
Preheat Zone (140°C ~ 190°C) : 60 ~ 120 sec.
Reflow Zone (above 227°C or 230°C) : 30 ~ 70 sec. (SN100C)

Caution: Do not reflow the module twice to avoid components to be short or damaged.

8. Safety Recommendation

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and must be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, and aircraft
- Where there is a risk of explosion such as gasoline stations and oil refineries

It is the responsibility of the user to comply with his or her country's regulations and any specific environmental regulations.

Do not disassemble the product; any mark of tampering will compromise the warranty's validity.

We recommend following the instructions of the hardware user guides to correctly wire the product. The product must be supplied with a stabilized voltage source, and the wiring must conform to all relevant security and fire-prevention regulations.

This product must be handled with care; avoid any contact with the pins because electrostatic discharge may damage the product. The same caution must be taken regarding the UIM card; carefully check the instructions for its use. Do not insert or remove the UIM when the product is in power-saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care must be taken for external components of the module as well as for project or installation issues—there may be a risk of disturbing the GSM network or external devices or of having an impact on device security. If you have any doubts, please refer to the technical documentation and the relevant regulations in force.

Every module must be equipped with a proper antenna with specific characteristics. The antenna must be installed with care in order to avoid any interference with other electronic devices.

FCC Statement:

Federal Communications Commission Statement

This device complies with FCC Rules Part 15. Operation is subject to the following two conditions:

• This device may not cause harmful interference.

• This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a class B digital device, pursuant to Part 15 of the Federal Communications Commission (FCC) rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by doing one or more of the following measures:

• Reorient or relocate the receiving antenna.

• Increase the separation between the equipment and receiver.

• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

• Consult the dealer or an experienced radio/TV technician for help.

FCC Caution

Any changes or modifications not expressly approved by the party responsible for compliance could void the user‘s authority to operate the equipment.

The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement:

This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated. Additional testing and certification may be necessary when multiple modules are used.

USERS MANUAL OF THE END PRODUCT

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated.

The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: NKRIMQC ".

Initialisms

Initialisms and definitions

Abbreviation	Definition
3GPP	3rd Generation Partnership Project
AC	Alternating Current
CDMA	Code Division Multiple Access
DC	Direct Current
DBI	Display Bus interface
FDMA	Frequency Division Multi Access
GND	Ground
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
LTE	Long Term Evolution
AP	Application Processor
MD	Modem
MIMO	Multiple Input Multiple Output
MNO	Mobile Network Operator
GRFC	Generic RF control
BB	Baseband
RFFE	RF Front End
I2S	Integrated Interchip Sound
SDIO	Secure Digital Input/Output
PCIEG3	PCI Express Generation 3
PCM	Pulse-Code Modulation
PMIC	Power Management Integrated Chip
TDM	Time-Division Multiplexing
SMA	Subscriber Mount Antenna

SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
ADC	Analog to Digital Converter
UART	Universal Asynchronous Receiver-Transmitter
eMMc	Embedded Multi Media Card
JTAG	Joint Test Action Group
USB	Universal Serial Bus
BGA	Ball Grid Array
PMX65	Qualcomm PMIC PMX65
PMK65	Qualcomm PMIC PMK65
SDX65	Qualcomm CPU SDX65