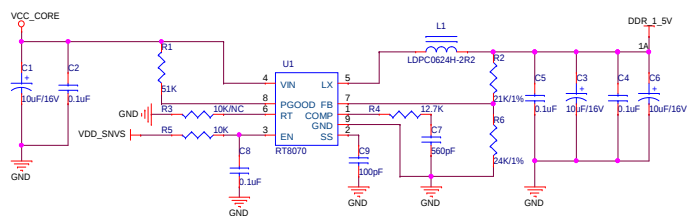
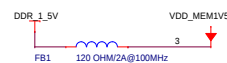


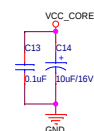
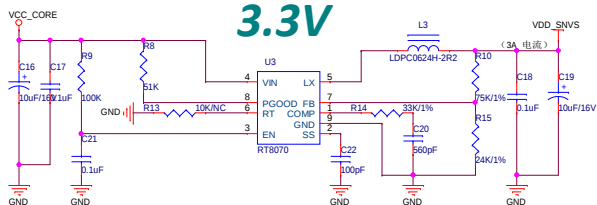
DDR 1.5V



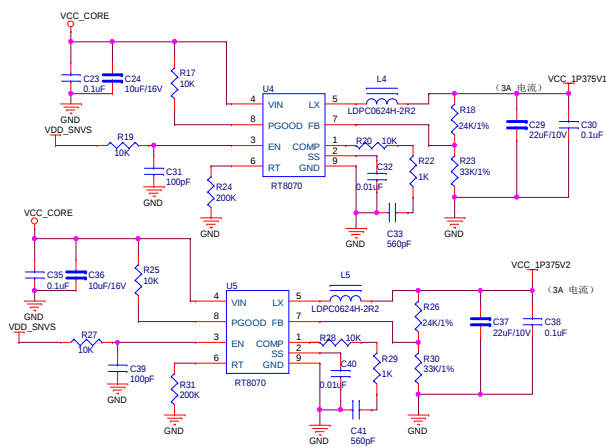
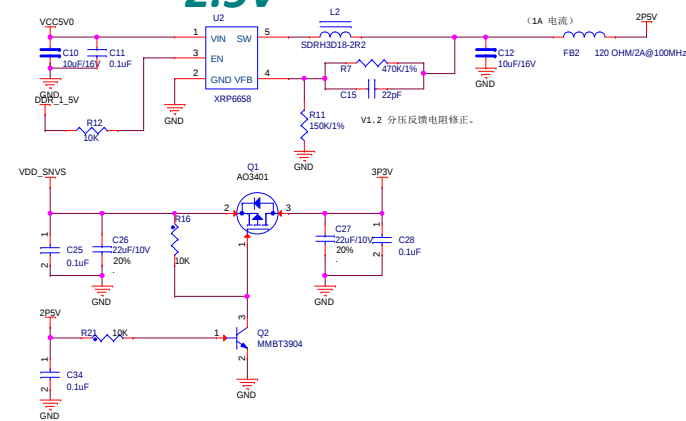
Enable Thread = 1.2v



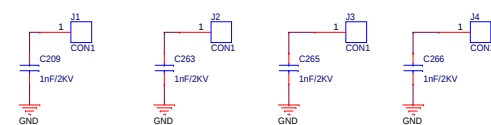
3.3V



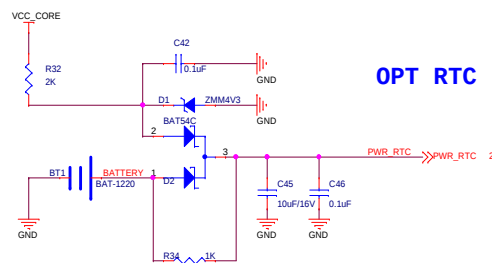
2.5V



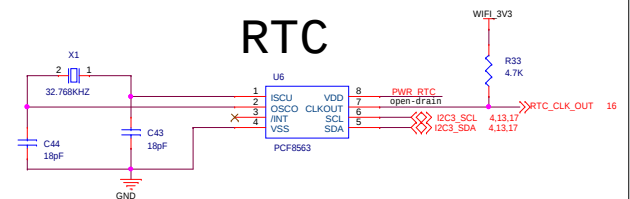
上电顺序 VDD_SNV5- VCC_1P375V- (DDR_1_5V 2P5V)- 3P3V



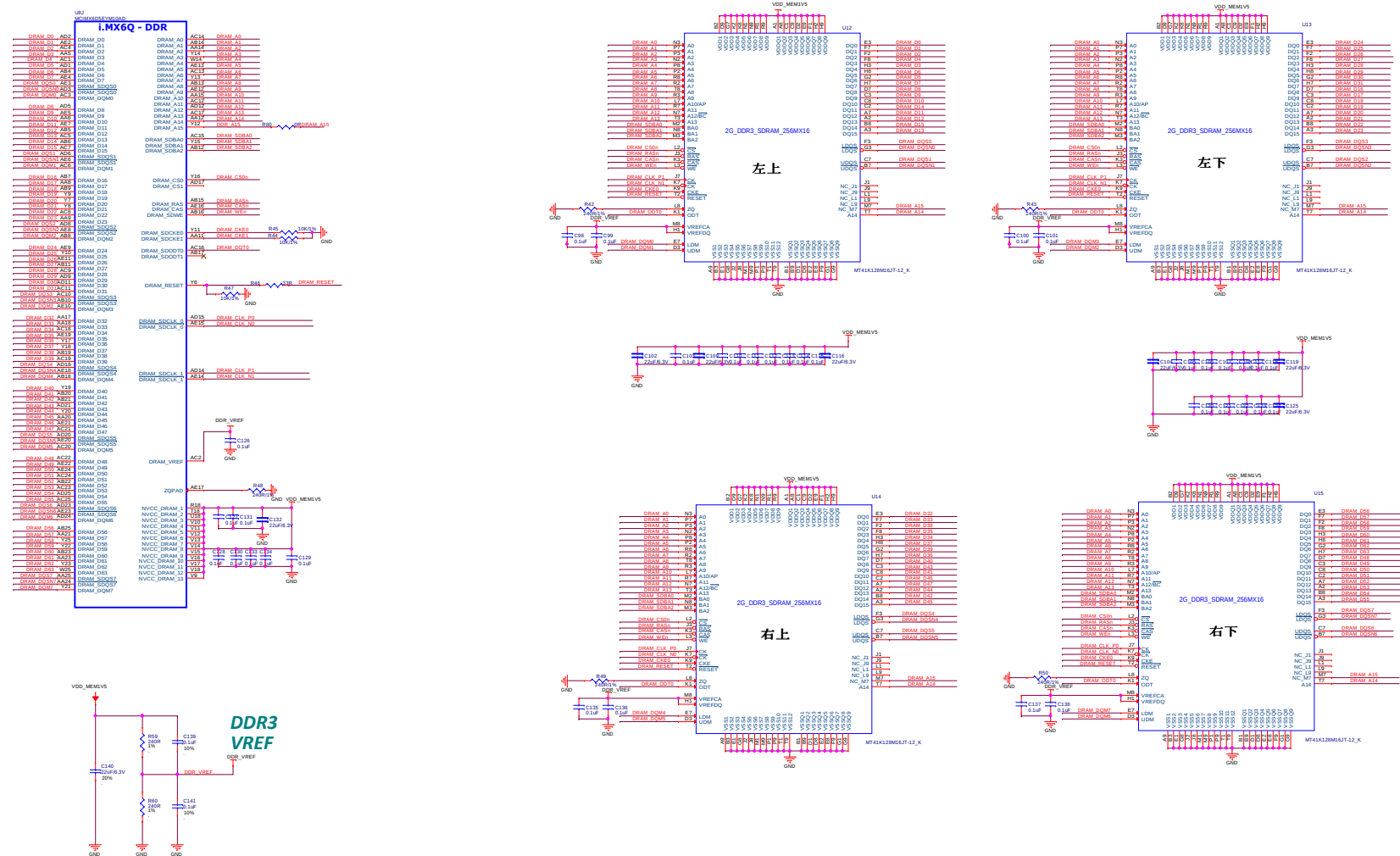
OPT RTC



RTC



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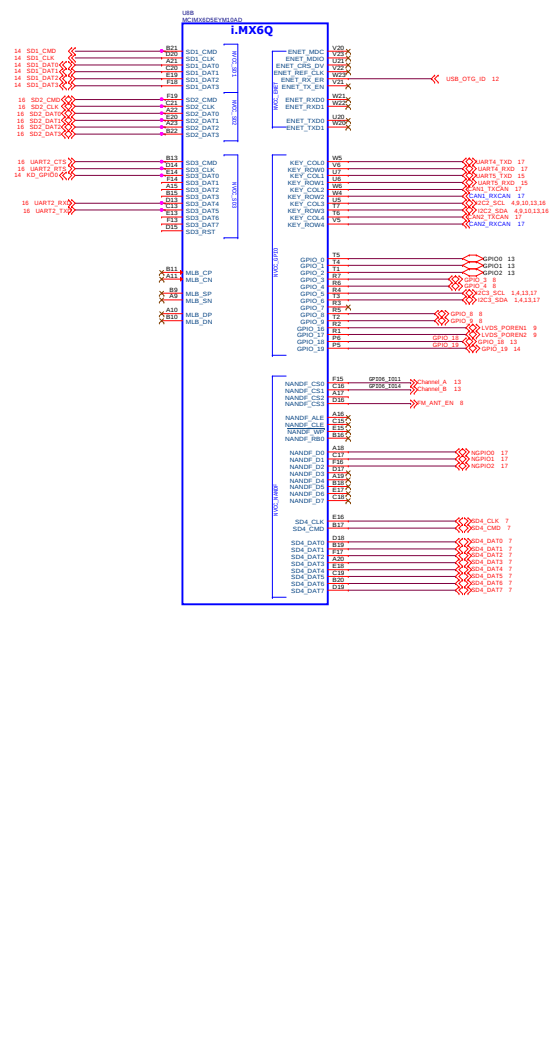


NOTE:
Using bit swapping for DATA bus to allow easy pcb routing.

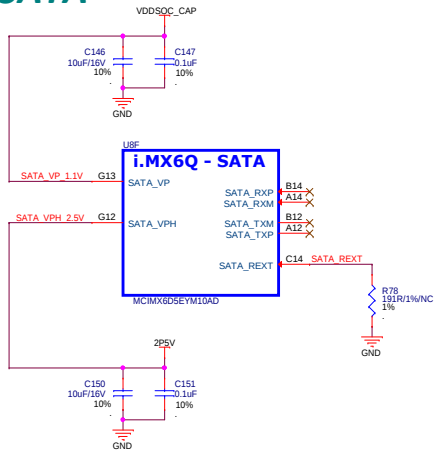
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.

Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

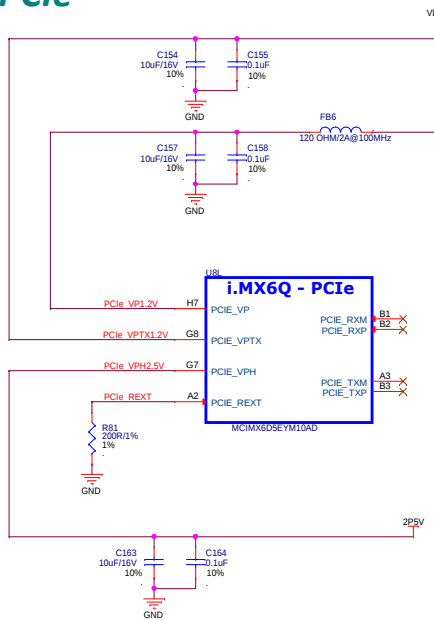
When swapping byte lanes on 16-bit memories, remember to move the DQM₀, DQS₀, and DQS_{0_8} signals for that byte lane.



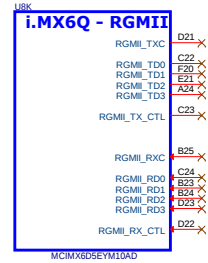
SATA



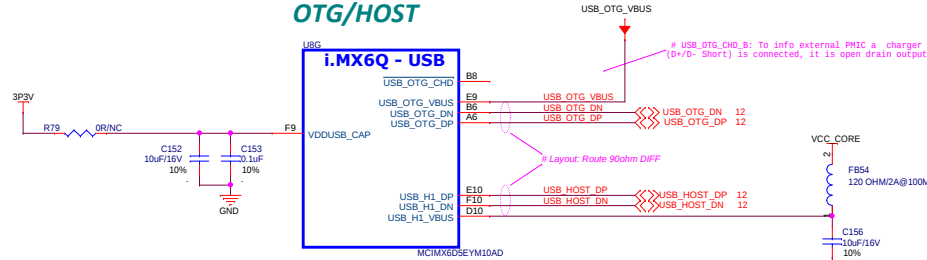
PCIe



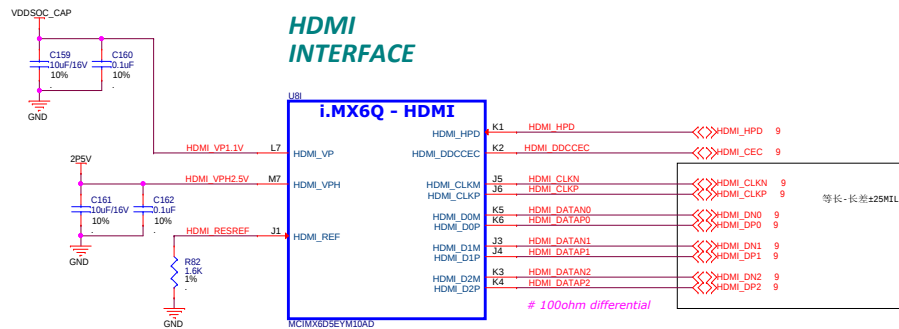
RGMII



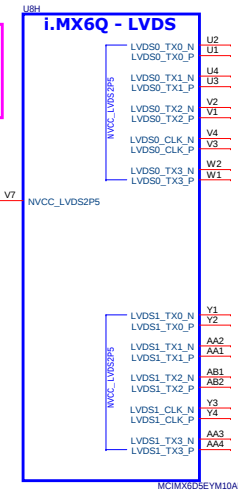
USB OTG/HOST



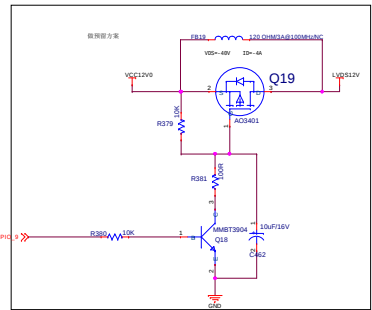
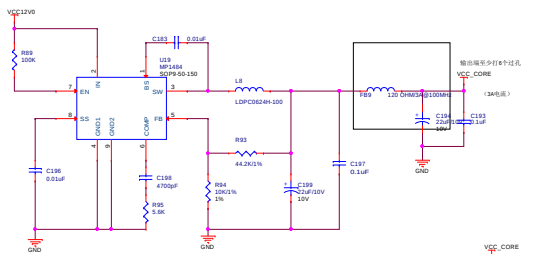
HDMI INTERFACE



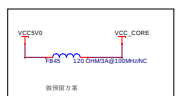
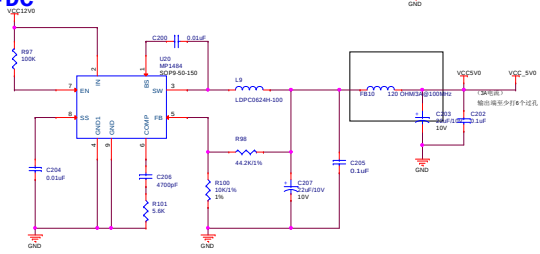
LVDS



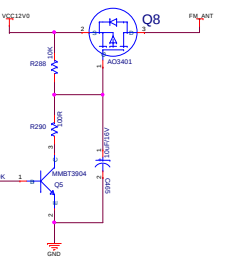
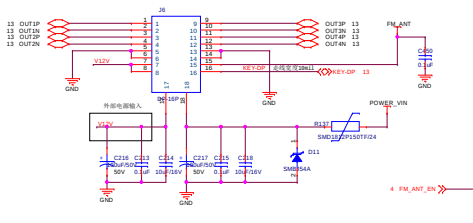
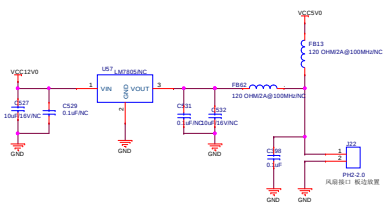
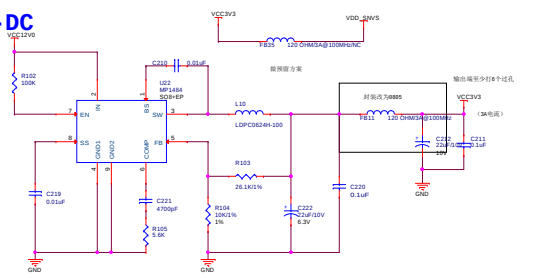
5.0V DC-DC



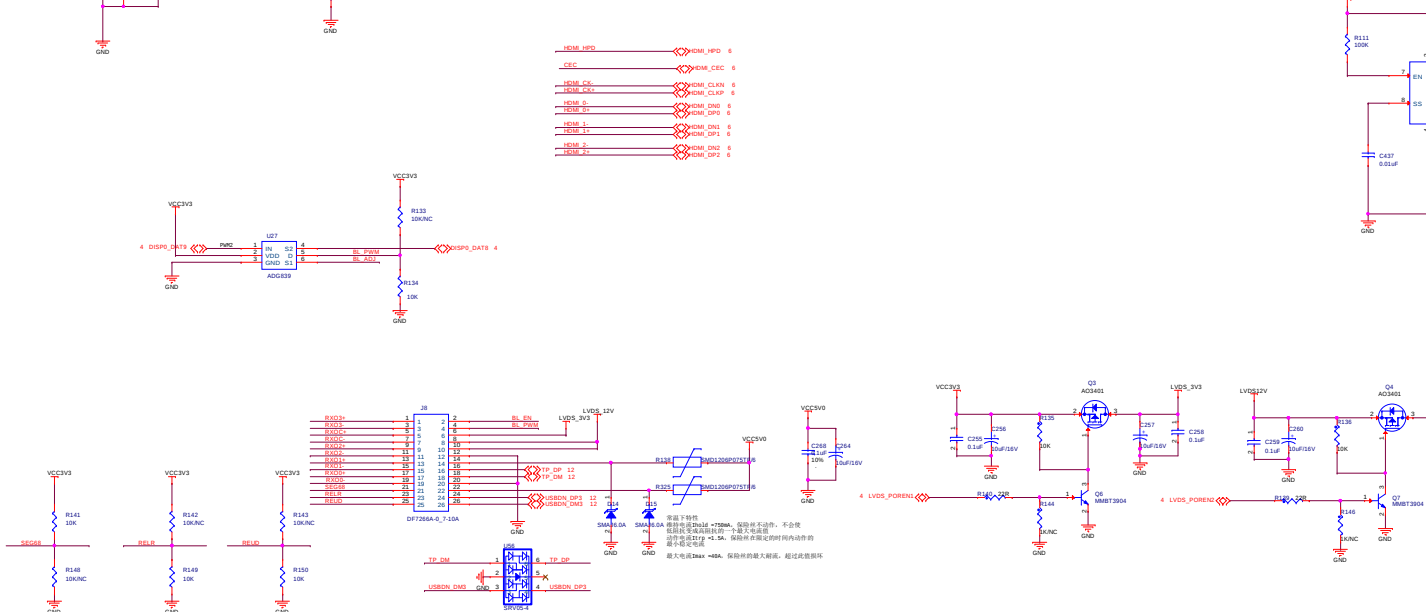
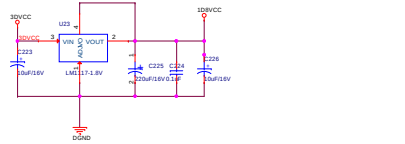
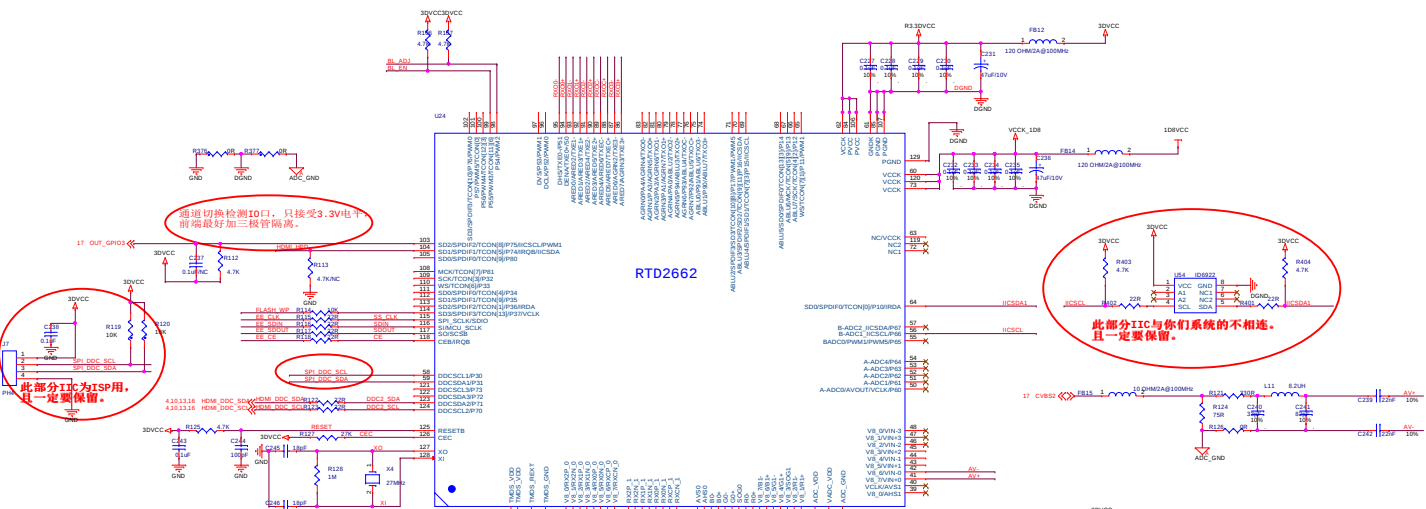
5.0V DC-DC

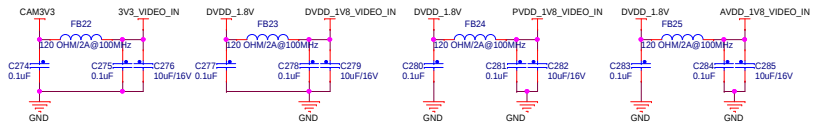


3.3V DC-DC



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Doc	Doc



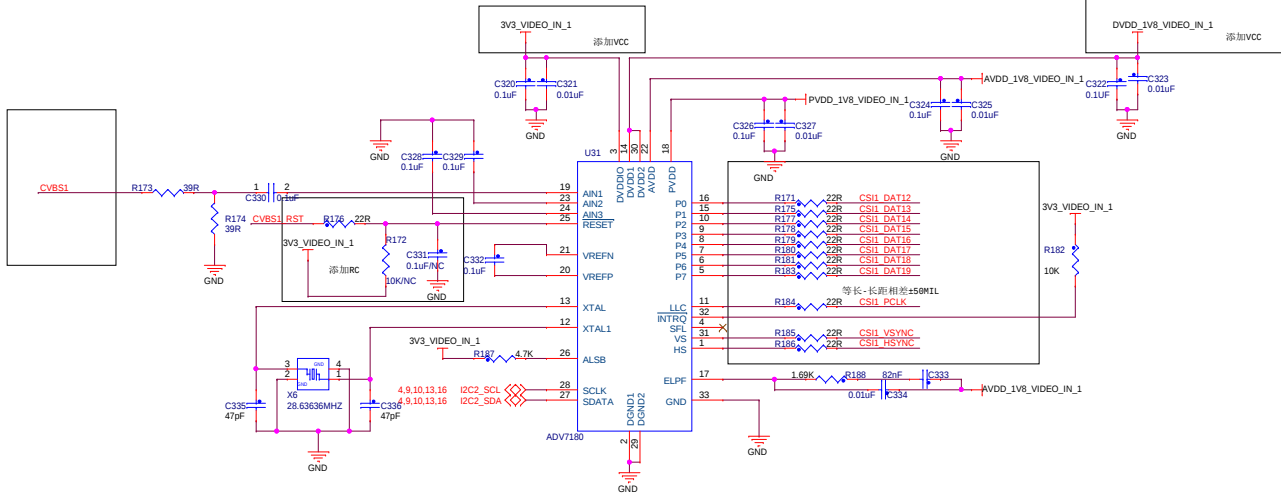
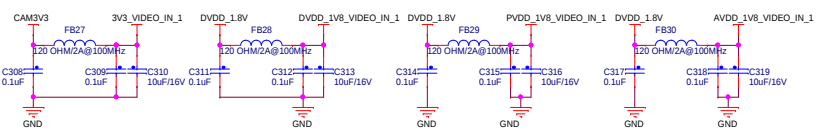
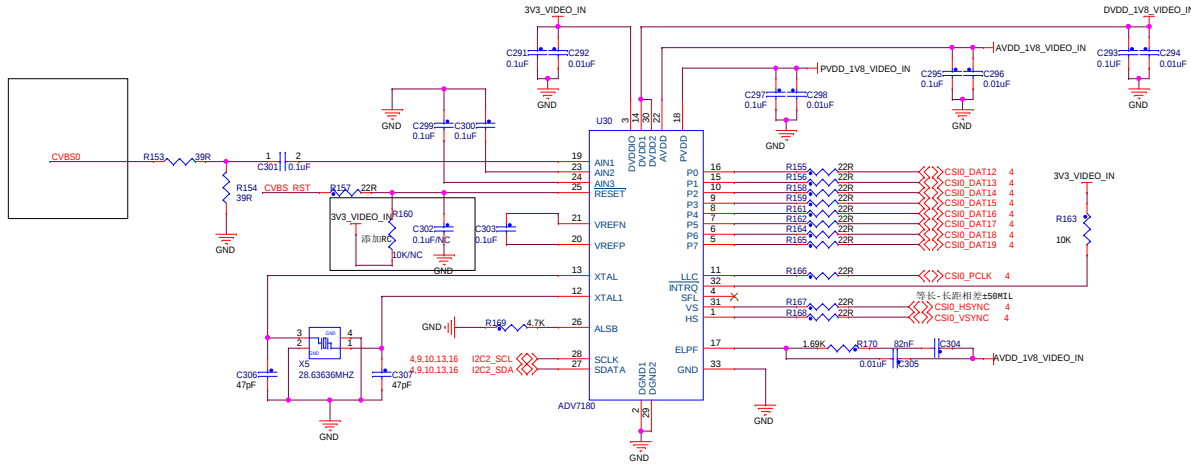
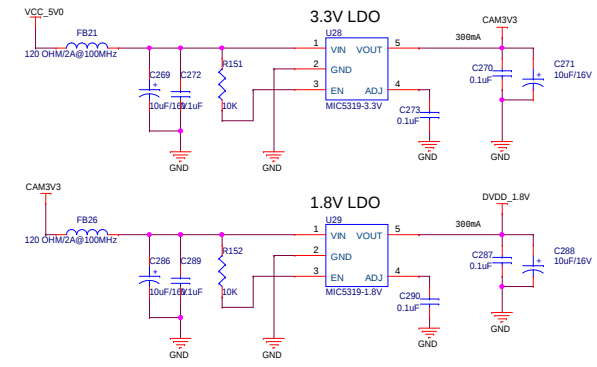


4 EIM_D17 CSU1_PCLK
 4 EIM_D28 CSU1_DAT12
 4 EIM_D27 CSU1_DAT13
 4 EIM_D26 CSU1_DAT14
 4 EIM_D25 CSU1_DAT15
 4 EIM_D20 CSU1_DAT16
 4 EIM_D19 CSU1_DAT17
 4 EIM_D18 CSU1_DAT18
 4 EIM_D16 CSU1_DAT19
 4 EIM_EB2 CSU1_VSYNC
 4 EIM_D09 CSU1_HSYNC
 4 EIM_EB3 CSU1_RST
 4 DISPO_DAT6 CVBS1_RST
 4 DISPO_DAT7 CVBS1_RST

CVBS0 CVBS1
 CVBS0 CVBS1

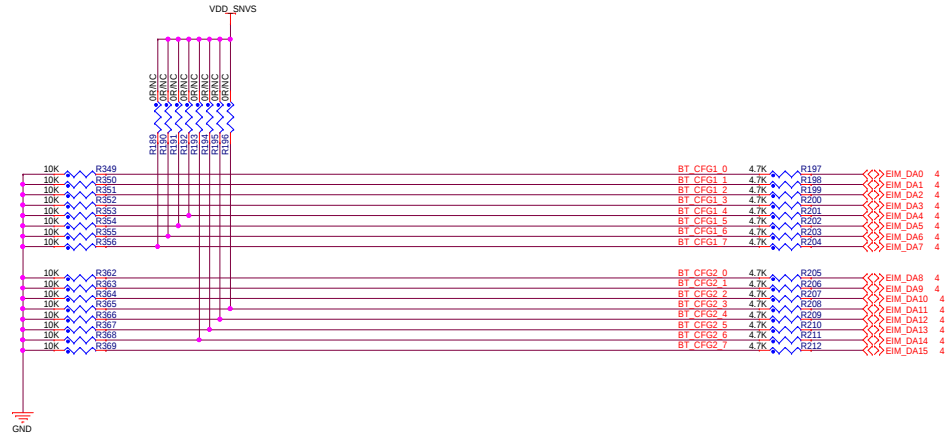
Layout Note :- VPLLND and VGND need a separate return path to DGND near the power supply and separate from each other.

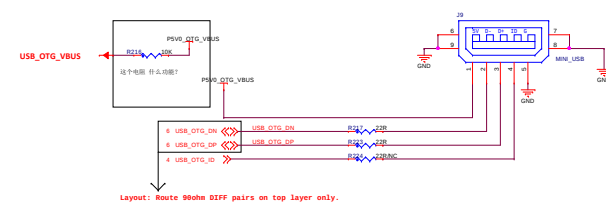
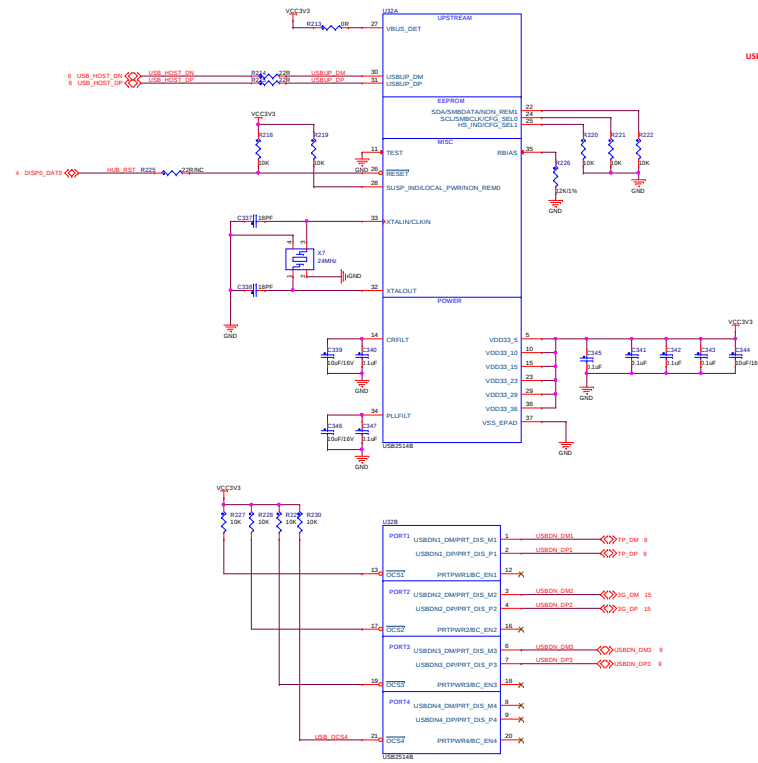
ALSB = '1' : I2C ADDRESS = (0x42 | R/w) (Default)
 ALSB = '0' : I2C ADDRESS = (0x40 | R/w)

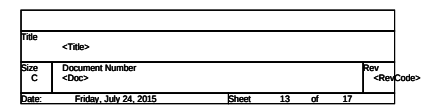


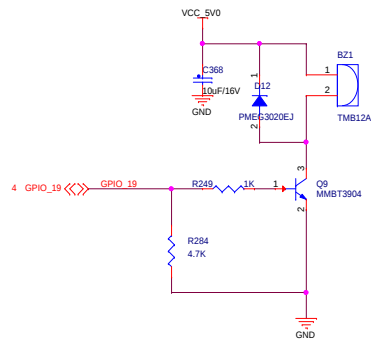
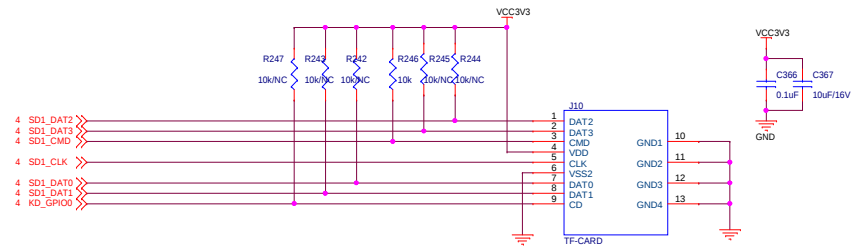
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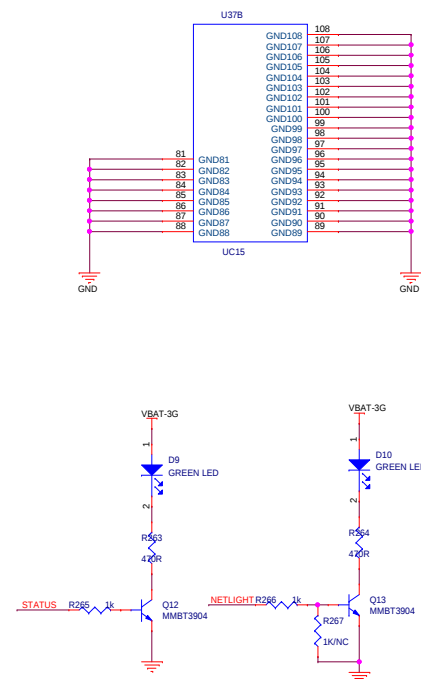
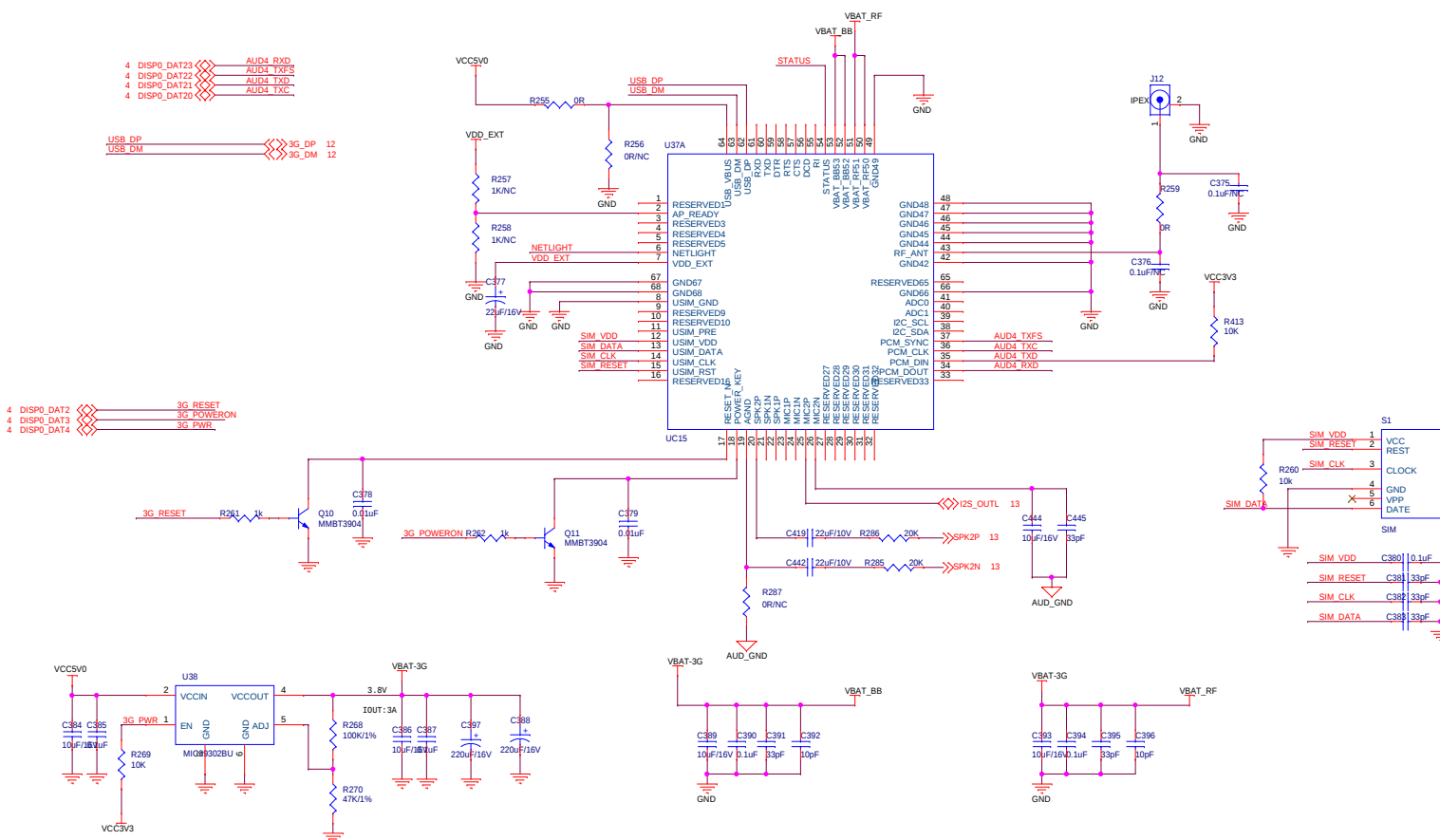
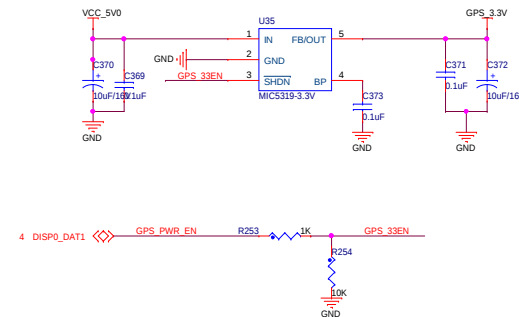
Boot Configuration Select



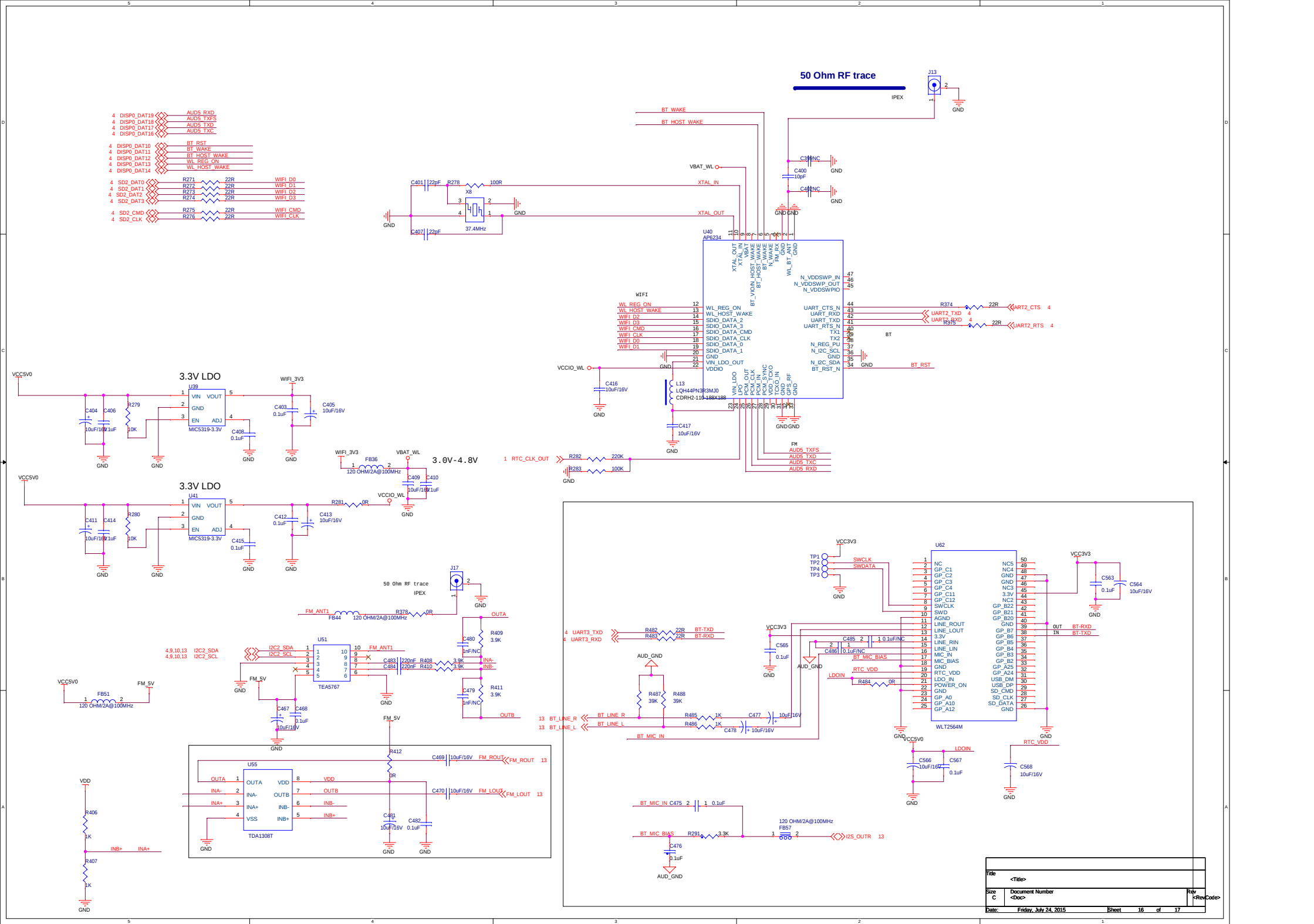


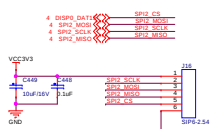
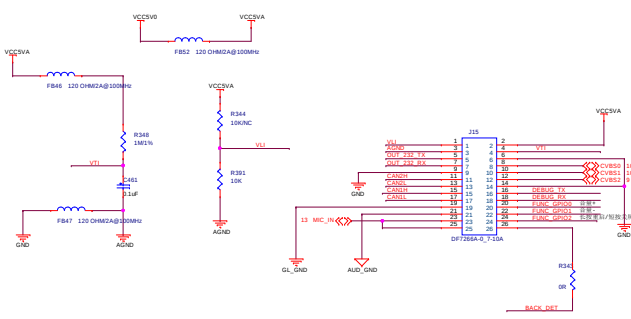
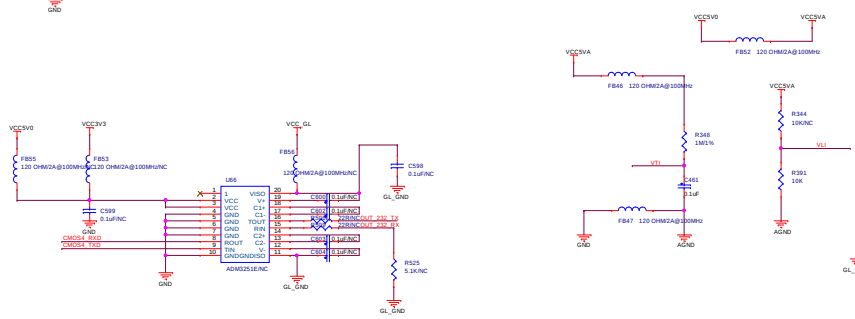
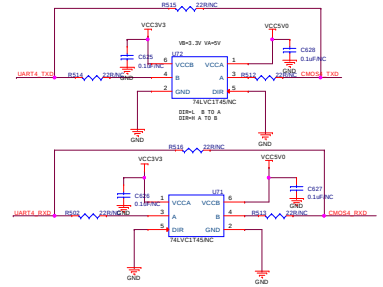
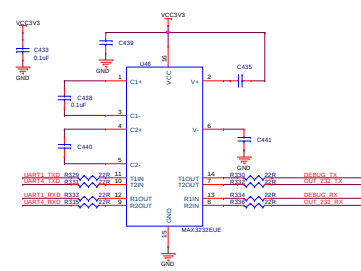
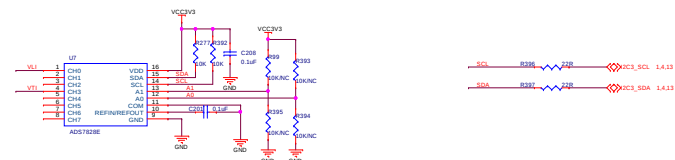
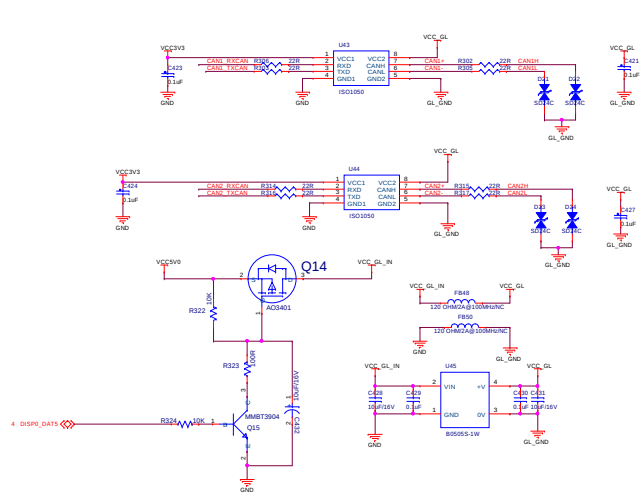




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