CIRCUIT DESCRIPTION

A general description of the overall circuit is covered in the instruction manual. This section provides the description of circuits required by subpart 2.983 of the Commissions' rules. Circuits not described in the manual are covered in this exhibit.

This exhibit contains descriptions of the frequency generation, modulation and transmitter circuits in accordance with FCC Rules Part 2.983(d).

The following descriptions are included:

EXHIBIT 4A - Means for Frequency Stabilization, 2.983 (d) 10

EXHIBIT 4B - Means for Limiting Modulation and Attenuation of Higher Audio Frequencies, 2.983 (d) 11

EXHIBIT 4C - Means for Attenuation of Spurious Emissions, 2.983 (d) 11

EXHIBIT 4D - Means for Limiting Power Output, 2.983 (d) 11

EXHIBIT 4E - Modulation Techniques, 2.983 (d) 12

CARRIER FREQUENCY GENERATION AND STABILIZATION

Circuit Description:

The carrier frequency is generated using a discrete Field Effect Transistor, Q251, as a voltage controlled oscillator (VCO) and a fractional-N, frequency synthesizer integrated circuit, U201. The IC, U201, consists of a phase-locked loop circuit with the output of the VCO fed to a programmable divider chain. The divide ratios are determined from information stored in the EEPROM (Electrically Erasable Programmable Read Only Memory) in the microcomputer and bussed to the synthesizer. The microcomputer extracts the data for the division ratios as determined by the mode (channel) of operation selected. Using a time averaged algorithm a combination of divide ratios is used so that the reference frequency can be a much higher value than the value of the frequency resolution. Modulation occurs by a combination of directly coupling the modulation signal to the low pass filter in the loop and by processing the modulation signal to alter the divider values.

Frequency stability is maintained by a 16.8 MHz Temperature Controlled Crystal Oscillator (TCXO) external to the frequency synthesizer IC. The TCXO features low current drain and a ±1 ppm frequency versus temperature capability. In addition, this TCXO offers digital tuning and a temperature referenced 5 bit Digital to Analog Converter (DAC). Frequency tuning has 128 steps of resolution.

The 16.8 MHz reference is further divided into one of three reference frequencies which is compared to the divided down VCO output in a phase detector. The output of the phase detector provides a DC correction voltage back to the VCO.

A Block diagram of the VCO/Synthesizer system is shown in Figure 4.1.

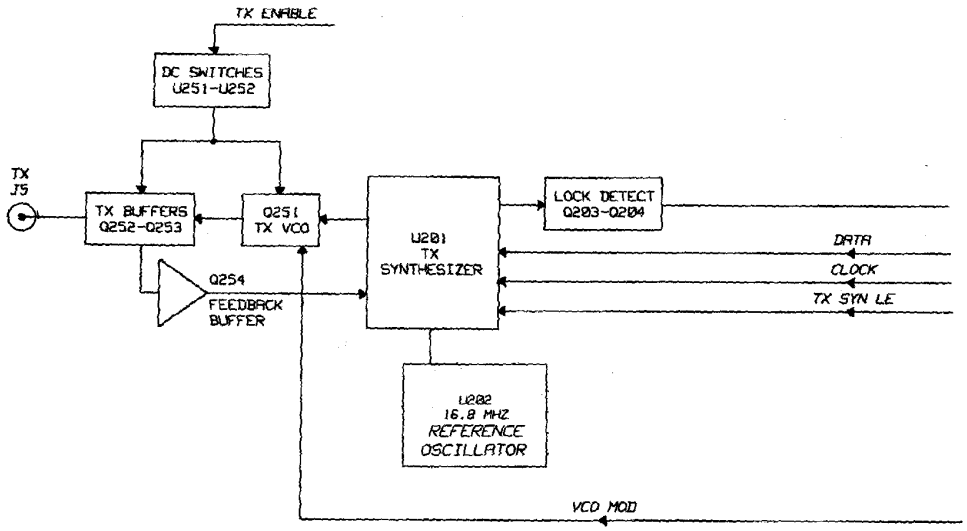

Figure 4.1 – Carrier Frequency Generation and Stabilization

MODULATION LIMITING AND LOW PASS FILTERING

Circuit Description:

Modulation limiting is accomplished within the custom audio processor IC, U651. The limiting action itself occurs at the rails (i.e., 5V and ground). Using an operational amplifier with feedback, very hard limiting is obtained.

The limited modulation signal output of the limiter is applied to a low-pass filter in U651. The filter is a fifth-order switched capacitor filter with the rolloff corner frequency located at 3000 Hz.

The output of the low-pass filter is applied to the input of the electronic attenuator. The electronic attenuator is controlled by the microcomputer of the transceiver. To keep the deviation constant over the RF frequency range, the microcomputer adds the proper correction factor to the attenuator.

A block diagram of the limiting and low pass filtering is shown in figure 4.2.

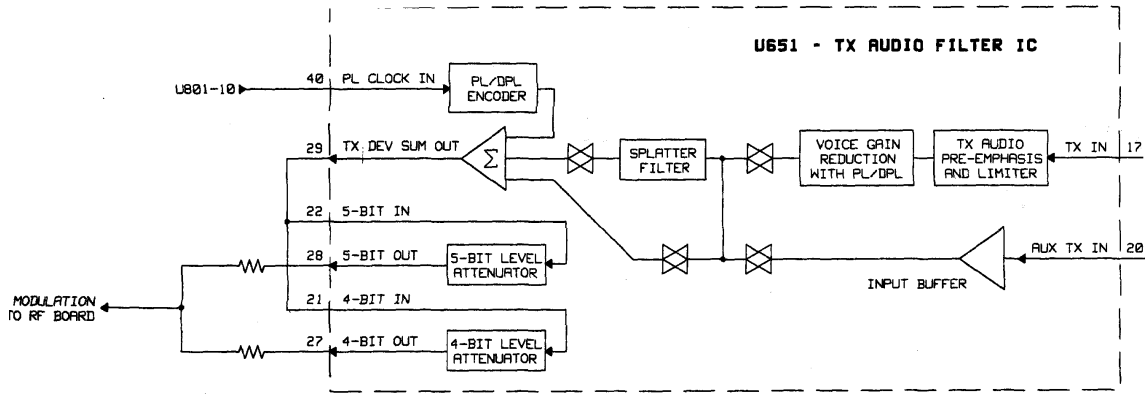

Figure 4.2 – Transmitter Modulation Limiting and Lowpass Filtering

MEANS FOR HARMONIC SUPPRESSION

Circuit Description:

The final stage of the RF power amplifier circuit feeds a low-pass filter in order to attenuate harmonics of the output frequency as well as spurious outputs. The filter is a seven pole, 0.1 dB Chebychev design using LC reactive elements.

Shielding of the transmitter RF power amplifier circuit also attenuates spurious emissions.

The circuit diagram may be found in Figure 4.3.

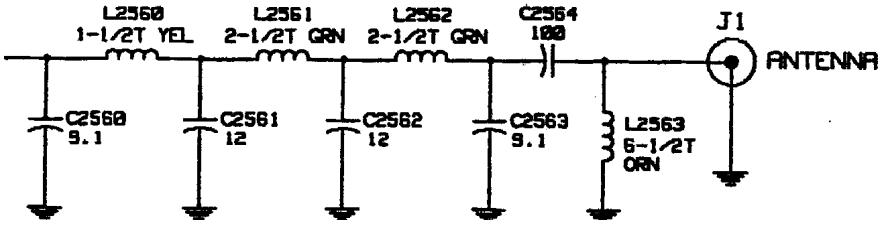

Figure 4.3 – Transmitter Lowpass Filter

POWER LIMITING

Circuit Description

Power is programmed electronically during radio tune-up and may be different for each channel. The microcomputer varies the DC output voltages of Digital to Analog Converters (DAC), U452 pin 9 and U452 pin 11. These voltages are applied to the (+) input of operational amplifier U451A pin 3. As the DAC voltage increases, U451A pin 1 output voltage increases, which causes greater conductance in Q451 and Q452. This increases the control voltage and the RF power output.

If the DC current of the final RF amplifier increases excessively, the increased voltage drop across a series resistor will be sensed by U451B, causing the current through Q453 to increase until the two inputs of U451B are again equal. The increase in Q453 current raises the emitter voltage which is applied to the (-) input of U451A. This will reduce the output voltage of U451A pin 1, reducing conduction in Q451 and Q452, and lowering the controlled B+ voltage to counteract the excessive current condition.

Under any circumstances, controlled B+ is prevented from exceeding a pre-programmed DC voltage. The controlled B+ voltage is divided by R471 and R472. It is then monitored every 17 milliseconds by one of the microcomputer Analog to Digital Converter inputs, U801 pin 34. If the voltage exceeds the maximum allowable, the DAC is decreased one step. This process is iterated as required to keep the transmitter current constant.

The block diagram of the power limiting circuit may be found in Figure 4.4.

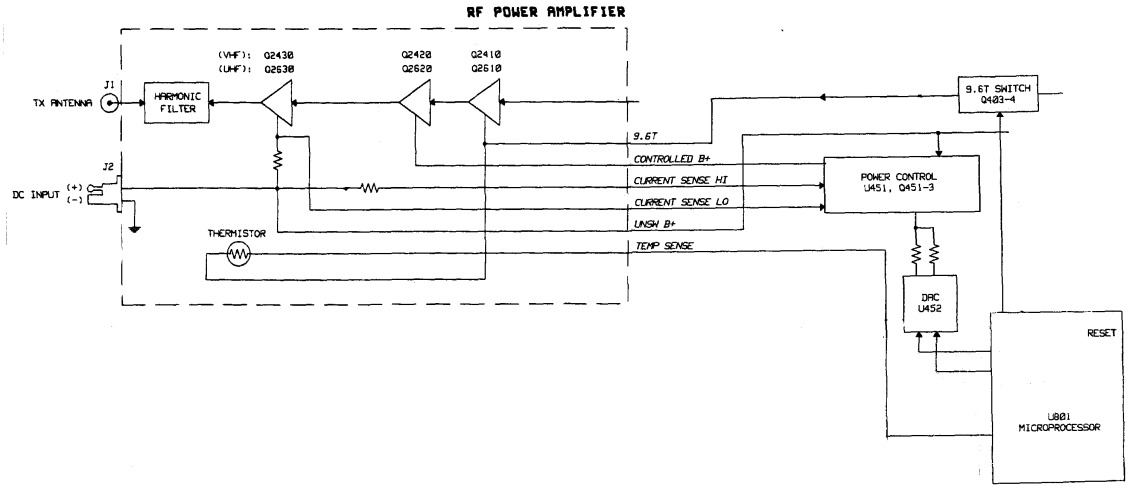

Figure 4.4 - Transmitter Power Limiting Block Diagram

Modulation Techniques

The transmitter is capable of the following types of modulation:

1) Modulation of TPL (Tone Private Line) - Direct FM tone modulation of 67 Hz to 250.3 Hz at 15% of full system deviation.

2) Modulation of DPL (Digital Private Line) - Direct FM modulation at 134 BPS at 15% of full system deviation.

3) Modulation of DTMF tones at nominally 60% of full system deviation.

4) Modulation of CWID tones at nominally 40% of full system deviation.

5) Modulation of 2000/3000 Hz FSK data at nominally 100% of full system deviation.

Note: AFSK is used only for MDC 1200 Selective Calling (which is consistent with the F3E designator) and is NOT the primary modulation technique.

Direct FM of TPL or DPL is generated by a 6-bit Digital to Analog Converter contained within U651. The frequency determining clock signal is generated by the radio microcomputer, U801. The modulation signal is processed through a five pole switched capacitor filter. The output of the filter is applied to the electronic attenuator circuit.

The microcomputer adjusts the attenuator to compensate for modulation sensitivity variations of the synthesizer, ensuring 15% of full system deviation for PL and DPL.

DTMF tones are generated by an external tone generator IC contained within the accessory DTMF microphone. The DTMF tones are routed and processed in the same manner as voice signals. A potentiometer inside the microphone allows adjustment of the DTMF tones to nominally 60% of full system deviation.