■Theory of Operation

■ 1. Frequency Configuration

The receiver utilizes double conversion superheterodyne. The first IF is 49.95MHz and the second is 450KHz. The first local oscillator signal is supplied by PLL circuit. The second local oscillator signal (50.4MHz) is generated from the frequency tripling of TCXO (16.8MHz).

The PLL circuit also generates the frequencies needed in the transmitter (See Fig.2).

Frequency Range: 136 MHz—174MHz

■ 2. Receiver Circuit

The receiver section configuration is shown as Fig. 1.

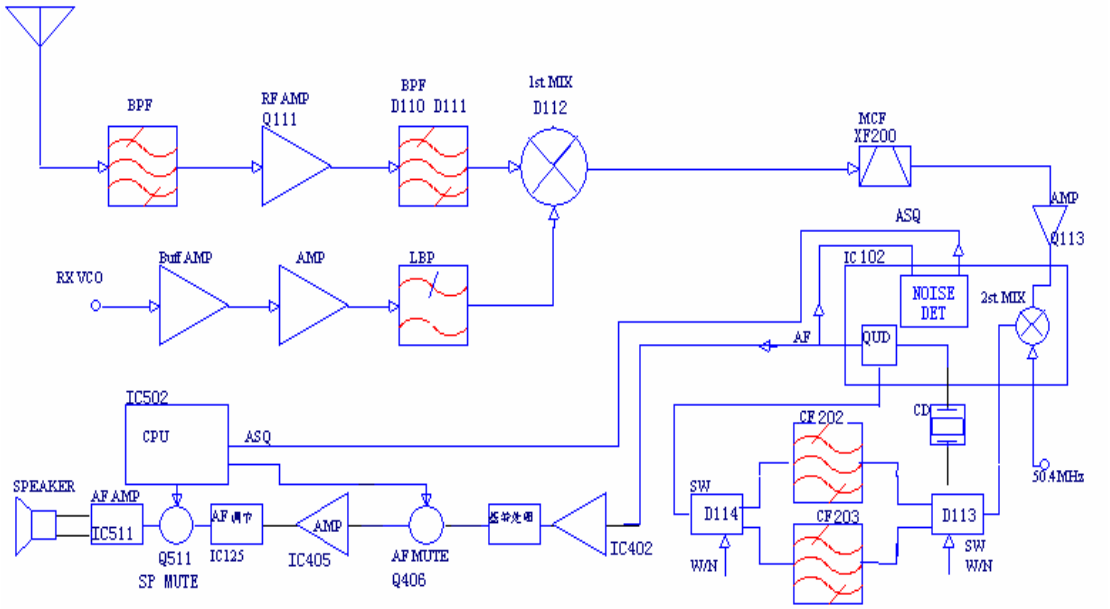

Figure 1 Receiver Section Configuration

2.1 RF AMP BPF

It consists of BPF (LC resonant circuit where D107, D108 and D109 are located) and RF amplifier (Q111). The range of bandpass frequency is from 136MHz to 174MHz. The signal is filtered by the RF Amp BPF to eliminate unwanted signals before going to the first mixer.

2.2 The First Mixer

The signal from RF AMP BPF is mixed with the first local oscillator signal from PLL circuit in the mixer (Q112) to generate a 49.95MHz first IF signal. The first IF signal is then fed through crystal filter (XF200) to further remove spurious signals.

2.3 IF Amplifier

The first IF signal is amplified by Q113 and then enters IC102 (TA31136FN), where the signal is mixed again with the second local oscillator signal (50.4MHz) to generate a 450KHz second IF signal. The second IF signal is then fed to a ceramic filter (N: CF202; W: CF203) to remove unwanted signal. The resulting signal then is detected by IC102 and output from Pin9 as an AF signal.

2.4 AF Amplifier

The AF signal from IC102 is amplified and filted by IC402 before amplified by IC401 (the received signalling is inputted into CPU for decoding). The resulting signalling passes through Q405 (AF MUTE) and is amplified by IC405. The amplified signal is fed to K301 (volume control), Q511 (SP MUTE) before entering AF AMP (IC511). The outputted AF signal is then delivered to the speaker through control panel.

2.5 Squelch

The AF signal from IC102 passes through IC102 Pin8 and is amplified by IC102 again, then is filted and rectified to produce an ASQ level. The ASQ level is comparaed in CPU (IC502) to genereate a level to control AF MUTE and SP MUTE. IC502 determines whether to output sounds from speaker by controlling Q405 and Q511.

■ 3. Transmitter Circuit

Transmitter circuit is composed of MIC circuit, modulation circuit, RFdirver, final power amplification circuit and APC circuit.

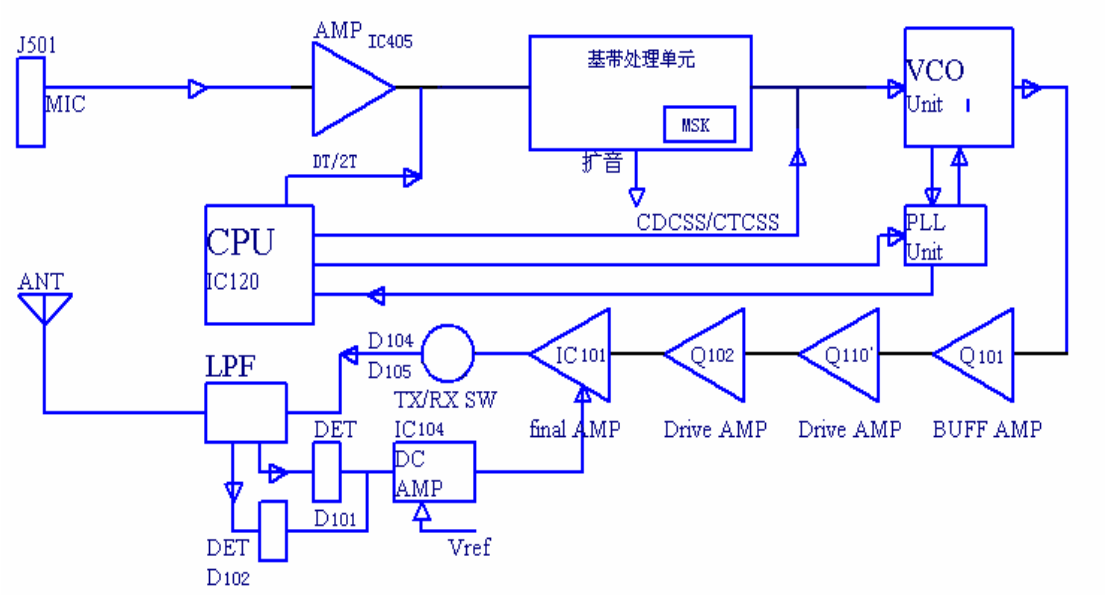

Fig2 Transmitter Circuit

3.1 MIC Circuit and Modulation Circuit

AF signal from MIC is amplified by IC405 before being pre-emphasized and encoded by IC401. The output AF signalling is added with signalling and then is fed to VCO for

modulation.

3.2 RFDriver and Final Power Amplification Circuit

The TX-RF signalling from Q703 in VCO circuit is amplified by Q101, driver Q110 and Q109, The amplified signal is then fed to IC101 (final PA) and passes through LPF before reaching the antenna terminal.

3.3 APC

The APC is used to keep the power output at a constant preset value. D101 and D102 transform the signal from detector into DC voltage, which is then compared with the reference voltage from CPU in IC104 and outputted as DC control voltage. The DC control voltage controls the output power by controlling the grid of IC101.

■ 4. PLL Circuit

PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission. PLL circuit consists of TX frequency oscillator (Q701), RX frequency oscillator (Q702), buffer amplifier (Q703), RF amplifier (Q102), PLL IC (IC801), LPF and TX/RX VCO control switch (Q704, Q706).

In transmit mode, IC120 transmits the frequency data to PLL IC. Q704 is turned on to activate TX VCO. The outputted signal is amplified by Q703, Q102, and then divided by PLL IC into 2.5KHz, 5KHz or 6.25KHz signal. The divided signal is compared with 2.5KHz, 5KHz or 6.25KHz reference signal from 16.8MHz crystal oscillator (2.5 PPM frequency stability) in the phase comparator. The frequency control voltage outputted from the phase comparator is sent to TX VCO after passing through LPF (Q802, Q803). In the meantime, modulation signal (TX) is passed to TX VCO for frequency modulation.

The working principle in receive mode is similar to that in transmit mode.

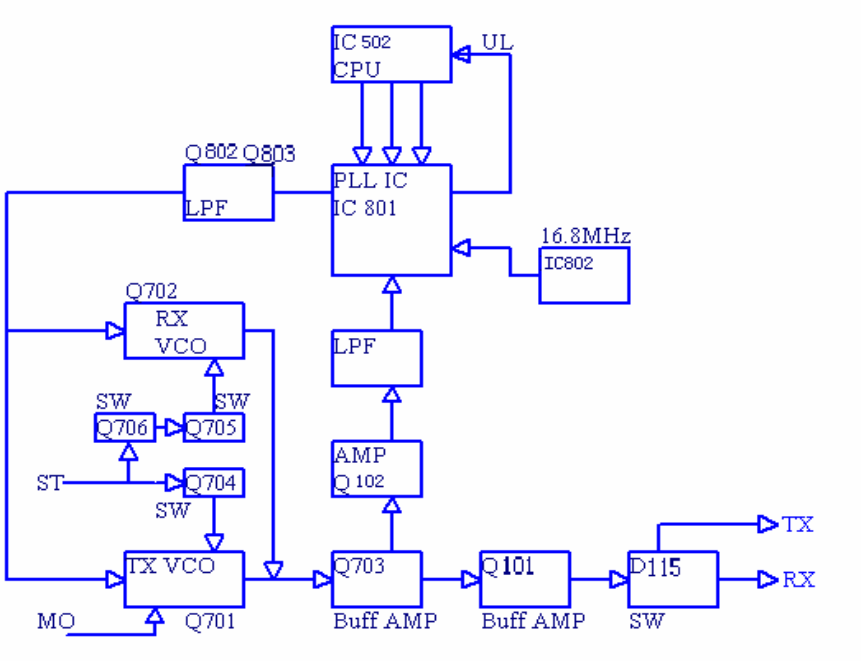

Fig3 PLL Circuit

■ 5. Control Circuit

The control circuit is composed of CPU, reset IC and power supply control circuit.

5.1 CPU

IC502 (CPU) operates at 9.8304MHz. CPU controls the data transmission between E2PROM (IC501), Rx circuit, Tx circuit, control circuit, display circuit and peripheral circuit.

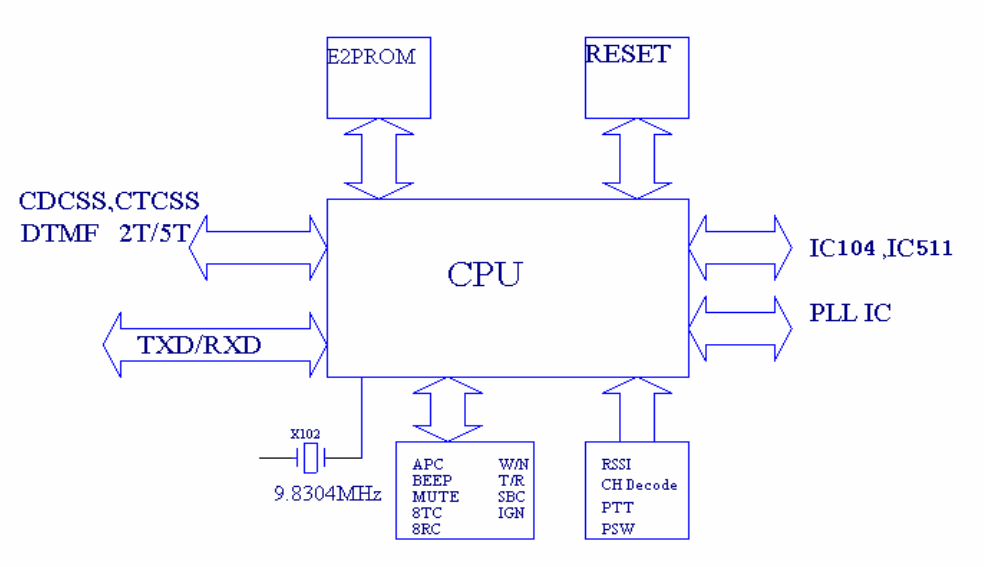

Fig4 Control Circuit

5.2 Power Supply

Power supply of the radio is derived from the battery which supplies battery B+. D135 and D137 are over-voltage protection diodes. Power-on/off can be controlled by software.

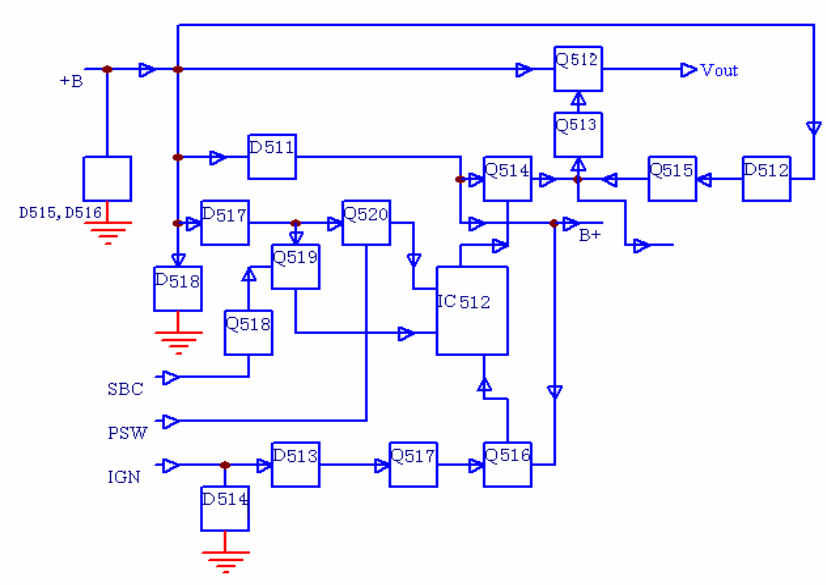

Fig 5 Power Switch Circuit

Vout provides power supply for IC601, IC602 and IC803, which producess 8V, 5V, 3.3V voltage to the circuit.

■ 6. Display Circuit

Display circuit is comprised of CPU (IC502), LCD module, 8-digit LED, LED and other components. Radio features are programmable by PF1-PF4. Data is displayed on the 8-digit LED in alphanumeric form.

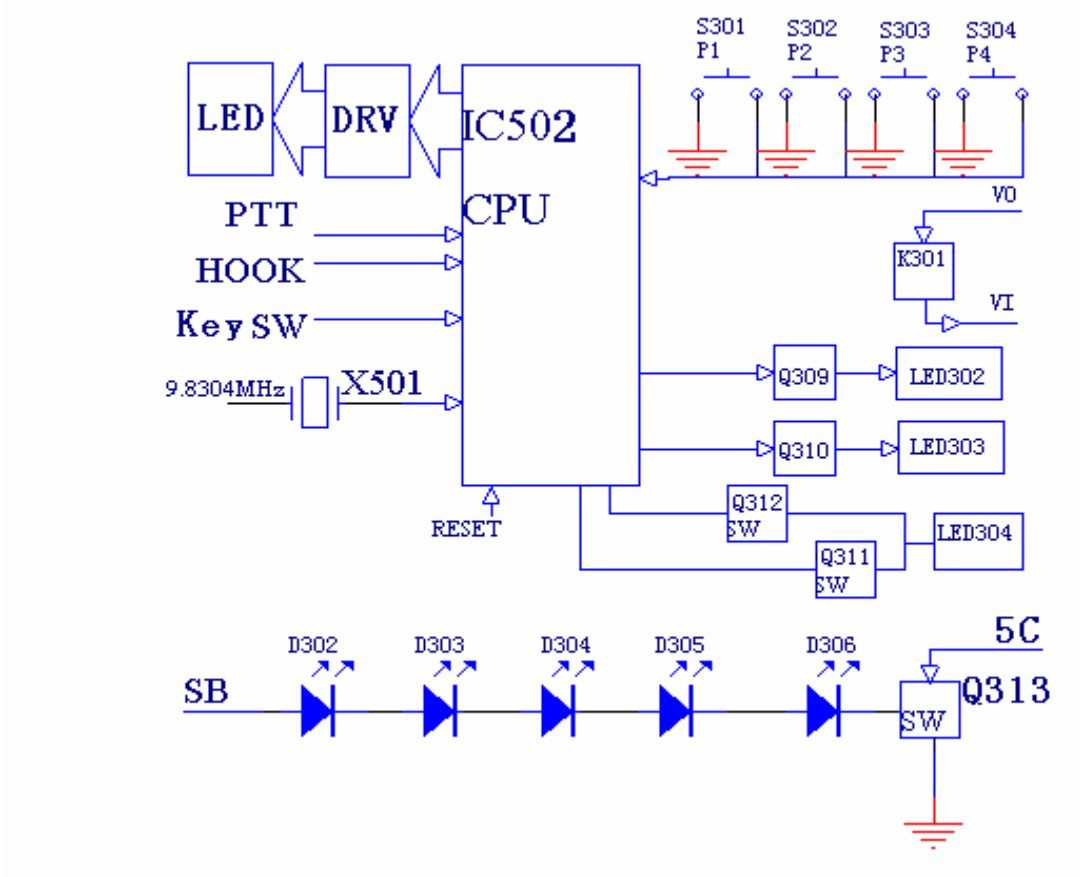

Fig6. Display Circuit