

# Evaluation board with increased-frequency 800 MHz STM32MP157 MPU

#### Introduction

The STM32MP157F-EV1 Evaluation board is designed as a complete demonstration and development platform for STMicroelectronics Arm®-based dual Cortex®-A7 32 bits and Cortex®-M4 32 bits MPUs in the STM32MP1 Series. It leverages the capabilities of increased-frequency 800 MHz STM32MP1 Series microprocessors for the user to develop applications, using STM32 MPU OpenSTLinux Distribution software for the main processor, and STM32CubeMP1 software for the co-processor. It includes an ST-LINK embedded debug tool, LEDs, push-buttons, one joystick, 1-Gbps Ethernet, CAN FD, one USB OTG Micro-AB connector, four USB Host Type-A connectors, LCD display with touch panel, camera, stereo headset jack with analog microphone input, four digital microphones, one SPDIF Rx/Tx, smartcard, microSD™ card, and eMMC, NOR and NAND Flash memories.

STM32MP157F-EV1, shown in Figure 1 and Figure 2, is used as the reference design for user application development, although it is not considered as final application.

To expand the functionality of the STM32MP157F-EV1 Evaluation board, two GPIO expansion connectors are also available for motor control and Raspberry Pi<sup>®</sup> shields.

An ST-LINK/V2-1 is integrated on the board, as embedded in-circuit debugger and programmer for the STM32 MPU and the USB Virtual COM port bridge.

Figure 1. STM32MP157F-EV1 top view



Figure 2. STM32MP157F-EV1 bottom view



Pictures are not contractual.



#### 1 Features

- STM32MP157 Arm<sup>®</sup>-based dual Cortex<sup>®</sup>-A7 800 MHz 32 bits + Cortex<sup>®</sup>-M4 32 bits MPU in LFBGA448 package
- ST PMIC STPMIC1
- 2 × 4-Gbit DDR3L, 16 bits, 533 MHz
- 2 × 512-Mbit Quad-SPI Flash memory
- 32-Gbit eMMC v5.0
- 8-Gbit SLC NAND, 8 bits, 8-bit ECC, 4-KB PS
- 1-Gbit/s Ethernet (RGMII) compliant with IEEE-802.3ab
- USB Host 4-port hub
- USB OTG HS
- CAN FD
- 5.5" TFT 720×1280 pixels with LED backlight, MIPI DSI<sup>™</sup> interface, and capacitive touch panel
- SAI audio codec
- 5-megapixel, 8-bit camera
- 4 × ST-MEMS digital microphones
- Smartcard
- microSD<sup>™</sup> card
- 2 user LEDs
- 2 user and reset push-buttons, 1 wake-up button
- 4-direction joystick with selection button
- 5 V / 4 A power supply
- Board connectors:
  - Ethernet RJ45
  - 4 × USB Host Type-A
  - USB OTG Micro-AB
  - SPDIF RCA input and output
  - CAN FD
  - Stereo headset jack including analog microphone input
  - Audio jack for external speakers
  - Motor control
  - External I<sup>2</sup>C
  - LTDC
  - Trace, JTAG, RS-232
  - GPIO expansion connector (Raspberry Pi<sup>®</sup> shields capability)
  - MEMS-microphone daughterboard expansion connector
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: Virtual COM port and debug port
- STM32CubeMP1 and full mainline open-source Linux<sup>®</sup> STM32 MPU OpenSTLinux Distribution (such as STM32MP1Starter) software and examples
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench<sup>®</sup>, MDK-ARM, and STM32CubeIDE

STM32 Arm Cortex MPUs are based on the Arm® Cortex®-A and Cortex®-M processors.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

arm

UM2648 - Rev 1 page 2/61



# 2 Ordering information

To order an STM32MP157 Evaluation board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. List of available products

Order code	Board reference	Target STM32	Differentiating features
	MB1262: mother board		
STM32MP157F-EV1	MB1263: MPU subsystem daughterboard	STM32MP157FAA1	Secure Boot and
	MB1230: DSI display board	311VI32IVIP 137FAA1	cryptography
	MB1379: camera board		

## 2.1 Product marking

Evaluation tools marked as "ES" or "E" are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

"E" or "ES" marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet "Package information" paragraph at the <a href="https://www.st.com">www.st.com</a> website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

#### 2.2 Codification

The meaning of the codification is explained in Table 2.

**Table 2. Codification explanation** 

STM32MP1XXY-EVZ	Description	Example: STM32MP157F-EV1
STM32MP1	MPU series in STM32 Arm Cortex MPUs	STM32MP1 Series
XX	MPU product line in the series STM32MP157	
Y Options: F: Secure Boot, cryptography hardware, 800 MHz increased frequency  Secure Boot, cryptography hardware, 800 MHz increased frequency		Secure Boot, cryptography hardware, 800 MHz increased frequency
EVZ	Evaluation board configuration • EV1: with PMIC	PMIC

The order code is mentioned on a sticker placed on the top or bottom side of the board.

UM2648 - Rev 1 page 3/61



# 3 Development environment

# 3.1 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit, or macOS®
- USB Type-C<sup>™</sup> to Type-A cable
- USB Type-A to Micro-B cable
- USB Type-A to Micro-AB cable

Note: macOS<sup>®</sup> is a trademark of Apple Inc. registered in the U.S. and other countries.

# 3.2 Development toolchains

- IAR Systems IAR Embedded Workbench®(1)
- Keil® MDK-ARM<sup>(1)</sup>
- STMicroelectronics STM32CubeIDE
- GCC
- 1. On Windows® only.

## 3.3 Demonstration software

The STM32 MPU OpenSTLinux Distribution and STM32CubeMP1 base demonstration software is preloaded in the microSD $^{\text{TM}}$  for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

UM2648 - Rev 1 page 4/61



# 4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition	
Jumper JPx ON	Jumper fitted	
Jumper JPx OFF	Jumper not fitted	
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2	
Solder bridge SBx ON	SBx connections closed by 0 $\Omega$ resistor	
Solder bridge SBx OFF	SBx connections left open	
Resistor Rx ON	Resistor soldered	
Resistor Rx OFF	Resistor not soldered	

UM2648 - Rev 1 page 5/61



# 5 Delivery recommendations

Before the first use, make sure that no damage occurred to the board during shipment and no socketed components are loose in their sockets or fallen into the plastic bag.

In particular, pay attention to the following components:

- 1. MB1263 daughterboard connected to the MB1262 mother board
- 2. microSD card in its MB1263/CN9 receptacle
- 3. LCD MB1230 daughterboard in MB1262/CN19 DSI connector, and screw, spacer and nut are in place
- 4. Camera module MB1379 board in MB1262/CN7 connector, and screw, spacer and nut are in place For product information related to the STM32MP157 microprocessors, visit the *www.st.com* website.

UM2648 - Rev 1 page 6/61



# 6 Hardware layout and configuration

The STM32MP157F-EV1 Evaluation board is designed around the STM32MP157FAA1 target microprocessor in LFBGA 448-pin package. Figure 3 illustrates the STM32MP157F-EV1 hardware block diagram. Figure 4 shows the location of main components on the Evaluation board.

UM2648 - Rev 1 page 7/61



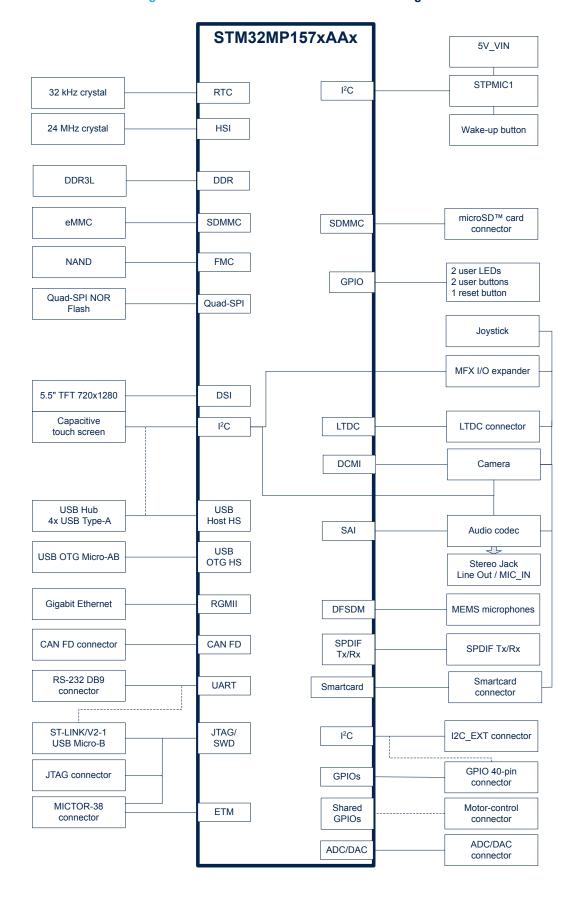


Figure 3. STM32MP157F-EV1 hardware block diagram

UM2648 - Rev 1 page 8/61



Ethernet Ethernet Module JTAG CAN FD MB1263C MB1262C T STM32MP15X-EVAL

Figure 4. STM32MP157F-EV1 board overview

Note: Numbers in yellow refer to positions explained in Table 4, Table 5, and Table 6.

UM2648 - Rev 1 page 9/61



Table 4. STM32MP157F-EV1 overview

Position	Description	
1	MB1262 mother board	
2	MB1263 daughterboard	
3	MB1230 DSI (MIPI <sup>®</sup> standard) 720p display	
4	MB1379 daughterboard camera	
5	microSD <sup>™</sup> card	

Table 5. MB1263 daughterboard overview

Position	Description	Position	Description
50 ( <b>B1</b> )	Reset button	59 ( <b>CN1</b> )	MB1263 power 5 V-3 A
51 ( <b>LD2</b> )	User LED (red)	60 ( <b>SW1</b> )	Boot mode selection
52 ( <b>B2</b> )	User button (PA13)	61 ( <b>U3</b> )	PMIC (STPMIC1A)
53 ( <b>LD3</b> )	User LED (green)	62 ( <b>LD6</b> )	ST-LINK LED (bicolor)
54 ( <b>B3</b> )	User button (PA14)	63 ( <b>CN4</b> )	USB Micro-B (ST-LINK/V2-1)
55 ( <b>LD5</b> )	User LED (blue)	64 ( <b>U4</b> )	STM32MP157FAA1 LFBGA448
56 ( <b>LD4</b> )	User LED (orange)	65 ( <b>U5</b> )	eMMC
57 ( <b>B4</b> )	Wake-up button	66 ( <b>U6/U7</b> )	2 x DDR3L 16 bits
58 ( <b>LD1</b> )	Power LED (green)	67 ( <b>µSD</b> )	microSD <sup>™</sup> 3.0 card (back side slot)

Table 6. MB1262 mother board overview

Position	Description	Position	Description
10 ( <b>CN3</b> )	Ethernet	11 ( <b>CN8</b> )	Microphone MEMS daughterboard connector
12 ( <b>CN4</b> )	Speaker audio output	13 ( <b>CN5</b> )	Headset audio output
14 ( <b>U8</b> )	Audio codec (Wolfson WM8994)	15 ( <b>CN1</b> )	SPDIF RX
16 ( <b>CN2</b> )	SPDIF TX	17 ( <b>U5</b> )	Smartcard (back side slot)
18 ( <b>LD1</b> )	Ethernet LED (green)	19 ( <b>CN6</b> )	Ethernet daughterboard connector
20 ( <b>U10</b> )	Trace connector	21 ( <b>CN11</b> )	LTDC LCD TFT display controller (STM32 specific) connector
22 ( <b>CN12</b> )	RS-232 (UART4)	23 (CN13)	External E2P connector
24 (CN16)	USB Micro-AB (USB OTG)	25 ( <b>LD2</b> )	USB OTG LED (green)
26 ( <b>LD3</b> )	USB Type-A port LED (red)	27 (CN17)	MFX header 4 pins
28 ( <b>CN14</b> )	JTAG connector	29 (CN15)	CAN FD
30 (CN18)	2 USB Type-A port (host)	31 (CN20)	2 USB Type-A port (host)
32 ( <b>B2</b> )	Reset button	33 ( <b>B1</b> )	Joystick
34 (CN22)	Motor control connector	35 (CN21)	GPIO expansion connector
4 (CN7)	Camera sensor connector	-	-

UM2648 - Rev 1 page 10/61



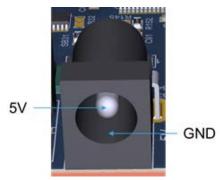
## 6.1 Power supply management

#### 6.1.1 5 V power supply

STM32MP157F-EV1 Evaluation board is designed to be powered from the 5 V DC power supply provided in the package.

MB1263/LD1 Green LED turns on when this power supply is connected to the power jack MB1263/CN1.





## 6.1.2 Platform power tree

All supply lines required for the operation of the components on STM32MP157F-EV1 are derived from the 5 V power source. Indeed, this 5 V power source is the input supply of the STPMIC1 that distributes then all the supplies to the subsystems as described in the power tree Figure 6.

The voltage on the VBAT pin of the STM32MP157FAA1 can be provided by an external battery. Use MB1263/BT1 to plug a CR1220 3 V lithium battery. Table 7 describes the HW configuration for the VBAT connection.

Table 7. HW configuration for the VBAT connection

Jumpers	Setting	Configuration <sup>(1)</sup>	
MB1263/JP3 JP3[1-2]		VBAT connected to VDD	
WID 1203/3F3	JP3[2-3]	VBAT connected to CR1220 battery holder MB1263/BT1	

1. Default configuration in bold

UM2648 - Rev 1 page 11/61



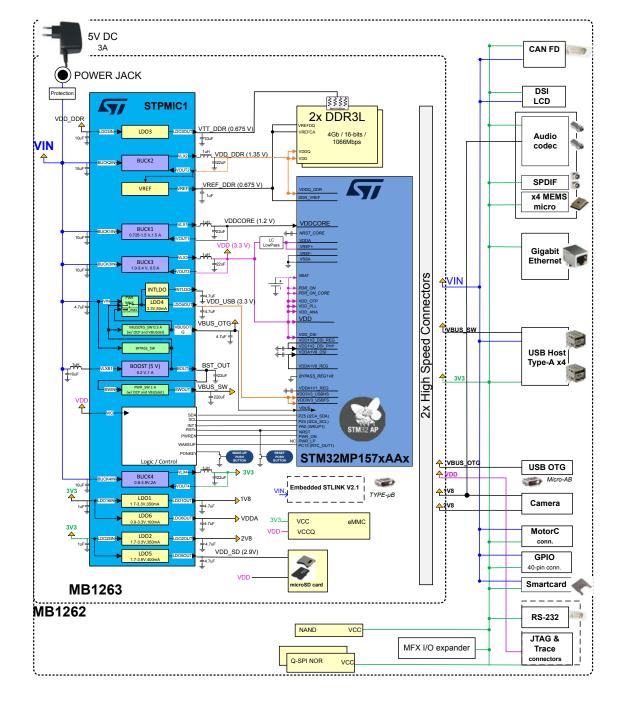


Figure 6. STM32MP157F-EV1platform power tree

## **6.1.3** STPMIC1

For general information concerning the STPMIC1, please refer to STPMIC1 datasheet at the www.st.com website.

UM2648 - Rev 1 page 12/61



#### 6.2 Clocks

Two clocks are available on STM32MP157F-EV1 for the STM32MP157FAA1 target microprocessor.

#### 6.2.1 LSE clock

External 32.768 kHz crystal

#### 6.2.2 HSE clock

External 24 MHz crystal

#### 6.3 Reset sources

The reset signal of the STM32MP157F-EV1 platform is active low.

The sources of the platform reset are:

- Two reset buttons MB1263/B1 and MB1262/B2 (black buttons)
- STM32MP157FAA1 microprocessor: internal voltage monitor, SW request or watchdog
- STPMIC1
- JTAG/SWD connector MB1262/CN14
- ETM Trace Mictor-38 connector MB1262/U10
- Embedded ST-LINK/V2-1

The STM32MP157FAA1 microprocessor also drives a subsystem reset, SUB\_NRST signal on PD10 IO, to the peripherals: USB Host Hub, MFX, Ethernet, and RGB\_LTDC connector.

## 6.4 User buttons and LEDs

Table 8 describes the HW configuration for the user buttons and LEDs.

Table 8. HW configuration for the user buttons and LEDs

I/O	LED color and label Button label	
PD8	PD8 is connected to the orange LD4. Active High -	
PD9	PD9 is connected to the blue LD5. Active High -	
PA13	PA13 is connected to red LD2. Active Low User PA13	
PA14	MFX_IO13 is connected to orange LED LD7. Active Low	User PA14

## 6.5 Physical input devices: buttons

The STM32MP157F-EV1 board provides a number of input devices for physical human control:

- Two reset buttons (MB1263/B1 and MB1262/B2)
- Four-way joystick controller with select key (MB1262/B1)
- Wake-up button (MB1263/B4)

Table 9. Physical user devices: buttons

Devices	Purpose - I/O
Wake-up button (MB1263/B4)	Awakes the platform from low-power modes. Connected to STPMIC1 PONKEY, which generates a wake-up signal on STM32MP157 PA0
Reset buttons (MB1263/B1 or MB1262/B2)	NRST signal
JOY_CENTER: Joystick select key (MB1262/B1 pin2)	MFX_IO0
JOY_DOWN: Joystick down direction (MB1262/B1 pin3)	MFX_IO1

UM2648 - Rev 1 page 13/61



Devices	Purpose - I/O
JOY_LEFT: Joystick left direction (MB1262/B1 pin1)	MFX_IO2
JOY_RIGHT: Joystick right direction (MB1262/B1 pin6)	MFX_IO3
JOY_UP: Joystick up direction (MB1262/B1 pin4)	MFX_IO4

# 6.6 Boot options

The STM32MP157x-EV1 board may boot from different sources as described in Table 10.

Table 10. HW configuration for the boot mode MB1263/SW1

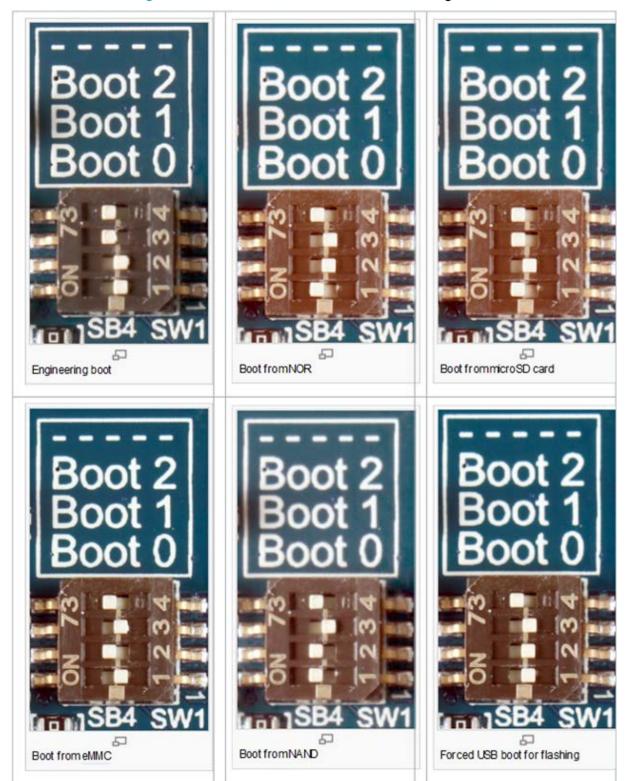
Boot mode	BOOT2	BOOT1	воот0
Serial NOR	0	0	1
microSD card	1	0	1
eMMC	0	1	0
NAND	0	1	1
UART and USB	0	0	0
UART and USB	1	1	0
Reserved	1	0	0

The boot related switches (MB1263/SW1) must be configured as illustrated by one of the following pictures:

UM2648 - Rev 1 \_\_\_\_\_\_ page 14/61



Figure 7. STM32MP157F-EV1 boot-related switch configuration



## 6.7 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated in the STM32MP157F-EV1 Evaluation board. The embedded ST-LINK/V2-1 supports JTAG, SWD and VCP for the target STM32 Arm Cortex MPUs.

UM2648 - Rev 1 page 15/61



For information about debugging and programming features refer to the *ST-LINK/V2 in-circuit debugger/* programmer for *STM8* and *STM32* user manual (UM1075) available on www.st.com, which describes in details all the ST-LINK/V2-1 features.

Figure 8 shows the ST-LINK USB Micro-B connector pinout.

Figure 8. ST-LINK USB Micro-B connector pinout MB1263/CN4

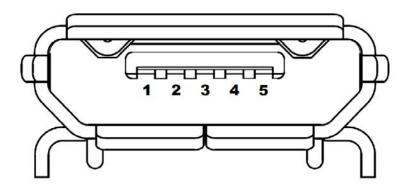


Table 11 describes the ST-LINK USB Micro-B connector pinout.

Pin **Board function** ST-LINK STM32 pin **VBUS** Power 1 2 PA11 DM 3 DP PA12 4 ID **GND** 5 GND **GND** 

Table 11. ST-LINK USB Micro-B connector pinout MB1263/CN4

Since the current consumption of the STM32MP157F-EV1 Evaluation board exceeds the permissible current on the USB, it is not possible to power the board through the ST-LINK/V2-1 USB. To use the ST-LINK/V2-1 for programming and debugging, it is mandatory to power the board first using the 5 V power supply, then connect the ST-LINK/V2-1 USB cable to the PC. Proceeding this way, the USB enumeration succeeds with the support of the external power source.

The user must respect the following power sequence procedure:

- Check that MB1263/JP1 is OFF, MB1263/JP4 [2-3] and JP5 [2-3] are ON to connect UART4 as ST-LINK VCP.
- 2. Connect the 5 V power source, MB1263/LD1 LED turns green, MB1263/LD6 LED flashes red.
- Connect the PC to USB connector MB1263/CN4, MB1263/LD6 LED is red and becomes green once the connection with the ST-LINK is established.

#### 6.7.1 Drivers

The ST-LINK/V2-1 requires a dedicated USB driver, which, for Windows 7<sup>®</sup>, Windows 8<sup>®</sup> and Windows 10<sup>®</sup>, is found at *www.st.com*.

In case the STM32MP157F-EV1 Evaluation board is connected to the PC before the driver is installed, some of its interfaces may be declared as "Unknown" in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager as shown in Figure 9.

Note: Prefer using the USB Composite Device handle for a full recovery.

UM2648 - Rev 1 page 16/61



**USB Composite Device Properties** Device Manager File Action View Help General Driver Details USB Composite Device Universal Serial Bus controllers Generic USB Hub Property Generic USB Hub Hardware Ids Generic USB Hub Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Contro Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Contro USB\VID\_0483&PID\_374B&REV\_0100 Intel(R) USB 3.0 eXtensible Host Controller USB\VID\_0483&PID\_374B Intel(R) USB 3.0 Root Hub USB Composite Device Update Driver Software... USB Mass Storage D Disable Launches the Update Driver Softwar Uninstall

Figure 9. USB composite device

## 6.7.2 ST-LINK/V2-1 firmware upgrade

For its own operation, ST-LINK/V2-1 embeds a dedicated microcontroller with Flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance.

The ST-LINK/V2-1 embeds a firmware mechanism for the in-situ upgrade through the USB port. As the firmware may evolve during the lifespan of the ST-LINK/V2-1 product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the STM32MP157F-EV1 Evaluation board and periodically, to stay up-to-date with the latest firmware version.

#### 6.8 ETM TRACE Mictor-38 connector

The Mictor-38 connector MB1262/U10 may output trace signals used for debug, as well as JTAG signals. Table 12 describes the HW configuration for the TRACE function.

Table 12. HW configuration for the TRACE connector MB1262/U10

I/O	Bridge	Setting <sup>(1)</sup>	Comment	
		ON	PI14 may be used for the trace function TRACE CLK	
PI14	SB38	OFF	PI14 is not connected to Trace	
		OFF	PI14 may be used for LTDC CLK	
		ON	PI12 may be used for the trace function TRACE_D0	
PI12	SB43	OFF	PI12 is not connected to Trace	
		OFF	PI12 may be used for LTDC HSYNC	
		ON	PI13 may be used for the trace function TRACE_D1	
PI13	SB42	OFF	PI13 is not connected to Trace	
		OFF	PI13 may be used for LTDC VSYNC	
		ON	PJ5 may be used for the trace function TRACE_D2	
PJ5	SB36	SB36	OFF	PJ5 is not connected to Trace
		OFF	PJ5 may be used forLTDC_R6	
	ON	ON	PJ6 be used for the trace function TRACE_D3	
PJ6 SI	SB41	OFF	PJ6 is not connected to Trace	
		UFF	PJ6 may be used for LTDC_R7	
PK1	SB40	ON	PK1 may be used for the trace function TRACE_D4	

UM2648 - Rev 1 page 17/61



I/O	Bridge	Setting <sup>(1)</sup>	Comment
PK1	SB40	OFF	PK1 is not connected to Trace
	3540	OFF	PK1 may be used for LTDC_G6
		ON	PK2 may be used for the trace function TRACE_D5
PK2	SB39		PK2 is not connected to Trace
		OFF	PK2 may be used for LTDC_G7
		ON	PK5 may be used for the trace function TRACE_D6
PK5	SB49	OFF	PK5 is not connected to Trace
		OFF	PK5 may be used for LTDC_B6
		ON	PK6 may be used for the trace function TRACE_D7
PK6	SB35	OFF	PK6 is not connected to Trace
		OFF	PK6 may be used for LTDC_B7
		ON	PJ0 may be used for the trace function TRACE_D8
PJ0	SB34	OFF	PJ0 is not connected to Trace
		OFF	PJ0 may be used for LTDC_R1
		ON	PJ1 may be used for the trace function TRACE_D9
PJ1	SB37	OFF	PJ1 is not connected to Trace
		OFF	PJ1 may be used for LTDC_R2
		ON	PJ2 may be used for the trace function TRACE_D10
PJ2	SB48	OFF	PJ2 is not connected to Trace
		OFF	PJ2 may be used for LTDC_R3
		ON	PJ3 may be used for the trace function TRACE_D11
PJ3	SB47	OFF	PJ3 is not connected to Trace
			PJ3 may be used for LTDC_R4
		ON	PJ4 may be used for the trace function TRACE_D12
PJ4	SB46	OFF	PJ4 is not connected to Trace
		OFF	PJ4 may be used for LTDC_R5
		ON	PJ7 may be used for the trace function TRACE_D13
PJ7	SB45	OFF	PJ7 is not connected to Trace
			PJ7 may be used for LTDC_G0
		ON	PJ8 may be used for the trace function TRACE_D14
PJ8	SB44	OFF	PJ8 is not connected to Trace
		OFF	PJ8 may be used for LTDC_G1
		ON	PJ9 may be used for the trace function TRACE_D15
PJ9	SB50	OFF	PJ9 is not connected to Trace
		OFF	PJ9 may be used for LTDC_G2

<sup>1.</sup> Default configuration is shown in **bold** 

Figure 10 shows the TRACE Mictor-38 connector

UM2648 - Rev 1 page 18/61





Figure 10. TRACE Mictor-38 connector: MB1262/U10

Table 13 describes the MICTOR-38 connector pinout for TRACE and JTAG signals.

Table 13. TRACE MICTOR-38 connector pinout: MB1262/U10

Board function	Pin	Pin	Board function
NC	1	2	NC
NC	3	4	NC
GND	5	6	TRACE_CLK
Pull-down	7	8	Pull-down
NRST	9	10	Pull-down
TDO/SWO	11	12	VDD
Pulldown	13	14	VDD
TCK/SWCLK	15	16	TRACE_D7
TMS/SWDIO	17	18	TRACE_D6
TDI	19	20	TRACE_D5
NJTRST	21	22	TRACE_D4
TRACE_D15	23	24	TRACE_D3
TRACE_D14	25	26	TRACE_D2
TRACE_D13	27	28	TRACE_D1
TRACE_D12	29	30	GND
TRACE_D11	31	32	GND
TRACE_D10	33	34	VDD
TRACE_D9	35	36	GND
TRACE_D8	37	38	TRACE_D0

## 6.9 JTAG connector

A JTAG/Serial Wire Debug 20-pin IDC connector (ARM JTAG 20, IDC 2.54 mm) MB1262/CN14 outputs the JTAG signals. The JTAG function is a dedicated interface of the STM32MP157FAA1 microprocessor.

Table 14 describes the JTAG connector pinout.

UM2648 - Rev 1 page 19/61



Table 14. MB1262/CN14 JTAG connector pinout

Board function	Pin	Pin	Board function
Power	1	2	Power
NJTRST	3	4	GND
JTDI	5	6	GND
JTMS/SWDIO	7	8	GND
JTCK/SWCLK	9	10	GND
Pull down	11	12	GND
JTDO/SWO	13	14	GND
NRST	15	16	GND
Pull down	17	18	GND
Pull down	19	20	GND

## 6.10 DDR3L

Two 16-bit DDR3L NT5CC256M16ER-EK of 4 Gbytes are implemented in flyby topology in MB1263/U6 and U7 positions. They are connected to the dedicated DDR interface of STM32MP157FAA1. For detailed information concerning the DDR HW design implementation, refer to the application note AN5122 available on the <a href="https://www.st.com">www.st.com</a> website.

## **6.11 eMMC**

The STM32MP157FAA1 SDMMC2 in 8-bit wide bus mode drives a THGBMNG5D1LBAIL 32-Gbit eMMC in MB1263/U5 position.

#### 6.11.1 eMMC I/O interface

Table 15 describes the HW configuration for the eMMC interface.

Table 15. HW configuration for the eMMC interface

I/O	Configuration <sup>(1)</sup>
PB14	SDMMC2_D0 connected to MB1263/U5 DAT0
PB15	SDMMC2_D1 connected to MB1263/U5 DAT1
PB3	SDMMC2_D2 connected to MB1263/U5 DAT2
PB4	SDMMC2_D3 connected to MB1263/U5 DAT3
PA8	SDMMC2_D4 connected to MB1263/U5 DAT4
PA9	SDMMC2_D5 connected to MB1263/U5 DAT5
PE5	SDMMC2_D6 connected to MB1263/U5 DAT6
PD3	SDMMC2_D7 connected to MB1263/U5 DAT7
PE3	SDMMC2_CK connected to MB1263/U5 CLK
PG6	SDMMC2_CMD connected to MB1263/U5 CMD

<sup>1.</sup> Minimum set of signals required by the boot ROM during eMMC boot in bold

# 6.12 NAND Flash memory

The STM32MP157FAA1 FMC interface is connected to an 8-Gbit SLC NAND, 8-bit, 8-bit ECC, and 4-KByte PS MT29F8G08ABACAH4 in MB1262/U11 position.

UM2648 - Rev 1 page 20/61



#### 6.12.1 NAND I/O interface

Table 16 features the HW configuration for the NAND interface.

Table 16. HW configuration for the NAND interface

I/O	Configuration <sup>(1)</sup>
PD6	NAND_NWAIT connected to MB1262/U11 R/B#
PD11	NAND_CLE connected to MB1262/U11 CLE
PD12	NAND_ALE connected to MB1262/U11 ALE
PG9	NAND_NCE connected to MB1262/U11 CE#
PD5	NAND_NWE connected to MB1262/U11 WE#
PD4	NAND_NOE connected to MB1262/U11 RE#
PD14	NAND_D0 connected to MB1262/U11 IO0
PD15	NAND_D1 connected to MB1262/U11 IO1
PD0	NAND_D2 connected to MB1262/U11 IO2
PD1	NAND_D3 connected to MB1262/U11 IO3
PE7	NAND_D4 connected to MB1262/U11 IO4
PE8	NAND_D5 connected to MB1262/U11 IO5
PE9	NAND_D6 connected to MB1262/U11 IO6
PE10	NAND_D7 connected to MB1262/U11 IO7

<sup>1.</sup> Minimum set of signals required by the boot ROM during NAND boot in bold

# 6.13 Quad-SPI NOR Flash memory

The STM32MP157FAA1 Quad-SPI interface is in dual-serial mode to interface with two NOR Flash memories in parallel. Two MX25L51245G-XD, 3V3/512-Mbit each, are fitted on the STM32MP157F-EV1MB1262, in MB1262/U14 and MB1262/U15 positions.

#### 6.13.1 Quad-SPI I/O interface

Table 17 describes the HW configuration for the Quad-SPI interface

Table 17. HW configuration for the Quad-SPI interface

I/O	Configuration <sup>(1)</sup>
PF8	QSPI_BK1_IO0 connected to MB1262/U14 SIO0
PF9	QSPI_BK1_IO1 connected to MB1262/U14 SIO1
PF7	QSPI_BK1_IO2 connected to MB1262/U14 SIO2
PF6	QSPI_BK1_IO3 connected to MB1262/U14 SIO3
PB6	QSPI_BK1_NCS connected to MB1262/U14 CS#
PH2	QSPI_BK2_IO0 connected to MB1262/U15 SIO0
PH3	QSPI_BK2_IO1 connected to MB1262/U15 SIO1
PG10	QSPI_BK2_IO2 connected to MB1262/U15 SIO2
PG7	QSPI_BK2_IO3 connected to MB1262/U15 SIO3
PC0	QSPI_BK2_NCS connected to MB1262/U15 CS#
PF10	QSPI_CLK connected to MB1262/U14 SCLK and MB1262/U15 SCLK

<sup>1.</sup> Minimum set of signals required by the boot ROM during dual-serial NOR boot in **bold** 

UM2648 - Rev 1 page 21/61



#### 6.14 microSD card

The MB1263/CN9 slot for microSD card is routed to the STM32MP157FAA1 SDMMC1 port. This SD card interface is compliant with SD Memory Card Specification Version 3.01, UHS-I, all operation modes up to SDR104 and DDR50. The SD card interface is compatible with 1.8 V or 2.9 V signal levels.

#### 6.14.1 SD card interface

The SD card interface, SDMMC1, is 4-bit wide with level shifter support, in order to connect to an SD 3.0-compliant bidirectional dual voltage level translator, interfacing with the memory card inserted in the SDCARD connector.

Table 18 describes the I/O for the SDMMC1 interface.

I/O Signal<sup>(1)</sup> PC12 SDMMC1\_CK PE4 SDMMC1\_CKIN PD2 SDMMC1\_CMD PB9 SDMMC1 CDIR PC8 SDMMC1\_D0 PC9 SDMMC1\_D1 PC10 SDMMC1\_D2 PC11 SDMMC1\_D3 PF2 SDMMC1\_D0DIR PC7 SDMMC1 D123DIR PF14 uSD\_LDO\_SEL

Table 18. I/O configuration for the SDIO interface

Figure 11 shows the SDCARD connector pinout MB1263/CN9.

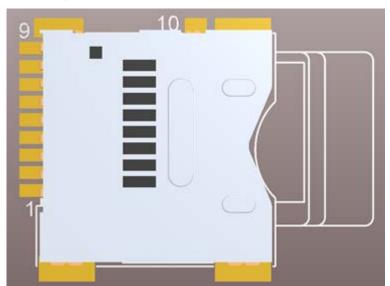


Figure 11. SDCARD connector pinout MB1263/CN9

Table 19 describes the SDCARD connector pinout MB1263/CN9.

UM2648 - Rev 1 page 22/61

<sup>1.</sup> Minimum set of signals required by the boot ROM during SD card boot in bold



Table 19. SDCARD connector pinout MB1263/CN9

Pin	Board function
1	DATA2_SD
2	DATA3_SD
3	CMD_SD
4	VDD_SD
5	CLK_SD
6	GND
7	DATA0_SD
8	DATA1_SD
9	GND
10	SDCARD_DETECT active LOW

## 6.15 Audio

A codec WM8994ECS/R connected to an SAI of STM32MP157FAA1 supports the TDM feature of the SAI port. The TDM feature offers to STM32MP157FAA1 the capability to stream stereo audio channels. There are four digital microphones on the STM32MP157F-EV1 board,. The STM32MP157F-EV1 also offers the possibility to connect a MEMS extension module.

#### 6.15.1 Audio codec interface

The audio codec has two supplies, 3V3 and 1V8, provided by STPMIC1.

The audio codec interfaces to the MPU are SAI2 and I2C2. Audio interrupt is connected to the I/O-expander MFX. SAI2A as Tx and SAI2B as Rx are connected to two different analog interfaces of the codec, to independently playback and record.

SAI2 is connected by default to the audio codec, and may be shared via solder bridge configuration with the expansion GPIO connector (refer to paragraph 6.28).

I2C2 is shared with all the peripherals: audio codec, DSI LCD, RGB LTDC, camera, and USB Hub. The audio codec  $I^2C$  address is 0x36

Table 20. I/O configuration for the audio codec interface

I/O	Board function
PI5	SAI2_SCKA
PI7	SAI2_FSA
PI6	SAI2_SDA
PF11	SAI2_SDB
PE12	SAI2_SCK_B
PE13	SAI2_FS_B
PE0	SAI2_MCLKA
PE14	SAI2_MCLKB
PH5	I2C2_SDA
PH4	12C2_SCL
MFX_IO5	AUDIO_INT

## 6.15.2 Digital microphones

MB1262/U1, U2, U3 and U4 are four MP34DT01TR MEMS digital omnidirectional microphones providing PDM (pulse-density modulation) outputs. The implementation allows the beam forming.

UM2648 - Rev 1 page 23/61



Those four digital microphones support two stereo inputs connected either to the audio codec or, by default, connected on two DFSDM odd channels of STM32MP157FAA1: DFSDM\_DATA1 and DFSDM\_DATA3 synchronized on DFSDM CKOUT.

The STM32MP157FAA1 DFSDM interface is shared among the four embedded digital microphones and the extension module on connector MB1262/CN8.

Table 21 describes the HW configuration for the digital microphones.

Table 21. HW configuration for the digital microphones

Jumpers	HW	Setting	Configuration <sup>(1)</sup>
MD4000/JD4	U1/U3 stereo output selection	JP1[1-2]	Connected to codec DMICDAT2
MB1262/JP1		JP1[2-3]	Connected to STM32MP157FAA1 DFSDM_DATA3
MD4000/JD0	U2/U4 stereo output selection	JP2[1-2]	Connected to codec DMICDAT1
MB1262/JP2		JP2[2-3]	Connected to STM32MP157FAA1 DFSDM_DATA1
MB1262/JP3	U1/U2/U3/U4 CLK selection	JP3[1-2]	Connected to STM32MP157FAA1DFSDM_CKOUT
WID 1202/JF3		JP3[2-3]	Connected to codec DMICCLK
MB1262/JP4	U1/U2/U3/U4 VDD selection	JP4[1-2]	3V3
		JP1[2-3]	Codec MICBIAS1

<sup>1.</sup> Default configuration in bold

## 6.15.3 Analog microphone and audio jack headphone

A headset including an analog microphone and a stereo headphone may be connected to the black 3.5 mm headset jack MB1262/CN5.



Figure 12. Audio jack connector MB1262/CN5

Table 22. Audio jack connector pinout MB1262/CN5

Pin	Board function
2	MIC_IN
3	GND
4	OUT_RIGHT
5	N/A
6	OUT_LEFT
7	N/A

UM2648 - Rev 1 page 24/61



## 6.15.4 Audio speaker out

The codec stereo speaker output is connected to a green 3.5 mm Speaker\_out jack MB1262/CN4.

Speaker\_out 4 7

Figure 13. Audio jack connector MB1262/CN4

Table 23. Audio jack connector pinout MB1262/CN4

Pin	Board function
2	GND
3	GND
4	OUT_RIGHT
5	N/A
6	OUT_LEFT
7	N/A

## 6.15.5 SPDIF input and output

An RCA (white) connector MB1262/CN1 followed by an amplifier/filter stage is connected to the STM32MP157FAA1 SPDIF RX\_IN.

The STM32MP157FAA1 SAI4\_SDA port provides SPDIF\_TX data to a RCA (yellow) connector MB1262/CN2.

UM2648 - Rev 1 page 25/61



RIS CIA SPDIF input SPDIF output

Figure 14. SPDIF input MB1262/CN1 and output MB1262/CN2 connectors

#### 6.15.6 I/O restriction to other features

Due to the sharing of some I/Os of STM32MP157FAA1 by multiple peripherals, the following limitations apply in using the audio features:

The SAI audio codec must not be operated simultaneously with expansion connector MB1262/CN21. The MEMS DFSDM must not be operated simultaneously with DFSDM of EXT MEMS module MB1262/CN8.

#### 6.16 **DSI LCD**

Through the MB1262/CN19 connector, a DSI LCD mounted on a daughterboard MB1230 is provided. MB1230 is a 5.5" TFT 720\*1280 pixels with LED backlight, MIPI DSI<sup>SM</sup> interface and capacitive touch panel based on RK055AHD042-CT module embedding the LCD driver IC RM68200 and a touch screen controller GT9147. 3V3 and VIN supply MB1230:

- 3V3: for the LCD module (VDD\_LCD and VIO\_LCD) and touch screen
- · VIN: for the LED backlight of the LCD

## 6.16.1 DSI LCD interface

MB1230 is connected to the STM32MP157FAA1 through the DSI interface,  $I^2C$  to control the GT9147, and LCD\_BL\_CTRL. LCD\_INT signal is connected to MFX.

The  $I^2C$  is I2C2 that is shared with all the peripherals: audio codec, MFX, RGB LTDC, camera, and USB Hub. The GT9147  $I^2C$  address is 0xBB.

Table 24 describes the I/O configuration for the LCD interface.

Table 24. I/O configuration for the LCD interface

I/O	Configuration
PH4	12C2_SCL
PH5	I2C2_SDA
DSI_D0P	DSI_D0_P is used as MIPI-DSI data Lane 0 positive
DSI_D0N	DSI_D0_N is used as MIPI-DSI data Lane 0 negative

UM2648 - Rev 1 page 26/61



I/O	Configuration	
DSI_D1P	DSI_D1_P is used as MIPI-DSI data Lane 1 positive	
DSI_D1N	DSI_D1_N is used as MIPI-DSI data Lane 0 negative	
DSI_CKP	DSI_CKP is used as clock Lane positive	
DSI_DKN	DSI_DKN is used as clock Lane negative	
PD13	LCD_BL_CTRL - Backlight Control	
PF15	DSI_RESET	
PC6	DSI_TE – Tearing Effect	
MFX_IO14	LCD_INT - interruption	

## 6.17 Camera

Through the MB1262/CN7 connector, a camera module mounted on a daughterboard MB1379 is provided. MB1379 is a 5 Mpixels, 8-bit color camera module based on OV5640 image sensor, clocked from a 24 MHz crystal (MB1379/X1). It is supplied by 2V8.

#### 6.17.1 Camera interface

MB1379 is connected to the STM32MP157FAA1 through the DCMI and I<sup>2</sup>C interfaces. RSTI, XSDN, PLUG signals are connected to MFX.

The  $I^2C$  is I2C2, which is shared with all the peripherals: audio codec, MFX, RGB LTDC, DSI LCD, and USB Hub. The camera  $I^2C$  address is 0x3C.

Table 25 describes the I/O configuration for the camera interface.

Table 25. I/O configuration for the camera interface

I/O	Configuration
PH4	12C2_SCL
PH5	I2C2_SDA
PH9	DCMI_D0
PH10	DCMI_D1
PH11	DCMI_D2
PH12	DCMI_D3
PH14	DCMI_D4
PI4	DCMI_D5
PB8	DCMI_D6
PE6	DCMI_D7
PI1	DCMI_D8 <sup>(1)</sup>
PH7	DCMI_D9 <sup>(1)</sup>
PI3	DCMI_D10 <sup>(1)</sup>
PH15	DCMI_D11 <sup>(1)</sup>
PB7	DCMI_VSYNC
PH8	DCMI_HSYNC
PA6	DCMI_PIXCLK
MFX_IO12	Camera plug detection
MFX_O3	RSTI - Camera RESETB, active low

UM2648 - Rev 1 page 27/61



I/O	Configuration	
MFX_O2	XSDN – Camera PWDN, active high	

<sup>1.</sup> Available on the MB1262/CN7 connector, but not used in the MB1379 module

## 6.18 1 Gbps Ethernet

The STM32MP157F-EV1 board provides a 1 Gbps Ethernet feature by means of an external physical interface device (PHY), RTL8211EG-VB-CG. This PHY is connected to the STM32MP157FAA1 gigabit reduced medium-independent interface (RGMII), and is clocked from a 25 MHz crystal (X1).

The Ethernet PHY is supplied by 3V3. It generates its own supply 1V05 and digital/analog 3V3.

LD1 LED blinks to indicate data transmission.

The Ethernet module connector MB1262/CN6 is for STMicroelectronics internal use only.

#### 6.18.1 RGMII interface

Table 26 describes the I/O configuration for the Ethernet interface.

Table 26. I/O configuration for the Ethernet interface

I/O	Configuration	
PD10	PD10 (SUB_NRST) is used as PHY_NRST active Low	
PA2	PA2 is used as ETH_MDIO	
PG0	PG0 is used as ETH_MDINT	
PC1	PB11 is used as ETH_MDC	
PA7	PA7 is used as ETH_RX_DV(PHY_AD2)	
PC4	PC4 is used as ETH_RXD0	
PC5	PC5 is used as ETH_RXD1	
PB0	PB0 is used as ETH_RXD2	
PB1	PB1 is used as ETH_RXD3	
PB11	PB11 is used as ETH_TX_EN	
PG13	PG13 is used as ETH_TXD0	
PG14	PG14 is used as ETH_TXD1	
PC2	PB11 is used as ETH_TXD2	
PE2	PE2 is used as ETH_TXD3	
PA1	PA1 is used as ETH_RX_CLK	
PG4	PG4 is used as ETH_GTX_CLK	
PG5	PG5 is used as ETH_CLK125	

UM2648 - Rev 1 page 28/61

Figure 15. Ethernet connector MB1262/CN3



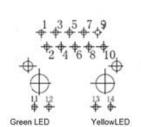


Table 27. Ethernet connector pinout MB1262/CN3

Pin number	Pin name	Function	
1	TX1+	First Didinational paints transmit and appains date	
2	TX1-	First Bidirectional pair to transmit and receive data	
3	TX2+	O- and Didinational ories to the oriest to t	
4	TX2-	Second Bidirectional pair to transmit and receive data	
5	CT1	Common connected to GND	
6	CT2	Common connected to GND	
7	TX3+		
8	TX3-	Third Bidirectional pair to transmit and receive data	
9	TX4+		
10	TX4-	Fourth Bidirectional pair to transmit and receive data	
11	GA	Green Led anode	
12	GC	Green Led cathode	
13	YA	Yellow Led anode	
14	YC	Yellow Led cathode	
15	GND	GND	
16	GND	GND	

## 6.19 USB OTG HS

The STM32MP157F-EV1 board supports USB OTG high-speed communication via a USB Micro-AB connector MB1262/CN16. OTG  $V_{BUS}$  supply is managed by the STPMIC1. MB1262/LD2 turns green when USB OTG connection is established.

#### 6.19.1 USB OTG interface

Table 28 describes the I/O configuration for the USB OTG interface.

Table 28. I/O configuration for the USB OTG interface

I/O	Configuration	
PA10	OTG_ID line detection	
OTG_VBUS	OTG_VBUS sensing	

UM2648 - Rev 1 page 29/61



I/O	Configuration
USB_DP2	USB_DP2
USB_DM2	USB_DM2

Figure 16. USB OTG Micro-AB connector MB1262/CN16



Table 29. USB OTG Micro-AB connector pinout MB1262/CN16

Pin CN16	Pin name	Signal name	Function
1	VBUS	OTG VBUS	V <sub>BUS</sub> supply and sensing
2	D-	DM	USB_DM2
3	D+	DP	USB_DP2
4	ID	ID	ID
5	GND	VBUS	GND

## 6.20 USB host

The STM32MP157F-EV1 board provides 4 USB host port (2 dual USB Type-A connectors MB1262/CN18 and CN20) by means of USB Hub USB2514B-AEZC. The USB2514B has a full power management for each USB Host port. The default configuration of USB2514B is done in HW, thus I<sup>2</sup>C is not needed by default. However, if required for a specific application, I<sup>2</sup>C may be accessed through MB1262/SB71 and SB68 to I2C2 as described in Table 30.

## 6.20.1 USB Host interface

Table 30 describes the I/O configuration for the USB Host interface.

Table 30. I/O configuration for the USB Host interface

I/O	SB	Setting	Configuration <sup>(1)</sup>
PH5	MB1262/SB71	OFF	PH5 is not used as I2C2_SDA
PH4	MB1262/SB68	OFF	PH4 is not used as I2C2_SCL
PD10	-	-	SUB_NRST
USB_DP1	-	-	USB1_P
USB_DM1	-	-	USB1_N

1. Default configuration in bold

UM2648 - Rev 1 page 30/61



Figure 17. Dual USB TYPE A connector MB1262/CN18 and CN20

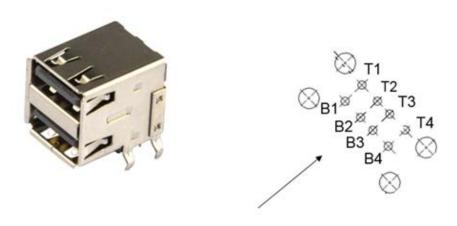


Table 31. USB Host connector pinout MB1262/CN18

Pin CN18	Pin name	Function
T1	Т1	VBUS
T2	T2	DM
Т3	ТЗ	DP
T4	T4	GND
B1	B1	VBUS
B2	B2	DM
В3	В3	DP
B4	B4	GND

Table 32. USB Host connector pinout MB1262/CN20

Pin CN20	Pin name	Function
T1	Т1	VBUS
T2	T2	DM
Т3	ТЗ	DP
T4	T4	GND
B1	B1	VBUS
B2	B2	DM
В3	В3	DP
B4	B4	GND

# 6.21 RS-232 port

The STM32MP157F-EV1 board offers one RS-232 communication port. The RS-232 communication port uses the DB9 male connector MB1262/CN12.

UM2648 - Rev 1 page 31/61



#### 6.21.1 RS-232 interface

The RS-232 transceiver MB1262/U12 supply is 3.3 V. The RS-232 interface is connected to the STM32MP157FAA1 UART4 that is shared exclusively with the USB Micro-B ST-LINK/V2-1 VCP as described in Table 33.

Table 33. HW configuration for the RS-232 interface

Jumpers	I/O	Setting	Configuration <sup>(1)</sup>
MB1263/JP4	UART4_TX	JP4[1-2]	Connected to RS-232 CN12
		JP4[2-3]	Connected to ST-LINK/V2-1 VCP RX
MB1263/JP5	UART4_RX	JP5[1-2]	Connected to RS-232 CN12
		JP5[2-3]	Connected to ST-LINK/V2-1 VCP TX

1. Default configuration in bold

Figure 18. HW configuration for the RS-232 interface



Figure 19. RS-232 connector pinout MB1262/CN12

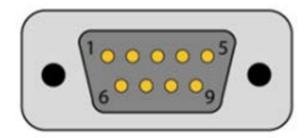


Table 34 details the RS-232 connector pinout MB1262/CN12

Table 34. RS-232 connector pinout MB1262/CN12

Board function	Pin	Pin	Board function
NC	1	6	DSR
RXD	2	7	NC
TXD	3	8	CTS

UM2648 - Rev 1 page 32/61



Board function	Pin	Pin	Board function
NC	4	9	NC
GND	5	-	

#### 6.21.2 I/O restriction to other features

The RS-232 must not be operated simultaneously with the ST-LINK VCP.

## **6.22 CAN FD**

The STM32MP157F-EV1 board supports one CAN FD compliant with ISO-11898-1 version 2.0 part A, B. The MB1262/CN15 DB9 male connector is available as CAN FD interface.

## 6.22.1 Operating voltage

A 5 V/3.3 V I/O compliant high-speed CAN FD transceiver is fitted between the MB1262/CN15 connector and the CAN controller port of the STM32MP157FAA1.

#### 6.22.2 CAN FD interface

Table 35 describes the I/O for the CAN interface.

Table 35. I/O configuration for the CAN interface

I/O	Signal
PG3	CAN_STBY
PH13	CAN_TX
PI9	CAN_RX

Figure 20 shows the CAN FD connector pinout MB1262/CN15.

Figure 20. CAN FD connector pinout CN15

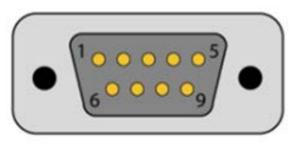


Table 36 describes the CAN FD interface and connector pinout CN15.

Table 36. CAN FD interface and connector pinout CN15

CAN transceiver	Board function	Pin	Pin	Board function	CAN transceiver
-	NC	1	6	GND	-
CANL	CANL	2	7	CANH	CANH
GND	GND	3	8	NC	-
-	NC	4	9	NC	-
-	GND	5	-		

UM2648 - Rev 1 page 33/61



# 6.23 Smartcard

The STM32MP157F-EV1 board supports one smartcard interface. The MB1262/CN23 smartcard connector is used as card reader.

#### **6.23.1** Smartcard interface

A 3V3 smartcard interface MB1262/U5 is used between the card reader connector MB1262/CN23 and the smartcard controller port of STM32MP157FAA1.

The smartcard interface is connected for some I/O to the STM32MP157FAA1 and for other IO to the MFX I/O expander.

Table 37. HW configuration for the smartcard interface

I/O	Configuration		
PZ7	PZ7 is connected to smartcard interface as SMARTCARD_IO		
PZ6	PZ6 is connected to smartcard interface as SMARTCARD_CLK		
MFX_IO6	MFX_IO6 used as SMARTCARD_3/5V		
MFX_IO7	MFX_IO7 used as SMARTCARD_OFF		
MFX_IO8	MFX_IO8 used as SMARTCARD_RST		
MFX_IO9	MFX_IO9 used as SMARTCARD_CMDVCC		

Figure 21. Smartcard connector pinout MB1262/CN23

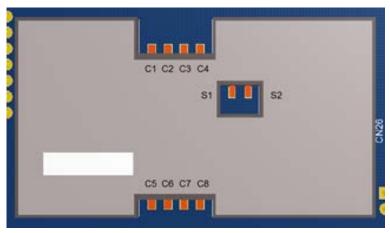


Table 38 describes the smartcard interface MB1262/U5 and connector pinout MB1262/CN23.

Table 38. Smartcard interface MB1262/U5 and connector pinout MB1262/CN23

Pin	Board function	U5 smartcard interface pin
C1	VCC: Card supply	U5-17
C2	RST: Card Reset	U5-16
C3	CLK: Card CLK	U5-15
C4	NC	U5-13
C5	GND: CARD GND	U5-14
C6	SWIO	-

UM2648 - Rev 1 page 34/61



Pin	Board function	U5 smartcard interface pin
C7	I/O CARD DATA	U5-11
C8	NC	U5-12
S1	GND: CAR GND	GND
S2	DETECT: CARD-Detect (LOW)	U5-9

#### 6.24 ADC/DAC

The STM32MP157F-EV1 provides some on-board analog-to-digital converters ADC and digital-to-analog converters DAC:

- 2x ADC/DAC
- 2x Fast ADC
- 1x Slow ADC

#### 6.24.1 ADC/DAC I/O interface

The STM32MP157FAA1 port PA4 may be configured to operate either as ADC input or as DAC output. PA4 is routed to two-way headers MB1263/JP11, to fetch signals to or from MB1263/JP11, or grounded by fitting a jumper into MB1263/JP11. Same situation for PA5 and its related MB1263/JP10 header.

Parameters of the ADC/DAC low-pass filters formed with MB1263/R24, C31, R19 for PA4 and MB1263/R25, C32, R20 for PA5 may be modified by replacing these components according to application requirements (Default configuration is: R24/R19/R25/R20 = 0  $\Omega$ , C31/C32 not fitted).

#### 6.24.2 Fast ADC

ANA0 may be configured as a fast ADC channel routed to MB1263/JP8. MB1263/SB6, closed by default, should be opened.

ANA1 may be configured as a fast ADC channel routed to MB1263/JP9. MB1263/SB7, closed by default, must be opened.

Parameters of the low-pass filters formed with MB1263/R22, C29, and R17 for ANA0 and MB1263/R23, C30 and R18 for ANA1 may be modified by replacing these components according to application requirements (Default configuration is: R22/R17/R23/R18 = 0  $\Omega$ , C29/C30 not fitted).

#### 6.24.3 Slow ADC

The port PF12 may be configured as slow ADC channel, routed to MB1263/JP7. MB1263/SB5, closed by default, must be opened.

Parameters of the low-pass filters formed with MB1263/R21, C28, and R16 may be modified to application requirements (Default configuration is R21/R16=0  $\Omega$ , C28 not fitted).

The VREF+ terminal of STM32MP157FAA1 is used as reference voltage for both ADC and DAC. By default, it is connected on board to VDDA through MB1263/R96, which may be removed to apply directly an external voltage to VREF+ for specific purposes.

Figure 22 shows ADC/DAC connectors MB1263/JP7, JP8, JP9, JP10, and JP11.

Figure 22. ADC/DAC connectors MB1263/JP7, JP8, JP9, JP10, and JP11



UM2648 - Rev 1 page 35/61



Table 39. ADC/DAC connectors JP7/JP8/JP9/JP10/JP11 pinout

Signal name	Pin	Pin	Signal name
ADC/DAC	1	2	GND

## 6.24.4 Limitations

Due to the sharing of some I/Os of STM32MP157FAA1 by multiple peripherals, the following limitations apply in using the PMOD button features:

The fast ADC ANA0/ANA1 and slow ADC PF12 may not be operated simultaneously with the motor control function.

# 6.25 I2C\_EXT connector

I2C\_EXT connector MB1262/CN13 may be connected to I<sup>2</sup>C bus daughterboard. CN13 connector pin 5 is connected to 3V3, meaning that the external module must be compliant with 3V3.

MFX\_GPIO0 of MFX MCU provides EXT\_RESET.

## 6.25.1 I2C\_EXT I/O interface

Table 40. HW configuration for the I2C\_EXT interface

I/O	Bridge	Setting <sup>(1)</sup>	Comment
		ON	PA11, used as I2C5_SCL, is connected to EXT_SCL
PA11	MB1262/ SB51	OFF	PA11 is not connected to EXT_SCL PA11 may be connected to the GPIO expansion connector through MB1262/SB52
		ON	PA12, used as I2C5_SDA, is connected to EXT_SDA
PA12	MB1262/ SB54 OFF		PA12 is not connected to EXT_SDA PA12 may be connected to the GPIO expansion connector through MB1262/SB55
MFX_GPIO0	-	-	Connected to EXT_RESET

<sup>1.</sup> Default configuration is shown in bold

Figure 23 shows the I2C\_EXT connector pinout MB1262/CN13.

Figure 23. I2C\_EXT connector pinout MB1262/CN13

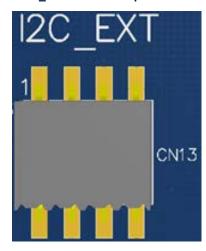


Table 41 describes the I2C\_EXT connector pinout MB1262/CN13.

UM2648 - Rev 1 page 36/61



Table 41. I2C\_EXT connector pinout MB1262/CN13

Signal name	Pin	Pin	Signal name
EXT_SDA	1	2	NC
EXT_SCL	3	4	EXT_RST
3V3	5	6	NC
GND	7	8	NC

## 6.26 MFX MCU

The MFX, Multi-Function eXpander MCU, is used as a GPIO expander, in position MB1262/U20.

### 6.26.1 MFX I/O expander

Supplied by 3V3.

The communication interface between MFX and STM32MP157FAA1 is an I<sup>2</sup>C bus and IRQOUT pin.

The  $I^2C$  is I2C2 that is shared with all the peripherals: audio codec, DSI LCD, RGB LTDC, camera, and USB Hub. The MFX  $I^2C$  address is 0x42h.

Table 42. HW configuration for the MFX interface

I/O	SB	Setting Configuration <sup>(1)</sup>	
PI8	R127	ON MFX_IRQ_OUT is connected to PI8	
PH5	R124	4 ON PH5 is used as I2C2_SDA	
PH4	R125	ON	PH4 is used as I2C2_SCL
PD10	-	-	SUB_NRST

<sup>1.</sup> Default configuration in bold

Table 43. I/O signals driven by the MFX

Pin number	Pin name	Signal name	Function
18	GPIO0	JOY_CENTER	MB1262/B1 joystick selection
19	GPIO1	JOY_DOWN	MB1262/B1 joystick down direction
20	GPIO2	JOY_LEFT	MB1262/B1 joystick left direction
39	GPIO3	JOY_RIGHT	MB1262/B1 joystick right direction
40	GPIO4	JOY_UP	MB1262/B1 joystick up direction
15	GPIO5	Audio_INT	MB1262/U8 audio codec interrupt
16	GPIO6	SMARTCARD_3V/5V	MB1262/U5 smartcard 3 V 5 V selection
17	GPIO7	SMARTCARD_OFF	MB1262/U5 smartcard OFF
29	GPIO8	SMARTCARD_RST	MB1262/U5 smartcard RESET
30	GPIO9	SMARTCARD_CMDVCC	MB1262/U5 smartcard VCC command
31	GPIO10	MIC_MEMS_LED	MB1262/CN8 pin12
32	GPIO11	-	-
33	GPIO12	CAMERA_PLUG	Camera plug detection
26	GPIO13	-	-
27	GPIO14	LCD_INT	DSI or LTDC interrupt
28	GPIO15	-	-

UM2648 - Rev 1 page 37/61



### 6.27 Motor control

The STM32MP157F-EV1 board supports both asynchronous and synchronous 3-phase brushless motor control via the 34-pin connector MB1262/CN22, which provides all required control and feedback signals, to and from the motor power-driving board.

Available signals on this connector include emergency stop, motor speed, 3-phase motor current, bus voltage, heatsink temperature coming from the motor driving board and 6 channels of PWM control signal (MC-xH/L) going to the motor driving circuit.

#### **6.27.1** Motor control I/O interface

Because of I/O consuming limitation, the motor control I/O interface is not enabled by default. As described below, some board modifications are needed to connect the motor control interface.

Table 44 describes the assignment of the MB1262/CN22 motor control interface and the I/O function associated from the STM32MP157FAA1.

Table 44. Motor control terminal and I/O function assignment

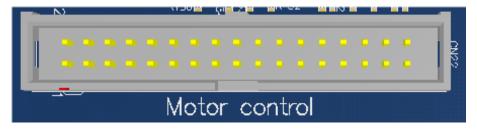
Motor co	ntrol connector CN22		STM32MP157FAA1 microprocessor					
Terminal	Terminal name	Port name	Function	Alternate function	Board configurations to enable motor control			
1	Emergency Stop	PA6	TIM8_BKIN	DCMI_PIXCLK	Close MB1262/SB22			
2	GND	-	-	-	-			
3	MC_UH	PI5	TIM8_CH1	SAI_2_SCK_A	Close MB1262/SB67 Open MB1262/SB9 and SB66			
4	GND	-	-	-	-			
5	MC_UL	PH13	TIM8_CH1N	CAN_1_TX	Close MB1262/SB76			
6	GND	-	-	-	-			
7	MC_VH	PI6	TIM8_CH2	SAI_2_SD_A	Close MB1262/SB75 Open MB1262/SB10 and SB73			
8	GND	-	-	-	-			
9	MC_VL	PH14	TIM8_CH2N	DCMI_D4	Close MB1262/SB21			
10	GND	-	-	-	-			
11	MC_WH	PI7	TIM8_CH3	SAI_2_FS_A	Close MB1262/SB65 Open MB1262/SB11 and SB63			
12	GND	-	-	-	-			
13	MC_WL	PH15	TIM8_CH3N	DCMI_D11	Close MB1262/SB33			
14	Bus Voltage	PA3	ADC_1_IN15	GPIO6_TIM2_CH4	Close MB1262/SB14			
15	PhaseA current	PF12	ADC_1_IN6	-	Close MB1262/SB20			
16	GND	-	-	-	-			
17	PhaseB current	ANA0	ADC_1_IN0	ADC_2_IN0	Close MB1262/SB12			
18	GND	-	-	-	-			
19	PhaseC current	ANA1	ADC_2_IN1	-	Close MB1262/SB13			
20	GND	-	-	-	-			
21	NTC Bypass	PF3	GPIO	GPI07	Close MB1262/SB19			
22	GND	-	-	-	-			
23	Dissipative Brake	PH6	TIM12_CH1	GPIO12_TIM12_CH	Close MB1262/SB29			

UM2648 - Rev 1 page 38/61



Motor co	ntrol connector CN22		STM32MP157FAA1 microprocessor				
Terminal	Terminal name	Port name	Function	Alternate function	Board configurations to enable motor control		
24	GND	-	-	-	-		
25	5V	-	-	-	-		
26	Heatsink Temp.	PF11	ADC_1_IN2	SAI_2_SD_B	Close MB1262/SB70 Open MB1262/SB8 and SB69		
27	PFC Sync	PE0	TIM4_ETR	SAI_2_MCLK_A	Close MB1262/SB53 Open MB1262/SB7		
28	3V3	-	-	-	-		
29	PFC PWM	PB8	TIM4_CH3	DCMI_D6	Close MB1262/SB24		
30	GND	-	-	-	-		
31	Encoder A	PH10	TIM5_CH1	DCMI_D1	Close MB1262/SB28		
32	GND	-	-	-	-		
33	Encoder B	PH11	TIM5_CH2	DCMI_D2	Close MB1262/SB30		
34	Encoder Index	PH12	TIM5_CH3	DCMI_D3	Close MB1262/SB26		

Figure 24. Motor control connector MB1262/CN22



#### 6.27.2 Limitations

Due to the sharing of some I/Os of STM32MP157FAA1 by multiple peripherals, the following limitations apply in using the motor control features:

The motor control may not be operated simultaneously with the camera, audio codec, CAN and GPIO expansion (GPIO6, 7 and 12).

# 6.28 GPIO 40-pin expansion connector

A 2×20-pin, 2.54 mm, GPIO connector is implemented on MB1262/CN21.

28 pins are GPIOs, 8 are GND, 2× 5V DC and 2× 3V3 DC are provided on this connector.

This GPIO 40-pin expansion connector has a Raspberry Pi® shield support capability.

Figure 25. MB1262/CN21 connector



Please note the pin1 position that is on the bottom right on MB1262/CN21.

Table 45 describes the MB12622/CN21 connector pinout.

UM2648 - Rev 1 page 39/61



Table 45. MB1262/CN21 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
-	3V3	1	2	5V	-
PA12	I2C5_SDA	3	4	5V	-
PA11	I2C5_SCL	5	6	GND	-
PI11	MCO1	7	8	USART3_TX	PB10
-	GND	9	10	USART3_RX	PB12
PG8	USART3_RTS	11	12	SAI2_SCKA	PI5
PD7	SDMMC3_D3	13	14	GND	GND
PG15	SDMMC3_CK	15	16	SDMMC3_CMD	PF1
-	3V3	17	18	SDMMC3_D0	PF0
PZ2	SPI1_MOSI	19	20	GND	GND
PZ1	SPI1_MISO	21	22	SDMMC3_D1	PF4
PZ0	SPI1_SCK	23	24	SPI1_NSS	PZ3
-	GND	25	26	GPIO	-
PH5	I2C2_SDA	27	28	I2C2_SCL	PH4
PG2	MCO2	29	30	GND	-
PA3	TIM2_CH4	31	32	TIM12_CH1	PH6
PI2	TIM8_CH4	33	34	GND	-
PI7	SAI2_FSA	35	36	USART3_CTS	PI10
PF5	SDMMC3_D2	37	38	SAI2_SDA	PI6
-	GND	39	40	SAI2_SDB	PF11

SAI2 on the GPIO connector supports PCM signals. SAI2 is shared between the audio codec and this GPIO expansion connector. By default, SAI2 is connected to the audio codec. I2C5 is connected by default to the I2C EXT connector.

The following HW board modifications are needed to enable SAI2 and I2C5 on the GPIO expansion connector, as described in Table 46.

Table 46. HW configurations to enable SAI2 on the GPIO connector

STM32 pin	Board function	Board modifications to enable SAI2 on the GPIO connector
PI5	SAI2_SCKA	Open MB1262/SB9 and SB67. Close MB1262/SB66
PI7	SAI2_FSA	Open MB1262/SB11 and SB65. Close MB1262/SB63
PI6	SAI2_SDA	Open MB1262/SB10 and SB75. Close MB1262/SB73
PF11	SAI2_SDB	Open MB1262/SB8 and SB70. Close MB1262/SB69
PA12	I2C5_SDA	Open MB1262/SB54. Close MB1262/SB55
PA11	I2C5_SCL	Open MB1262/SB51. Close MB1262/SB52

### 6.29 RGB LTDC connector

A 2×30-pin RGB LTDC connector is implemented on MB1262/CN11.

UM2648 - Rev 1 page 40/61



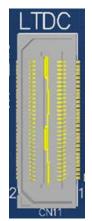


Figure 26. MB1262/CN11 connector

A 24-bit RGB interface, LCD control signals (INT, Backlight BL\_CTRL, LCD\_RESET, I2C), HDMI\_CEC and SPDIF\_TX are available as described in the connector pinout Section 6.29.

Table 47. MB1262/CN21 connector pinout

I/O	Board function	Pin	Pin	Board function	I/O
PK7	LTDC_DE	1	2	LTDC_R7	PJ6
-	-	3	4	LCD_INT	MFX_IO14
-	-	5	6	LTDC_B7	PK6
PJ4	LTDC_R5	7	8	-	-
PI12	LTDC_HSYNC	9	10	LTDC_VSYNC	PI13
-	-	11	12	-	-
MFX_O1	HDMI_PD	13	14	LTDC_R0	PI15
-	-	15	16	-	-
PJ0	LTDC_R1	17	18	LTDC_R2	PJ1
-	-	19	20	-	-
PJ2	LTDC_R3	21	22	LTDC_R4	PJ3
PK0	LTDC_G5	23	24	LTDC_G6	PK1
PJ4	LTDC_R5	25	26	LTDC_R6	PJ5
PK3	LTDC_B4	27	28	LTDC_B5	PK4
PJ6	LTDC_R7	29	30	LTDC_G0	PJ7
PK5	LTDC_B6	31	32	-	-
PJ8	LTDC_G1	33	34	LTDC_G2	PJ9
-	-	35	36	-	-
PJ10	LTDC_G3	37	38	LTDC_G4	PJ11
PJ12	LTDC_B0	39	40	LTDC_B1	PJ13
PJ14	LTDC_B2	41	42	LTDC_B3	PJ15
-	-	43	44	-	-
-	-	45	46	LCD_RESET (SUB_NRST)	PD10
-	3V3	47	48	5V	-
PK2	LTDC_G7	49	50	GND	-

UM2648 - Rev 1 page 41/61



I/O	Board function	Pin	Pin	Board function	I/O
PA15	HDMI_CEC	51	52	-	-
PH4	I2C2_SCL	53	54	SPDIF_TX	PB5
PH5	I2C2_SDA	55	56	GND	-
-	LCD_BL_CTRL	57	58	LTDC_CLK	PI14
-	-	59	60	GND	-

# 6.29.1 Limitations

LCD\_INT and LCD\_BL\_CTRL are shared exclusively with the DSI.

UM2648 - Rev 1 page 42/61



# 7 STM32MP157F-EV1 Evaluation board information

### 7.1 Identification

The STM32MP157F-EV1 product, composed of several boards, is identified using the product sticker whose identification is:

- Product name
- Sales type
- FCC ID

Each board is further identified with its own dedicated board sticker. The board sticker identification is the following:

- MBxxxx-...-yzz with xxxx being the board reference, y the PCB revision, and zz the bom revision
- 1yywwxxxxx with yy being the year of assembly, ww the week of assembly, and xxxxx the board serial number

The product and board stickers are detailed in Table 48.

Table 48. Product and board stickers

Sticker	Information				
	STM32MP157F-EV1				
Product	VA32MP157F1\$AU1				
	FCC ID: YCP-MB1263-001				
MB1263 board	MB1263-MP157FAA-C03				
IND 1203 DOUTU	1yywwxxxxx				
MAC address	00:80:E1:XX:XX				
MB1262 board	MB1262-C01				
IND 1202 DOUTU	1yywwxxxxx				
MD1270 board	MB1379-A02				
MB1379 board	1yywwxxxxx				
MB1230 board	MB1230-C01				
IVID 1230 DOMIU	1yywwxxxxx				

### 7.2 Product revision history

STM32MP157F-EV1 VA32MP157F1\$AU1 is the initial released version.

### 7.3 Known limitations

None.

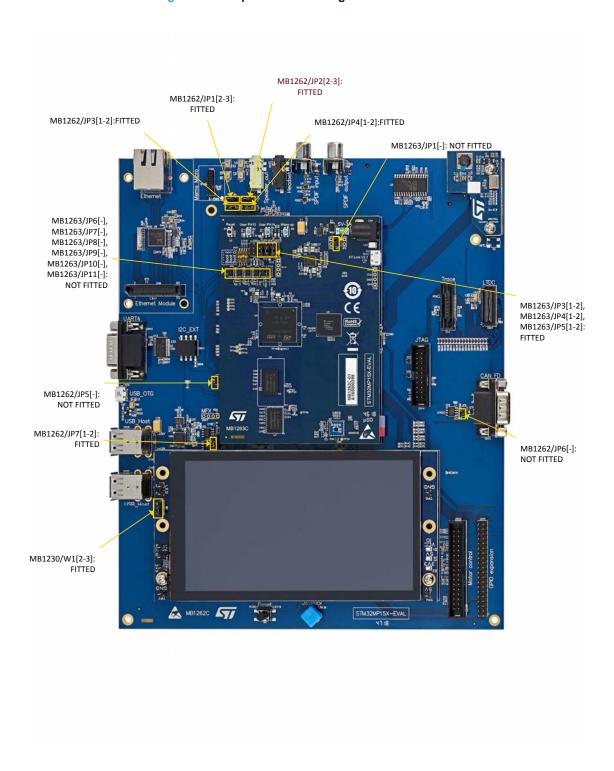
UM2648 - Rev 1 page 43/61



# **Appendix A STM32MP157F-EV1 jumper summary**

Figure 27 summarizes the jumper default setting of the STM32MP157F-EV1.

Figure 27. Jumper default setting of the STM32MP157x-EV1



UM2648 - Rev 1 page 44/61



# Appendix B STM32MP157F-EV1 I/O assignment

Table 49. STM32MP157F-EV1 I/O assignment

LFBGA448 ball	I/O port	Main function	Motor control connector
AA3	PA0	WAKE_UP	-
V4	PA1	ETH_RX_CLK	-
AB2	PA2	ETH_MDIO	-
T4	PA3	TIM2_CH4	Bus voltage
V6	PA4	ADC1_IN18_DACOUT1	-
U5	PA5	ADC1_IN19_DACOUT2	-
W9	PA6	DCMI_PIXCLK	Emergency Stop
Y9	PA7	ETH_RX_DV	-
B13	PA8	SDMMC2_D4	-
A11	PA9	SDMMC2_D5	-
Y17	PA10	OTG_ID	-
Y16	PA11	12C5_SCL	-
W16	PA12	I2C5_SDA	-
W3	PA13	PA13 GPIO	-
R3	PA14	PA14 GPIO	-
E11	PA15	HDMI_CEC	-
AB5	PB0	ETH_RXD2	-
AA5	PB1	ETH_RXD3	-
V13	PB2	UART4_RX	-
A12	PB3	SDMMC2_D2	-
C13	PB4	SDMMC2_D3	-
AA8	PB5	SPDIF_TX	-
W13	PB6	QSPI_BK1_NCS	-
F11	PB7	DCMI_VSYNC	-
AB8	PB8	DCMI_D6	PFC PWM
F12	PB9	SDMMC1_CDIR	-
V9	PB10	USART3_TX	-
Y5	PB11	ETH_TX_EN	-
AA7	PB12	USART3_RX	-
V10	PB13	DFSDM_CKOUT	-
A13	PB14	SDMMC2_D0	-
B12	PB15	SDMMC2_D1	-
U10	PC0	QSPI_BK2_NCS	-
AB3	PC1	ETH_MDC	-
Y1	PC2	ETH_TXD2	-
U3	PC3	DFSDM_DATA1	-
AB6	PC4	ETH_RXD0	-

UM2648 - Rev 1 page 45/61



LFBGA448 ball	I/O port	Main function	Motor control connector
AA6	PC5	ETH_RXD1	-
E13	PC6	DSI_TE	-
D13	PC7	SDMMC1_D123DIR	-
E14	PC8	SDMMC1_D0	-
D14	PC9	SDMMC1_D1	-
F14	PC10	SDMMC1_D2	-
D15	PC11	SDMMC1_D3	-
E12	PC12	SDMMC1_CK	-
N2	PC13	PMIC_WAKEUP	-
P1	PC14	LSE_IN	-
P2	PC15	LSE_OUT	-
C10	PD0	NAND_D2	-
B10	PD1	NAND_D3	-
D12	PD2	SDMMC1_CMD	-
B11	PD3	SDMMC2_D123DIR	-
C9	PD4	NAND_NOE	-
A9	PD5	NAND_NWE	-
L3	PD6	NAND_NWAIT	-
F10	PD7	SDMMC3_D3	-
M1	PD8	NAND_D13	-
M2	PD9	NAND_D14	-
A8	PD10	NAND_D15	-
AB9	PD11	NAND_CLE	-
W12	PD12	NAND_ALE	-
V14	PD13	LCD_BL_CTRL	-
M3	PD14	NAND_D0	-
L1	PD15	NAND_D1	-
C5	PE0	SAI2_MCLKA	PFC Sync
D7	PE1	-	-
Y2	PE2	ETH_TXD3	-
A10	PE3	SDMMC2_CK	-
F15	PE4	SDMMC1_CKIN	-
C12	PE5	SDMMC2_D6	-
E9	PE6	DCMI_D7	-
W10	PE7	NAND_D4	-
Y12	PE8	NAND_D5	-
W11	PE9	NAND_D6	-
W14	PE10	NAND_D7	-
D5	PE11	uSD_LS_EN	-
E4	PE12	SAI2_SCKB	-

UM2648 - Rev 1 page 46/61



LFBGA448 ball	I/O port	Main function	Motor control connector
A4	PE13	SAI2_FSB	-
B4	PE14	SAI2_MCLKB	-
C4	PE15	-	-
E10	PF0	SDMMC3_D0	-
B9	PF1	SDMMC3_CMD	-
F13	PF2	SDMMC1_D0DIR	-
V3	PF3	GPIO	NTC Bypass
F9	PF4	SDMMC3_D1	-
D9	PF5	SDMMC3_D2	-
AA11	PF6	QSPI_BK1_IO3	-
AA10	PF7	QSPI_BK1_IO2	-
AB10	PF8	QSPI_BK1_IO0	-
AB11	PF9	QSPI_BK1_IO1	-
V12	PF10	QSPI_CLK	-
W8	PF11	SAI_2_SDB	Heatsink Temp.
V8	PF12	SLOW ADC	PhaseA current
W7	PF13	DFSDM_DATA3	-
V7	PF14	uSD_LDO_SEL	-
W6	PF15	DSI_RESET	-
W5	PG0	ETH_MDINT	-
Y4	PG1	uSD_DETECT	-
W4	PG2	MCO2	-
U4	PG3	CAN_STBY	-
AB4	PG4	ETH_GTX_CLK	-
U8	PG5	ETH_CLK125	-
D11	PG6	SDMMC2_CMD	-
Y11	PG7	QSPI_BK2_IO3	-
Y8	PG8	USART3_RTS	-
W15	PG9	NAND_NCE	-
AA9	PG10	QSPI_BK2_IO2	-
U11	PG11	UART4_TX	-
J4	PG12	SPDIF_RX	-
AA1	PG13	ETH_TXD0	-
AA2	PG14	ETH_TXD1	-
D10	PG15	SDMMC3_CK	-
T1	PH0	HSE_IN	-
T2	PH1	HSE_OUT	-
AB7	PH2	QSPI_BK2_IO0	-
Y6	PH3	QSPI_BK2_IO1	-
A3	PH4	I2C2_SCL	-

UM2648 - Rev 1 page 47/61



LFBGA448 ball	I/O port	Main function	Motor control connector
A2	PH5	I2C2_SDA	-
V11	PH6	TIM12_CH1	Dissipative Brake
W2	PH7	DCMI_D9	-
D6	PH8	DCMI_HSYNC	-
E6	PH9	DCMI_D0	-
B1	PH10	DCMI_D1	Encoder A
B3	PH11	DCMI_D2	Encoder B
F5	PH12	DCMI_D3	Encoder Index
D3	PH13	CAN_TX	MC_UL
C2	PH14	DCMI_D4	MC_VL
C1	PH15	DCMI_D11	MC_WL
D1	PI0	-	-
E2	PI1	DCMI_D8	-
E1	PI2	TIM8_CH4	-
E3	PI3	DCMI_D10	-
J6	PI4	DCMI_D5	-
F2	PI5	SAI2_SCKA	MC_UH
G5	PI6	SAI2_SDA	MC_VH
F1	PI7	SAI2_FSA	MC_WH
N1	PI8	MFX_IRQ_OUT	-
J5	PI9	CAN_RX	-
W1	PI10	USART3_CTS	-
Т3	PI11	MCO1	-
H2	PI12	LTDC_HSYNC	TRACE_D0
H1	PI13	LTDC_VSYNC	TRACE_D1
D2	PI14	LTDC_CLK	TRACE_CLK
F3	PI15	LTDC_R0	-
J2	PJ0	LTDC_R1	TRACE_D8
L6	PJ1	LTDC_R2	TRACE_D9
K4	PJ2	LTDC_R3	TRACE_D10
J1	PJ3	LTDC_R4	TRACE_D11
K2	PJ4	LTDC_R5	TRACE_D12
K1	PJ5	LTDC_R6	TRACE_D2
L5	PJ6	LTDC_R7	TRACE_D3
L4	PJ7	LTDC_G0	TRACE_D13
H6	PJ8	LTDC_G1	TRACE_D14
L2	PJ9	LTDC_G2	TRACE_D15
J3	PJ10	LTDC_G3	-
K6	PJ11	LTDC_G4	-
B8	PJ12	LTDC_B0	-

UM2648 - Rev 1 page 48/61



LFBGA448 ball	I/O port	Main function	Motor control connector
A7	PJ13	LTDC_B1	-
B7	PJ14	LTDC_B2	-
C7	PJ15	LTDC_B3	-
D8	PK0	LTDC_G5	-
E7	PK1	LTDC_G6	TRACE_D4
E8	PK2	LTDC_G7	TRACE_D5
B6	PK3	LTDC_B4	-
A6	PK4	LTDC_B5	-
C6	PK5	LTDC_B6	TRACE_D6
A5	PK6	LTDC_B7	TRACE_D7
B5	PK7	LTDC_DE	-
G2	PZ0	SPI1_SCK	-
H5	PZ1	SPI1_MISO	-
K5	PZ2	SPI1_MOSI	-
F4	PZ3	SPI1_NSS	-
G1	PZ4	I2C4_SCL	-
H4	PZ5	I2C4_SDA	-
G3	PZ6	SMARTCARD_CLK	-
H3	PZ7	SMARTCARD_IO	-

UM2648 - Rev 1 page 49/61



# Appendix C Federal Communications Commission (FCC) and ISED Canada Compliance Statements

### C.1 FCC Compliance Statement

#### FCC ID

FCC ID: YCP-MB1263-001.

#### Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

#### Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

#### Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

#### C.2 ISED Compliance Statement

Industry Canada ICES-003 Compliance Label: *CAN ICES-3 (A) / NMB-3 (A)*. Étiquette de conformité à la NMB-003 d'Industrie Canada: *CAN ICES-3 (A) / NMB-3 (A)*.

UM2648 - Rev 1 page 50/61



# **Appendix D CE conformity**

# D.1 Warning

### EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

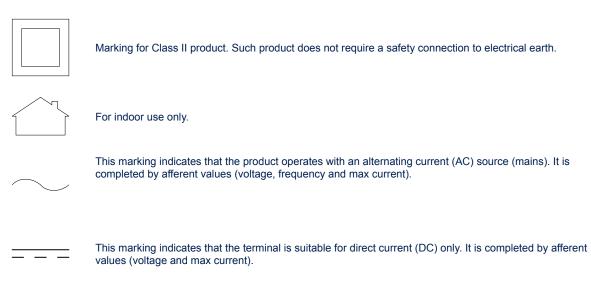
UM2648 - Rev 1 page 51/61



# **Appendix E Safety instructions**

# E.1 Safety instructions

- The STM32MP157x-EV1 Evaluation board is designed to be powered from the 5 V DC power supply unit provided in the package. The power supply acting as a disconnection device must remain easily accessible in case of issue.
- Marking observed on the power supply unit:





The associated symbol means that WEEE and waste batteries must not be thrown away but collected separately and recycled.

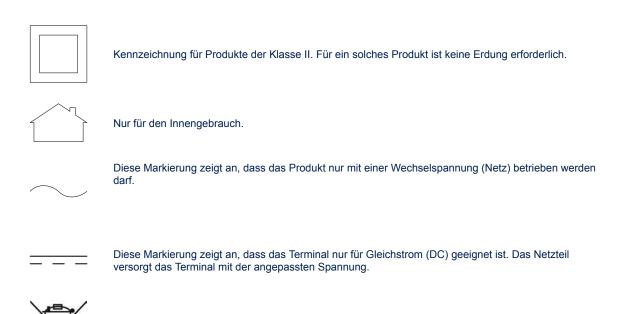
- Do not expose it to heat from any source.
- Do not expose it to water, moisture or place on a conductive surface while in operation.

UM2648 - Rev 1 page 52/61



### E.2 Sicherheitshinweise

- Das Evaluierungsboard STM32MP157x-EV1 ist ausgelegt für den Betrieb mit dem im Lieferumfang enthaltenen 5V DC Netzteil. Das Netzteil muss frei zugänglich sein damit es jederzeit im Fall einer Gefahr oder einer Störung vom Netz getrennt werden kann.
- Kennzeichnung am Netzteil beachtet:



- Setzen Sie es keiner Wärmequelle aus.
- Setzen Sie es während des Betriebs weder Wasser noch Feuchtigkeit aus und legen Sie es nicht auf eine leitfähige Oberfläche.

getrennt gesammelt und recycelt werden müssen.

Das zugehörige Symbol bedeutet, dass Elektro- und Elektronik-Altgeräte nicht weggeworfen, sondern

UM2648 - Rev 1 page 53/61



# **Revision history**

Table 50. Document revision history

Date	Version	Changes
9-Jun-2020	1	Initial release.

UM2648 - Rev 1 page 54/61



# **Contents**

1	Feat	ures		2
2	Orde	ering inf	formation	3
	2.1	Produc	ct marking	3
	2.2	Codific	cation	3
3	Deve	elopmer	nt environment	4
	3.1	System	n requirements	4
	3.2	Develo	opment toolchains	4
	3.3	Demor	nstration software	4
4	Conv	vention	s	5
5	Deliv	ery rec	commendations	6
6	Hard	lware la	yout and configuration	7
	6.1	Power	supply management	11
		6.1.1	5 V power supply	11
		6.1.2	Platform power tree	11
		6.1.3	STPMIC1	12
	6.2	Clocks	i	13
		6.2.1	LSE clock	13
		6.2.2	HSE clock	13
	6.3	Reset	sources	13
	6.4	User buttons and LEDs1		
	6.5	Physical input devices: buttons		
	6.6	Boot o	ptions	14
	6.7	6.7 Embedded ST-LINK/V2-1		15
		6.7.1	Drivers	16
		6.7.2	ST-LINK/V2-1 firmware upgrade	17
	6.8	ETM T	RACE Micto-38 connector	17
	6.9	JTAG (	connector	19
	6.10	DDR3L	L	20
	6.11	eMMC	'	20



	6.11.1	eMMC I/O interface	20			
6.12	NAND F	Flash memory	20			
	6.12.1	NAND I/O interface	21			
6.13	Quad-S	PI NOR Flash memory	21			
	6.13.1	Quad-SPI I/O interface	21			
6.14	microSE	O card	22			
	6.14.1	SD card interface	22			
6.15	Audio		23			
	6.15.1	Audio codec interface	23			
	6.15.2	Digital microphones	23			
	6.15.3	Analog microphone and audio jack headphone	24			
	6.15.4	Audio speaker out	25			
	6.15.5	SPDIF input and output	25			
	6.15.6	I/O restriction to other features	26			
6.16	DSI LCI	DSI LCD				
	6.16.1	DSI LCD interface	26			
6.17	Camera		27			
	6.17.1	Camera interface	27			
6.18	1 Gbps	Ethernet	28			
	6.18.1	RGMII interface	28			
6.19	USB 01	rg hs	29			
	6.19.1	USB OTG interface	29			
6.20	USB ho	st	30			
	6.20.1	USB Host interface	30			
6.21	RS-232	RS-232 port				
	6.21.1	RS-232 interface	32			
	6.21.2	I/O restriction to other features	33			
6.22	CAN FE	D	33			
	6.22.1	Operating voltage	33			
	6.22.2	CAN FD interface	33			
6.23	Smartca	ard	34			
	6.23.1	Smartcard interface	34			



	6.24	ADC/DA	AC	35		
		6.24.1	ADC/DAC I/O interface	35		
		6.24.2	Fast ADC	35		
		6.24.3	Slow ADC	35		
		6.24.4	Limitations	36		
	6.25	I2C_EX	(T connector	36		
		6.25.1	I2C_EXT I/O interface	36		
	6.26	MFX M	CU	37		
		6.26.1	MFX I/O expander	37		
	6.27	Motor c	ontrol	38		
		6.27.1	Motor control I/O interface	38		
		6.27.2	Limitations	39		
	6.28	GPIO 4	GPIO 40-pin expansion connector			
	6.29	RGB LT	TDC connector	40		
		6.29.1	Limitations	42		
7	STM	32MP15	7F-EV1 Evaluation board information	43		
	7.1	Identific	cation	43		
	7.2	Product	t revision history	43		
	7.3	Known	limitations	43		
App	endix	A STN	M32MP157F-EV1 jumper summary	44		
App	endix	B STN	//32MP157F-EV1 I/O assignment	45		
App			eral Communications Commission (FCC) and ISED Canada Co	_		
	C.1	FCC Cc	ompliance Statement	50		
	<b>C.2</b>	ISED C	ompliance Statement	50		
App	endix	D CE	conformity	51		
	D.1	Warning	g	51		
App	endix	E Safe	ety instructions	52		
	E.1	Safety i	nstructions	52		
	<b>E.2</b>	Sicherh	eitshinweise	53		
Rev	ision h	nistory .		54		



Contents	55
List of tables	59
List of figures	60



# **List of tables**

Table 1.	List of available products	
Table 2.	Codification explanation	. 3
Table 3.	ON/OFF convention	
Table 4.	STM32MP157F-EV1 overview	
Table 5.	MB1263 daughterboard overview	10
Table 6.	MB1262 mother board overview	
Table 7.	HW configuration for the VBAT connection	. 11
Table 8.	HW configuration for the user buttons and LEDs	13
Table 9.	Physical user devices: buttons	13
Table 10.	HW configuration for the boot mode MB1263/SW1	. 14
Table 11.	ST-LINK USB Micro-B connector pinout MB1263/CN4	16
Table 12.	HW configuration for the TRACE connector MB1262/U10	. 17
Table 13.	TRACE MICTOR-38 connector pinout: MB1262/U10	19
Table 14.	MB1262/CN14 JTAG connector pinout	20
Table 15.	HW configuration for the eMMC interface	20
Table 16.	HW configuration for the NAND interface	21
Table 17.	HW configuration for the Quad-SPI interface	21
Table 18.	I/O configuration for the SDIO interface	22
Table 19.	SDCARD connector pinout MB1263/CN9	23
Table 20.	I/O configuration for the audio codec interface	23
Table 21.	HW configuration for the digital microphones	24
Table 22.	Audio jack connector pinout MB1262/CN5	24
Table 23.	Audio jack connector pinout MB1262/CN4	25
Table 24.	I/O configuration for the LCD interface	26
Table 25.	I/O configuration for the camera interface	27
Table 26.	I/O configuration for the Ethernet interface	28
Table 27.	Ethernet connector pinout MB1262/CN3	29
Table 28.	I/O configuration for the USB OTG interface	29
Table 29.	USB OTG Micro-AB connector pinout MB1262/CN16	30
Table 30.	I/O configuration for the USB Host interface	30
Table 31.	USB Host connector pinout MB1262/CN18	31
Table 32.	USB Host connector pinout MB1262/CN20	31
Table 33.	HW configuration for the RS-232 interface	32
Table 34.	RS-232 connector pinout MB1262/CN12	32
Table 35.	I/O configuration for the CAN interface	33
Table 36.	CAN FD interface and connector pinout CN15	33
Table 37.	HW configuration for the smartcard interface	34
Table 38.	Smartcard interface MB1262/U5 and connector pinout MB1262/CN23	34
Table 39.	ADC/DAC connectors JP7/JP8/JP9/JP10/JP11 pinout	36
Table 40.	HW configuration for the I2C_EXT interface	36
Table 41.	I2C_EXT connector pinout MB1262/CN13	37
Table 42.	HW configuration for the MFX interface	37
Table 43.	I/O signals driven by the MFX	37
Table 44.	Motor control terminal and I/O function assignment	38
Table 45.	MB1262/CN21 connector pinout	40
Table 46.	HW configurations to enable SAI2 on the GPIO connector	
Table 47.	MB1262/CN21 connector pinout	41
Table 48.	Product and board stickers	43
Table 49.	STM32MP157F-EV1 I/O assignment	45
Table 50	Document revision history	54

UM2648 - Rev 1



# **List of figures**

Figure 1.	\$1M32MP157F-EV1 top view	. 1
Figure 2.	STM32MP157F-EV1 bottom view	. 1
Figure 3.	STM32MP157F-EV1 hardware block diagram	. 8
Figure 4.	STM32MP157F-EV1 board overview	. 9
Figure 5.	5 V power supply connector: MB1263/CN1	11
Figure 6.	STM32MP157F-EV1platform power tree	12
Figure 7.	STM32MP157F-EV1 boot-related switch configuration	15
Figure 8.	ST-LINK USB Micro-B connector pinout MB1263/CN4	16
Figure 9.	USB composite device	17
Figure 10.	TRACE Mictor-38 connector: MB1262/U10.	19
Figure 11.	SDCARD connector pinout MB1263/CN9	22
Figure 12.	Audio jack connector MB1262/CN5	24
Figure 13.	Audio jack connector MB1262/CN4	25
Figure 14.	SPDIF input MB1262/CN1 and output MB1262/CN2 connectors	26
Figure 15.	Ethernet connector MB1262/CN3	29
Figure 16.	USB OTG Micro-AB connector MB1262/CN16	30
Figure 17.	Dual USB TYPE A connector MB1262/CN18 and CN20	31
Figure 18.	HW configuration for the RS-232 interface	32
Figure 19.	RS-232 connector pinout MB1262/CN12	32
Figure 20.	CAN FD connector pinout CN15	33
Figure 21.	Smartcard connector pinout MB1262/CN23	34
Figure 22.	ADC/DAC connectors MB1263/JP7, JP8, JP9, JP10, and JP11	35
Figure 23.	I2C_EXT connector pinout MB1262/CN13	36
Figure 24.	Motor control connector MB1262/CN22	39
Figure 25.	MB1262/CN21 connector	
Figure 26.	MB1262/CN11 connector	41
Figure 27.	Jumper default setting of the STM32MP157x-EV1	44

UM2648 - Rev 1 page 60/61



#### **IMPORTANT NOTICE - PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics - All rights reserved

UM2648 - Rev 1 page 61/61