Datasheet

LC840PA Series

Version 1.1

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	21 Sept 2021	Initial version	Raj Khatri	Henry Wagner
1.1	19 Oct 2021	Corrected FCC ID	Henry Wagner	Henry Wagner

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1 Overview and Key Features

The LC840PA module firmware (Laird Connectivity ProFLEX-like firmware) only supports 2405–2480 MHz IEEE 802.15.5-2006 radio transceiver, 250kbps operation. All references to Bluetooth Low Energy (Bluetooth LE), NFC and *smart*BASIC firmware in this LC840PA datasheet are to be ignored. The standard BL654PA module comes with *smart*BASIC firmware which supports Bluetooth Low Energy (Bluetooth LE) and NFC.

Every LC840PA module is designed to simplify OEMs enablement of Thread (IEEE 802.15.4) applications to small, portable, highly power-conscious devices. The LC840PA provides engineers with considerable design flexibility in both hardware and software programming capabilities.

Based on the world-leading Nordic Semiconductor nRF52840 chipset, the LC840PA modules provide ultra-low power consumption with outstanding wireless range via +18 dBm of transmit power and the Long Range (CODED PHY) Bluetooth 5 feature (Bluetooth LE only). New circuitry both increases TX power and decreases sleep current for impeccable power management. The LC840PA is programmable via AT commands and Laird's *smart*BASIC language (Bluetooth LE only).

*smart*BASIC is an event-driven programming language that is highly optimized for memory-constrained systems such as embedded modules. It was designed to make Bluetooth LE development quicker and simpler, vastly cutting down time to market.

Note: LC840PA hardware provides all functionality of the nRF52840 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the LC840PA.

For customers using *smart*BASIC, refer to the *smart*BASIC extensions guide (available from the BL654PA product page of the Laird website. *smart*BASIC functions and capabilities can only be realized through the use of a suitable smartBASIC application running on the module. Laird smartBASIC functionality is only available in conjunction with the Bluetooth LE stack firmware. The ProFLEX (IEEE 802.15.4) firmware does not support any smartBASIC capabilities. When referencing ProFLEX functionality, sections explaining Bluetooth LE and smartBASIC operation can be disregarded and are indicated by **grayed-out text**.

1.1 Features and Benefits

- Bluetooth v5.1 – Single mode
- NFC
- IEEE 802.15.4:2006 (Thread) radio support (ProFLEX FW)
- External or internal antennas
- Multiple programming options (for Bluetooth LE)
  - *smart*BASIC
  - AT command set
- Programmable Tx power +18 dBm to -6 dBm, -26 dBm
  - LE Coded max Tx is +14 dBm
- Bluetooth LE Rx sensitivity – -98.5 dBm (1 Mbps), - 107 dBm (125 kbps)
- IEEE 802.15.4:2006 Rx sensitivity – -103.5 dBm (250kbps)
- Ultra-low power consumption
- Tx @ +18 dBm– 102.2 mA peak (at 18 dBm, DCDC on) (See Note 1 in the *Power Consumption* section)
- Rx: 10.9 mA peak (DCDC on) (See Note 1 in the *Power Consumption* section)
- Standby Doze – 5.9 uA typical
- Deep Sleep – 2.0 uA – (See Note 4 in the *Power Consumption* section)
- UART, GPIO, ADC, PWM, FREQ output, timers, I2C, SPI, I2S, PDM, and USB interfaces
- Fast time-to-market
- FCC, ISED, AS/NZS, and Korea-certified for Bluetooth LE operation
- FCC, ISED for IEEE 802.15.4 operation
- Full Bluetooth Declaration ID
- Other regulatory certifications on request
- No external components required
- Industrial temperature range (-40° C to +85° C)
- Compact footprint

1.2 Application Areas

- Medical devices
- IoT Sensors
- Factory Automation
- HVAC Controllers
- Location awareness
- Home automation

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2 SPECIFICATION

2.1 Specification Summary

Categories/Feature	Implementation
Wireless Specification	
Bluetooth®	▪ BT 5.1 – Single mode ▪ 4x Range (CODED PHY support) – BT 5.1 ▪ 2x Speed (2M PHY support) – BT 5.1 ▪ Concurrent master, slave ▪ Diffie-Hellman based pairing (LE Secure Connections) – BT 4.2 ▪ Data Packet Length Extension – BT 4.2 ▪ Link Layer Privacy (LE Privacy 1.2) – BT 4.2 ▪ LE Dual Mode Topology – BT 4.1 ▪ LE Ping – BT 4.1
IEEE 802.15.4-2006 250kbps PHY (Laird FCC and ISED certified for HW with Laird supplied FW only, customer must implement in their FW conditions in Note 1, Note 2)	▪ 2405-2475 MHz IEEE 802.15.4-2006 radio transceiver, implementing 802.15.4-2006 compliant ▪ 250 kbps, 2450 MHz, O-QSPK PHY ▪ Channel 11-25, channel 11 2405 MHz and CH25 2475 MHz (CH26 not certified) ▪ Clear channel assessment (CCA) ▪ Energy detection (ED) scan ▪ CRC generation
Frequency	2.402 - 2.480 GHz for Bluetooth LE (CH0 to CH39) 2.405 - 2.475 GHz for IEEE 802.15.4-2006 (CH1 to CH25). **CH26 (2480 MHz) not certified and therefore customer must not operate at CH26 (2480 MHz).**
Raw Data Rates	1 Mbps Bluetooth LE (over-the-air) 2 Mbps Bluetooth LE (over-the-air) 125 kbps Bluetooth LE (over-the-air) 250 kbps IEEE 802.15.4-2006 (over-the-air)
Maximum Transmit Power Setting See Note 6 in *Module Specification Notes*.	+18 dBm conducted — 453-00087 (integrated antenna) +18 dBm conducted — 453-00088 (external antenna)
Minimum Transmit Power Setting	-26 dBm, -6 dBm, 0 dBm, 6 dBm, 14 dBm
Receive Sensitivity (≤37-byte Bluetooth LE packet)	Bluetooth LE 1 Mbps (BER=1E-3) — -98.5 dBm typical Bluetooth LE 2 Mbps — -95 dBm typical Bluetooth LE 125 kbps — -107 dBm typical IEEE 802.15.4-2006 250 kbps — -103.5 dBm typical
Link Budget (conducted)	116.5 dB @ Bluetooth LE 1 Mbps 121 dB @ Bluetooth LE 125 kbps 121.5 dB @ IEEE 802.15.4-2006 250 kbps
Maximum Received Signal Strength at <0.1% PER	-11 dBm (limited by 11dB RX LNA gain)
RF Cellular Coexistence	
RF Band Pass Filter	Assists with cellular RF co-existence

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Categories/Feature	Implementation
NFC	
NFC-A Listen mode compliant	**Based on NFC forum specification** ▪ 13.56 MHz ▪ Date rate 106 kbps ▪ NFC Type 2 and Type 4 emulation **Modes of Operation:** ▪ Disable ▪ Sense ▪ Activated **Use Cases:** ▪ Touch-to-Pair with NFC ▪ NFC enabled out of band (OOB) pairing
System Wake-On-Field function	Proximity Detection
Host Interfaces and Peripherals	
Total	46 x multifunction I/O lines
UART	▪ 2 UARTs ▪ Tx, Rx, CTS, RTS ▪ DCD, RI, DTR, DSR (See Note 3 in the Module Specification Notes) ▪ Default 115200, n, 8, 1 ▪ From 1,200 bps to 1 Mbps
USB	▪ USB 2.0 FS (Full Speed, 12 Mbps) ▪ CDC driver/virtual UART (baud rate TBD)
GPIO	Up to 46, with configurable: ▪ I/O direction ▪ O/P drive strength (standard 0.5 mA or high 3mA/5 mA), ▪ Pull-up/pull-down ▪ Input buffer disconnect
ADC	▪ Eight 8/10/12-bit channels 0.6 V internal reference ▪ Configurable 4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6 (default) pre-scaling ▪ Configurable acquisition time 3uS, 5uS, 10uS (default), 15uS, 20uS, 40uS. ▪ One-shot mode
PWM Output	PWM outputs on 16 GPIO output pins. ▪ PWM output duty cycle: 0%-100% (per frequency) ▪ PWM output frequency: Up to 500 kHz
FREQ Output	FREQ outputs on 16 GPIO output pins. ▪ FREQ output frequency: 0 MHz to 4 MHz (50% duty cycle per frequency)
I2C	Two I2C interface (up to 400 kbps) – See Note 4 in the Module Specification Notes
SPI	Four SPI Master Slave interface (up to 4 Mbps)
QSPI	▪ One 32-MHz QSPI interface. Gives XIP (execute in place) capability ▪ External serial flash IC must be fitted as per Nordic specifications
Temperature Sensor	▪ One temperature sensor ▪ Temperature range equal to the operating temperature range ▪ Resolution 0.25 degrees
RSSI Detector	▪ One RF received signal strength indicator ▪ ±2 dB accuracy (valid over -101 dBm to -31 dBm) – added 11 dB LNA gain ▪ 1 dB resolution

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Categories/Feature	Implementation
I2S	One inter-IC sound interface
PDM	One pulse density modulation interface
Optional (External to the LC840PA module)	
External 32.768 kHz crystal	For customer use, connect +/-20 ppm accuracy crystal for more accurate protocol timing. **Crystal is required for IEEE 802.15.4 operation.**
Bluetooth LE Profiles	
Services supported	▪ Central mode ▪ Peripheral mode ▪ Custom and adopted profiles
Bluetooth LE Programmability	
*smart*BASIC	▪ FW upgrade via JTAG or UART ▪ Application download via UART or via over-the-air (if SIO_02 pin is pulled high externally)
Bluetooth LE Operating Modes	
*smart*BASIC	**Self-contained Run mode** ▪ Selected by nAutoRun pin status: LOW (0V). ▪ Then runs $autorun$ (*smart*BASIC application script) if it exists. **Interactive/Development mode** ▪ HIGH (VDD). ▪ Then runs via at+run (and *file name* of *smart*BASIC application script).
IEEE 802.15.4-2006 250kbps PHY Operating Modes	
Self-Contained Run mode	▪ Dedicated ProFLEX compatible operation ▪ Host interface via serial port
Supply Voltage	
Supply (VDD or VDD_HV) options	▪ Normal voltage mode VDD 3.0- 3.6 V – Internal DCDC converter or LDO (See Note 5 in the *Module Specification Notes*) OR ▪ High voltage mode VDD_HV 3.0V-5.5V Internal DCDC converter or LDO (See Note 5 in the *Module Specification Notes*)
Power Consumption	
Active Modes Peak Current (for maximum Tx power +18 dBm) – Radio only	102.2 mA peak Tx (with DCDC)
Active Modes Peak Current (for Tx power -26 dBm) – Radio only	18.5 mA peak Tx (with DCDC)
Active Modes Average Current	Depends on many factors, see *Power Consumption*
Ultra-low Power Modes	Standby Doze (System ON Idle) 5.9 uA typical Deep Sleep (System OFF) 2.0 uA
Antenna Options	
Internal	Printed PCB monopole antenna – on-board **453-00087 variant**
External	▪ Dipole antenna (with IPEX connector) ▪ Dipole PCB antenna (with IPEX connector) ▪ Connection via IPEX MH4 – **453-00088 variant** See the Antenna Information sections for FCC, ISED, AS/NZS, and Korea

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Categories/Feature	Implementation
Physical	
Dimensions	22.0 mm x 10 mm x 2.2 mm Pad Pitch – 0.8 mm Pad Type – Two rows of pads
Weight	<1 gram
Environmental	
Operating	-40 ˚C to +85 ˚C
Storage	-40 ˚C to +85 ˚C
Miscellaneous	
Lead Free	Lead-free and RoHS compliant
Warranty	One-year warranty
Development Tools	
Development Kit	BL654PA Development kit per module SKU (455-00022 and 455-00023) and free software tools
Approvals	
Bluetooth®	Full Bluetooth SIG Declaration ID
FCC/ISED	All LC840PA types (IEEE 802.15.4-2006 250kbps operation)
KC/AS/NZS	BL654PA Bluetooth LE operation only

Module Specification Notes:

Note 1	The LC840PA module PROFLEX FW only supports IEEE 802.15.4-2006 250 kbps operation. The LC840PA module IEEE 802.15.4-2006 250 kbps certifications for FCC and ISED are for HW + Laird factory firmware only. For customer implemented firmware, certifications are for HW only. It is the customer's responsibility to follow the mandatory conditions highlighted in this Note 1 and Note 2 in the FW that the customer implements. When used in IEEE 802.15.4-2006 250 kbps mode, channel 26 (2480 MHz) is unavailable for use due to the presence of out of band emissions. All other IEEE 802.15.4-2006 250 kbps channels (11-25) may be used up to the maximum +18 dBm conducted output power provided the maximum RF TX duty cycle per frequency is not exceeded (see Note 2). As module Tx power is controlled by the nRF52840 RF drive level into the FEM, the nRF52840 Tx RF drive level must be limited to a maximum drive of -4 dBm for IEEE 802.15.4-2006 250 kbps channels 11-25. Exceeding this drive level results in damage to the LC840PA and cause the LC840PA to fail regulatory Tx power certifications.
Note 2	The LC840PA module IEEE 802.15.4-2006 250 kbps certifications for FCC and ISED are for HW + Laird factory firmware only. For customer implemented firmware, certifications are for HW only. It is the customer's responsibility to follow the mandatory conditions highlighted in this Note 1 and Note 2 in the FW that the customer implements. When used in IEEE 802.15.4-2006 250 kbps mode, in addition to the maximum conducted power limits, a maximum RF TX operational duty cycle of 58% or less (per frequency) must always be maintained, under all operating modes and power levels, to remain compliant with harmonic emission regulatory limits FCC (47 CFR 15.247) and ISED (RSS-247). This RF TX duty cycle limit is measured during any 100 mS period of operation.
Note 3	DSR, DTR, RI, and DCD can be implemented in the *smart*BASIC application.
Note 4	With I2C interface selected, pull-up resistors on I2C SDA and I2C SCL ***must*** be connected externally as per I2C standard.

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Module Specification Notes:

Note 5	Use of the internal DCDC convertor or LDO is decided by the underlying Bluetooth LE stack.
Note 6	For BL654PA (not LC840PA) Bluetooth LE coded PHY 125kbps (s=8), the conducted RF TX power is limited to 14 dBm (conducted) to be within the FCC/ISED TX power spectral density limit.

3 HARDWARE SPECIFICATIONS

3.1 Block Diagram and Pin-out

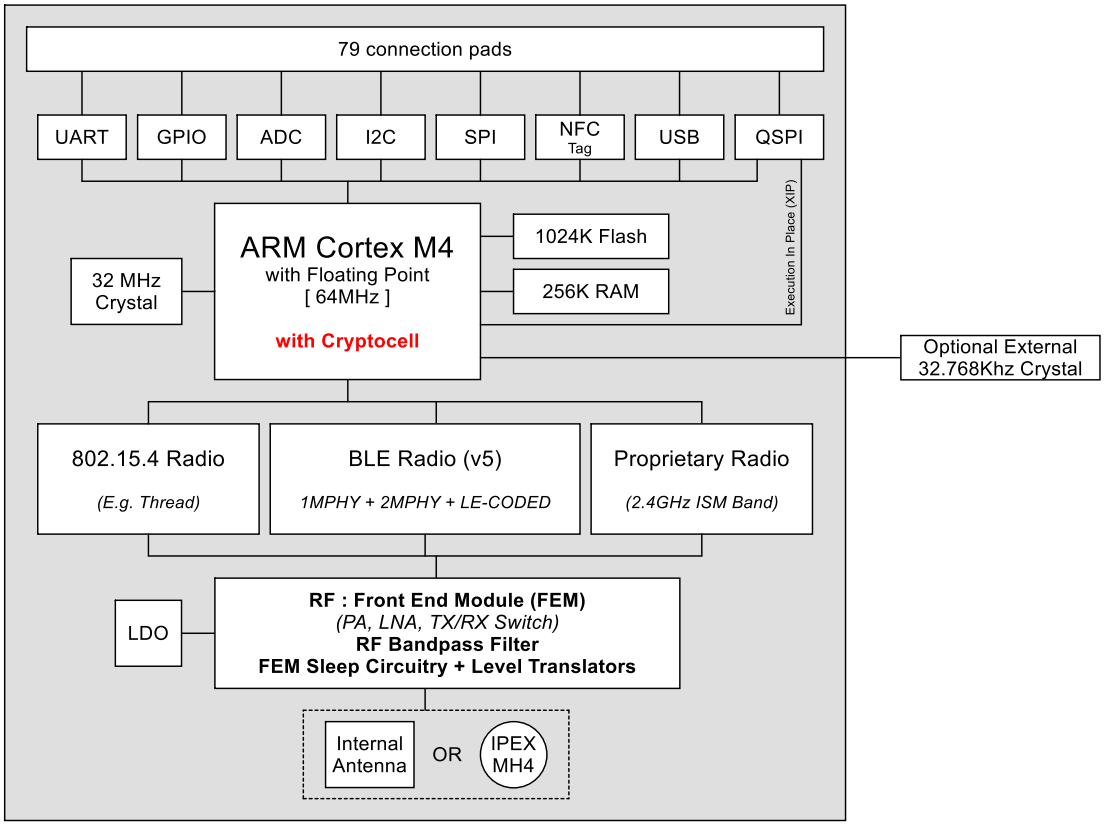

Figure 1: LC840PA block diagram

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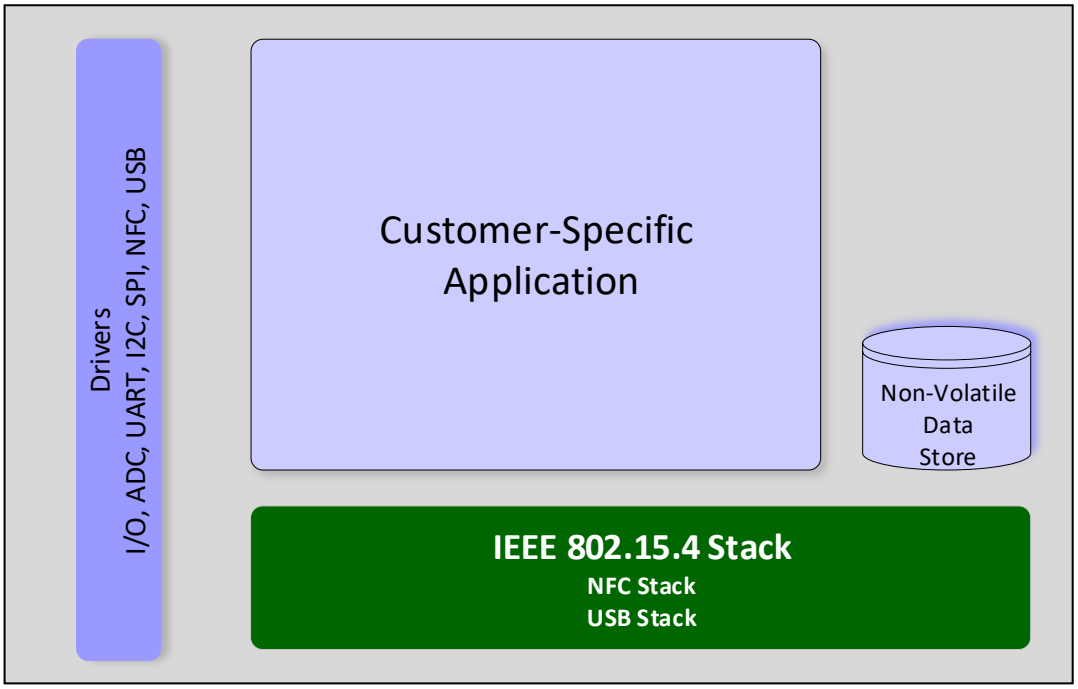

Figure 2: Functional HW and SW block diagram for LC840PA Bluetooth LE module

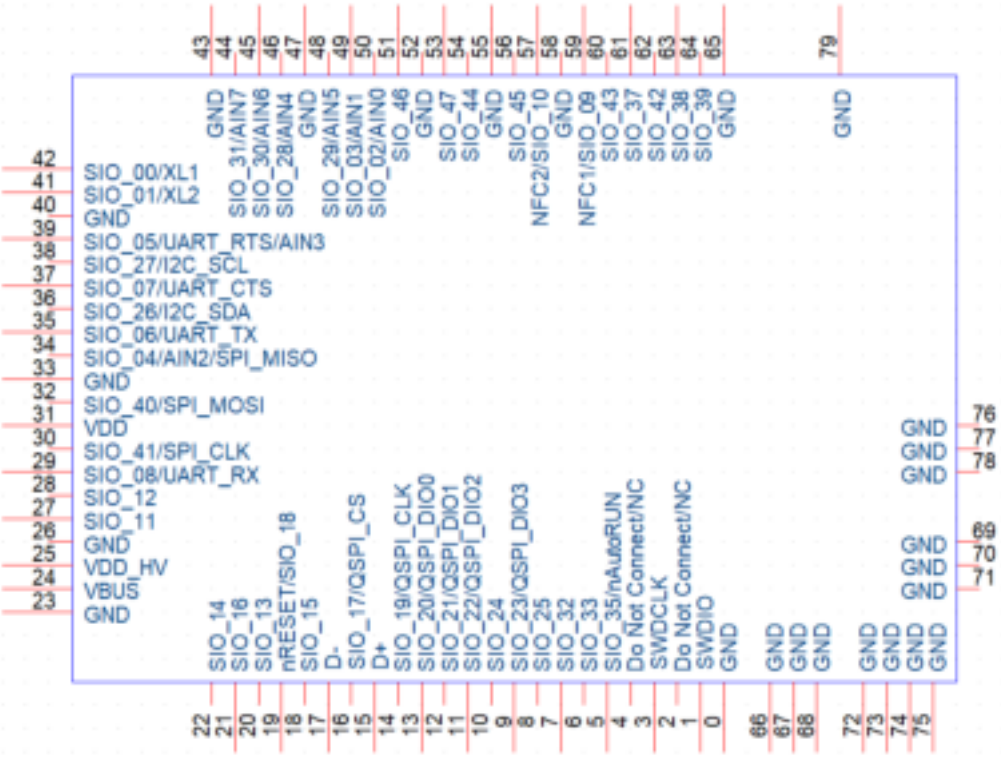

Figure 3: LC840PA module pin-out (top view). Outer row pads (long red line) and inner row pads (short red line) shown.

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3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
0	GND	-	-	-	-	-	-	-
1	SWDIO	SWDIO	-	IN	PULL-UP	AC24	SWDIO	-
2	DO NOT CONNECT/NC	No Connect		IN	PULL-UP	U24	P1.04	Do Not Connect.
3	SWDCLK	SWDCLK	-	IN	PULL-DOWN	AA24	SWDCLK	
4	DO NOT CONNECT/NC	No Connect	-	-	PULL-UP	W24	P1.02	Do Not Connect.
5	SIO_35/ nAutoRUN	nAutoRUN (smartBASIC only)	SIO_35	IN	PULL-DOWN	V23	P1.03	**Laird Devkit:** FTDI USB_DTR via jumper on J12 pin1-2.
6	SIO_33	SIO_33		IN	PULL-UP	Y23	P1.01	-
7	SIO_32	SIO_32	-	IN	PULL-UP	AD22	P1.00	-
8	SIO_25	SIO_25	-	IN	PULL-UP	AC21	PO.25	**Laird Devkit:** BUTTON4
9	SIO_23	SIO_23	QSPI_DIO3	IN	PULL-UP	AC19	PO.23	-
10	SIO_24	SIO_24		IN	PULL-UP	AD20	PO.24	**Laird Devkit:** BUTTON3
11	SIO_22	SIO_22	QSPI_DIO2	IN	PULL-UP	AD18	PO.22	-
12	SIO_21/ DEBUG_RX	DEBUG_RX	SIO_21/ QSPI_DIO1	IN	PULL-UP	AC17	PO.21	***ProFLEX:*** Debug UART Rx (Fixed 115.2kBaud, 8N1)
13	SIO_20/ DEBUG_TX	DEBUG_TX	SIO_20/ QSPI_DIO0	IN	PULL-UP	AD16	PO.20	***ProFLEX:*** Debug UART Tx (Fixed 115.2kBaud, 8N1)
14	SIO_19	SIO_19	QSPI_CLK	IN	PULL-UP	AC15	PO.19	-
15	D+	D+	-	IN		AD6	D+	-
16	SIO_17/WAKE	WAKE	SIO_17/ QSPI_CS	IN	PULL-UP	AD12	PO.17	***ProFLEX:*** wake (Active Low)
17	D-	D-	-	IN		AD4	D-	-
18	SIO_15	SIO_15	-	IN	PULL-UP	AD10	PO.15	**Laird Devkit:** LED3 ***ProFLEX:*** Rx LED
19	nRESET	nRESET	SIO_18	IN	PULL-UP	AC13	PO.18	System Reset (Active Low)

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
20	SIO_13	SIO_13	-	IN	PULL-UP	AD8	PO.13	**Laird Devkit:** LED1 ***ProFLEX:*** Undefined
21	SIO_16	SIO_16	-	IN	PULL-UP	AC11	PO.16	**Laird Devkit:** LED4 ***ProFLEX:*** Tx LED
22	SIO_14	SIO_14	-	IN	PULL-UP	AC9	PO.14	**Laird Devkit:** LED2 ***ProFLEX:*** Heartbeat LED
23	GND	-	-	-	-	-	-	-
24	VBUS							4.35V – 5.5V
25	VDD_HV	-	-	-	-	-	-	3.0V to 5.5V
26	GND	-	-	-	-	-	-	-
27	SIO_11	SIO_11	-	IN	PULL-UP	T2	PO.11	**Laird Devkit:** BUTTON1
28	SIO_12	SIO_12	-	IN	PULL-UP	U1	PO.12	BUTTON2
29	SIO_08/ UART_RX	HOST_UART_RX	SIO_08	IN	PULL-UP	N1	PO.08	smartBASIC:UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behavior ProFLEX:HOST_UART_RX
30	SIO_41/ SPI_CLK	SIO_41	SPI_CLK	IN	PULL-UP	R1	P1.09	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_CLK, Output: smartBASIC:SPIOPEN() selects SPI function, MOSI and CLK are outputs when in SPI master mode.
31	VDD	-	-	-	-			3.0V to 3.6V
32	SIO_40/ SPI_MOSI	SIO_40	SPI_MOSI	IN	PULL-UP	P2	P1.08	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_MOSI, Output smartBASIC:SPIOPEN() selects SPI function, MOSI and CLK are outputs in SPI master.
33	GND	-	-	-	-	-	-	-
34	SIO_04/ AIN2/ SPI_MISO	SIO_04	AIN2/ SPI_MISO	IN	PULL-UP	J1	PO.04/AIN2	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_MISO, Input. smartBASIC:SPIOPEN() selects SPI function; MOSI and CLK are outputs when in SPI master mode

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
35	SIO_06/ UART_TX	SIO_06	UART_TX	OUT	Set High in FW	L1	P0.06	smartBASIC:UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behavior ProFLEX: HOST_UART_TX
36	SIO_26/ I2C_SDA	SIO_26	I2C_SDA	IN	PULL-UP	G1	P0.26	**Laird Devkit:** I2C RTC chip. I2C data line.
37	SIO_07/ UART_CTS	SIO_07	UART_RTS	IN	PULL-DOWN	M2	P0.07	smartBASIC:UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behavior
38	SIO_27/ I2C_SCL	SIO_27	I2C_SCL	IN	PULL-UP	H2	P0.27	**Laird Devkit:** I2C RTC chip. I2C clock line.
39	SIO_05/ UART_RTS/ AIN3	SIO_05/ UART_RTS	AIN3	OUT	Set Low in FW	K2	P0.05/AIN3	smartBASIC:UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behavior ProFLEX: UART_CTS
40	GND	-	-	-	-	-	-	-
41	SIO_01/ XL2	XL2	SIO_01	IN	PULL-UP	F2	P0.01/XL2	Laird Devkit: Optional 32.768kHz crystal pad XL2 and associated load capacitor.
42	SIO_00/ XL1	XL1	SIO_00	IN	PULL-UP	D2	P0.00/XL1	Laird Devkit: Optional 32.768kHz crystal pad XL1 and associated load capacitor.
43	GND	-	-	-	-	-	-	-
44	SIO_31/ AIN7	SIO_31	AIN7	IN	PULL-UP	A8	P0.31/AIN7	-
45	SIO_30/ AIN6	SIO_30	AIN6	IN	PULL-UP	B9	P0.30/AIN6	-
46	SIO_28/ AIN4	SIO_28	AIN4	IN	PULL-UP	B11	P0.28/AIN4	-
47	GND	-	-	-	-	-	-	-
48	SIO_29/ AIN5	SIO_29	AIN5	IN	PULL-UP	A10	P0.29/AIN5	-
49	SIO_03/ AIN1	SIO_03	AIN1	IN	PULL-UP	B13	P0.03/AIN1	**Laird Devkit:** Temp Sens Analog
50	SIO_02/ AIN0	SIO_02	AIN0	IN	PULL-DOWN	A12	P0.02/AIN0	smartBASIC: Internal pull-down. Pull High externally to enter VSP (Virtual Serial Port) Service.

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
51	SIO_46	SIO_46	-	IN	PULL-UP	B15	P1.14	-
52	GND	-	-	-	-	-	-	-
53	SIO_47	SIO_47	-	IN	PULL-UP	A14	P1.15	-
54	SIO_44	SIO_44	-	IN	PULL-UP	B17	P1.12	**Laird Devkit:** SPI EEPROM. SPI_Eeprom_CS, Input
55	GND	-	-	-	-	-	-	-
56	SIO_45	SIO_45	-	IN	PULL-UP	A16	P1.13	-
57	NFC2/ SIO_10	NFC2	SIO_10	IN	-	J24	PO.10/NFC2	-
58	GND	-	-	-	-	-	-	-
59	NFC1/ SIO_09	NFC1	SIO_09	IN	-	L24	PO.09/NFC1	-
60	SIO_43	SIO_43	-	IN	PULL-UP	B19	P1.11	-
61	SIO_37	SIO_37	-	IN	PULL-UP	T23	P1.05	-
62	SIO_42	SIO_42	-	IN	PULL-UP	A20	P1.10	-
63	SIO_38	N/C	-	IN	PULL-UP	R24	P1.06	Reserved for future use. Do not connect.
64	SIO_39	SIO_39	-	IN	PULL-UP	P23	P1.07	-
65	GND	-	-	-	-	-	-	-
66	GND	-	-	-	-	-	-	-
67	GND	-	-	-	-	-	-	-
68	GND	-	-	-	-	-	-	-
69	GND	-	-	-	-	-	-	-
70	GND	-	-	-	-	-	-	-
71	GND	-	-	-	-	-	-	-
72	GND	-	-	-	-	-	-	Added GND in the LC840PA
73	GND	-	-	-	-	-	-	Added GND in the LC840PA
74	GND	-	-	-	-	-	-	Added GND in the LC840PA
75	GND	-	-	-	-	-	-	Added GND in the LC840PA

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull Up/ Down	nRF52840 QFN Pin	nRF52840 QFN Name	Comment
76	GND	-	-	-	-	-	-	Added GND in the LC840PA
77	GND	-	-	-	-	-	-	Added GND in the LC840PA
78	GND	-	-	-	-	-	-	Added GND in the LC840PA
79	GND	-	-	-	-	-	-	Added GND in the LC840PA

Pin Definition Notes:

Note 1	SIO = Signal Input or Output. Secondary function is selectable in *smart*BASIC application or via Nordic SDK. I/O voltage level tracks VDD. AIN = Analog Input.
Note 2	At reset, all SIO lines are configured as the defaults shown above. SIO lines can be configured through the *smart*BASIC application script to be either inputs or outputs with pull-ups or pull-downs. When an alternative SIO function is selected (such as I2C or SPI), the firmware does not allow the setup of internal pull-up/pull-down. Therefore, when I2C interface is selected, pull-up resistors on I2C SDA and I2C SCL ***must*** be connected externally as per I2C standard.
Note 3	JTAG (two-wire SWD interface), pin 1 (SWDIO) and pin 3 (SWDCLK). JTAG is required because Nordic SDK and ProFLEX applications can only be loaded using JTAG (*smart*BASIC firmware can be loaded using the JTAG as well as UART). We recommend that you use JTAG (2-wire interface) to handle future LC840PA module *smart*BASIC firmware upgrades. You ***must*** wire out the JTAG (2-wire interface) on your host design (see Figure 7, where four lines – SWDIO, SWDCLK, GND and VDD – should be wired out. *smart*BASIC firmware upgrades can still be performed over the UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the LC840PA JTAG (2-wire interface). Upgrading *smart*BASIC firmware or loading the *smart*BASIC applications is done using the UART interface.
Note 4	Pull the nRESET pin (pin 19) low for minimum 100 milliseconds to reset the LC840PA.
Note 5	The SIO_02 pin (pin 50) must be pulled high externally to enable VSP (Virtual Serial Port) which would allow OTA (over-the-air) *smart*BASIC application download. Refer to the latest firmware release documentation for details.
Note 6	Ensure that SIO_02 (pin 50) and AutoRUN (pin 5) are ***not both high*** (externally), in that state, the UART is bridged to Virtual Serial Port service (this comment is for BL654PA *smart*BASIC). **The LC840PA module does not respond to AT commands and cannot load *smart*BASIC application scripts.**
Note 7	Pin 5 (nAutoRUN) is an input, with active low logic. In the development kit it is connected so that the state is driven by the host's DTR output line. The nAutoRUN pin must be externally held high or low to select between the following two LC840PA operating modes: ▪ Self-contained Run mode (nAutoRUN pin held at 0V –this is the default (internal pull-down enabled)) ▪ Interactive/Development mode (nAutoRUN pin held at VDD) The *smart*BASIC firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application script named **$autorun$**, then the *smart*BASIC firmware executes the application script automatically, hence the name S*elf-contained Run Mode*.

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Pin Definition Notes:

Note 8	The *smartBASIC* firmware has SIO pins as Digital (Default Function) INPUT pins, which are set PULL-UP by default. This avoids floating inputs (which can cause current consumption to drive with time in low power modes (such as Standby Doze). You can disable the PULL-UP through your *smart*BASIC application. All of the SIO pins (with a default function of DIO) are inputs (apart from SIO_05 and SIO_06, which are outputs): ▪ SIO_06 (alternative function UART_TX) is an output, set High (in the firmware). ▪ SIO_05 (alternative function UART_RTS) is an output, set Low (in the firmware) (optional use by ProFLEX). ▪ SIO_08 (alternative function UART_RX) is an input, set with internal pull-up (in the firmware). ▪ SIO_07 (alternative function UART_CTS) is an input, set with internal pull-down (in the firmware) (unused by ProFLEX). ▪ SIO_02 is an input set with internal pull-down (in the firmware). It is used for OTA downloading of *smart*BASIC applications. Refer to the latest firmware extension documentation for details. ▪ UART_RX, UART_TX, and UART_CTS are 3.3 V level logic (if VDD is 3.3 V; such as SIO pin I/O levels track VDD). For example, when Rx and Tx are idle, they sit at 3.3 V (if VDD is 3.3 V). Conversely, handshaking pins CTS and RTS at 0V are treated as assertions. ▪ SIO_20 (alternative function UART2_RX) is an input, set with internal pull-up (in the firmware) ▪ SIO_21 (alternative function UART2_TX) is an output, set High (in the firmware).
Note 9	LC840PA also allows an option to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the LC840PA pins SIO_01/XL2 (pin 41) and SIO_00/XL1 (pin 42). This provides higher accuracy protocol timing and helps with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the Rx window must be open. External 32.768kHz crystal not required for LC840PA module normal operation with Bluetooth LE/smartBASIC firmware. The on-chip 32.768 kHz LFRC oscillator provides the standard accuracy of ±500 ppm, with calibration required every eight seconds (default) to stay within ±500 ppm. **External 32.768kHz crystal is required for IEEE802.15.4:2006 ProFLEX firmware.**
Note 10	LC840PA power supply options: ▪ **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 3.0V to 3.6V range to LC840PA VDD and VDD_HV pins. *OR* ▪ **Option 2** – High voltage mode power supply mode (using LC840PA VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDDH pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 3.0V to 5.5V range to LC840PA VDD_HV pin. LC840PA VDD pin left unconnected. For either option, if you use USB interface then the LC840PA VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the LC840PA VBUS pin, you MUST externally fit a 4.7uF to ground.

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3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Maximum current ratings

Parameter	Min	Max	Unit
Voltage at VDD pin	-0.3	+3.9 (Note 1)	V
Voltage at VDD_HV pin	-0.3	+5.5	V
VBUS	-0.3	+5.8	V
Voltage at GND pin		0	V
Voltage at SIO pin (at VDD≤3.6V)	-0.3	VDD +0.3	V
Voltage at SIO pin (at VDD≥3.6V)	-0.3	3.9	V
NFC antenna pin current (NFC1/2)	-	80	mA
Radio RF input level	-	-1	dBm
Environmental			
Storage temperature	-40	+85	ºC
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489)			
Conductive		4	KV
Air Coupling		8	KV
Flash Memory (Endurance) (Note 2)	-	10000	Write/erase cycles
Flash Memory (Retention)	-	10 years at 40°C	-

Maximum Ratings Notes:

Note 1	The absolute maximum rating for VDD pin (max) is 3.9V for the LC840PA.
Note 2	Wear levelling is used in file system.

3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD (independent of DCDC)[1] supply range	3.0	3.3	3.6	V
VDD_HV (independent of DCDC) supply range	3.0	3.7	5.5	V
VBUS USB supply range	4.35	5	5.5	V
VDD Maximum ripple or noise[2]	-	-	10	mV
VDD supply rise time (0V to 1.7V)[3]	-	-	60	mS
Time in Power				mS
				mS
				mS
VDD_HV supply rise time (0V to 3.7V) [3]			100	mS
Operating Temperature Range	-40	-	+85	ºC
Maximum Received Signal Strength at <0.1% PER		-11		dBm

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Recommended Operating Parameters Notes:

Note 1	4.7 uF internal to module on VDD. The internal DCDC convertor or LDO is decided by the underlying Bluetooth LE stack. **For IEEE802.15.4:2006 operation, the internal DCDC convertor is enabled to minimize power consumption.**
Note 2	This is the maximum VDD or VDD_HV ripple or noise (at any frequency) that does not disturb the radio.
Note 3	The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.
Note 4	LC840PA power supply options: ▪ **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 3.0V to 3.6V range to LC840PA VDD and VDD_HV pins. *OR* ▪ **Option 2** – High voltage mode power supply mode (using LC840PA VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 3.0V to 5.5V range to LC840PA VDD_HV pin. LC840PA VDD pin left unconnected. For either option, if you use USB interface then the LC840PA VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the LC840PA VBUS pin, you MUST externally fit a 4.7uF to ground. **For IEEE 802.15.4:2006 operation, the USB interface is not supported.**

Table 4: Signal levels for interface, SIO

Parameter	Min	Typ	Max	Unit
V_{IH} Input high voltage	0.7 VDD		VDD	V
V_{IL} Input low voltage	VSS		0.3 x VDD	V
V_{OH} Output high voltage				
(std. drive, 0.5 mA) (Note 1)	VDD -0.4		VDD	V
(high-drive, 3 mA) (Note 1)	VDD -0.4		VDD	V
(high-drive, 5mmA) (Note 2)	VDD -0.4		VDD	
V_{OL} Output low voltage				
(std. drive, 0.5 mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 3nmA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 5mmA) (Note 2)	VSS		VSS+0.4	
V_{OL} Current at VSS+0.4V, Output set low				
(std. drive, 0.5 mA) (Note 1)	1	2	4	mA
(high-drive, 3 mA) (Note 1)	3	-	-	mA
(high-drive, 5 mA) (Note 2)	6	10	15	mA
V_{OL} Current at VDD -0.4, Output set low				
(std. drive, 0.5 mA) (Note 1)	1	2	4	mA
(high-drive, 3 mA) (Note 1)	3	-	-	mA
(high-drive, 5 mA) (Note 2)	6	9	14	mA
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ
Pad capacitance		3		pF
Pad capacitance at NFC pads		4		pF

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Signal Levels Notes:

Note 1	For VDD≥1.7V. The firmware supports high drive (3 mA, as well as standard drive).
Note 2	For VDD≥2.7V. The firmware supports high drive (5 mA (since VDD≥2.7V), as well as standard drive). The GPIO (SIO) high reference voltage always equals the level on the **VDD** pin. ▪ Normal voltage mode – The GPIO high level equals the voltage supplied to the VDD pin ▪ High voltage mode – The GPIO high level equals the level specified (is configurable to 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V). In High voltage mode, the VDD pin becomes an output voltage pin. The VDD output voltage and hence the GPIO is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. Refer to Table 15 for additional details.

Table 5: SIO pin alternative function AIN (ADC) specification

Parameter	Min	Typ	Max	Unit
Maximum sample rate			**200**	**kHz**
ADC Internal reference voltage	-1.5%	0.6 V	+1.5%	%
ADC pin input internal selectable scaling		4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6		scaling
ADC input pin (AIN) voltage maximum without damaging ADC w.r.t (see Note 1) VCC Prescaling 0V-VDD 4, 2, 1, ½, 1/3, ¼, 1/5, 1/6		VDD+0.3		V
Configurable Resolution	8-bit mode	10-bit mode	12-bit mode	bits
Configurable (see Note 2) Acquisition Time, source resistance ≤10kΩ Acquisition Time, source resistance ≤40kΩ Acquisition Time, source resistance ≤100kΩ Acquisition Time, source resistance ≤200kΩ Acquisition Time, source resistance ≤400kΩ Acquisition Time, source resistance ≤800kΩ		 3 5 10 15 20 40		 uS uS uS uS uS uS
Conversion Time (see Note 3)		<2		uS
ADC input impedance (during operation) (see Note 3) Input Resistance Sample and hold capacitance at maximum gain		 >1 2.5		 MOhm pF

Recommended Operating Parameters Notes:

Note 1	Stay within internal 0.6 V reference voltage with given pre-scaling on AIN pin and do not violate ADC maximum input voltage (for damage) for a given VCC, e.g. If VDD is 3.6V, you can only expose AIN pin to VDD+0.3 V. Default pre-scaling is 1/6 which configurable via *smart*BASIC.
Note 2	Firmware allows configurable resolution (8-bit, 10-bit or 12-bit mode) and acquisition time. LC840PA ADC is a Successive Approximation type ADC (SSADC), as a result no external capacitor is needed for ADC operation. Configure the acquisition time according to the source resistance that customer has. The sampling frequency is limited by the sum of sampling time and acquisition time. The maximum sampling time is 2us. For acquisition time of 3us the total conversion time is therefore 5us, which makes maximum sampling

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Recommended Operating Parameters Notes:	
	frequency of 1/5us = 200kHz. Similarly, if acquisition time of 40us chosen, then the conversion time is 42us and the maximum sampling frequency is 1/42us = 23.8 kHz.
Note 3	ADC input impedance is estimated mean impedance of the ADC (AIN) pins.

3.4 Programmability

3.4.1 LC840PA Default Firmware

The LC840PA module comes loaded with a customer specific Laird ProFLEX-like firmware application that is IEEE802.15.4 compliant. This firmware enables backwards compatibility with the Laird ProFLEX01-R2 module firmware.

If Bluetooth LE operation is desired, it is recommended to use the Laird BL654PA module.

3.4.2 BL654PA Special Function Pins in *smart*BASIC

Refer to the *smart*BASIC extension manual for details of functionality connected to this:

- nAutoRUN pin (SIO_35), see for default
- VSP pin (SIO_02), see for default
- SIO_38 – Reserved for future use. Do not connect. See

Table 6: nAutoRUN pin

Signal Name	Pin #	I/O	Comments
nAutoRUN /(SIO_35)	5	I	Input with active low logic. Internal pull down (default). Operating mode selected by nAutoRun pin status: ▪ Self-contained Run mode (nAutoRUN pin held at 0V). ▪ If Low (0V), runs $autorun$ if it exists ▪ Interactive/Development mode (nAutoRUN pin held at VCC). ▪ If High (VCC), runs via at+run (and file name of application)

In the development board nAutoRUN pin is connected so that the state is driven by the host's DTR output line.

Table 7: VSP mode

Signal Name	Pin #	I/O	Comments
SIO_02	50	I	Internal pull down (default). VSP mode selected by externally pulling-up SIO_02 pin: **High (VCC),** then OTA *smart*BASIC application download is possible.

Table 8: SIO_38

Signal Name	Pin #	I/O	Comments
SIO_38	63	I	Internal pull up (default). Reserved for future use. Do not connect if using smartBASIC FW.

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4 Power Consumption

Data at VDD of 3.3 V with internal (to chipset) LDO ON or with internal (to chipset) DCDC ON (see Power Consumption Note 1) and 25°C.

4.1 Power Consumption

Table 9: Power consumption

Parameter	Min	Typ	Max	Unit
Active mode 'peak' current (Note 1)		With DCDC [with LDO]		
(Advertising or Connection)				
Tx only run peak current @ Txpwr = +18 dBm		102.2 [112.7]		mA
Tx only run peak current @ Txpwr = +14 dBm		65.9 [77.0]		mA
Tx only run peak current @ Txpwr = 6 dBm		37.2 [44.4]		mA
Tx only run peak current @ Txpwr = 0 dBm		25.5 [30.5]		mA
Tx only run peak current @ Txpwr = -6 dBm		21.2 [25.3]		mA
Tx only run peak current @ Txpwr = -26 dBm		18.5 [21.8]		mA
Active Mode Rx only 'peak' current, Bluetooth LE 1 Mbps (Note 1)		10.9 [17.3]		mA
Ultra-Low Power Mode 1 (Note 2) Standby Doze /System ON Idle, 256 k RAM retention		5.9		uA
Ultra-Low Power Mode 2 (Note 3) Deep Sleep /System OFF (no RAM retention)		2.0		uA
Active Mode Average current (Note 4)				
Advertising Average Current draw				
Max, with advertising interval (min) 20 mS		Note4		uA
Min, with advertising interval (max) 10240 mS		Note4		uA
Connection Average Current draw				
Max, with connection interval (min) 7.5 mS		Note4		uA
Min, with connection interval (max) 4000 mS		Note4		uA

Power Consumption Notes:

Note 1	This is for Peak Radio Current only, but there is additional current due to the MCU. The Normal Voltage mode internal REG1 DCDC convertor or LDO is decided by the underlying Bluetooth LE stack.
Note 2	LC840PA modules Standby Doze (System ON Idle) is 5.9uA typical. When using *smart*BASIC firmware, Standby Doze is entered automatically (when a waitevent statement is encountered within a smartBASIC application script). In Standby Doze, all peripherals that are enabled stay on and may re-awaken the chip. Depending on active peripherals, current consumption ranges from 5.9 µA to 370 uA (when UART is ON). See individual peripherals current consumption data in the Peripheral Block Current Consumption section. smartBASIC firmware has functionality to detect GPIO change with no current consumption cost, it is possible to close the UART and get to the 5.9 uA current consumption regime and still be able to detect for incoming data and be woken up so that the UART can be re-opened at expense of losing that first character. The LC840PA Standby Doze current consists of the below nRF52840 blocks: ▪ nRF52 System ON IDLE current (no RAM retention) (0.97 uA) – This is the base current of the CPU

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Power Consumption Notes:

	▪ LFRC (0.7 uA) and RTC (0.1uA) running as well as 256k RAM retention (1.4 uA) – This adds to the total of 3.1 uA typical. The RAM retention is 20nA per 4k block (1.28uA), but this can vary to 30nA per 4k block (1.92uA) which would make the total 3.7uA. ▪ LC840PA PA and LNA and associated circuitry takes the rest.
Note 3	In Deep Sleep (System OFF), everything is disabled, and the only wake-up sources (including NFC to wakeup) are reset and changes on SIO or NFC pins on which sense is enabled. The current consumption seen is ~2.0 uA typical in LC840PA modules. ▪ Coming out from Deep Sleep (System OFF) to Standby Doze (System ON Idle) through the reset vector.
Note 4	Average current consumption depends on several factors (including Tx power, VCC, accuracy of 32MHz and 32.768 kHz). With these factors fixed, the largest variable is the Bluetooth LE advertising or Bluetooth LE connection interval set. Bluetooth LE Advertising Interval range: ▪ 20 milliseconds to 10240 mS (10485759.375 mS in BT 5.1) in multiples of 0.625 milliseconds. For a Bluetooth LE advertising event: ▪ The minimum average current consumption is when the advertising interval is large 10240 mS (10485759.375 mS in BT 5.1) although this may cause long discover times (for the advertising event) by scanners ▪ The maximum average current consumption is when the advertising interval is small 20 mS Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether it's continuously advertising or periodically advertising. Bluetooth LE Connection Interval range (for a peripheral): ▪ 7.5 milliseconds to 4000 milliseconds in multiples of 1.25 milliseconds. For a Bluetooth LE connection event (for a peripheral device): ▪ The minimum average current consumption is when the connection interval is large 4000 milliseconds ▪ The maximum average current consumption is with the shortest connection interval of 7.5 ms; no slave latency. Other factors that are also related to average current consumption include: ▪ Number packets per connection interval with each packet payload size ▪ An inaccurate 32.768 kHz master clock accuracy would increase the average current consumption. Bluetooth LE Connection Interval range (for a central device): ▪ 2.5 milliseconds to 40959375 milliseconds in multiples of 1.25 milliseconds.

4.2 Peripheral Block Current Consumption

The values below are calculated for a typical operating voltage of 3V.

Table 10: UART power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
UART Run current @ 115200 bps	-	729	951	-	uA
UART Run current @ 1200 bps	-	729	951	-	uA
Idle current for UART (no activity)	-	29	29	-	uA
UART Baud rate	1.2	-		1000	kbps

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Table 11: SPI power consumption

Parameter	Min	Typ		Max	Unit
		With DCDC (REG1)	With LDO (REG1)		
SPI Master Run current @ 2 Mbps	-	803	1040	-	uA
SPI Master Run current @ 8 Mbps	-	803	1040	-	uA
Idle current for SPI (no activity)	-	<1	<1	-	uA
SPI bit rate	-	-		8	Mbps

Table 12: I2C power consumption

Parameter	Min	Typ		Max	Unit
		With DCDC (REG1)	With LDO (REG1)		
I2C Run current @ 100 kbps	-	967	1250	-	uA
I2C Run current @ 400 kbps	-	967	1250	-	uA
Idle current for I2C (no activity)	-	3.2	3.2	-	uA
I2C Bit rate	100	-		400	kbps

Table 13: ADC power consumption

Parameter	Min	Typ		Max	Unit
		With DCDC (REG1)	With LDO (REG1)		
ADC current during conversion	-	1640	2010	-	uA
Idle current for ADC (no activity)	-	0	0	-	uA

The above current consumption is for the given peripheral including the internal blocks that are needed for that peripheral for both the case when DCDC(REG1) is on and off. The peripheral Idle current is when the peripheral is enabled but not running (not sending data or being used) and must be added to the LC840PA StandByDoze current (Nordic System ON Idle current). In all cases radio is not turned on.

For asynchronous interface, like the UART (asynchronous as the other end can communicate at any time), the UART on the LC840PA must be kept open (by a command in *smart*BASIC application script), resulting in the base current consumption penalty.

For a synchronous interface like the I2C or SPI (since LC840PA side is the master), the interface can be closed and opened (by a command in *smart*BASIC application script) only when needed, resulting in current saving (no base current consumption penalty). There's a similar argument for ADC (open ADC when needed).

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5 FUNCTIONAL DESCRIPTION

To provide the widest scope for integration, a variety of physical host interfaces/sensors are provided. The major LC840PA module functional blocks described below.

5.1 Power Management

Power management features:

- System Standby Doze (System ON Idle) and Deep Sleep (System OFF) modes
- Open/Close peripherals (UART, SPI, QSPI, I2C, SIO's, ADC, NFC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption
- Use of the internal DCDC convertor or LDO is decided by the underlying Bluetooth LE stack (Bluetooth LE mode) or internal DCDC (IEEE 802.15.4:2006 mode)
- *smart*BASIC command allows the supply voltage to be read (through the internal ADC)
- Pin wake-up system from deep sleep/System OFF (including from NFC pins)

Power supply features:

- Supervisor hardware to manage power during reset, brownout, or power fail.
- 3.0V to 3.6V supply range for normal power supply (VDD pin) using internal DCDC convertor or LDO decided by the underlying Bluetooth LE stack.
- 3.0V to 5.5 supply range for High voltage power supply (VDD_HV pin) using internal DCDC convertor or LDO decided by the underlying Bluetooth LE stack.
- 4.35V to 5.5V supply range for powering USB (VBUS pin) portion of LC840PA only. The remainder of the LC840PA module circuitry must still be powered through the VDD (or VDD_HV) pin.

5.2 LC840PA Power Supply Options

The LC840PA module power supply internally contains the following two main supply regulator stages (Figure 4):

- REG0 – Connected to the VDD_HV pin
- REG1 – Connected to the VDD pin

The USB power supply is separate (connected to the VBUS pin).

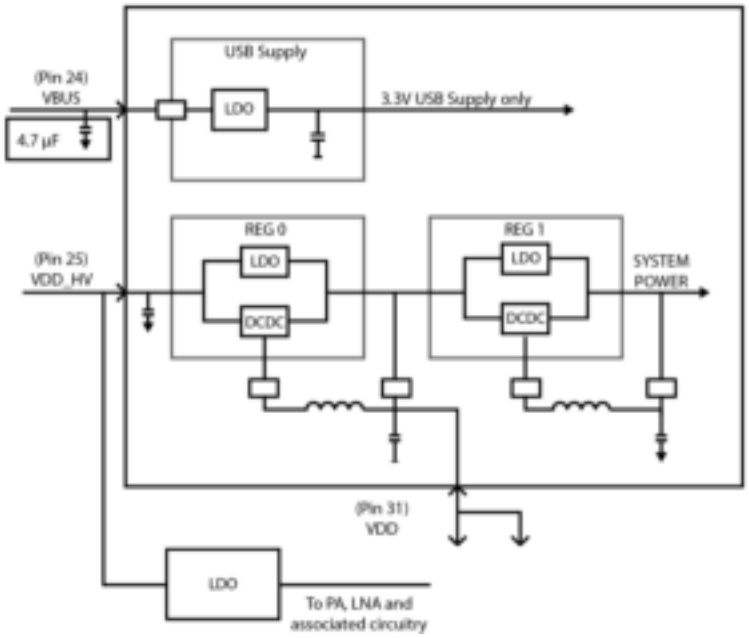

Figure 4: LC840PA power supply block diagram (adapted from the following resource: http://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.0.pdf

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The LC840PA power supply system enters one of two supply voltage modes, normal or high voltage mode, depending on how the external supply voltage is connected to these pins.

LC840PA power supply options:

- **Option 1 –** Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 3.0V to 3.6V range to LC840PA VDD and VDD_HV pins.

  OR

- **Option 2 –** High voltage mode power supply mode (using LC840PA VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 3.0V to 5.5V range to LC840PA VDD_HV pin. LC840PA VDD pin left unconnected.

For either option, if you use USB interface then the LC840PA VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the LC840PA VBUS pin, you **MUST** externally fit a 4.7uF to ground.

Table 14 summarizes these power supply options.

Table 14: LC840PA powering options

Power Supply Pins and Operating Voltage Range	OPTION 1 Normal voltage mode operation connect?	OPTION 2 High voltage mode operation connect?	OPTION 1 with USB peripheral, operation, and normal voltage connect?	OPTION 2 with USB peripheral, operation, and high voltage connect?
VDD (pin31) 3.0V to 3.6V	Yes (Note 1)	No (Note 2)	Yes	No (Note 2)
VDD_HV (pin25) 3.0V to 5.5V	No	Yes	No	Yes (Note 5)
VBUS (pin24) 4.35V to 5.5V	No	(Note 3)	Yes (Note 4)	Yes (Note 4)

Power Supply Option Notes:

Note 1	**Option 1 –** External supply voltage is connected to BOTH the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 3.0V to 3.6V range to BOTH LC840PA VDD and VDD_HV pins.

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Power Supply Option Notes:

Note 2

Option 2 – External supply within range 3.0V to 5.5V range to the LC840PA VDD_HV pin ONLY. LC840PA VDD pin left unconnected.

In High voltage mode, the VDD pin becomes an output voltage pin. It can be used to supply external circuitry from the VDD pin. Before any current can be taken from the LC840PA VDD pin, this feature must be enabled in the LC840PA. Additionally, the VDD output voltage is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V.

The supported LC840PA VDD pin output voltage range depends on the supply voltage provided on the LC840PA VDD_HV pin. The minimum difference between voltage supplied on the VDD_HV pin and the voltage output on the VDD pin is 0.3 V. The maximum output voltage of the VDD pin is VDDH – 0.3V. Table4 shows the current that can be drawn by external circuitry from VDD pin in high voltage mode (supply on VDD_HV).

Table 15: Current that can be drawn by external circuitry from VDD pin in High voltage mode (supply on VDD_HV)

Parameter	Min	Typ	Max	Unit
External current draw (from VDD pin) allowed in High Voltage mode (supply on VDD_HV) during System OFF (LC840PA Deep Sleep)			1	mA
External current draw (from VDD pin) allowed in High Voltage mode (supply on VDD_HV) when radio Tx RF power **higher** than 4dBm.			5	mA
External current draw (from VDD pin) allowed in High Voltage mode (supply on VDD_HV) when radio Tx RF power **lower** than 4dBm.			25	mA
Minimum difference between voltage supplied on VDD_HV pin and voltage on VDD pin		0.3		V

Note 3

External current draw is the sum of all GPIO currents and current being drawn from VDD.

Depends on whether USB operation is required

Note 4

When using the LC840PA **VBUS** pin, you **must** externally fit a 4.7uF capacitor to ground.

Note 5

To use the LC840PA USB peripheral:

1. Connect the LC840PA VBUS pin to the external supply within the range 4.35V to 5.5V. When using the LC840PA VBUS pin, you **MUST** externally fit a 4.7 uF to ground.

2. Connect the external supply to either the VDD (Option 1) or VDD_HV (Option 2) pin to operate the rest of LC840PA module.

   When using the LC840PA USB peripheral, the VBUS pin can be supplied from same source as VDD_HV (within the operating voltage range of the VBUS pin and VDD_HV pin).

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5.3 Clocks and Timers

5.3.1 Clocks

The integrated high accuracy 32 MHz (±10 ppm) crystal oscillator helps with radio operation and reducing power consumption in the active modes.

The integrated on-chip 32.768 kHz LFRC oscillator (±500 ppm) provides protocol timing and helps with radio power consumption in the system StandByDoze and Deep Sleep modes by reducing the time that the RX window needs to be open.

To keep the on-chip 32.768 kHz LFRC oscillator within ±500 ppm (which is needed to run the Bluetooth LE stack) accuracy, RC oscillator needs to be calibrated (which takes 33 mS) regularly. The default calibration interval is eight seconds which is enough to keep within ±500 ppm. The calibration interval ranges from 0.25 seconds to 31.75 seconds (in multiples of 0.25 seconds) and configurable via firmware

The ProFLEX firmware does not use the on-chip 32.768kHz LFRC oscillator but instead requires an externa 32.768 crystal to be attached. The external crystal enables high baud rate communications and ensures the lowest power operation in sleep mode.

5.3.2 Timers

When using *smart*BASIC, the timer subsystem enables applications to be written which allows future events to be generated based on timeouts.

- **Regular Timer** – There are eight built-in timers (regular timers) derived from a single RTC clock which are controlled solely by *smart*BASIC functions. The resolution of the regular timer is 976 microseconds.
- **Tick Timer –** A 31-bit free running counter that increments every (1) millisecond. The resolution of this counter is 488 microseconds.

Refer to the ***smart*BASIC User Guide** available from the Laird BL654PA product page.

The ProFLEX firmware uses timers as needed internally for RTOS, internal and external events and scheduling.

5.4 Radio Frequency (RF)

- **2402–2480 MHz Bluetooth Low Energy (Bluetooth LE) BT5.2 radio transceiver**
  - RX sensitivity -98.5 dBm 1Mbps Bluetooth LE
  - RX sensitivity -95 dBm 2Mbps Bluetooth LE
  - RX sensitivity -107 dBm 125 kbps coded PHY Bluetooth LE (long-range).
  - Tx output power of +18 dBm programmable down to 14 dBm, 6 dBm, 0 dBm, -6 dBm and final TX power level of -26 dBm.
  - TX power for coded PHY 125 kbps (s=8) is limited to 14 dBm to stay within regulatory TX power spectral density requirements (Bluetooth LE only)
- **2405–2480 MHz IEEE 802.15.5-2006 radio transceiver, implementing IEEE 802.15.5-2006 compliant**
  - 250 kbps, 2450 MHz, O-QSPK PHY
  - Channel 11-25, channel 11 2405 MHz and CH25 2475 MHz (CH26 not certified)
  - Clear channel assessment (CCA)
  - Energy detection (ED) scan
  - CRC generation

  MANDITORY: Please read the radio regulatory information in **Note 1** and **Note 2** including RF duty cycle limitations.
- RF band pass filter to help with cellular RF co-existence.
- **RF conducted interface available in the following two ways:**
  - 453-00087: RF connected to on-board PCB trace antenna
  - 453-00088: RF connected to on-board IPEX MH4 RF connector
    - Antenna options:
      - Integrated PCB trace antenna on the 453-00087
      - External dipole antenna connected with to IPEX MH4 RF connector on the 453-00088
- **Received Signal Strength Indicator (RSSI)**
  - RSSI accuracy (valid range -90 to -20 dBm) is ±2 dB typical
    - LC840PA RX LNA gain is 11dB, so RSSI valid range becomes -101 dB to -31 dBm
  - RSSI resolution 1 dB typical
- Maximum Received Signal Strength (at <0.1% PER) of -11 dBm. Limited by RX LNA gain of 11 dB in front end module

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5.5 NFC

NFC support:

- Based on the NFC forum specification
  - 13.56 MHz
  - Date rate 106 kbps
  - NFC Type 2 and Type 4 tag emulation
- Modes of operation:
  - Disable
  - Sense
  - Activated

5.5.1 Use Cases

- Touch to pair with NFC
- Launch a smartphone app (on Android)
- NFC enabled Out-of-Band Pairing
- System Wake-On-Field function
  - Proximity Detection
  -

The ProFLEX firmware does not use NFC.

Table 16: NFC interface

Signal Name	Pin No	I/O	Comments
NFC1/SIO_09	59	I/O	The NFC pins are by default NFC pins and an alternate function on each pin is GPIO. Refer to the *smart*BASIC. User manual.
NFC2/SIO_10	57	I/O	

5.5.2 NFC Antenna Coil Tuning Capacitors

From Nordic's *nRF52840 Objective Product Specification v1.0*: http://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.0.pdf

The NFC antenna coil must be the connected differential between the NFC1 and NFC2 pins of the LC840PA. Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz (Figure 5).

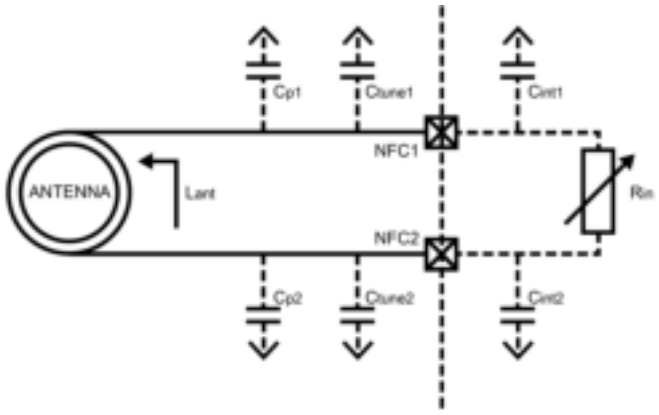

Figure 5: NFC antenna coil tuning capacitors

The required external tuning capacitor value is given by the following equation:

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_p - C_{int}$$

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An antenna inductance of Lant = 0.72 uH provides tuning capacitors in the range of 300 pF on each pin. The total capacitance on NFC1 and NFC2 must be matched. Cint and Cp are small usually (Cint is 4pF), so can be omitted from calculation.

Battery Protection Note: If the NFC coil antenna is exposed to a strong NFC field, the supply current may flow in the opposite direction due to parasitic diodes and ESD structures.

If the battery does not tolerate a return current, a series diode must be placed between the battery and the LC840PA to protect the battery.

5.6 UART Interface

Note: The LC840PA has two UARTs. The ProFLEX firmware designates these UARTs as HOST and DEBUG, see section 3.2.

The Universal Asynchronous Receiver/Transmitter (UART) offers fast, full-duplex, asynchronous serial communication with built-in flow control support (UART_CTS, UART_RTS) in HW up to one Mbps baud. Parity checking and generation for the ninth data bit are supported.

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signaling levels are nominal 0 V and 3.3 V (tracks VDD) and are inverted with respect to the signaling on an RS232 cable.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input. Both are active low.

These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS are all 3.3 V level logic (tracks VDD). For example, when RX and TX are idle, they sit at 3.3 V. Conversely for handshaking pins CTS, RTS at 0 V is treated as an assertion.

The module communicates with the customer application using the following signals:

- Port/TxD of the application sends data to the module's UART_RX signal line
- Port/RxD of the application receives data from the module's UART_TX signal line

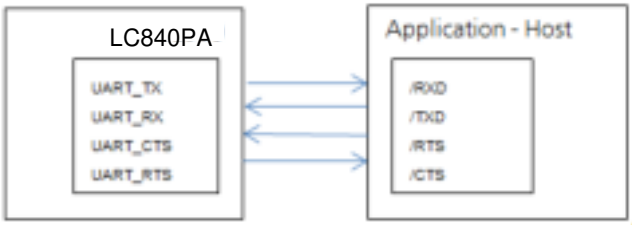

Figure 6: UART signals

Note: The LC840PA serial module output is at 3.3V CMOS logic levels (tracks VDD). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS other than for testing and prototyping. If these pins are linked and the host sends data at the point that the LC840PA de-asserts its RTS signal, there is significant risk that internal receive buffers will overflow which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

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Table 17: UART interface

Signal Name	Pin No	I/O	Comments
SIO_06 / UART_Tx	35	O	SIO_06 (alternative function UART_Tx) is an output, set high (in firmware).
SIO_08 / UART_Rx	29	I	SIO_08 (alternative function UART_Rx) is an input, set with internal pull-up (in firmware).
SIO_05 / UART_RTS	39	O	SIO_05 (alternative function UART_RTS) is an output, set low (in firmware). (Optional in ProFLEX)
SIO_07 / UART_CTS	37	I	SIO_07 (alternative function UART_CTS) is an input, set with internal pull-down (in firmware). (Unused in ProFLEX)
SIO_21 / UART2_Tx	12	O	SIO_21 (alternative function UART_Tx) is an output, set high (in firmware).
SIO_20 / UART2_Rx	13	I	SIO_21 (alternative function UART_Rx) is an input, set with internal pull-up (in firmware).

In ProFLEX, UART is the Host Interface and UART2 is the Debug Interface.

The UART interface is also used to load customer developed *smart*BASIC application script.

5.7 USB interface

LC840PA has USB2.0 FS (Full Speed, 12 Mbps) hardware capability. **The ProFLEX firmware does not use the USB interface.**

Table 18: USB interface

Signal Name	Pin No	I/O	Comments
D-	17	I/O	
D+	15	I/O	
VBUS	24		When using the LC840PA VBUS pin (which is mandatory when a USB interface is used), you MUST connect a 4.7uF capacitor to ground. ***Note:*** *You MUST power the rest of LC840PA module circuitry through the VDD pin (OPTION1) or VDD_HV pin (OPTION2).*

5.8 SPI Bus

The SPI interface is an alternate function on SIO pins. **The ProFLEX firmware does not use SPI Bus.**

The module is a master device that uses terminals SPI_MOSI, SPI_MISO, and SPI_CLK. SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping.

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SPI_MOSI, SPI_MISO, SPI_SCK,) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals are necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double buffered.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Table 19: SPI interfaces

Signal Name	Pin No	I/O	Comments
SIO_40/SPI_MOSI	32	O	This interface is an alternate function configurable by *smart*BASIC. Default in the FW pin 56 and 53 are SIO inputs. SPIOPEN() in *smart*BASIC selects SPI function and changes pin 56 and 53 to outputs (when in SPI master mode).
SIO_04/AIN2/SPI_MISO	34	I	
SIO_41/SPI_CLK	30	O	

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Signal Name	Pin No	I/O	Comments
Any_SIO/SPI_CS	54	I	SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping. On Laird devboard SIO_44 (pin54) used as SPI_CS.

5.9 I2C Interface

The I2C interface is an alternate function on SIO pins. **The ProFLEX firmware does not use the I2C interface.**

The two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master/slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

An I2C interface allows multiple masters and slaves to communicate over a shared wired-OR type bus consisting of two lines which normally sit at VDD. The SCL is the clock line which is always sourced by the master and SDA is a bi-directional data line which can be driven by any device on the bus.

IMPORTANT: You must remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.

Table 20: I2C interface

Signal Name	Pin No	I/O	Comments
SIO_26/I2C_SDA	36	I/O	This interface is an alternate function on each pin, configurable by *smart*BASIC. I2COPEN() in *smart*BASIC selects I2C function.
SIO_27/I2C_SCL	38	I/O	

5.10 General Purpose I/O, ADC, PWM, and FREQ

5.10.1 GPIO

The 19 SIO pins are configurable by *smart*BASIC application script. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5 mA or high drive 5mA)
- Internal pull-up and pull-down resistors (13 K typical) or no pull-up/down or input buffer disconnect
- Wake-up from high or low-level triggers on all pins including NFC pins

5.10.2 ADC

The ADC is an alternate function on SIO pins, configurable by *smart*BASIC. The ProFLEX firmware uses ADC to measure module supply voltage.

The LC840PA provides access to 8-channel 8/10/12-bit successive approximation ADC in one-shot mode. This enables sampling up to eight external signals through a front-end MUX. The ADC has configurable input and reference pre-scaling and sample resolution (8, 10, and 12 bit).

5.10.2.1 Analog Interface (ADC)

Table 21: Analog interface

Signal Name	Pin No	I/O	Comments
SIO_05/UART_RTS/AIN3 – Analog Input	39	I	This interface is an alternate function on each pin, configurable by *smart*BASIC. AIN configuration selected using GpioSetFunc() function. Configurable 8, 10, 12-bit resolution. Configurable voltage scaling 4, 2, 1/1, 1/3, 1/3, 1/4, 1/5, 1/6(default).
SIO_04/AIN2/SPI_MISO – Analog Input	34	I	
SIO_03/AIN1 – Analog Input	49	I	
SIO_02/AIN0 – Analog Input	50	I	
SIO_31/AIN7 – Analog Input	44	I	
SIO_30/AIN6 – Analog Input	45	I	

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Signal Name	Pin No	I/O	Comments
SIO_29/AIN5 – Analog Input	48	I	Configurable acquisition time 3uS, 5uS, 10uS(default), 15uS, 20uS, 40uS. Full scale input range (VDD)
SIO_28/AIN4 – Analog Input	46	I	

5.10.3 PWM Signal Output on up to 16 SIO Pins

The PWM output is an alternate function on ALL (GPIO) SIO pins, configurable by *smart*BASIC. **The ProFLEX firmware does not use the PWM interface.**

The **PWM output** signal has a frequency and duty cycle property. Frequency is adjustable (up to 1 MHz) and the duty cycle can be set over a range from 0% to 100%.

PWM output signal has a frequency and duty cycle property. PWM output is generated using dedicated hardware in the chipset. There is a trade-off between PWM output frequency and resolution.

For example:

- PWM output frequency of 500 kHz (2 uS) results in resolution of 1:2.
- PWM output frequency of 100 kHz (10 uS) results in resolution of 1:10.
- PWM output frequency of 10 kHz (100 uS) results in resolution of 1:100.
- PWM output frequency of 1 kHz (1000 uS) results in resolution of 1:1000.

5.10.4 FREQ Signal Output on up to 16 SIO Pins

The FREQ output is an alternate function on 16 (GPIO) SIO pins, configurable by *smart*BASIC.

Note: The frequency driving each of the 16 SIO pins is the same but the duty cycle can be independently set for each pin.

FREQ output signal frequency can be set over a range of 0 Hz to 4 MHz (with 50% mark-space ratio).

The ProFLEX firmware does not use the FREQ interface.

5.11 nRESET pin

Table 22: nRESET pin

Signal Name	Pin No	I/O	Comments
nRESET	19	I	LC840PA HW reset (active low). Pull the nRESET pin low for minimum 100mS for the LC840PA to reset.

5.12 Two-wire Interface JTAG

The LC840PA firmware hex file consists of two elements:

- ProFLEX IEEE 802.15.4:2006 Application firmware
- MCUboot Bootloader

The bootloader allows for an application firmware image to be signed and enable a more secure upgrade path for firmware. Programming the firmware must be performed using the JTAG interface.

Laird BL654PA *smart*BASIC firmware (FW) image part numbers are referenced as w.x.y.z (ex. v29.x.y.z). The BL654PA *smart*BASIC runtime engine and Softdevice combined image can be upgraded by the customer over the UART interface.

You also have the option to use the two-wire (JTAG) interface, during production, to clone the file system of a Golden preconfigured LC840PA to others using the Flash Cloning process. This is described in the following application note *Flash Cloning for the LC840PA*. In this case, the file system is also part of the .hex file.

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Signal Name	Pin No	I/O	Comments
SWDIO	1	I/O	Internal pull-up resistor
SWDCLK	3	I	Internal pull-down resistor

The Laird development board incorporates an on-board JTAG J-link programmer for this purpose. There is also the following JTAG connector which allows on-board JTAG J-link programmer signals to be routed off the development board. The only requirement is that you should use the following JTAG connector on the host PCB.

The JTAG connector MPN is as follows:

Reference	Part	Description and MPN (Manufacturers Part Number)
JP1	FTSH-105	Header, 1.27mm, SMD, 10-way, FTSH-105-01-L-DV Samtech

Note: Reference on the BL654PAdevelopment board schematic (Figure 7) shows the DVK development schematic wiring only for the JTAG connector and the BL654PA (LC840PA) module JTAG pins.

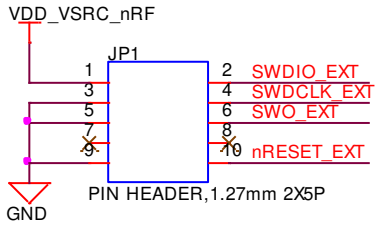

Figure 7:BL654PA development board schematic

Note: The BL654PA development board allows Laird on-board JTAG J-link programmer signals to be routed off the development board by from connector JP1

JTAG is require because Nordic SDK application and the ProFLEX application can only be loaded using the JTAG (*smart*BASIC firmware can be loaded using JTAG as well as over the UART). We recommend that you use JTAG (2-wire SWD interface) to handle future LC840PA module firmware upgrades. You **must** wire out the JTAG (2-wire SWD interface) on your host design (see Figure 7, where the following four lines should be wired out – SWDIO, SWDCLK, GND and VCC). *smart*BASIC firmware upgrades can still be performed over the LC840PA UART interface, but this is slower than using the LC840PA JTAG (2-wire SWD interface) – (60 seconds using UART vs. 10 seconds when using JTAG).

SWO (SIO_32) is a Trace output (called SWO, Serial Wire Output) and is not necessary for programming LC840PA over the SWD interface.

nRESET_BLE is not necessary for programming LC840PA over the SWD interface.

5.13 LC840PA Wakeup

5.13.1 Waking Up LC840PA from Host

In Bluetooth LE mode, you may configure the LC840PA's wakeup pins via *smart*BASIC to do any of the following:

- Wake up when signal is low
- Wake up when signal is high
- Wake up when signal changes

Refer to the *smart*BASIC user guide for details. You can access this guide from the Laird BL654PA product page.

When running the ProFLEX firmware, wake the LC840PA from the host using the WAKE pin. The pin is active low with internal pull-up. A pulse of 20uS or greater will wake the module when in sleep mode.

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5.13.2 Low Power Modes

The LC840PA has three power modes: Run, Standby Doze (System ON Idle), and Deep Sleep (System OFF).

The module is placed automatically in Standby Doze if there are no pending events (when WAITEVENT statement is encountered within a customer's *smart*BASIC script). The module wakes from Standby Doze via any interrupt (such as a received character on the UART Rx line). If the module receives a UART character from either the external UART or the radio, it wakes up.

Deep sleep is the lowest power mode. Once awakened, the system goes through a system reset. When running ProFLEX firmware, the module will restore saved NVM settings to internal registers after any reset.

5.14 Temperature Sensor

The on-silicon temperature sensor has a temperature range greater than or equal to the operating temperature of the device. Resolution is 0.25°C degrees. The on-silicon temperature sensor accuracy is ±5°C.

To read temperature from on-silicon temperature sensor (in tenth of centigrade, so 23.4°C is output as 234) using *smart*BASIC:

- In command mode, use **ATI2024**
  or
- From running a *smart*BASIC application script, use **SYSINFO(2024)**

The ProFLEX firmware does not use the temperature sensor.

5.15 Security/Privacy

The ProFLEX firmware uses the security and privacy functions to provide security functionally as described in the Host Interface Document.

5.15.1 Random Number Generator

Exposed via an API in *smart*BASIC (see *smart*BASIC documentation available from the LC840PA product page). The **rand()** function from a running *smart*BASIC application returns a value.

5.15.2 AES Encryption/Decryption

Exposed via an API in *smart*BASIC (see *smart*BASIC documentation available from the LC840PA product page). Function called **aesencrypt** and **aesdecrypt**.

5.15.3 ARM Cryptocell

ARM Cryptocell incorporates a true random generator (TRNG) and support for a wide range of asymmetric, symmetric and hashing cryptographic services for secure applications. For more information, please check the Nordic SDK.

5.15.4 Readback Protection

The LC840PA supports readback protection capability that disallows the reading of the memory on the nrf52840 using a JTAG interface. Available via *smart*BASIC

5.15.5 Elliptic Curve Cryptography

The LC840PA offers a range of functions for generating public/private keypair, calculating a shared secret, as well as generating an authenticated hash. Available via *smart*BASIC

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5.16 External 32.768 kHz Crystal

This is not required for normal BL654PA module operation. **The ProFLEX firmware requires the external 32.768kHz crystal to enable high baud rate communications and ensure lowest power operation in sleep mode.**

The LC840PA uses the on-chip 32.76 kHz RC oscillator (LFCLK) by default (which has an accuracy of ±500 ppm) which requires regulator calibration (every eight seconds) to within ±500 ppm. This is insufficient for ProFLEX operation.

An external high accuracy (±20 ppm) 32.768 kHz crystal (and associated load capacitors) must be connected to the LC840PASIO_01/XL2 (pin 41) and SIO_00/XL1 (pin 42) to provide improved protocol timing and to help with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the RX window needs to be open. Table 23 compares the current consumption difference between RC and crystal oscillator.

Table 23: Comparing current consumption difference between LC840PA on-chip RC 32.76 kHz oscillator and optional external crystal (32.768kHz) based oscillator

	LC840PA On-chip 32.768 kHz RC Oscillator (±500 ppm) LFRC	Optional External Higher Accuracy (±20 ppm) 32.768 kHz Crystal-based Oscillator LFXO
Current Consumption of 32.768 kHz Block	0.7 uA	0.23 uA
Standby Doze Current (SYSTEM ON IDLE +full RAM retention +RTC run current + LFRC or LFXO)	3.1 uA	2.6 uA
Calibration	Calibration required regularly (default eight seconds interval). Calibration takes 33 ms; with DCDC used, the total charge of a calibration event is 16 uC. The average current consumed by the calibration depends on the calibration interval and can be calculated using the following formula: **CAL_charge/CAL_interval –** The lowest calibration interval (0.25 seconds) provides an average current of (DCDC enabled): **16uC/0.25s = 64uA** To get the 500-ppm accuracy, the Bluetooth LE stack specification states that a calibration interval of eight seconds is enough. This gives an average current of: **16uC/8s = 2 uA** Added to the LFRC run current and Standby Doze (IDLE) base current shown above results in a total average current of: **LFRC + CAL = 3.1 + 2 = 5.1 uA**	Not applicable
Total	5.1 uA	2.6 uA
Summary	▪ Low current consumption ▪ Accuracy 500 ppm	▪ Lowest current consumption ▪ Needs external crystal ▪ High accuracy (depends on the crystal, usually 20 ppm)

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Table 24: Optional external 32.768 kHz crystal specification

Optional external 32.768kHz crystal	Min	Typ	Max
Crystal Frequency	-	32.768 kHz	-
Frequency tolerance requirement of Bluetooth LE stack	-	-	±500 ppm
Load Capacitance	-	-	12.5 pF
Shunt Capacitance	-	-	2 pF
Equivalent series resistance	-	-	100 kOhm
Drive level	-	-	1 uW
Input capacitance on XL1 and XL2 pads	-	4 pF	-
Run current for 32.768 kHz crystal based oscillator	-	0.23 uA	-
Start-up time for 32.768 kHz crystal based oscillator	-	0.25 seconds	-
Peak to peak amplitude for external low swing clock input signal must not be outside supply rails	200 mV	-	1000 mV

Be sure to tune the load capacitors on the board design to optimize frequency accuracy (at room temperature) so it matches that of the same crystal standalone, Drive Level (so crystal operated within safe limits) and oscillation margin (R_{neg} is at least 3 to 5 times ESR) over the operating temperature range.

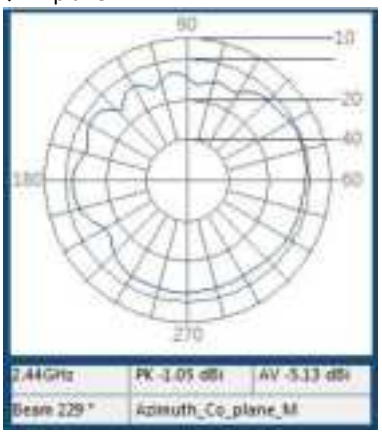
5.17 453-00087 On-board PCB Antenna Characteristics

The 453-00087 on-board PCB trace monopole antenna radiated performance depends on the host PCB layout.

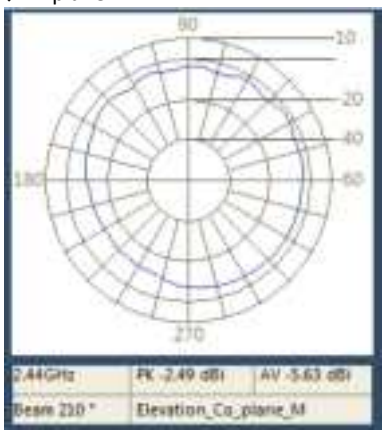
The BL654PA development board was used for LC840PA development and the 453-00087 PCB antenna performance evaluation. To obtain similar performance, follow guidelines in section *PCB Layout on Host PCB for the 453-00087* to allow the on-board PCB antenna to radiate and reduce proximity effects due to nearby host PCB GND copper or metal covers.

Unit in dBi @2440MHz	XY-plane		XZ-plane		YZ-plane	
	Peak	Avg	Peak	Avg	Peak	Avg
453-00087 PCB trace antenna	-1.05	-5.13	-1.51	-7.43	-2.49	-5.63

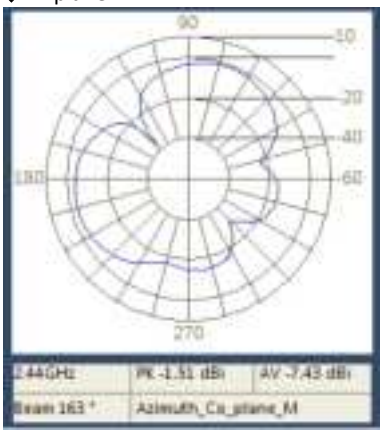
◆XY-plane



◆XZ-plane



◆YZ-plane



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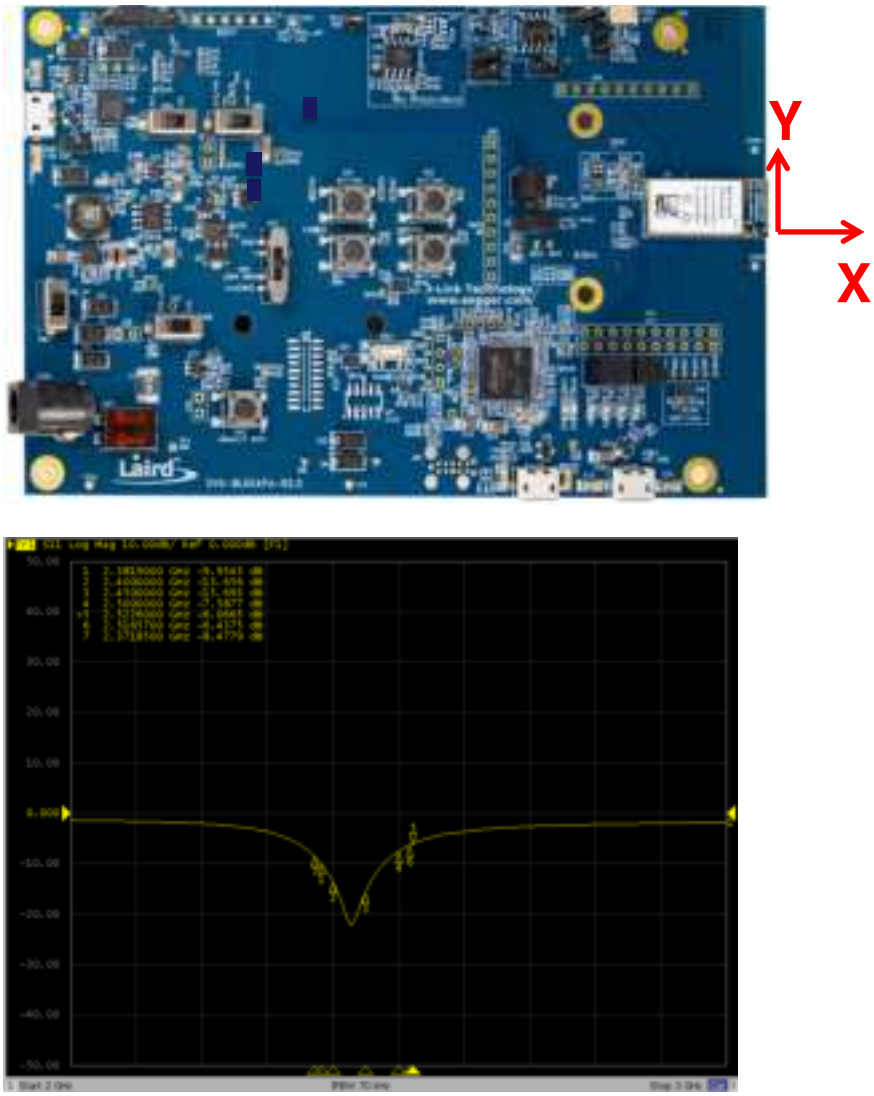

Figure 8: 453-00087 on-board PCB antenna performance (Antenna Gain and S11 – whilst 453-00087 module sitting on Devboard 455-00022)

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6 HARDWARE INTEGRATION SUGGESTIONS

6.1 Circuit

The LC840PA is easy to integrate, requiring no external components on your board apart from those which you require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **LC840PA power supply options:**

  Option 1 – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDDH pins (so that VDD equals VDD_HV). Connect external supply within range 3.0V to 3.6V range to LC840PA VDD and VDD_HV pins.

  OR

  Option 2 – High voltage mode power supply mode (using LC840PA VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDDH pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 3.0V to 5.5V range to LC840PA VDD_HV pin. LC840PA VDD pin left unconnected.

  For either option, if you use USB interface then the LC840PA VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the LC840PA VBUS pin, you MUST externally fit a 4.7uF to ground.

  External power source should be within the operating range, rise time and noise/ripple specification of the LC840PA. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within LC840PA module incorporates brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.

- **VDD and coin-cell operation**
  With a built-in DCDC (operating range 3.0V to 3.6V) that reduces the peak current required from a coin cell battery, making it easier to use with a coin cell. The coin cell battery MUST be able to service the peak and average current requirements of the customer application.
- **AIN (ADC) and SIO pin IO voltage levels**
  LC840PA SIO voltage levels are at VDD. Ensure input voltage levels into SIO pins are at VDD also (if VDD source is a battery whose voltage will drop). Ensure ADC pin maximum input voltage for damage is not violated.
- **AIN (ADC) impedance and external voltage divider setup**
  If you need to measure with ADC a voltage higher than 3.6V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.
- **JTAG**
  This is REQUIRED as Nordic SDK applications can only be loaded using the JTAG (*smart*BASIC firmware can be loaded using the JTAG as well as the UART).
  Laird recommends you use JTAG (2-wire interface) to handle future LC840PA module firmware upgrades. You MUST wire out the JTAG (2-wire interface) on your host design (see Figure 7, where four lines should be wired out, namely SWDIO, SWDCLK, GND and VCC). Firmware upgrades can still be performed over the LC840PA UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the LC840PA JTAG (2-wire interface).
  JTAG may be used if you intend to use Flash Cloning during production to load *smart*BASIC scripts.
- **UART**
  Required for loading your *smart*BASIC application script during development (or for subsequent firmware upgrades (except JTAG for FW upgrades and/or Flash Cloning of the *smart*BASIC application script). Add connector to allow interfacing with UART via PC (UART–RS232 or UART-USB). **UART is required for IEEE802.15.4 ProFLEX application for host interface and optional debug interface.**
- **UART_RX and UART_CTS**
  SIO_08 (alternative function UART_RX) is an input, set with internal weak pull-up (in firmware). The pull-up prevents the module from going into deep sleep when UART_RX line is idling.
  SIO_07 (alternative function UART_CTS) is an input, set with internal weak pull-down (in firmware). This pull-down ensures the default state of the UART_CTS will be asserted which means can send data out of the UART_TX line. Laird recommends that UART_CTS be connected.
- **nAutoRUN pin and operating mode selection (smartBASIC only)**
  nAutoRUN pin needs to be externally held high or low to select between the two LC840PA operating modes at power-up:
  – Self-contained Run mode (nAutoRUN pin held at 0V).

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  - Interactive / development mode (nAutoRUN pin held at VDD).
    Make provision to allow operation in the required mode. Add jumper to allow nAutoRUN pin to be held high or low (LC840PA has internal 13K pull-down by default) OR driven by host GPIO.

- **I2C**
  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the LC840PA module and MUST be provided external to the module as per I2C standard if I2C is utilized..
- **SPI**
  Implement SPI chip select using any unused SIO pin within your *smart*BASIC application script or Nordic application then SPI_CS is controlled from the software application allowing multi-dropping.
- **SIO pin direction**
  LC840PA modules shipped from production with *smart*BASIC FW, all SIO pins (with default function of DIO) are mostly digital inputs (see Pin Definitions Table2). Remember to change the direction SIO pin (in your *smart*BASIC application script) if that particular pin is wired to a device that expects to be driven by the LC840PA SIO pin configured as an output. Also, these SIO pins have the internal pull-up or pull-down resistor-enabled by default in firmware (see Pin Definitions Table 2). This was done to avoid floating inputs, which can cause current consumption in low power modes (e.g. StandbyDoze) to drift with time. You can disable the PULL-UP or Pull-down through their *smart*BASIC application.

  Note: Internal pull-up, pull down will take current from VDD.

- **SIO_02 pin** and OTA *smart*BASIC application download feature

  SIO_02 is an input, set with internal pull-down (in FW). Refer to latest firmware release documentation on how SIO_02 is used for Over the Air *smart*BASIC application download feature. The SIO_02 pin must be pulled high externally to enable the feature. Decide if this feature is required in production. When SIO_02 is high, ensure nAutoRun is NOT high at same time; otherwise you cannot load the *smart*BASIC application script.

- **NFC antenna connector**
  To make use of the Laird flexi-PCB NFC antenna, fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810594

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.
- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VCC pins.
- **External 32.768kHz crystal**
  A crystal that meets specification should be used. The capacitance value of added load capacitors should be tuned to meet all specifications for frequency and oscillation margin.
- **SIO_38 special function pin**
  This is for future use by Laird. It is currently a Do Not Connect pin if using the *smart*BASIC FW.
- **LC840PA pin2 and pin4 are Do No Connect pins (on BL654 SIO_34 and SIO_36)**
  Customer MUST NOT connect anything to LC840PA pin2 and pin4 which are Do No connect pins.
- **LC840PA pin16 (WAKE) (active low)**
  Wake module from sleep in IEEE 802.15.4 ProFLEX application. Signal is active LOW (internal pull-up) and requires a minimum 20uS pulse to awaken a sleeping module.
- **LC840PA pins 18, 20, 21 and 22 (LED1 – LED4)**
  In IEEE 802.15.4 ProFLEX application, LEDs provide status for heartbeat (module operating), RF packet Tx and RF packet Rx events. This pins may be connected to LEDs, connected to Host for status information, or remain unconnected.

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6.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate LC840PA module close to the edge of PCB (mandatory for the 453-00087 for on-board PCB trace antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD, VDDH, VBUS supply and AIN (analogue) and SIO (digital) traces. LC840PA pin 2 and 4 (SIO_34 and SIO_36) which are Do No Connect pins are especially important.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of LC840PA development board).

6.3 PCB Layout on Host PCB for the 453-00087 w/integrated PCB trace antenna

6.3.1 Antenna Keep-out on Host PCB

The 453-00087 has an integrated PCB trace antenna and its performance is sensitive to host PCB. It is critical to locate the 453-00087 on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section ***PCB land pattern and antenna keep-out area for the 453-00087***. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00087 module on the edge of the host PCB, preferably in the edge center.
- The LC840PA development board has the 453-00087 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the LC840PA development board which was used for module development and antenna performance evaluation is shown in Figure 9, where the antenna keep-out area is ~5 mm wide, ~39.95 mm long; with PCB dielectric (no copper) height ~1 mm sitting under the 453-00087 PCB trace antenna.
- The 453-00087 PCB trace antenna is tuned when the 453-00087 is sitting on development board (host PCB) with size of 132 mm x 85 mm x 1mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in the Host PCB Land Pattern and Antenna Keep-out for the 453-00087 section.
- Host PCB land pattern and antenna keep-out for the LC840PA applies when the 453-00087 is placed in the edge of the host PCB preferably in the edge center. Figure 9 shows an example.

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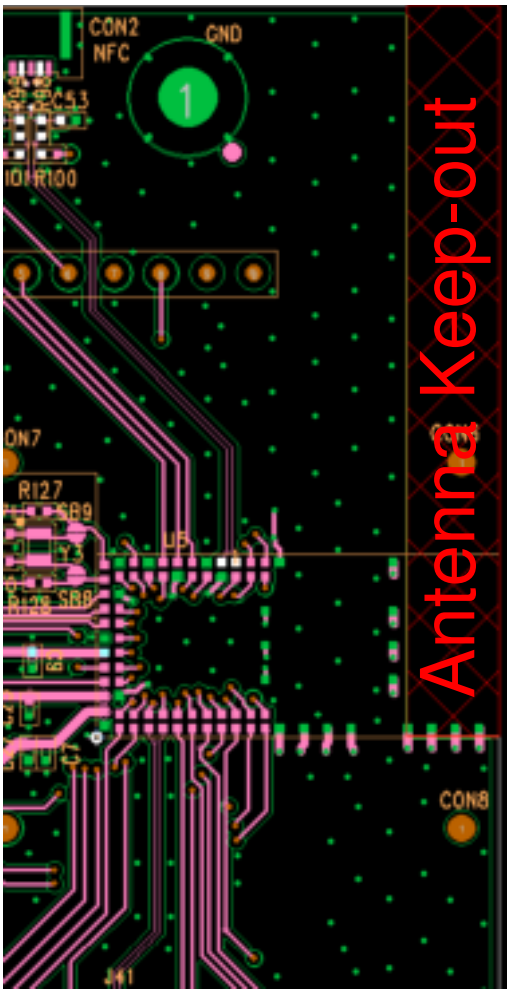

Figure 9: PCB trace Antenna keep-out area (shown in red), corner of the LC840PA development board for the 453-00087 module.

Antenna Keep-out Notes:

Note 1	The LC840PA module is placed on the edge, preferably edge centre of the host PCB.
Note 2	Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00087 on host PCB.

6.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00087 PCB trace monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic).

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6.4 External Antenna Integration with the 453-00088

Please refer to the regulatory sections for FCC, ISED for details of use of LC840PA-with external antennas in each regulatory region.

The LC840PA family has been designed to operate with the below external antennas (with a maximum gain of 2.0 dBi). The required antenna impedance is 50 ohms. See Table 25. External antennas improve radiation efficiency.

Table 25: External antennas for the LC840PA

Manufacturer	Model	Laird Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Laird	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Laird	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Laird	2.4 GHz dipole	001-0001	Dipole	RP-SMA male	2 dBi	-
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2 dBi	-
Laird	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBI
Laird	Laird NFC	0600-00061	NFC	N/A	-	-
Laird	LC840PA PCB printed antenna	NA	Printed PCB	N/A	0 dBi	-

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7 MECHANICAL DETAILS

7.1 LC840PA Mechanical Details

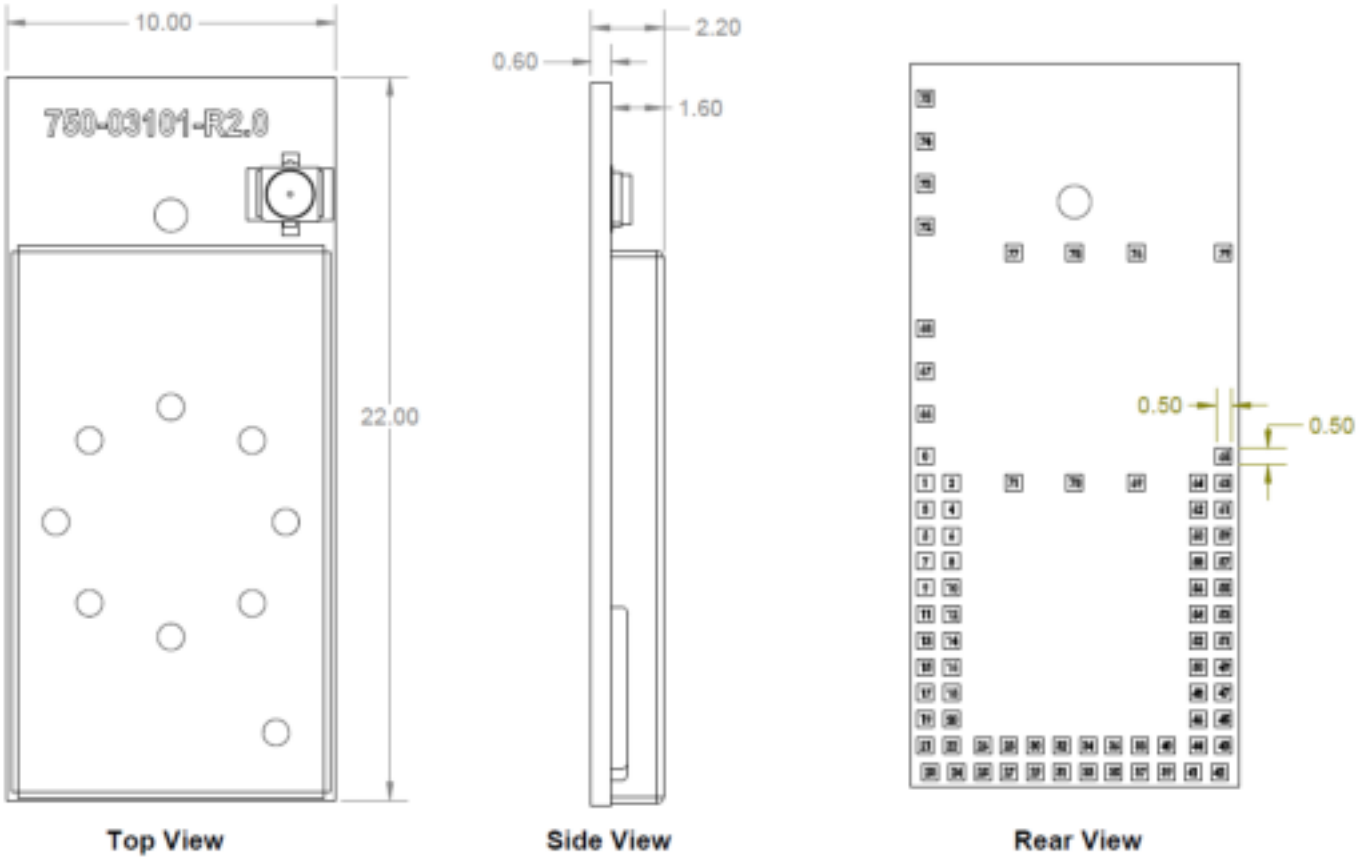

Figure 10: LC840PA mechanical drawings

Development Kit Schematics for the LC840PA can be found in the software downloads tab of the BL654PA product page: https://www.lairdconnect.com/bl654-pa

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7.2 Host PCB Land Pattern and Antenna Keep-Out for the 453-00087

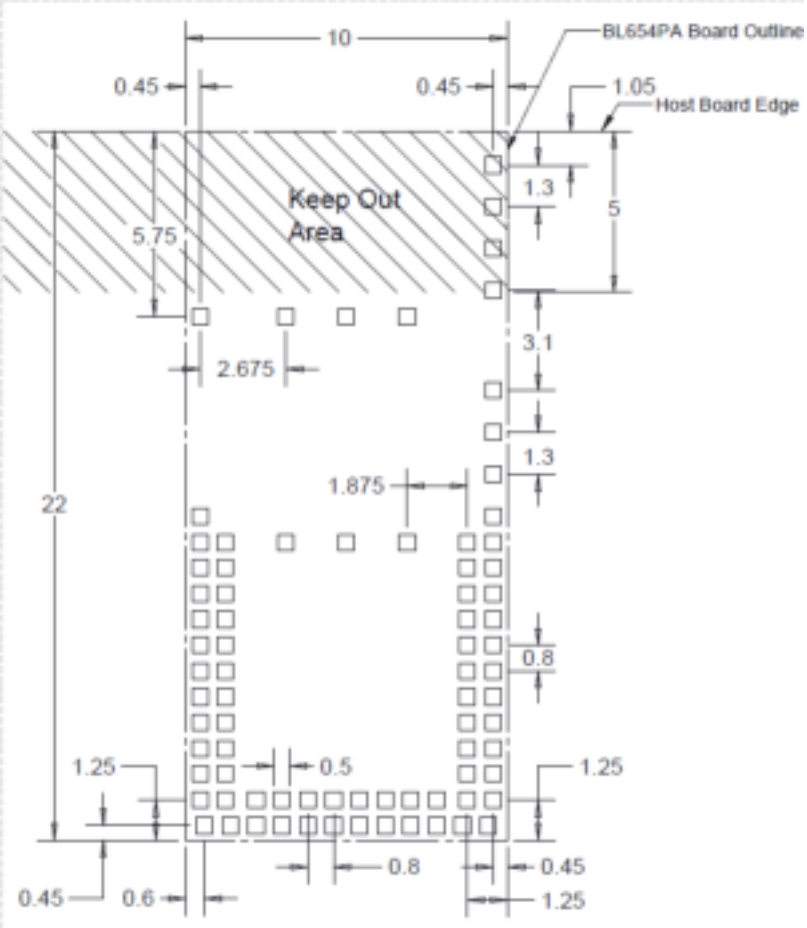

Figure 11: Land pattern and Keep-out for the 453-00087

All dimensions are in mm.

Host PCB Land Pattern and Antenna Keep-out for the 453-00087 Notes:

Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 6.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board antenna performance, the module 453-00087 MUST be placed on the edge of the host PCB and preferably in the edge centre and host PCB, the antenna "Keep Out Area" is extended (see Note 4).
Note 3	LC840PA development board has the 453-00087 placed on the edge of the PCB board (and not in corner) for that the Antenna keep out area is extended down to the corner of the development board, see section *PCB Layout on Host PCB for the 453-00087*, Figure 11. This was used for module development and antenna performance evaluation.
Note 4	Ensure that there is no exposed copper under the module on the host PCB.
Note 5	You may modify the PCB land pattern dimensions based on their experience and/or process capability.

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8 Application Note for Surface Mount Modules

8.1 Introduction

Laird Technologies surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the User Manual. This Application Note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

8.2 Shipping

8.2.1 Tape and Reel Package Information

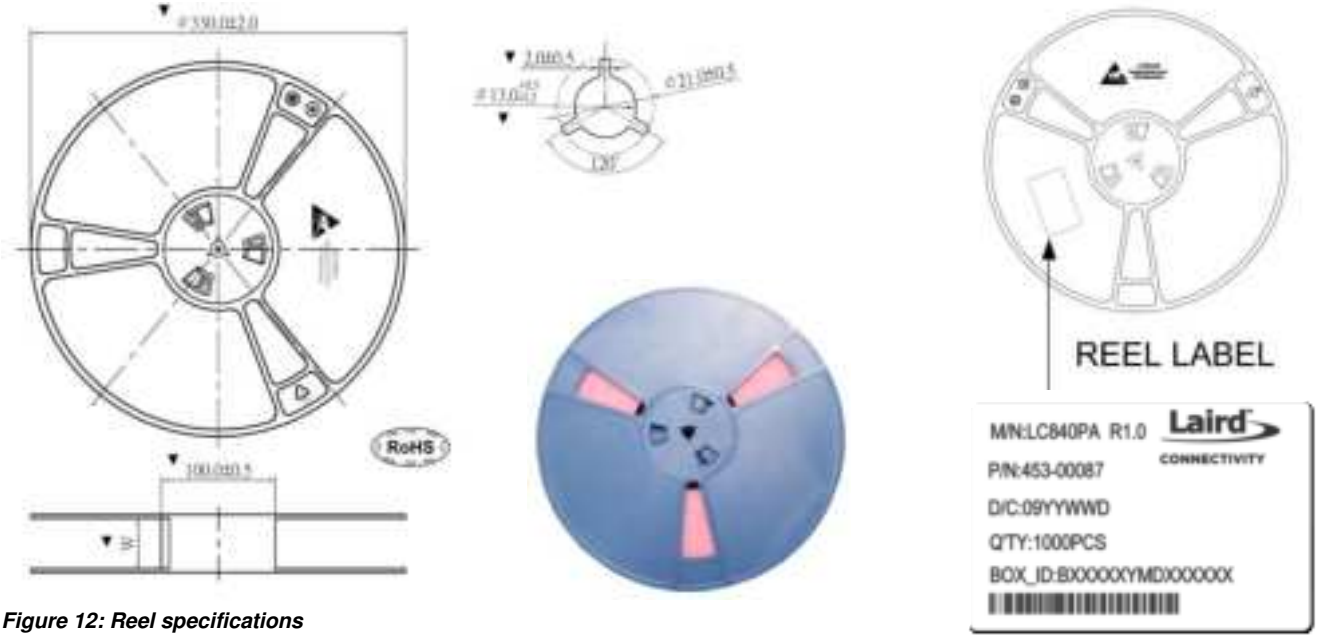

Figure 12: Reel specifications

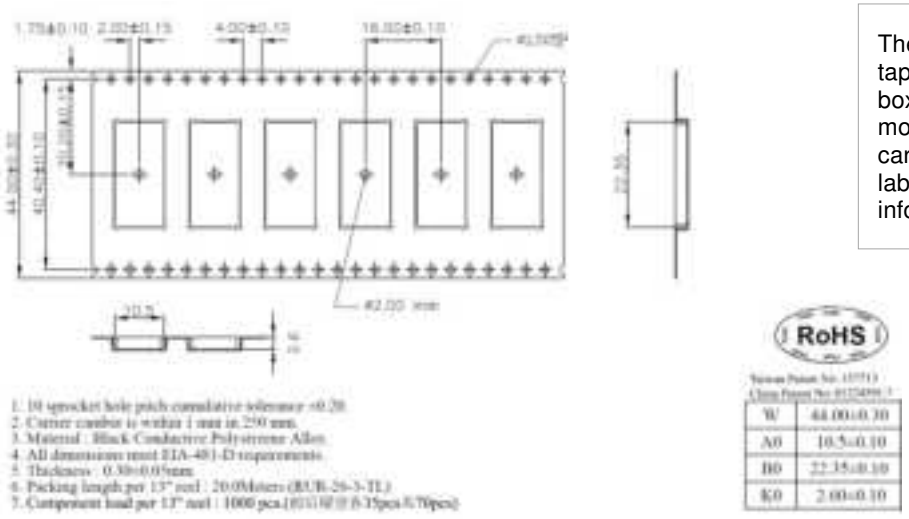

Figure 13: Tape specifications

There are 1,000 x LC840PA modules taped in a reel (and packaged in a pizza box) and five boxes per carton (5000 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels. See Carton Contents for more information.

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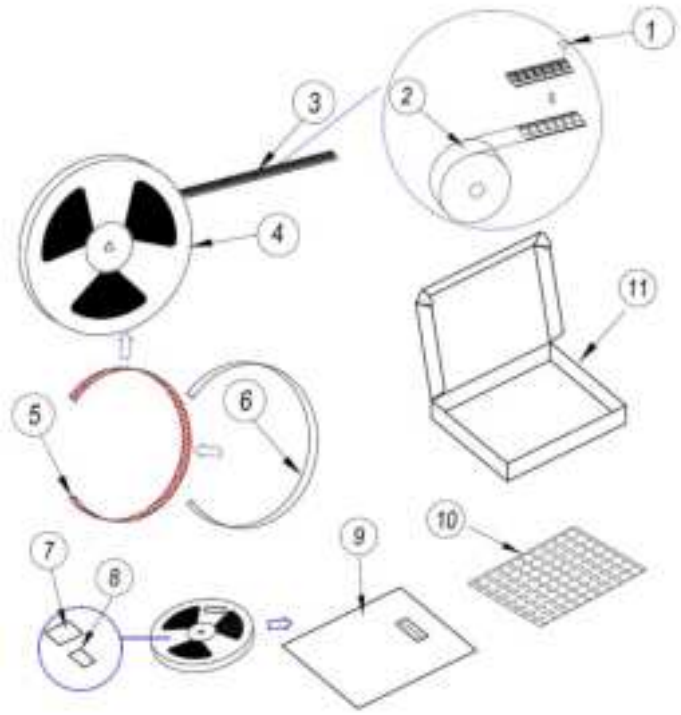
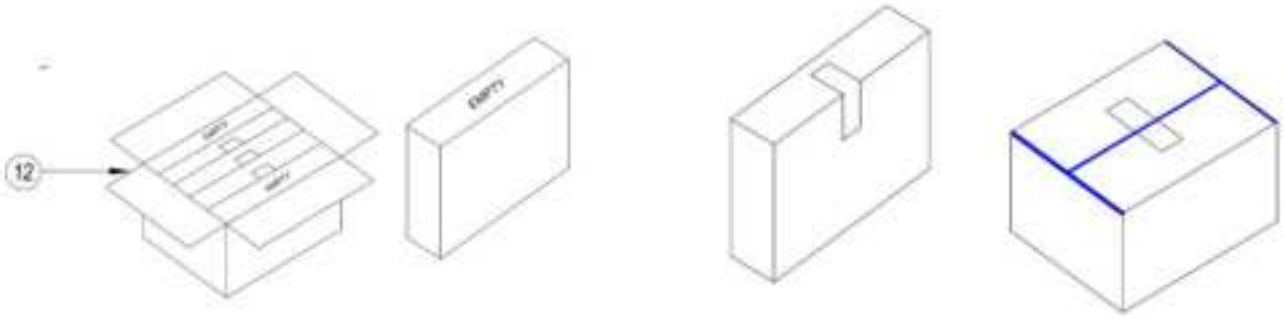
8.2.2 Carton Contents

The following are the contents of the carton shipped for the LC840PA modules.



#	Item	Qty	#	Item	Qty
1	Module	1	7	Drier (60 g)	1/1000
2	Cover Tape	(1/1000)*20m	8	Humidity Card	1/1000
3	Carrier Tape	(1/1000)*20m	9	Bag	1/1000
4	Reel	1/box 5/carton	10	Bubble Cloth	1/1000
5	Foam Belt	1/1000	11	Box	1/1000 5/carton
6	Protective Band	1/1000	12	Carton	1/1000



8.2.3 Labeling

The following labels are included in each shipment.

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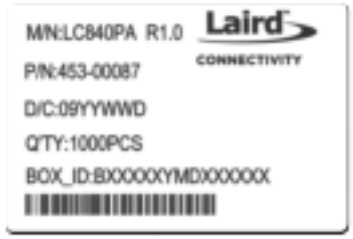

Figure 14: Reel/bag/box label

Figure 15: Carton label

Figure 16: MSL label

8.3 Reflow Parameters

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to *bake units* on the card, see Table 26 and follow instructions specified by IPC/JEDEC J-STD-033. A copy of this standard is available from the JEDEC website: http://www.jedec.org/sites/default/files/docs/jstd033b01.pdf

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) four devices is 72 hours in ambient environment ≤30°C/60%RH.

Table 26: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
4	11 hours	7 hours	37 hours	23 hours	15 days	9 days

Laird surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Laird surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds. In addition, we recommend that the LC840PA module **does not** go through the reflow process more than one time; otherwise the LC840PA internal component soldering may be impacted.

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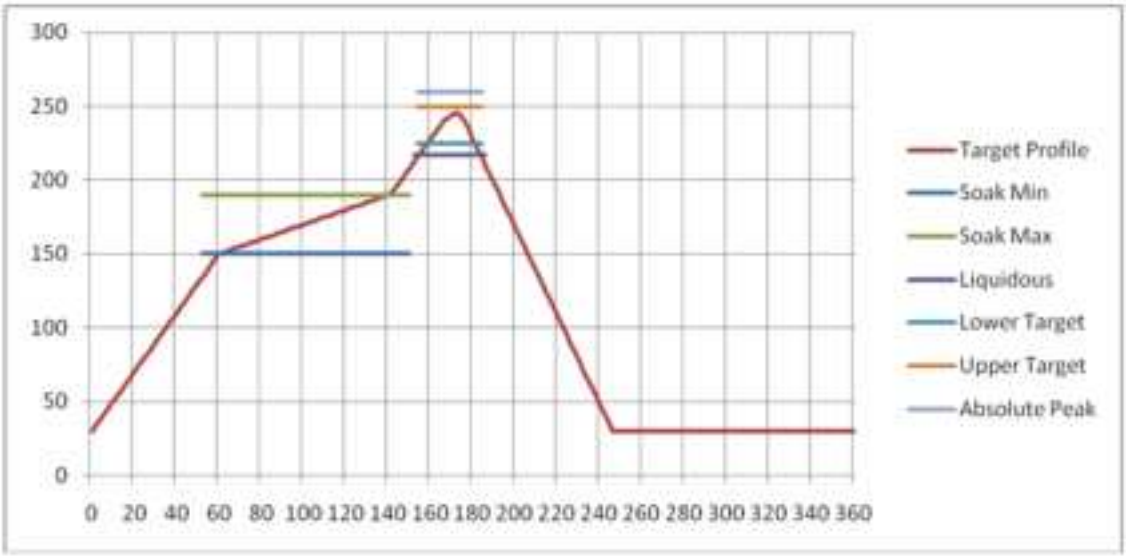

Figure 17: Recommended reflow temperature

Temperatures should not exceed the minimums or maximums presented in Table 27.

Table 27: Recommended maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

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9 REGULATORY INFORMATION

Note: For complete regulatory information, refer to the LC840PA Regulatory Information document.

The LC840PA holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-LC840PA
Canada (ISED)	3147A-LC840PA

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10 Ordering Information

Part Number	Product Description
453-00087	LC840PA ProFLEX compatible PA module – Integrated antenna
453-00088	LC840PA ProFLEX compatible PA module – External antenna
455-00022	Development Kit for 453-00087 module – Integrated antenna
455-00023	Development Kit for the 453-00088 module – External antenna
453-00087R	LC840PA ProFLEX compatible PA module – Integrated antenna T/R
453-00088R	LC840PA ProFLEX compatible PA module – External antenna T/R

11 Bluetooth SIG Qualification

Bluetooth SIG qualification is available for the BL654PA only, not the LC840PA.

11.1 Overview

The BL654PA module is listed on the Bluetooth SIG website as a qualified End Product.

Note: The LC840PA is included under the BL654 listing.

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
BL654PA	Laird	D040166	114304	https://launchstudio.bluetooth.com/ListingDetails/63185
BL654PA	Laird	D041400	117615	https://launchstudio.bluetooth.com/ListingDetails/67595
BL654PA	Laird	D049255	145177	https://launchstudio.bluetooth.com/ListingDetails/102275

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to registered as a member of the Bluetooth SIG – www.bluetooth.org

The following link provides a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document:

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

11.2 Qualification Steps When Referencing a Laird End Product Design

To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

In step 1, select the option, **Reference a Qualified Design** and enter D040166, D041400, or D049255 in the End Product table entry. You can then select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page, (please note that unless the Declaration ID is pre-paid or purchased with a credit card, it will not be possible to proceed until the SIG invoice is paid.

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Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document. Your new Design will be listed on the SIG website and you can print your Certificate and Declaration of Conformity.

For further information, please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

Note: If using the BL654PA with Laird Firmware and *smart*BASIC script, you can skip "Controller Subsystem", "Host Subsystem", and "Profile Subsystem".

11.3 Qualification Steps When Deviating from a Laird End Product Design

If you wish to deviate from the standard End Product design listed under D040166, D041400 or D049255, the qualification process follows the Traditional Project route, creating a new design. When creating a new design, it is necessary to complete the full qualification listing process and also maintain a compliance folder for the new design.

The BL654PA design under D040166 incorporates the following components:

Listing reference	Design Name	Core Spec Version
D038622	S140 Host v6.0.0	5.0
D038623	S140 Link layer v6.0.0	5.0

The BL654PA design under D041400 incorporates the following components:

Listing reference	Design Name	Core Spec Version
D039780	S140 Host v6.1.0	5.0
D040756	S140 Link layer v6.1.0x	5.0

The BL654PA design under D049255 incorporates the following components:

Listing reference	Design Name	Core Spec Version
D043345	S140 SoftDevice Link Layer v7.0.1	5.1
D043346	S140 Host Layer v7.0.1	5.1

of these components and it is possible to use them in your new design. Please check with Nordic to make sure these software components are compatible with the nRF52 hardware.

If your design is based on un-modified BL654PA hardware it is possible use the following process:

1. Reference the existing RF-PHY test report from the BL654PA listing.
2. Combine the relevant Nordic Link Layer (LL) – check QDID with Nordic.
3. Combine in a Host Component (covering L2CAP, GAP, ATT, GATT, SM) - check QDID with Nordic.
4. Test any standard SIG profiles that are supported in the design (customs profiles are exempt).

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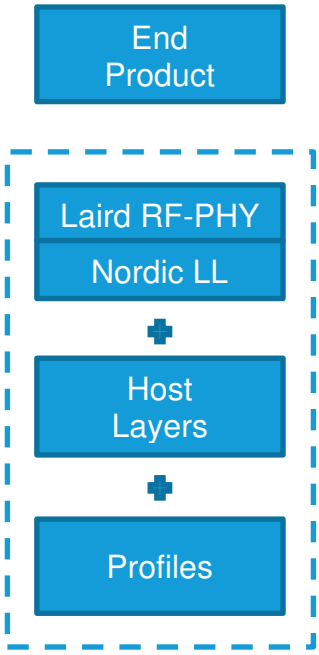

Figure 18: Scope of the qualification for an End Product Design

The first step is to generate a project on the TPG (Test Plan Generator) system. This determines which test cases apply to demonstrate compliance with the Bluetooth Test Specifications. If you are combining pre-tested and qualified components in your design and they are within their three-year listing period, you are not required to re-test those layers covered by these components.

If the design incorporates any standard SIG LE profiles (such as Heart Rate Profile), it is necessary to test these profiles using PTS or other tools where permitted; the results are added to the compliance folder.

You are required to upload your test declaration and test reports (where applicable) and then complete the final listing steps on the SIG website. Remember to purchase your Declaration ID before you start the qualification process, as it's impossible to complete the listing without it.

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12 Reliability Tests

The LC840PA module went through the below reliability tests and passed.

Test Sequence	Test Item	Test Limits and Pass	Test Conditions
1	Vibration Test	JESD22-B103B Vibration, Variable frequency	**Sample:** Unpowered **Sample number:** 3 **Vibration waveform:** Sine waveform **Vibration frequency /Displacement:** 20 to 80 Hz /1.52 mm **Vibration frequency /Acceleration:** 80 to 2000 Hz/20 g **Cycle time:** 4 minutes **Number of cycles:** 4 cycles for each axis **Vibration axis:** X, Y and Z (Rotating each axis on vertical vibration table).
2	Mechanical Shock	JESD22-B104C	**Sample:** Unpowered **Sample number:** 3 **Pulse shape:** Half-sine waveform **Impact acceleration:** 1500 g **Pulse duration:** 0.5 ms **Number of shocks:** 30 shocks (5 shocks for each face) **Orientation:** Bottom, top, left, right, front and rear faces
3	Thermal Shock	JESD22-A104E Temperature cycling	**Sample:** Unpowered **Sample number**: 3 **Temperature transition time**: Less than 30 seconds **Temperature cycle:** -40℃ (10 minutes), +85℃ (10 minutes) **Number of cycles:** 350

Before and after the testing, visual inspection showed no physical defect on samples.

After Vibration test and Mechanical Shock testing, the samples were functionally tested, and all samples functioned as normal. After the thermal shock test, the samples were functionally tested, and all samples functioned as normal.

13 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

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Note: Information contained in this document is subject to change.