Tune up procedure

1、Max TX Power

band	Mode	Frequency(MHz)	Subtest	Modulation	Power(dBm)
WCDMA B5	RMC	/	/	QPSK	25±1
	HSDPA	/	1	QPSK	24±1
		/	2	QPSK	22±1
		/	3	QPSK	21±1
		/	4	QPSK	21±1
	HSUPA	826.4	1	QPSK/16QAM	21.5±1
		826.4	2	QPSK/16QAM	23±1
		826.4	3	QPSK/16QAM	20±1
		826.4	4	QPSK/16QAM	24±1
		826.4	5	QPSK/16QAM	21±1
		836.6	1	QPSK/16QAM	23±1
		836.6	2	QPSK/16QAM	23±1
		836.6	3	QPSK/16QAM	21±1
		836.6	4	QPSK/16QAM	24±1
		836.6	5	QPSK/16QAM	22±1
		846.6	1	QPSK/16QAM	23±1
		846.6	2	QPSK/16QAM	23±1
		846.6	3	QPSK/16QAM	22±1
		846.6	4	QPSK/16QAM	24±1
		846.6	5	QPSK/16QAM	22±1

band	Bandwidth	Frequency(MHz)	Modulation	Power(dBm)
LTE B4	1.4MHz	1710.7	QPSK	25.3±1
	1.4MHz	1710.7	16QAM	24±1
	1.4MHz	1732.5	QPSK	24.5±1
	1.4MHz	1732.5	16QAM	23.5±1
	1.4MHz	1754.3	QPSK	25.5±1
	1.4MHz	1754.3	16QAM	24.5±1
	3MHz	1711.5	QPSK	25.3±1
	3MHz	1711.5	16QAM	24.2±1
	3MHz	1732.5	QPSK	24±1
	3MHz	1732.5	16QAM	24.5±1
	3MHz	1753.5	QPSK	25.5±1
	3MHz	1753.5	16QAM	24.5±1
	5MHz	1712.5	QPSK	25.5±1
	5MHz	1712.5	16QAM	25±1

	5MHz	1732.5	QPSK	24.5±1
	5MHz	1732.5	16QAM	23.5±1
	5MHz	1752.5	QPSK	25.5±1
	5MHz	1752.5	16QAM	24±1
	10MHz	1715	QPSK	25.5±1
	10MHz	1715	16QAM	24.5±1
	10MHz	1732.5	QPSK	24.61±1
	10MHz	1732.5	16QAM	23.6±1
	10MHz	1750	QPSK	25±1
	10MHz	1750	16QAM	24±1
	15MHz	1717.5	QPSK	25±1
	15MHz	1717.5	16QAM	24±1
	15MHz	1732.5	QPSK	24.9±1
	15MHz	1732.5	16QAM	22.9±1
	15MHz	1747.5	QPSK	25.2±1
	15MHz	1747.5	16QAM	24.2±1
	20MHz	1720	QPSK	25.2±1
	20MHz	1720	16QAM	24.2±1
	20MHz	1732.5	QPSK	24.5±1 (1RB)
	20MHz	1732.5	QPSK	24±1 (100%RB)
	20MHz	1732.5	16QAM	23.87±1
	20MHz	1745	QPSK	25.2±1
	20MHz	1745	16QAM	24.2±1

2、 Antenna Gain

Tecknology/Band	Gain
FDD-LTE Band4	6dBi
WCDMA B5	6dBi

3、Power on/off and reset interface

/3.1 Pin Description

When the VBAT is in normal state(3.4<VBAT<4.2), the Module will be powered on by the following two ways:

- Pulling the PWRKEY low more than 0.5s, then release

- Pulling the EXTON1N low

Any of the above events will trigger system power on.

There are two ways to reset the module. Pulling the PWRKEY long time, will reboot the PMIC, PMIC powered on will reboot the CPU;

- Pulling the PWRKEY long time, will reboot the PMIC, PMIC powered on will reboot the

CPU

- Pulling the RESET, will reboot the CPU

Interface definitions are shown in the following table:
Table 1 boot and reset key interface definitions

Pin No.	Pin Name	I / O type	Functional description
3	EXTON1N	AI	Power-on trigger, level trigger (active low)
4	RESET	DI	reset input. Active low
86	PWRKEY	AI	Input pad generally connected to a keypad power-on Button. Active low

Note: The pull-up voltage of PWRKEY and EXTON1N was consistent with that of VBAT, and the pull-up voltage of RESET was 1.8V.

3.2 Power-on sequence

VBAT power, VAON (RTC clock source), PWRKEY also synchronous power. After the PWRKEY pin is lowered, the module starts up, and all internal power sources such as VDD1V8 start up one after another. When the Status pin becomes high, it means the module starts up and can be used normally.

Table 38 power-on sequencing

Symbols	Pin Name	Min	Typ	Max	Unit
Ton	Start-up low level pulse width	0.5	16	--	s
TSTATUS	BOOT time (based on the Status Pin)	12	13	--	s
TUART	BOOT time (according to UART judgement)	11	12	--	s
VIH	PWRKEY pin input high level voltage	0.7*VBAT	--	VBAT	V
VIL	PWRKEY pin input low level voltage	0	--	0.3*VBAT	V

3.3 Power-off sequence

Modules have the following shutdown methods:

- Shut down using the PWRKEY Pin

- Shutdown using the "AT CPOF" command

Note: 1. For a detailed description of "AT + CPOF" , refer to documentation [1] .
2. Overvoltage (high or low) may also cause the module to shut down automatically.
3. Exceeding the limit temperature of the module may also cause the module to shut down automatically.

Table 39 Power-off sequencing

Symbols	Pin Name	Min	Typ	Max	Unit
TOFF	Power off low level pulse width	16	--	--	s
TSTATUS	Shutdown time (judged by the Status Pin)	25	26	--	s
TUART	BOOT time (according to UART judgement)	14	15	--	s

3.4 Reset sequence

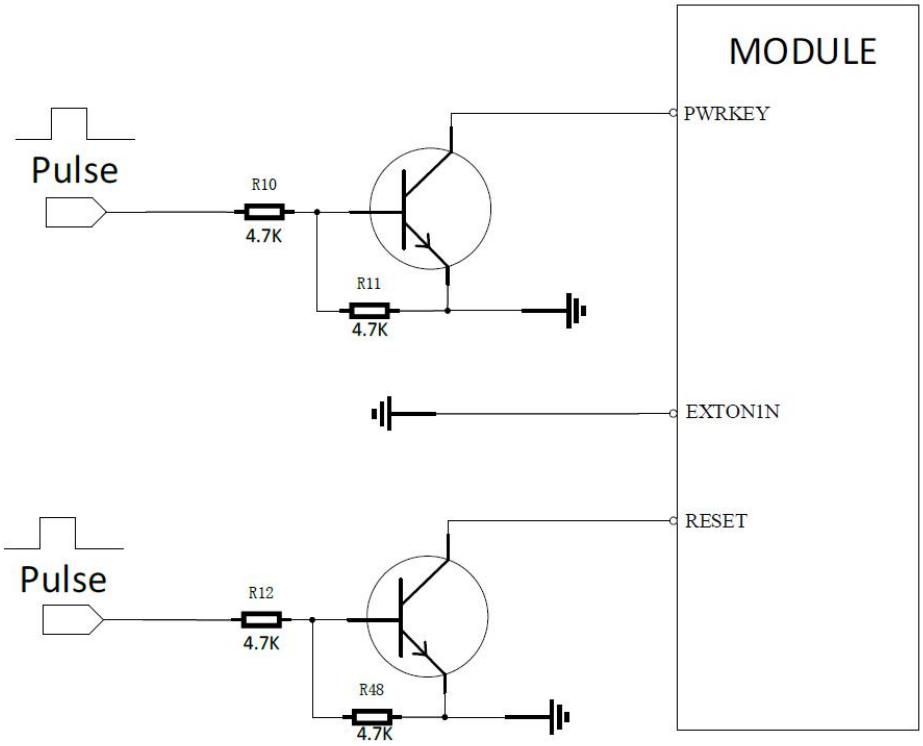
L508 can reset the module by pulling down the RESET or PWRKEY pin. Refer to 4.22.1 for a description of restarting the module.

Table 40 electrical properties of reset key signals

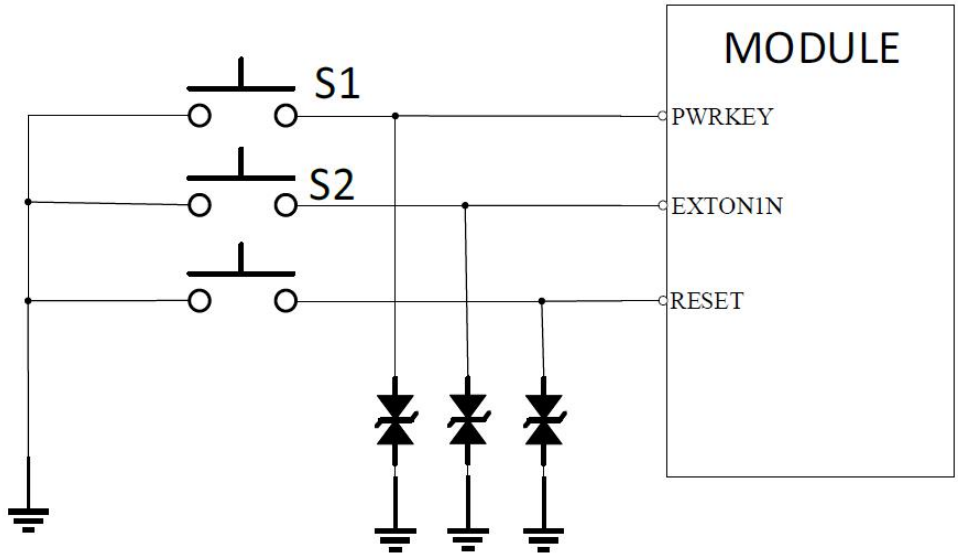
Symbols	Pin Name	Min	Typ	Max	Unit
VIH	Reset pin input high level voltage	1.26	1.8	2.0	V
VIL	Reset pin input low level voltage	-0.3	0	0.54	V

3.5 Interface application

PWRKEY, EXTON1N and RESET circuit can refer to the following diagram of the design circuit.



Another way to control the PWRKEY, RESET, EXTON1N pin, is to use a physical key switch directly. Place a TVS near the button for ESD protection. The following is the reference circuit:


MODULE
S1
S2
PWRKEY
EXTON1N
RESET