

# AIROC™ Bluetooth® LE module

## General description

The CYBLE-416070-02 is a fully certified and qualified module supporting, features out-of-box security functionality, providing an isolated root-of-trust with between communication and Bluetooth® Low Energy wireless communication. The CYBLE-416070-02 is a turnkey solution and includes onboard crystal oscillators, trace antenna, passive components, and the Infineon PSoC™ 64 Bluetooth® LE silicon device. Refer to the PSoC™ 64 Bluetooth® LE [datasheet](#) for additional details on the capabilities of the PSoC™ 64 Bluetooth® LE device used on this module.

The AIROC™ Bluetooth® LE module is a scalable and reconfigurable platform architecture. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The CYBLE-416070-02 also includes digital programmable logic, high-performance analog-to-digital conversion (ADC), low-power comparators, and standard communication and timing peripherals.

The CYBLE-416070-02 includes a royalty-free Bluetooth® LE stack compatible with Bluetooth® 5.0 and provides up to 36 GPIOs in a 14 × 18.5 × 2.00 mm package.

The CYBLE-416070-02 is a complete solution and an ideal fit for applications seeking a high-performance Bluetooth® LE wireless solution.

## Module description

- Module size: 14.0 mm × 18.5 mm × 2.00 mm (with shield)
- 1 MB Application Flash with 32-KB EEPROM area and 32-KB Secure Flash
- 288-KB SRAM with Selectable Retention Granularity
- Up to 36 GPIOs with programmable drive modes, strengths, and slew rates
- Bluetooth® 5.0 qualified single-mode module
  - QDID: **D040144**
  - Declaration ID: **112778**
- Certified to FCC, CE, MIC, and ISED regulations
- Industrial temperature range: -40°C to +85°C
- 150-MHz Arm® Cortex® -M4F CPU with single-cycle multiply (Floating Point Unit (FPU) and Memory Protection Unit (MPU))
- 100-MHz Cortex® -M0+ CPU with single-cycle multiply and MPU

**Note:** In PSoC™ 64 the Cortex® M0+ is reserved for system functions, and is not available for applications.

- OTP eFuse memory for validation and security
- Power consumption
  - TX output power: -20 dbm to +4 dbm
  - Received signal strength indication (RSSI) with 4-dB resolution
  - TX current consumption of 5.7 mA (radio only, 0 dbm)
  - RX current consumption of 6.7 mA (radio only)
- Hardware-Based Root-of-Trust (RoT)
  - RoT based on immutable boot-up code, flash content hash, and Infineon public key that ensures firmware integrity prior to provisioning
  - Supports trusted RoT handover to maintain chain of trust and establish OEM trust anchor for secured boot
  - Device generates a unique device ID and a device secret key during the provisioning process, which can be used for attestation and signing

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**Module description**

- Immutable “Secure Boot” support
  - Flexible chain of trust can use different signatures for different images
  - ECC-based image signature validation
- Infineon bootloader
  - Open source MCUBoot<sup>[1]</sup> based bootloader optimized for PSoC™ 64 MCU
  - Pre-built bootloader binary capable of validating, launching and updating signed user application images
  - Tightly integrated with provisioned debug and boot policies to inherit and implement security policies
- Low-power 1.71 V to 3.6 V operation
  - Active, Low-power Active, Sleep, Low-power Sleep, Deep Sleep, and Hibernate modes for fine-grained power management
  - Deep Sleep mode current with 64K SRAM retention is 7  $\mu$ A with 3.3-V external supply and internal buck
  - On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, less than 1  $\mu$ A quiescent current
  - Backup domain with 64 bytes of memory and Real-Time-Clock (RTC) programmable analog
- Serial communication
  - Five independent runtime reconfigurable serial communication blocks (SCBs), each is software configurable as I<sup>2</sup>C, SPI, or UART
- Timing and Pulse-Width Modulation (TCPWM)
  - Thirty-two TCPWM blocks
  - Center-aligned, Edge, and Pseudo-random modes
  - Comparator-based triggering of Kill signals
- Up to 36 programmable GPIOs
  - Any GPIO pin can be CAPSENSE™, analog/digital
- Audio subsystem
  - I<sup>2</sup>S interface; up to 192 kilosamples (ksps) word clock
  - Two pulse-density modulation (PDM) channels for stereo digital microphones
- Programmable analog
  - 12-bit 1 Msps SAR ADC with differential and single-ended modes and Sequencer with signal averaging
  - One 12-bit voltage mode DAC with less than 5  $\mu$ s settling time
  - Two opamps with low-power operation modes
  - Two low-power comparators that operate in Deep Sleep and Hibernate modes
  - Built-in temperature sensor connected to ADC
- Programmable digital
  - 12 programmable logic blocks, each with eight macrocells and an 8-bit data path (called universal digital blocks or UDBs)
  - Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog programmable blocks
  - Infineon-provided peripheral component library using UDBs to implement functions such as communication peripherals (for example, LIN, UART, SPI, I<sup>2</sup>C, S/PDIF and other protocols), waveform generators, pseudo-random sequence (PRS) generation, and other functions.
  - Smart I/O (Programmable I/O) blocks enable Boolean operations on signals coming from, and going to, GPIO pins
  - Two ports with Smart I/O block capability are provided and are available during Deep Sleep

**Note**

1. For details, refer to [mcuboot.com](https://www.infineon.com/mcuboot).

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## Module description

- Capacitive sensing
  - Infineon Capacitive Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
  - Mutual capacitance sensing (Infineon CSX) with dynamic usage of both self and mutual sensing
  - Wake-on-Touch (WOT) with very low current
  - Infineon-supplied software component makes capacitive sensing design fast and easy
  - Automatic hardware tuning (SmartSense)
- Energy profiler
  - Block that provides history of time spent in different power modes
  - Software energy profiling to observe and optimize energy consumption
- Security built into platform architecture
  - Multi-faceted secure architecture based on ROM-based root of trust
  - Secure boot uninterruptible until system protection attributes are established
  - Authentication during boot using hardware hashing
  - Step-wise authentication of execution images
  - Secure execution of code in execute only mode for protected routines
  - All debug and test ingress paths can be disabled
- Cryptography accelerators
  - Hardware acceleration for Symmetric and Asymmetric Cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)
  - True Random Number Generator (TRNG) function

More information

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## More information

Infineon provides a wealth of data at [www.infineon.com](http://www.infineon.com) to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: [Module roadmap](#)
- [PSoC™ 6 Bluetooth® LE silicon datasheet](#)
- Application Notes cover a broad range of topics, from basic to advanced level, and include the following:
  - [AN221774](#): Getting Started with PSoC™ 6 MCU
  - [AN218241](#): PSoC™ 6 MCU hardware design guide
  - [AN213924](#): PSoC™ 6 MCU device firmware update guide
  - [AN215656](#): PSoC™ 6 MCU dual-CPU system design
  - [AN219528](#): PSoC™ 6 MCU power reduction techniques
  - [AN85951](#): PSoC™ 4, PSoC™ 6 MCU CAPSENSE™ design guide
- [Code examples](#) demonstrate product features and usage, and are also available on [Infineon GitHub](#) repositories
- [Technical Reference Manuals \(TRMs\)](#) provide detailed descriptions of PSoC™ 6 MCU architecture and registers.
- [PSoC™ 6 MCU programming specification](#) provides the information necessary to program PSoC™ 6 MCU nonvolatile memory
- Development kits:
  - CYBLE-416070EVAL, CYBLE-416070-02 evaluation board
  - [CY8CKIT-064S0S2-4343W](#), AWS AIROC™ Wi-Fi Bluetooth® pioneer kit
- Test and debug tools:
  - [CYSmart](#), Bluetooth® LE test and debug tool (Windows)
  - [CYSmart Mobile](#), Bluetooth® LE test and debug tool (Android/iOS Mobile App)

## ModusToolbox™ software

**ModusToolbox™ software** is Infineon comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

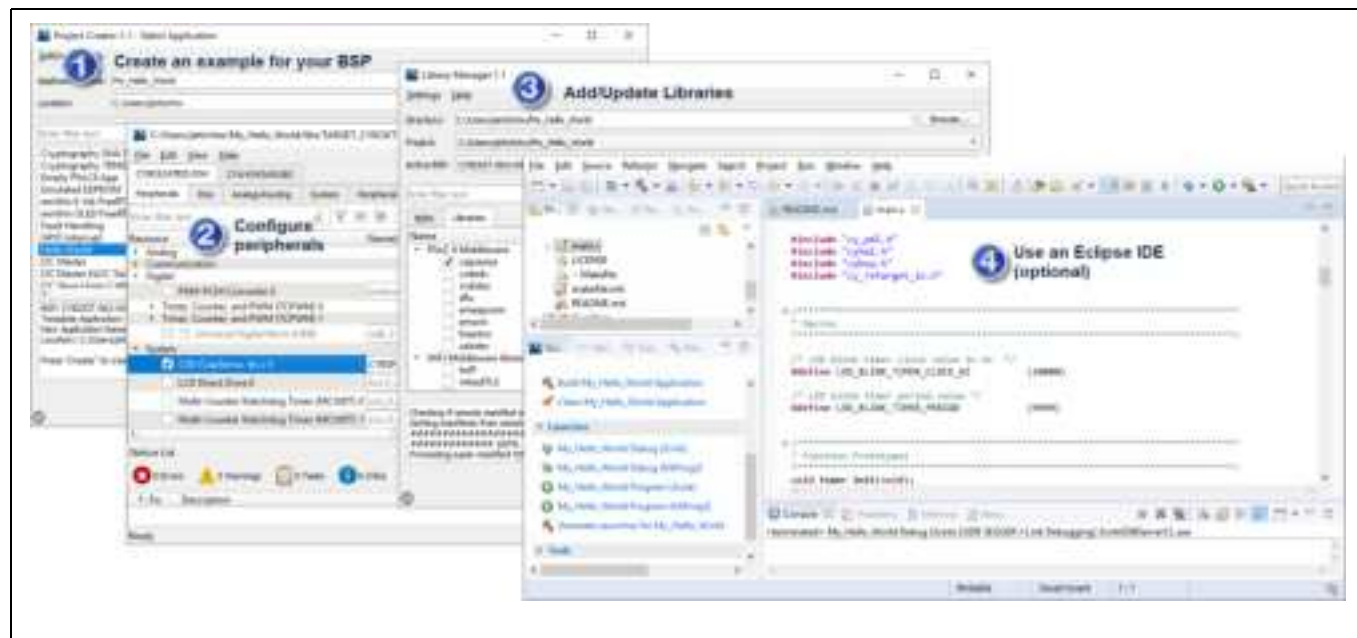
- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code **repositories on GitHub**. This includes:

- Board support packages (BSPs) aligned with Infineon kits
- Low-level resources, including a hardware abstraction layer (HAL) and peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™, Bluetooth® Low Energy, and mesh networks
- An extensive set of thoroughly tested **code example applications**

**Note:** The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. For example, it wraps the PSoC™ 6 PDL with a simplified API, but the PDL exposes all low-level peripheral functionality. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control.

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™ software. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software, and **AN228571- Getting started with PSoC™ 6 MCU on ModusToolbox™ software**.



**Figure 1** ModusToolbox™ software tools

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# 1 Functional description

The following sections provide an overview of the features, capabilities and operation of each functional block. For more detailed information, refer to the following documentation:

- Board support package (BSP) documentation  
 BSPs are available on [GitHub](#). They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example [here](#). This [search link](#) finds all currently available BSPs on the Infineon GitHub site.
- Hardware abstraction layer API reference manual  
 The hardware abstraction layer (HAL) provides a high-level interface to configure and use hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The [HAL API reference](#) provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.
- Peripheral driver library (PDL) API reference manual  
 The peripheral driver library (PDL) integrates device header files and peripheral drivers into a single package and supports all PSoC™ 6 MCU product lines. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the [PDL API reference](#). Example applications that use the PSoC™ 6 PDL download it automatically from the GitHub repository.
- Architecture technical reference manual (TRM)  
 The architecture TRM provides a detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.
- Register technical reference manual  
 The register TRM provides a complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

## 1.1 CPU and memory subsystem

PSoC™ 6 has multiple bus masters. They are: CPUs, DMA controllers, QSPI, USB, SD host controller, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm® AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

### 1.1.1 CPUs

There are two Arm® Cortex® CPUs:

The Cortex®-M4 (CM4) has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the [Armv7-M Architecture Reference Manual](#)).

The Cortex®-M0+ (CM0+) has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

In PSoC™ 64 MCU, the initial CM0+ frequency is set according to a provisioned security policy (see PSoC™ 64 security). The frequency ranges from 8 MHz to 50 MHz.



## Functional description

CM0+ is the secondary CPU; it is used to implement system calls and device-level security, safety, and protection features. CM0+ provides a secured, uninterruptible boot function. This helps ensure that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the [Armv6-M Architecture Reference Manual](#)). The CPUs have the following power draw, at  $V_{DD} = 3.3\text{ V}$  and using the internal buck regulator:

**Table 1 Active current slope at  $V_{DD} = 3.3\text{ V}$  using the internal buck regulator**

| CPU |             | System power mode           |                             |
|-----|-------------|-----------------------------|-----------------------------|
|     |             | ULP                         | LP                          |
|     |             |                             |                             |
|     | Cortex®-M0+ | 15 $\mu\text{A}/\text{MHz}$ | 20 $\mu\text{A}/\text{MHz}$ |
|     | Cortex®-M4  | 22 $\mu\text{A}/\text{MHz}$ | 40 $\mu\text{A}/\text{MHz}$ |

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm®.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. PSoC™ 6 MCU has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4-KB dedicated RAM.

PSoC™ 6 MCU also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

### 1.1.2 Interrupts

This product line has 174 system and peripheral interrupt sources, and supports interrupts and system exceptions on both CPUs. CM4 has 174 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has eight interrupts IRQ[7:0] with configurable mapping of one or more interrupt sources to any of the IRQ[7:0]. CM0+ also supports eight internal (software only) interrupts.

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). Up to four system interrupts can be mapped to each of the CPUs' non-maskable interrupts (NMI). Up to 39 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. Refer to the technical reference manual for details.

### 1.1.3 InterProcessor Communication (IPC)

In addition to the Arm® SEV and WFE instructions, a hardware InterProcessor Communication (IPC) block is included. It includes 16 IPC channels and 16 IPC interrupt structures. The IPC channels can be used to implement data communication between the processors. Each IPC channel also implements a locking scheme which can be used to manage shared resources. The IPC interrupts let one processor interrupt the other, signaling an event. This is used to trigger events such as notify and release of the corresponding IPC channels. Some IPC channels and other resources are reserved, as [Table 2](#) shows:

**Table 2 Distribution of IPC channels and other resources**

| Resources available             | Resources consumed |
|---------------------------------|--------------------|
| IPC channels,<br>16 available   | 13 reserved        |
| IPC interrupts,<br>16 available | 13 reserved        |

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Functional description

**Table 2**      **Distribution of IPC channels and other resources** *(continued)*

| Resources available                                    | Resources consumed   |
|--|----------------------|
| Other interrupts                                       | 1 reserved           |
| CM0+ NMI   | Reserved             |
| Other resources:<br>clock dividers, DMA channels, etc. | 4 CM0+ interrupt mux |

### 1.1.4      **Direct memory access (DMA) controllers**

This product line has three DMA controllers, with 32, 29, and 2 channels, which support CPU-independent accesses to memory and peripherals. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors is limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. Refer to the technical reference manual for detail.

### 1.1.5      **Cryptography accelerator (Crypto)**

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The Crypto subsystem supports the following:

- Encryption/decryption functions
  - Data Encryption Standard (DES)
  - Triple DES (3DES)
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
  - Elliptic Curve Cryptography (ECC)
  - RSA cryptography functions
- Hashing functions
  - Secure Hash Algorithm (SHA)
  - SHA-1
  - SHA-224/-256/-384/-512
- Message authentication functions (MAC)
  - Hashed message authentication code (HMAC)
  - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
  - Pseudo random number generator (PRNG)
  - True random number generator (TRNG)

### 1.1.6      **Protection units**

This product line has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm® MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement protection for memory resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secured/non-secured, and protection context.

Protection units are configured at boot to control access privileges and rights for bus masters and peripherals.

Up to eight protection contexts (boot is in protection context 0) allow access privileges for memory and system resources to be set by the boot process per protection context by bus master and code privilege level.

## Functional description

In PSoC™ 64 MCU, multiple protection contexts are used to isolate the different security levels within the device. The CM0+ makes use of several of them during the boot sequence, bootloading, system calls, etc. Protection context 6 is used for the user application code that runs on the CM4 CPU. The SMPUs are set up by default and cannot be modified by the user. See section 8 in the Architecture TRM for the protection context assignment. See section 8 in the Architecture TRM for the protection context assignment.

### 1.1.7 Memory

PSoC™ 6 MCU contains flash, SRAM, ROM, and eFuse memory blocks.

- Flash

There is up to 512 KB of flash; however 128 KB is reserved for system usage, leaving 384 KB for applications. The 32-KB auxiliary flash (AUXflash) is also reserved, and is not available for applications.

There are also two 32-KB flash sectors:

- AUXflash
- Supervisory flash (SFlash). Data stored in Sflash includes device trim values, **Flash boot** code, and encryption keys. After the device transitions into the “Secure” lifecycle stage, SFlash can no longer be changed.

The flash uses 128-bit-wide accesses to reduce power. Write operations can be performed at the row level. A row is 512 bytes. Read operations are supported in both Low Power and Ultra-Low Power modes, however write operations may not be performed in Ultra-Low Power mode.

The flash controller has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

- SRAM

Up to 256 KB of SRAM is provided, however, 80 KB is reserved for system usage, leaving 176 KB for applications.. Power control and retention granularity is implemented in 32-KB blocks allowing the user to control the amount of memory retained in Deep Sleep. Memory is not retained in Hibernate mode.

- ROM

The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code (**ROM boot**) for several system functions. The ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

- eFuse

A one-time-programmable (OTP) eFuse array consists of 1024 bits, all of which are reserved for system use. The bits are used for storing hash values, unique IDs, or other similar PSoC™ 64 MCU parameters.

Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse,  $V_{DDIO0}$  must be at  $2.5\text{ V} \pm 5\%$ , at 14 mA.

Because blowing an eFuse is an irreversible process, programming is recommended only in mass production under controlled factory conditions. For more information, see **PSoC™ 6 MCU Programming Specifications**.

### 1.1.8 Boot code

Two blocks of code, **ROM boot** and **Flash boot**, are pre-programmed into the device and work together to provide device startup and configuration, basic security features, life-cycle stage management and other system functions.

- ROM boot

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Integrity checks of flash boot code
- Device trim setting (calibration)
- Setting the device protection units
- Setting device access restrictions for “Secure” lifecycle states

ROM cannot be changed and acts as the root of trust in a secured system.

## Functional description

### • Flash boot

Flash boot is firmware stored in SFlash that ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

Flash boot:

- Is validated by ROM Boot
- Runs after ROM Boot and before the user application
- Enables system calls
- Enables provisioning and device policy features
- Implements RoT-based services for cryptography
- Provides secured storage for keys and certificates
- Validates and launches first image based on policies provisioned in the device

If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state. Refer to the **PSoc™ 64 MCU security** section for more details.

### 1.1.9 Memory map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the Arm®-defined regions shown in **Table 3**. Note that code can be executed from the Code and External RAM regions.

**Table 3. Address map for CM4 and CM0+**

| Address range              | Name                   | Use  |
|----------------------------|------------------------|--|
| 0x0000 0000 – 0x1FFF FFFF  | Code                   | Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0.            |
| 0x2000 0000 – 0x3FFF FFFF  | SRAM                   | Data region. This region is not supported in PSoC™ 6 MCU.  |
| 0x4000 0000 – 0x5FFF FFFF  | Peripheral             | All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in PSoC™ 6 MCU. |
| 0x6000 0000 – 0x9FFF FFFF  | External RAM           | SMIF or Quad SPI, (see the <b>Quad-SPI/Serial Memory Interface (SMIF)</b> section). Code can be executed from this region.       |
| 0xA000 0000 – 0xDFFF FFFF  | External Device        | Not used.  |
| 0xE000 0000 – 0xE00F FFFF  | Private Peripheral Bus | Provides access to peripheral registers within the CPU core.   |
| 0xE010 0A000 – 0xFFFF FFFF | Device                 | Device-specific system registers.  |

The device memory map shown in **Table 4** applies to both CPUs. That is, the CPUs share access to all PSoC™ 6 MCU memory and peripheral registers.

**Table 4 Internal memory address map for CM4 and CM0+**

| Address range  | Memory type  | Size                   |
|--|--|------------------------|
| 0x0000 0000 – 0x0000 FFFF                              | ROM  | 64 KB                  |
| 0x0800 0000 – 0x0802 BFFF<br>0x0802 C000 – 0x0803 FFFF | Application SRAM<br>System SRAM  | Up to 176 KB<br>80 KB  |
| 0x1000 0000 – 0x1005 FFFF<br>0x1006 0000 – 0x1007 FFFF | Application flash<br>Secured code flash<br>Used for secured boot, secured bootloader, and system calls | Up to 384 KB<br>128 KB |
| 0x1400 0000 – 0x1400 7FFF                              | Auxiliary flash, reserved for system use   | 32 KB                  |
| 0x1600 0000 – 0x1600 7FFF                              | Supervisory flash, for secured access  | 32 KB                  |

Note that PSoC™ 6 MCU SRAM is located in the Arm® Code region for both CPUs (see [Table 3](#)). There is no physical memory located in the CPUs' Arm® SRAM regions.

## 1.2 System resources

### 1.2.1 Power system

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The  $V_{DD}$  supply (1.7 to 3.6 V) powers an on-chip buck regulator or a low-dropout regulator (LDO), selectable by the user. In addition, both the buck and the LDO offer a selectable (0.9 or 1.1 V) core operating voltage ( $V_{CCD}$ ). The selection lets users choose between two system power modes:

- System Low Power (LP) operates  $V_{CCD}$  at 1.1 V and offers high performance, with no restrictions on device configuration.
- System Ultra Low Power (ULP) operates  $V_{CCD}$  at 0.9 V for exceptional low power, but imposes limitations on clock speeds.

In addition, a backup domain adds an “always on” functionality using a separate power domain supplied by a backup supply ( $V_{BACKUP}$ ) such as a battery or supercapacitor.

It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control. Refer to [Power](#) for more details.

### 1.2.2 Power modes

PSoC™ 6 MCU can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, [AN219528: PSoC™ 6 MCU Low-Power Modes and Power Reduction Techniques](#) and the [Architecture TRM, Power Modes chapter](#) (contact your local Infineon sales representative for the latest TRM).

Power modes supported by PSoC™ 6 MCUs, in order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode
- CPU Sleep – CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). System LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSoC 6 MCU.

### 1.2.3 Clock system

[Figure 2](#) shows that the clock system of this product line consists of the following:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- Watch crystal oscillator (WCO)
- External MHz crystal oscillator (ECO)

## Functional description

- External clock input
- One phase locked-loop (PLL)
- One frequency-locked loop (FLL)

Clocks may be buffered and brought out to a pin on a Smart I/O port.

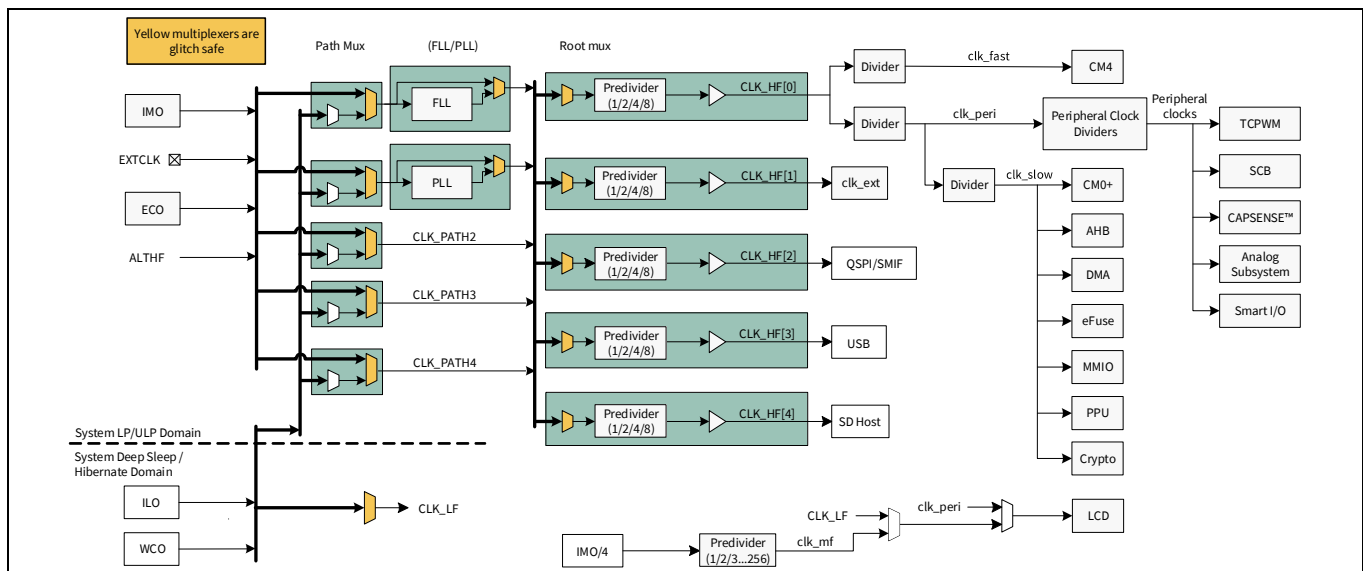
### 1.2.4 Internal main oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed at the factory to achieve the specified accuracy. The IMO frequency is 8 MHz and tolerance is  $\pm 2\%$ .

The IMO can operate in system Deep Sleep mode to drive the LCD block for better contrast (and higher power) than is possible with the 32-kHz mode.

### 1.2.5 Internal low-speed oscillator (ILO)

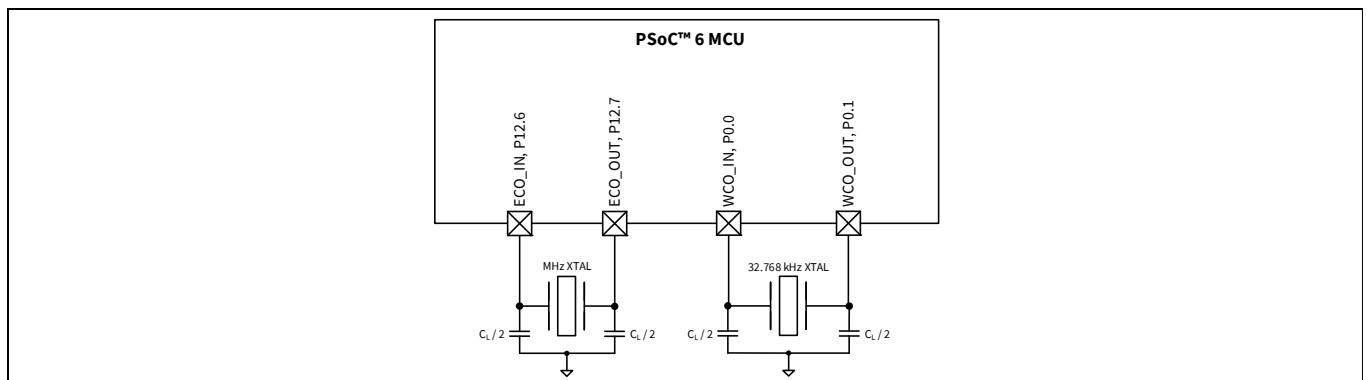
The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.



**Figure 2** Clocking diagram

### 1.2.6 External crystal oscillators

**Figure 3** shows all of the external crystal oscillator circuits for this product line. The component values shown are typical; check the crystal values, and the crystal datasheet for the load capacitor values. The ECO and WCO require balanced external load capacitors. For more information, see the TRM and [AN218241, PSoc™ 6 MCU hardware design considerations](#).



**Figure 3** Oscillator circuits



## Functional description

If the ECO is used, note that its performance is affected by GPIO switching noise. GPIO ports should be used as [Table 5](#) shows. See also [Table 6](#) for additional restrictions for general analog subsystem use.

**Table 5 ECO usage guidelines**

| Ports           | Max frequency          | Drive strength for $V_{DD} \leq 2.7$ V | Drive strength for $V_{DD} \leq 2.7$ V |
|-----------------|------------------------|--|--|
| Port 11         | 60 MHz for SMIF (QSPI) | DRIVE_SEL 2                            | DRIVE_SEL 3                            |
| Ports 12 and 13 | Slow slew rate setting | No restrictions                        | No restrictions                        |

### 1.2.7 Watchdog timers (WDT, MCWDT)

PSoC™ 6 MCU has one WDT and two multi-counter WDTs (MCWDT). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event. The WDT is clocked by the ILO. It can generate interrupt/wakeup in system LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can generate periodic interrupt/wakeup in system LP/ULP and Deep Sleep power modes.

### 1.2.8 Clock dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Four 8-bit clock dividers
- Eight 16-bit integer clock dividers
- Two 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

### 1.2.9 Trigger routing

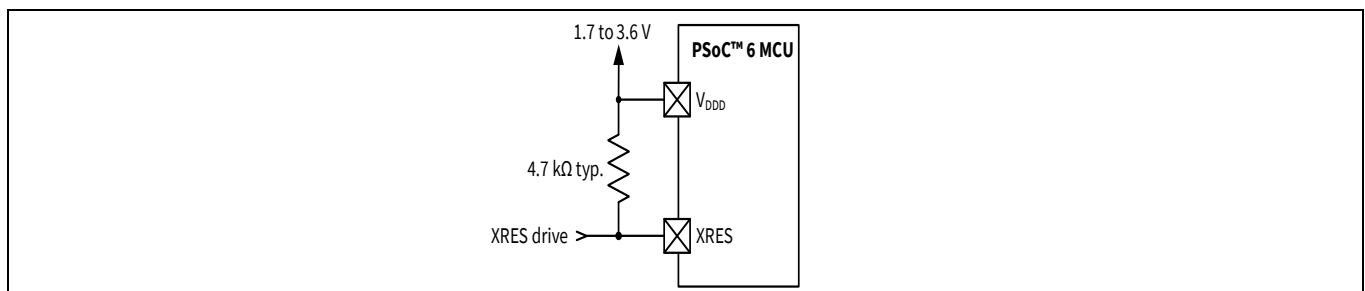
PSoC™ 6 MCU contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers”, which connect a specific source to a destination. The user can enable or disable the route.

### 1.2.10 Reset

PSoC™ 6 MCU can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply  $V_{DD}$  and generate a reset if  $V_{DD}$  falls below the minimum required logic operating voltage.
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active low. It can be connected either to a pull-up resistor to  $V_{DD}$ , or to an active drive circuit, as [Figure 4](#) shows. If a pull-up resistor is used, select its value to minimize current draw when the pin is pulled low; 4.7 kΩ is typical.



**Figure 4 XRES connection diagram**



## Functional description

- Watchdog timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the system Hibernate power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

### 1.3 Programmable analog subsystems

#### 1.3.1 12-bit SAR ADC

The 12-bit, 2-Msps SAR ADC can operate at a maximum clock rate of 36 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal reference voltages may be used for the ADC reference voltage. The references are,  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{REF}$  (nominally 1.2 V and trimmed to  $\pm 1\%$ ). An external reference may also be used, by either driving the VREF pin or routing an external reference to GPIO pin P9.3. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADC is the full supply voltage between  $V_{SS}$  and  $V_{DDA}/V_{DDIOA}$ . The SAR ADC may be configured with a mix of single-ended and differential signals in the same configuration.

The SAR ADC's sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle sufficiently, if required. System performance is 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve performance in noisy conditions, an external bypass capacitor for the internal reference amplifier (through the fixed "VREF" pin), may be added.

The SAR is connected to a fixed set of pins through an input multiplexer. The multiplexer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 2 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. The SAR can also be connected, under firmware control, to most other GPIO pins via the Analog Multiplexer Bus (AMUXBUS). The SAR is not available in system Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 36 MHz). The SAR operating range is 1.71 to 3.6 V.

#### 1.3.2 Temperature sensor

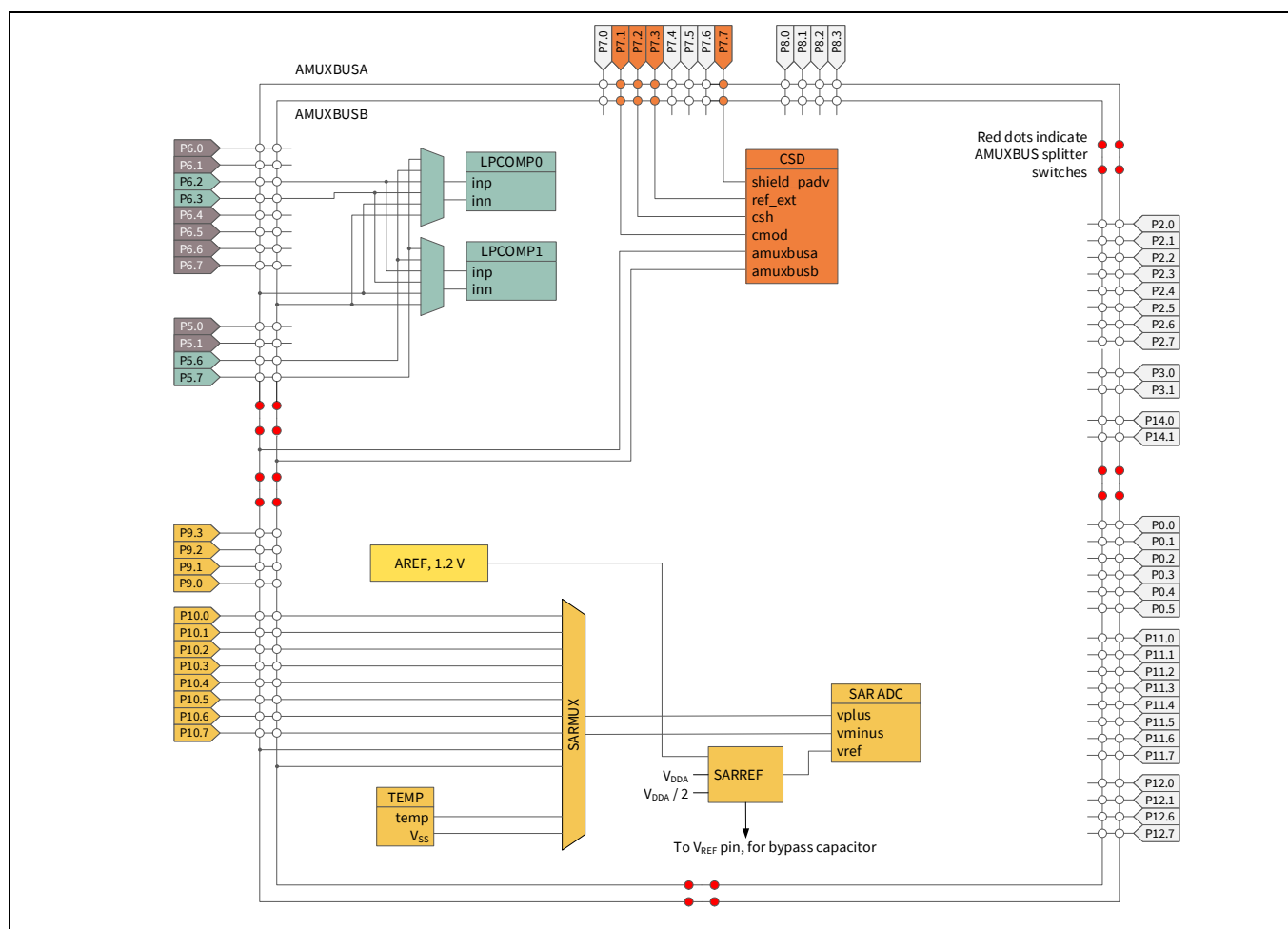
An on-chip temperature sensor is part of the SAR and may be scanned by the SAR ADC. It consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor may be connected directly to the SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor's output and a Infineon-supplied software function may be used to convert the reading to temperature which includes calibration and linearization.

#### 1.3.3 Low-power comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during system Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

**Figure 5** shows an overview of the analog subsystem. This diagram is a high-level abstraction. See the **TRM** for detailed connectivity information.

### Functional description



**Figure 5**      **Analog subsystem**

## 1.4 Programmable digital

### 1.4.1 Smart I/O

Smart I/O is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. A Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

There are two Smart I/O blocks: one on Port 8 and one on Port 9. When Smart I/O is not enabled, all signals on Port 8 and Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- System Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

Each Smart I/O block contains a data unit (DU) and eight lookup tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode.
- Can source input signals from internal resources, the GPIO port, or a value in the DU register.

Each LUT:

- Has three selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU.

## Functional description

- Acts as a programmable Boolean logic table.
- Can be synchronous or asynchronous.

### 1.5 Fixed-function digital

#### 1.5.1 Timer/Counter/Pulse-width Modulator (TCPWM)

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes.
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Four 32-bit TCPWMs
- Eight 16-bit TCPWMs

#### 1.5.2 Serial Communication Blocks (SCB)

This product line has seven SCBs:

- Six can implement either I<sup>2</sup>C, UART, or SPI.
- One SCB (SCB #6) can operate in system Deep Sleep mode with an external clock; this SCB can be either SPI slave or I<sup>2</sup>C slave.

**I<sup>2</sup>C mode:** The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI<sup>2</sup>C, which creates a mailbox address range and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. The SCB supports a 256-byte FIFO for receive and transmit.

The I<sup>2</sup>C peripheral is compatible with I<sup>2</sup>C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

**UART mode:** This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

**SPI mode:** The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with a 25-MHz clock.

### 1.5.3 USB Full-Speed device interface

This product line incorporates a full-speed USB device interface. The device can have up to eight endpoints. A 512-byte SRAM buffer is provided and DMA is supported.

### 1.5.4 Quad-SPI/Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, and quad SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the PSoC™ 6 MCU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secured storage and access of code and data in the external memory.

### 1.5.5 LCD

This block drives LCD commons and segments; routing is available to most of the GPIOs. One to eight of the GPIOs must be used for commons, the rest can be used for segments.

The LCD block has two modes of operation: high speed (8 MHz) and low speed (32 kHz). Both modes operate in system LP, ULP, and Deep Sleep modes, however the low-speed mode operates with reduced contrast in system Deep Sleep mode. The 8-MHz IMO is available in system Deep Sleep mode, and can be used to generate a clock for the LCD block. Review the number of common and segment lines, viewing angle requirements, and prototype performance, and then select the appropriate LCD clock frequency before using system Deep Sleep mode.

### 1.5.6 SD host controller

This product line contains one Secure Digital (SD) host controller. It provides communication with IoT connectivity devices such as Bluetooth®, Bluetooth® Low Energy and WiFi radios, as well as combination devices. The controller also supports embedded MultiMediaCards (eMMC) and Secure Digital (SD) cards.

Several bus speed modes under the SD specification are supported:

- DS (default speed)
- HS (high speed)
- SDR12 (single data rate)
- SDR25
- SDR50
- DDR50 (double data rate)

For eMMC, the supported modes are:

- BWC (backward compatibility)
- SDR

Maximum clock restrictions and capacitive loads apply to some modes, and are also dependent on system power mode (LP/ULP).

The SD Host Controller complies with the following standards. Refer to the specifications documents for more information on the protocol and operations.

- SD Specifications Part 1 Physical Layer Specification Version 6.00, supporting card capacities for SDSC (up to 2 GB), SDHC (up to 32 GB) and SDXC (up to 2 TB).
- SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20
- SD Specifications Part E1 SDIO Specifications Version 4.10
- Embedded Multi-Media Card (eMMC) Electrical Standard 5.1

## Functional description

The SD host controller is configured as a master. To be fully compatible with features provided in the driver software for speed and efficiency, it supports advanced DMA version 3 (ADMA3), defined by the SDIO standard, and has a 1 KB RX/TX FIFO allowing double buffering of 512-byte blocks.

### 1.5.7 CAN FD block

This product line has one CAN FD block for industrial and automotive applications. The block includes Time-Stamp support and has a 4-KB message RAM. FD Data rates of up to 5 Mbps are supported. DMA transfers are supported.

### 1.6 GPIO

This product line has up to 53 GPIOs, which implement the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8 pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 3 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than  $V_{DD}$ . OVT pins are commonly used with I<sup>2</sup>C, to allow powering the chip OFF while maintaining a physical connection to an operating I<sup>2</sup>C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see [Electrical specification](#).

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

Analog performance is affected by GPIO switching noise. In order to get the best analog performance, the following frequency and drive mode constraints must be applied. The DRIVE\_SEL values (see [Table 6](#)) represent drive strengths (please see the [Architecture and Register TRMs](#) for further detail).

See also [Table 5](#) for additional restrictions for ECO use.

**Table 6** DRIVE\_SEL values

| Ports         | Max frequency          | Drive strength for $V_{DD} \leq 2.7$ V | Drive strength for $V_{DD} > 2.7$ V |
|---------------|------------------------|--|-------------------------------------|
| Ports 0, 1    | 8 MHz                  | DRIVE_SEL 2                            | DRIVE_SEL 3                         |
| Port 2        | 50 MHz                 | DRIVE_SEL 1                            | DRIVE_SEL 2                         |
| Ports 3 to 10 | 16 MHz; 25 MHz for SPI | DRIVE_SEL 2                            | DRIVE_SEL 3                         |

**Table 6** **DRIVE\_SEL values** (continued)

| Ports          | Max frequency  | Drive strength for $V_{DD} \leq 2.7 \text{ V}$ | Drive strength for $V_{DD} > 2.7 \text{ V}$ |
|----------------|--|--|---|
| Ports 11 to 12 | 80 MHz for SMIF (QSPI).                                      | DRIVE_SEL 1                                    | DRIVE_SEL 2                                 |
| Ports 9 and 10 | Slow slew rate setting for TQFP Packages for ADC performance | No restrictions                                | No restrictions                             |

## 1.7 Special-function peripherals

### 1.7.1 CAPSENSE™ subsystem

CAPSENSE™ is supported in PSoC™ 6 MCU through a CAPSENSE™ sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CAPSENSE™, the CSD hardware block supports three general-purpose functions. These are available when CAPSENSE™ is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CAPSENSE™
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

#### 1.7.1.1 CAPSENSE™

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. CAPSENSE™ solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The Infineon-proprietary CAPSENSE™ technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CAPSENSE™ tuner for real-time tuning, testing, and debugging

#### 1.7.1.2 ADC

The CAPSENSE™ subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to  $V_{REF}$  and GND to  $V_{DDA}$  on any GPIO input
- Measurement of  $V_{DDA}$  against an internal reference without the use of GPIO or external components



### 1.7.1.3 IDAC

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609  $\mu$ A
- Two IDACs that can be used in parallel to form one 8-bit IDAC

### 1.7.1.4 Comparator

The CAPSENSE™ subsystem comparator operates in the system Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

### 1.7.1.5 CAPSENSE™ hardware subsystem

**Figure 6** shows the high-level hardware overview of the CAPSENSE™ subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

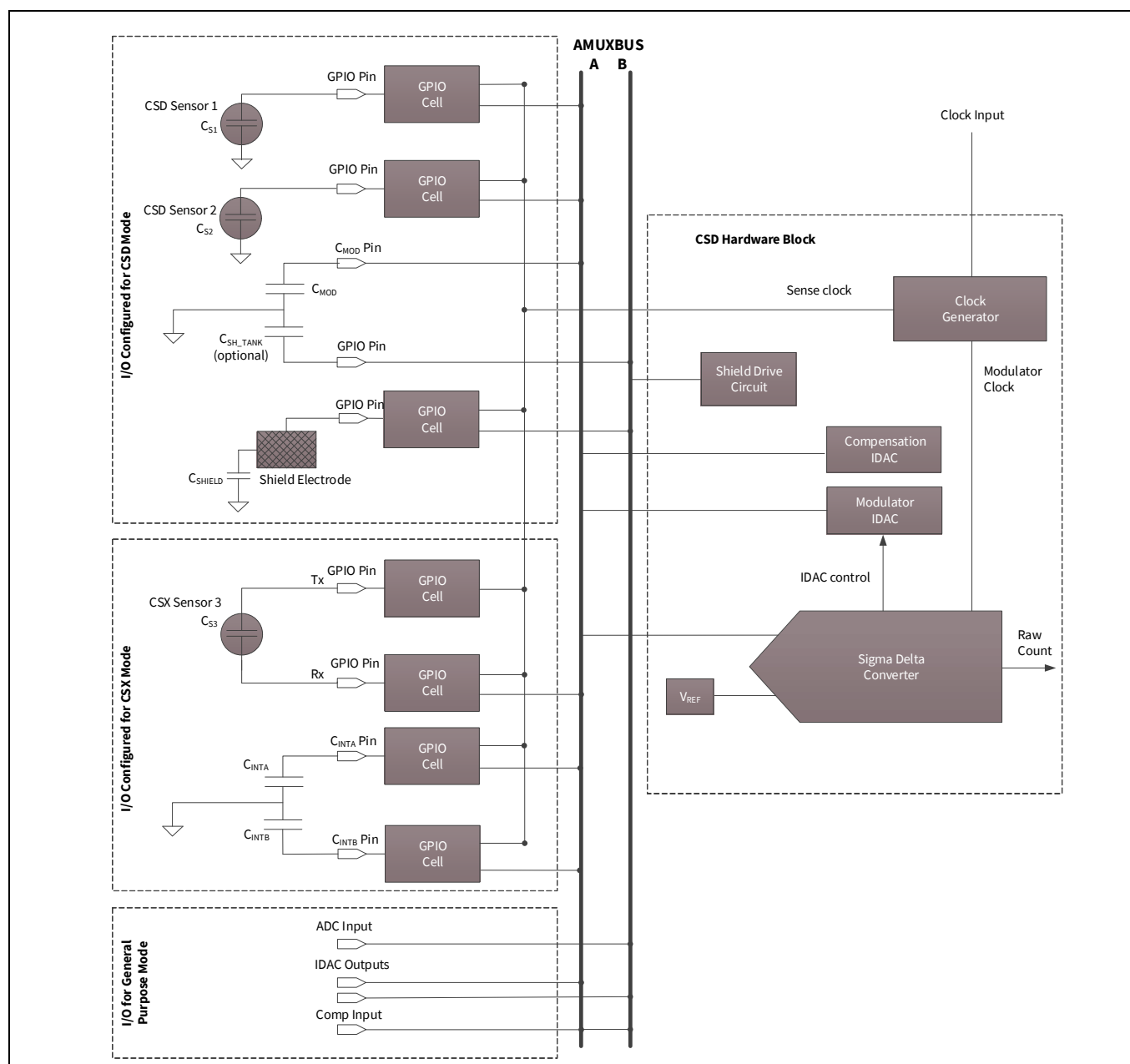
The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept  $V_{DDA}$  as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The comparator inverting input can be connected to the reference. Both comparator inputs can be connected to any GPIO using AMUXBUS B; see **Figure 5**. The reference has a direct connection to a dedicated GPIO; see **Table 10**.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between system LP and ULP modes. It can be powered down in system Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.



## Functional description



**Figure 6** CAPSENSE™ hardware subsystem

**Figure 7** shows the high-level software overview. Infineon provides middleware libraries for **CAPSENSE™**, **ADC**, and **IDAC** on GitHub to enable quick integration. The board support package for any kit with CAPSENSE™ capabilities automatically includes the CAPSENSE™ library in any application that uses the BSP.

User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

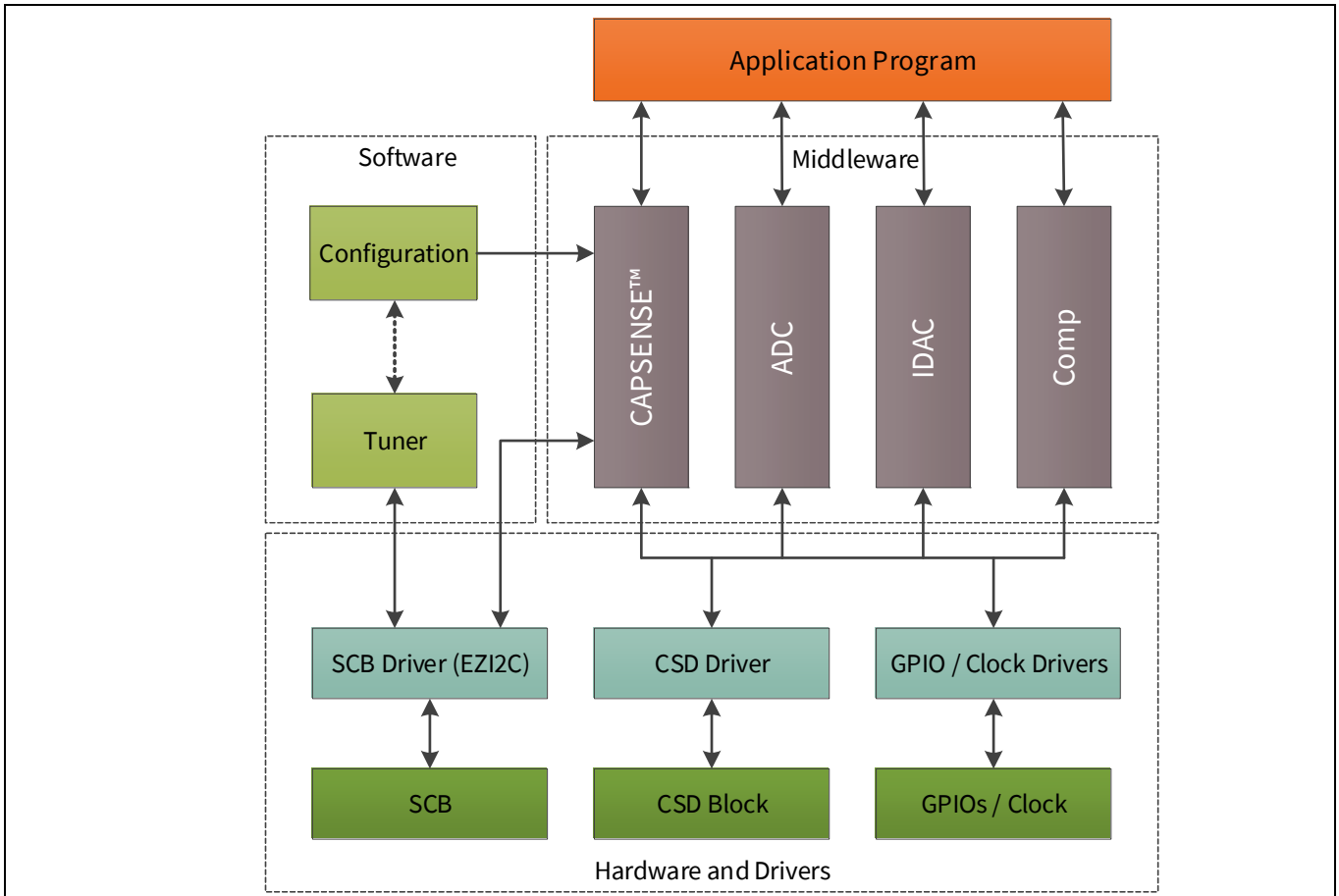
ModusToolbox™ software provides a CAPSENSE™ configurator to enable fast library configuration. It also provides a tuner for performance evaluation and real-time tuning of the system. The tuner requires an EZI2C communication interface in the application to enable real-time tuning capability. The tuner can update configuration parameters directly in the device as well as in the configurator.

Functional description

CAPSENSE™ and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. Middleware and drivers can operate on either CPU. Infineon recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to [AN85951: PSoC™ 4 and PSoC™ 6 MCU CAPSENSE design guide](#) for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines.

Refer to the API reference guides for [CAPSENSE™](#), [ADC](#), and [IDAC](#) available on GitHub.



**Figure 7** CAPSENSE™ software/firmware subsystem

## 1.8 PSoC™ 64 MCU security

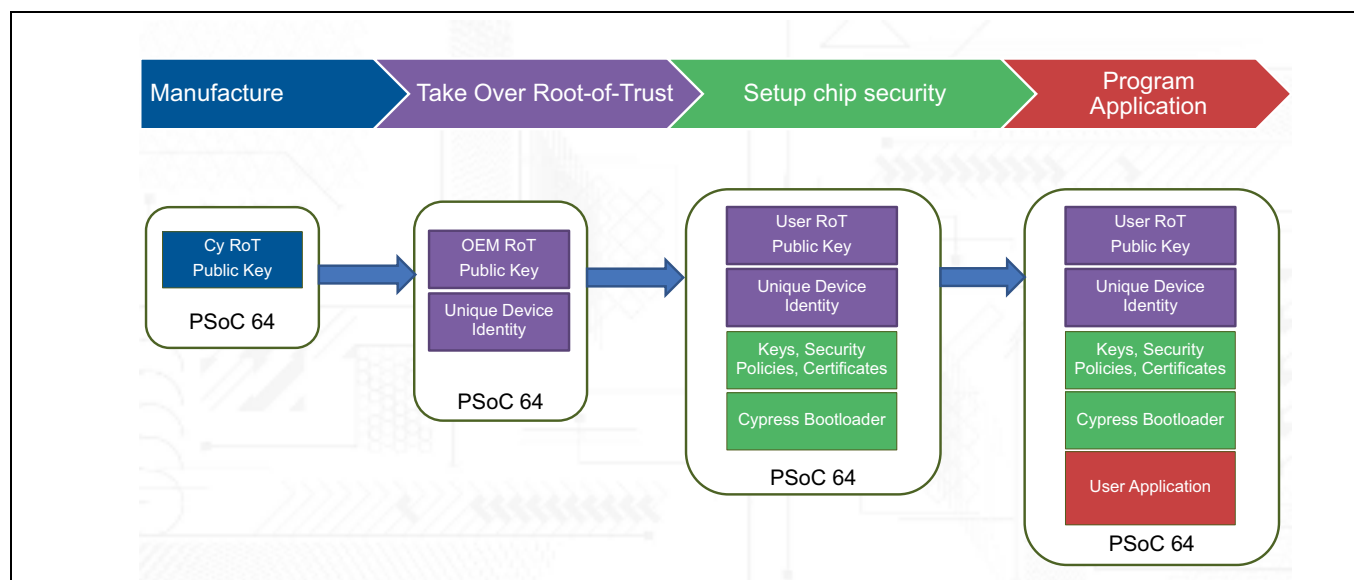
All PSoC™ 64 “Secure” MCU product lines feature enhanced security functionality. They provide an isolated root of trust (RoT) with true attestation and provisioning services. Infineon also provides a “Secure Boot” SDK which includes all required libraries, tools, and sample code to provision PSoC™ 64 MCU devices. The SDK also provides provisioning scripts with sample keys and policies, a pre-built bootloader image, and tools for signing firmware images. For more information, see the [“Secure Boot” SDK User Guide](#).

The “Secure Boot” SDK also includes entrance exam scripts. An entrance exam can optionally be run on PSoC™ 64 MCU devices before provisioning to ensure that no device tampering has occurred.

The first step in using a PSoC™ 64 MCU device is to inject the following information into the device - a process called provisioning:

- A set of cryptographic public keys, which are used to:
  - Transfer the RoT from Infineon to the user/OEM, as [Figure 8](#) shows
  - Validate applications
- A set of security policies that define how the device should behave
- Certificates (optional) used to bind device identity or provide a chain of trust to a higher certifying authority
- The Infineon bootloader

Provisioning is done before an application is programmed into the device.



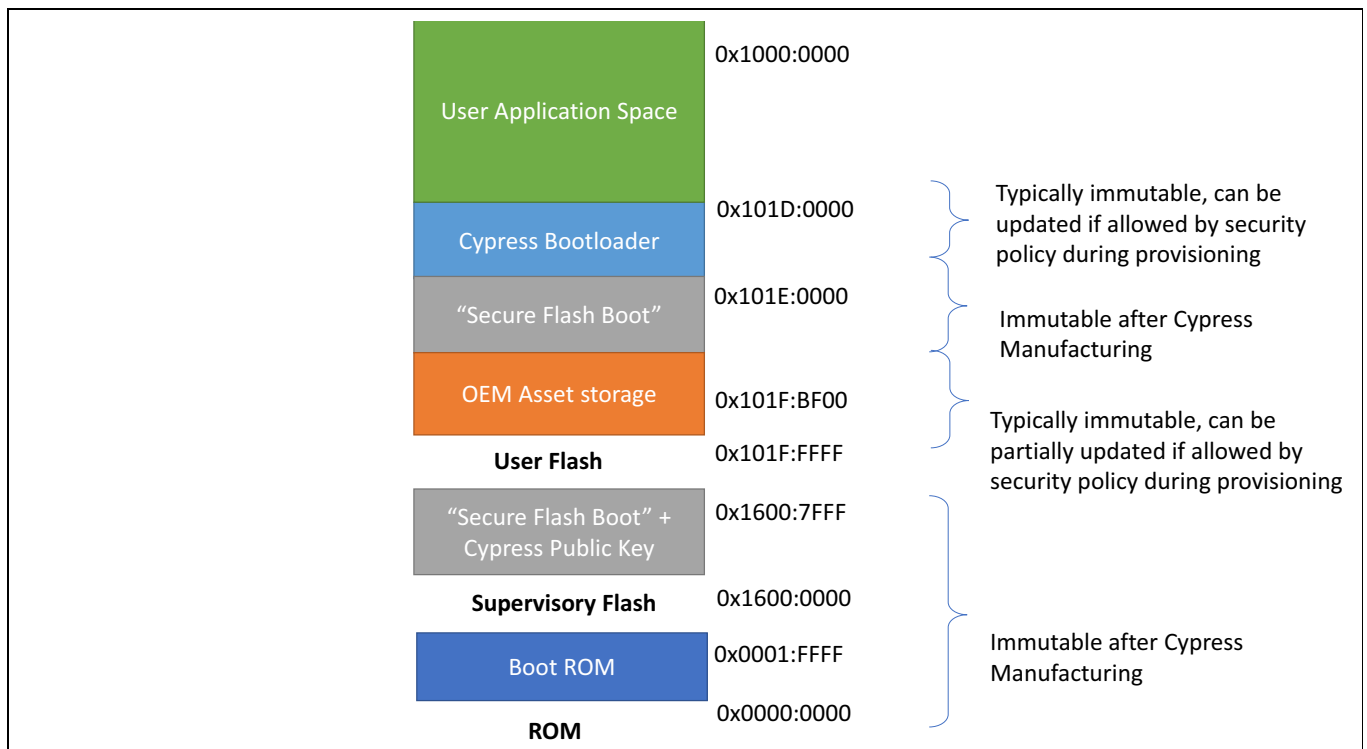
**Figure 8 PSoC™ 64 MCU usage processes**

Provisioning is done using a hardware security module (HSM). An HSM is a physical computing device, placed in a secured facility, that safeguards and manages digital keys for strong authentication, and provides cryptographic processing.

After the device is provisioned, it can be programmed with signed applications. The signature and authenticity of the application is verified before control is transferred to it.

[Figure 9](#) shows a simplified flash memory map of PSoC™ 64 MCU assets and immutable sections. As noted in [Memory](#), a portion of device SRAM is also reserved for system usage.

## Functional description



**Figure 9** PSoC™ 64 “Secure” MCU asset memory map

## 1.9 Infineon bootloader

Infineon bootloader is a port of the open source [MCUBoot](#) library. For more details about this library, refer to [MCUBoot Bootloader design](#). The current version of Infineon Bootloader for this device does not support the swap-based images feature as documented in the MCUBoot design document.

Infineon bootloader is included in the **“Secure Boot” SDK** as a pre-built hex image. This image acts as the first image launched by the PSoC™ 64 MCU boot code. It parses the provisioned Boot&Upgrade policy to launch an application image.

Infineon bootloader supports external memory over the PSoC™ 64 Serial Memory Interface (SMIF). The bootloader currently supports only external memory vendors who support the Serial Flash Discovery Protocol (SFDP).

Infineon bootloader enforces protection contexts for the bootloader code, so code running in another protection context cannot overwrite/tamper with the bootloader code. [Figure 10](#) shows the launch sequence of Infineon bootloader:

Functional description

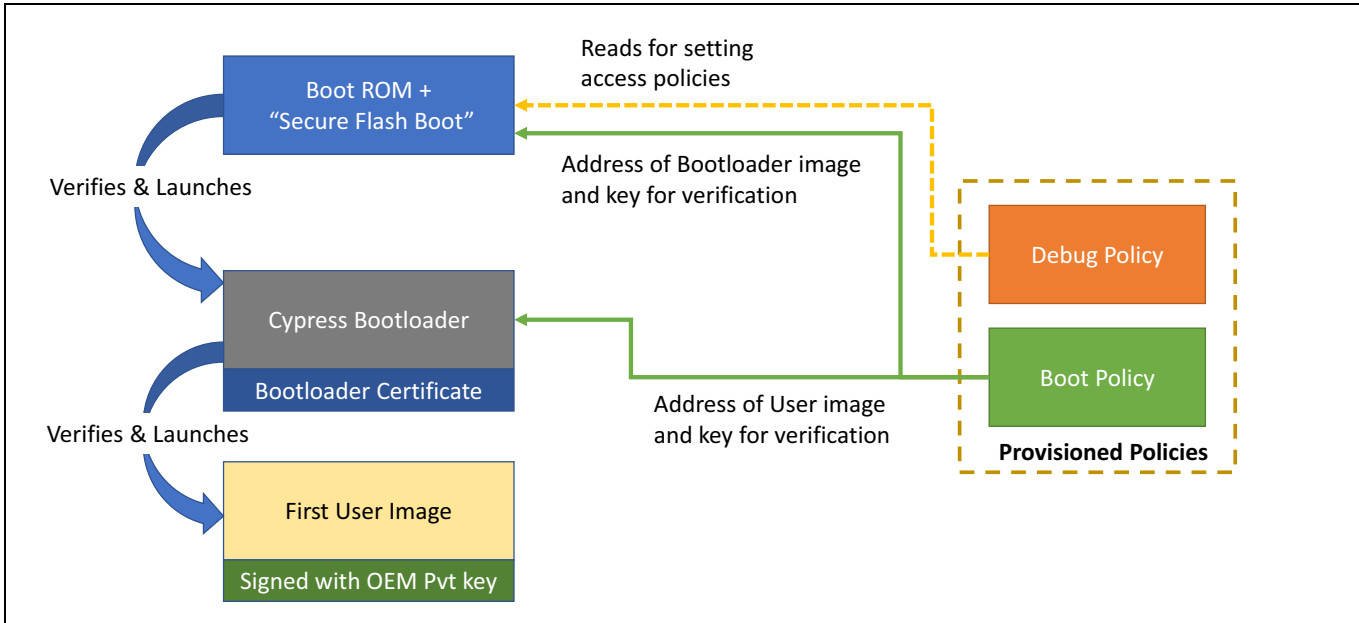


Figure 10 Bootloader launch sequence

Figure 11 shows a typical application update scenario using Infineon bootloader:

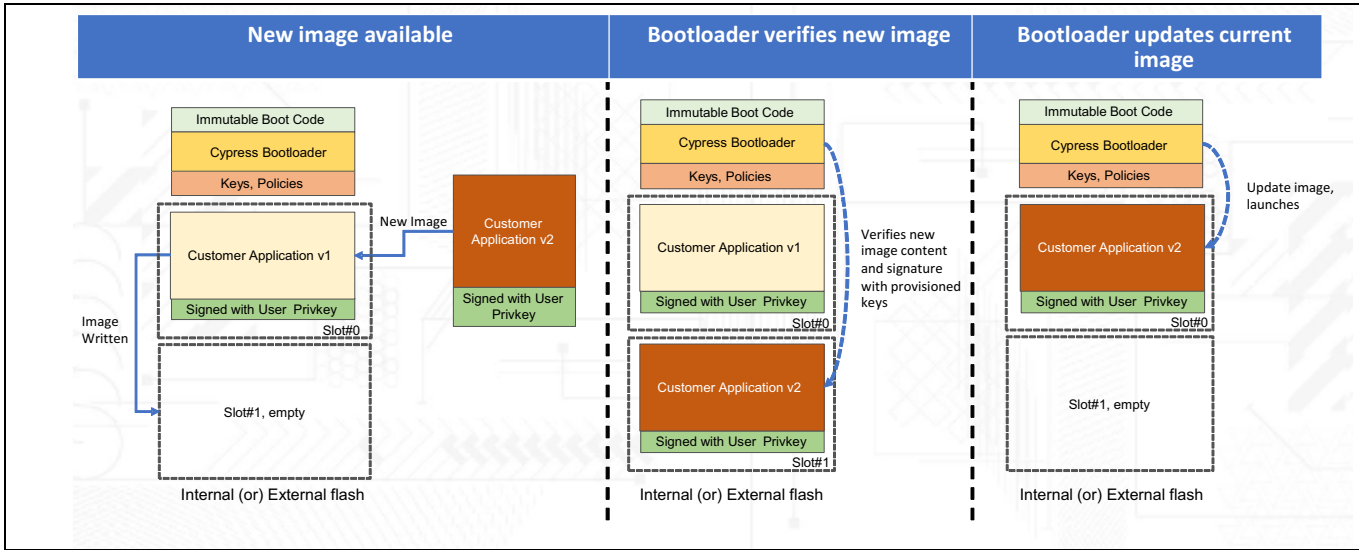


Figure 11 Bootloader application update sequence

## 2 Module overview

### 2.1 Module description

The CYBLE-416070-02 module is a complete module designed to be soldered to the main host board.

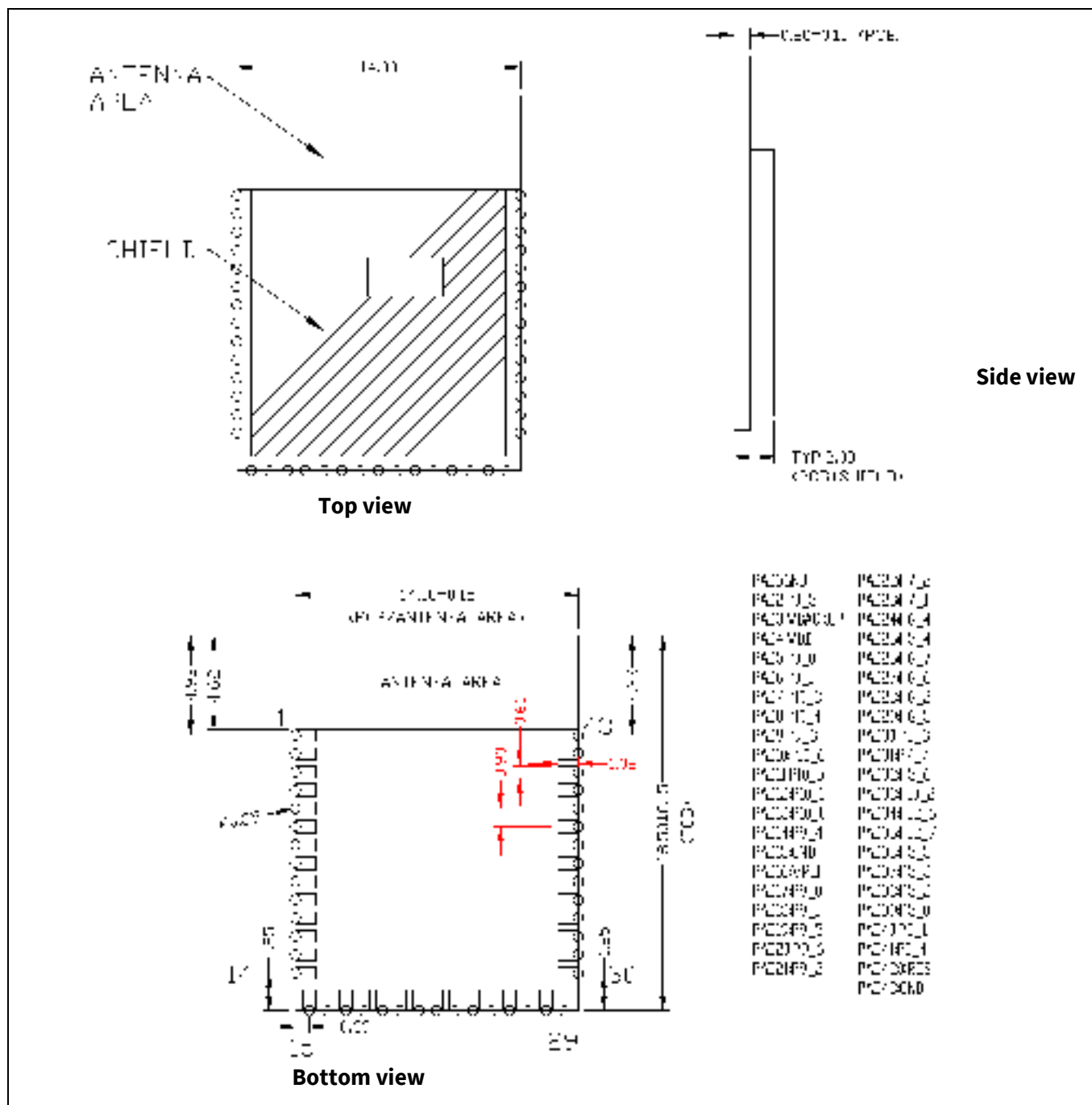
#### 2.1.1 Module dimensions and drawing

Infineon reserves the right to select components (including the appropriate Bluetooth® LE device) from various vendors to achieve the Bluetooth® LE module functionality. Such selections will guarantee that all height restrictions of the component area are maintained. Designs should be completed with the physical dimensions shown in the mechanical drawings in [Figure 12](#). All dimensions are in millimeters (mm).

**Table 7**      **Module design dimension**

| Dimension item   |            | Specification            |
|--|------------|--------------------------|
| Module dimensions  | Length (X) | 14.00 ± 0.15 mm          |
|  | Width (Y)  | 18.50 ± 0.15 mm          |
| Antenna location dimensions                                    | Length (X) | 14.00 ± 0.15 mm          |
|  | Width (Y)  | 4.62 ± 0.15 mm           |
| PCB thickness  | Height (H) | 0.80 ± 0.10 mm           |
| Shield height  | Height (H) | 1.20 ± 0.10 mm           |
| Maximum component height                                       | Height (H) | 1.20 mm typical (shield) |
| Total module thickness (bottom of module to highest component) | Height (H) | 2.00 mm typical          |

See [Figure 12](#) for the mechanical reference drawing for CYBLE-416070-02.



**Figure 12**      **Module mechanical drawing**<sup>[2]</sup>

### Note

2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see [Figure 14](#), [Figure 15](#) and [Figure 16](#), and [Figure 17](#) and [Table 9](#).

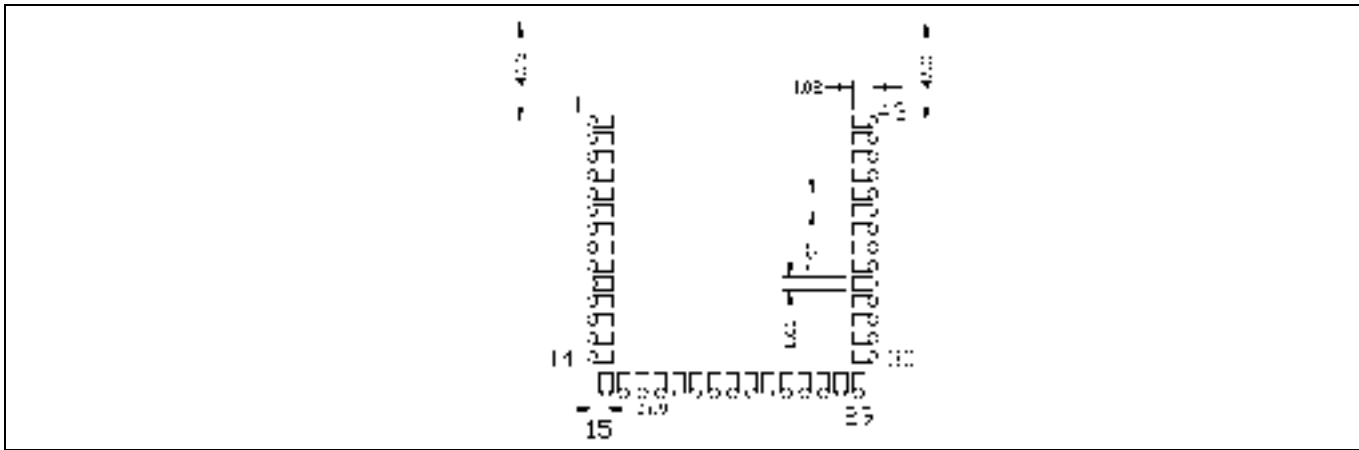


### 3 Pad connection interface

As shown in the bottom view of [Figure 12](#), the CYBLE-416070-02 connects to the host board via solder pads on the back of the module. [Table 8](#) and [Figure 13](#) detail the solder pad length, width, and pitch dimensions of the CYBLE-416070-02 module.

**Table 8 Solder pad connection description**

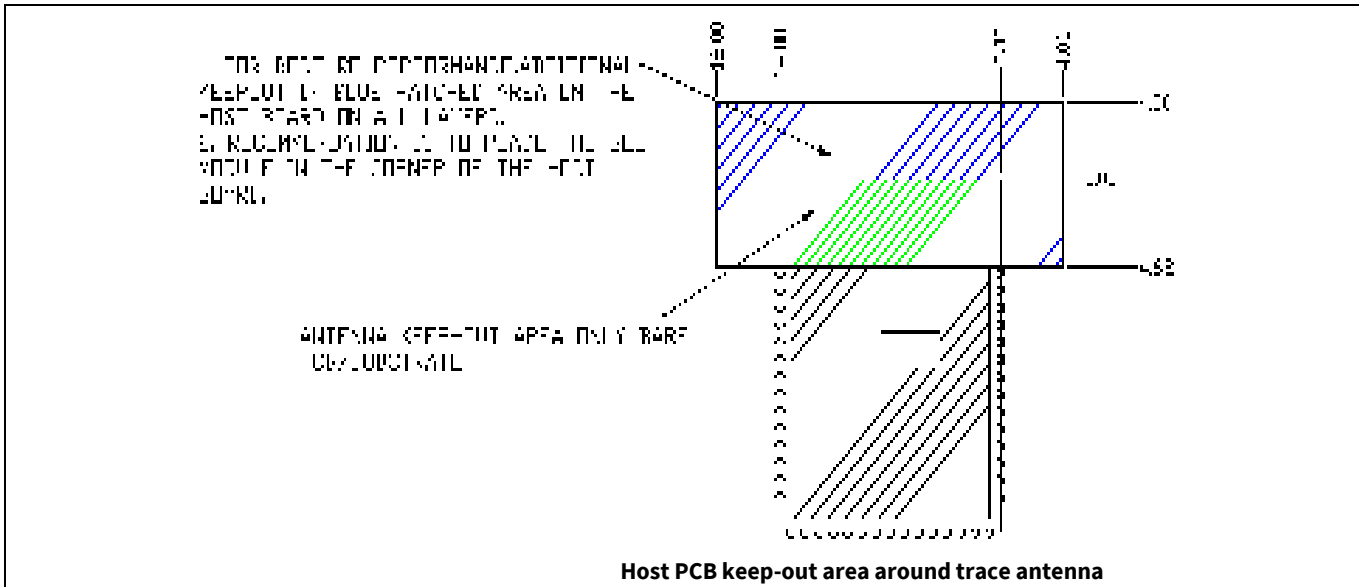
| Name | Connections | Connection type | Pad length dimension | Pad width dimension | Pad pitch |
|------|-------------|-----------------|----------------------|---------------------|-----------|
| SP   | 43          | Solder pads     | 1.02 mm              | 0.61 mm             | 0.90 mm   |



**Figure 13 Solder pad dimensions**

To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Infineon Bluetooth® LE Module is in a corner of the host board with the antenna located on the edge of the host board. This placement minimizes the additional recommended keep-out area stated in item 2. Refer to [AN96841](#) for module placement best practices.
2. To maximize RF performance, the area immediately around the Infineon Bluetooth® LE Module trace antenna should contain an additional keep-out area, where no grounding or signal traces are contained. The keep-out area applies to all layers of the host board. The recommended dimensions of the host PCB keep-out area are shown in [Figure 14](#) (dimensions are in mm).



**Figure 14 Recommended host PCB keep-out area around the CYBLE-416070-02 trace antenna**

## 4 Recommended host PCB layout

Figure 15 through Figure 17 and Table 9 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-416070-02. Dimensions are in millimeters unless otherwise noted. Pad length of 0.99 mm (0.494 mm from center of the pad on either side) shown in Figure 17 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 15, Figure 16, or Figure 17. It is not necessary to use all figures to complete the host PCB layout pattern.

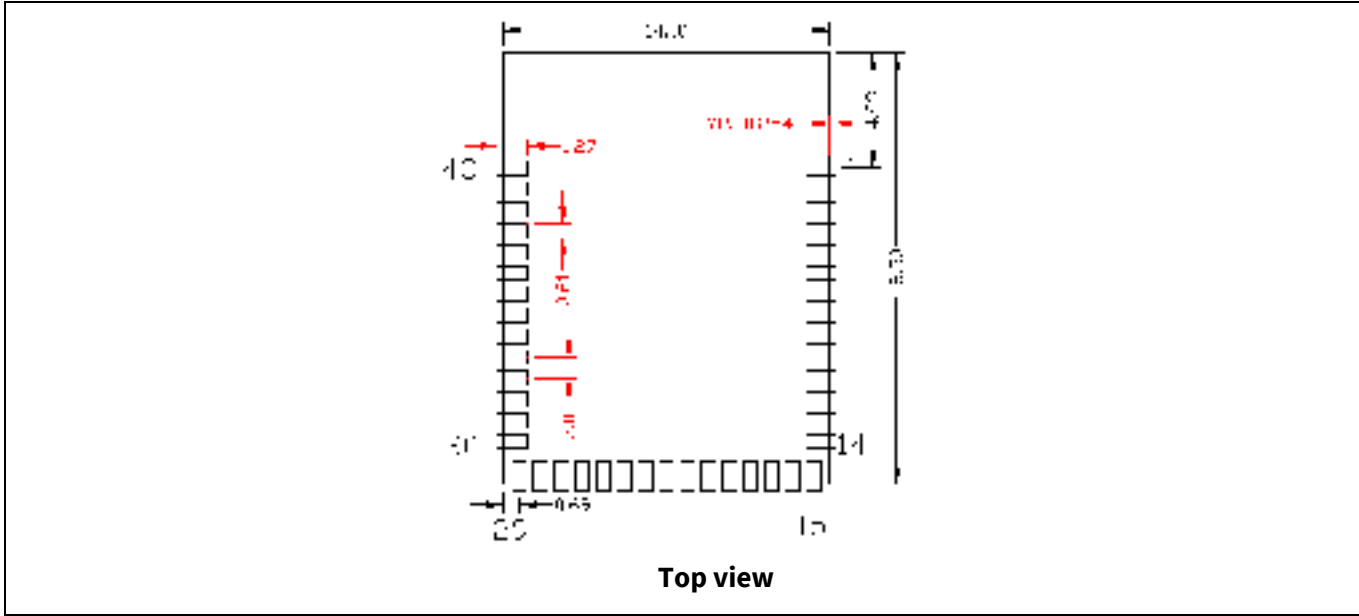


Figure 15 Host layout pattern for CYBLE-416070-02

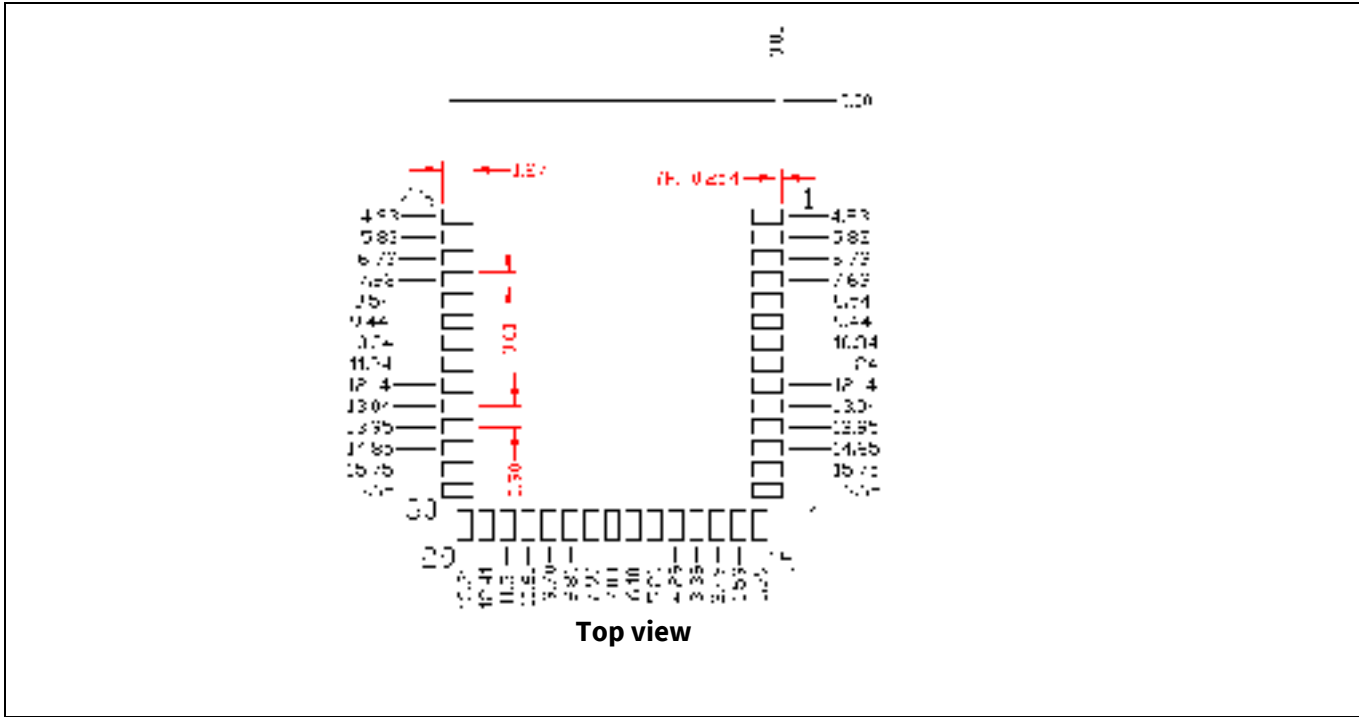


Figure 16 Module pad location from origin

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Recommended host PCB layout

**Table 9** provides the center location for each solder pad on the CYBLE-416070-02. All dimensions reference the to the center of the solder pad. Refer to **Figure 17** for the location of each module solder pad.

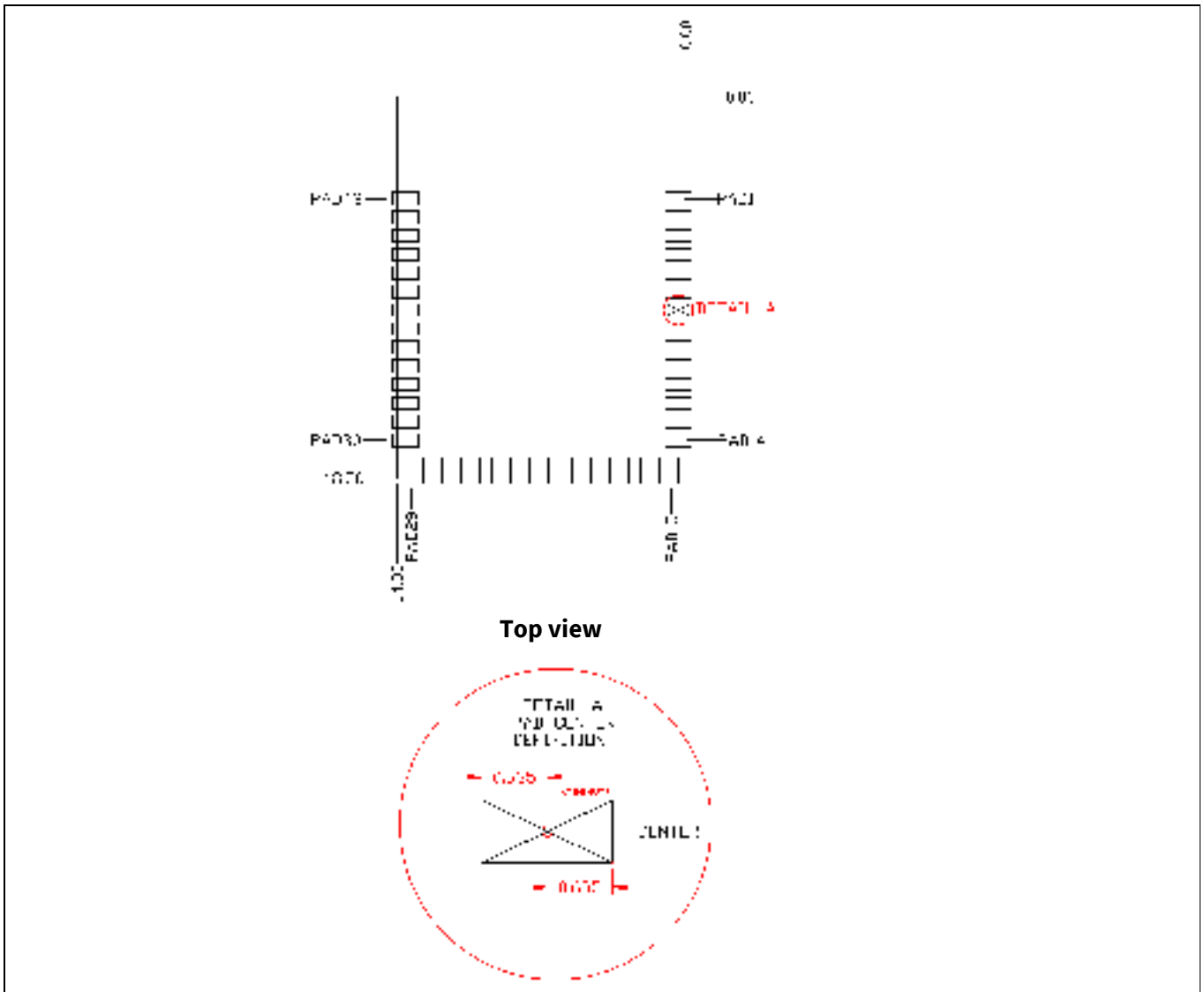
**Table 9**      **Module solder pad location**

| Solder pad<br>(Center of pad) | Location (X,Y) from<br>origin (mm) | Dimension from origin (mils) |
|-------------------------------|------------------------------------|------------------------------|
| 1                             | (0.38, 4.93)                       | (14.96, 194.09)              |
| 2                             | (0.38, 5.83)                       | (14.96, 229.53)              |
| 3                             | (0.38, 6.73)                       | (14.96, 264.96)              |
| 4                             | (0.38, 7.63)                       | (14.96, 300.39)              |
| 5                             | (0.38, 8.54)                       | (14.96, 336.22)              |
| 6                             | (0.38, 9.44)                       | (14.96, 371.65)              |
| 7                             | (0.38, 10.34)                      | (14.96, 407.09)              |
| 8                             | (0.38, 11.24)                      | (14.96, 442.52)              |
| 9                             | (0.38, 12.14)                      | (14.96, 477.95)              |
| 10                            | (0.38, 13.04)                      | (14.96, 513.38)              |
| 11                            | (0.38, 13.95)                      | (14.96, 549.21)              |
| 12                            | (0.38, 14.85)                      | (14.96, 584.64)              |
| 13                            | (0.38, 15.75)                      | (14.96, 620.08)              |
| 14                            | (0.38, 16.65)                      | (14.96, 655.51)              |
| 15                            | (0.69, 18.12)                      | (27.17, 713.38)              |
| 16                            | (1.59, 18.12)                      | (62.60, 713.38)              |
| 17                            | (2.49, 18.12)                      | (98.03, 713.38)              |
| 18                            | (3.39, 18.12)                      | (133.46, 713.38)             |
| 19                            | (4.29, 18.12)                      | (168.90, 713.38)             |
| 20                            | (5.20, 18.12)                      | (204.72, 713.38)             |
| 21                            | (6.10, 18.12)                      | (240.16, 713.38)             |
| 22                            | (7.00, 18.12)                      | (275.59, 713.38)             |
| 23                            | (7.90, 18.12)                      | (311.02, 713.38)             |
| 24                            | (8.80, 18.12)                      | (346.46, 713.38)             |
| 25                            | (9.70, 18.12)                      | (381.89, 713.38)             |
| 26                            | (10.61, 18.12)                     | (417.72, 713.38)             |
| 27                            | (11.51, 18.12)                     | (453.15, 713.38)             |
| 28                            | (12.41, 18.12)                     | (488.58, 713.38)             |
| 29                            | (13.31, 18.12)                     | (524.01, 713.38)             |
| 30                            | (13.62, 16.65)                     | (536.22, 655.51)             |
| 31                            | (13.62, 15.75)                     | (536.22, 620.08)             |
| 32                            | (13.62, 14.85)                     | (536.22, 584.64)             |
| 33                            | (13.62, 13.95)                     | (536.22, 549.21)             |
| 34                            | (13.62, 13.04)                     | (536.22, 513.38)             |
| 35                            | (13.62, 12.14)                     | (536.22, 477.95)             |
| 36                            | (13.62, 11.24)                     | (536.22, 442.52)             |
| 37                            | (13.62, 10.34)                     | (536.22, 407.09)             |

Recommended host PCB layout

**Table 9**      **Module solder pad location** *(continued)*

| Solder pad<br>(Center of pad) | Location (X,Y) from<br>origin (mm) | Dimension from origin (mils) |
|-------------------------------|------------------------------------|------------------------------|
| 38                            | (13.62, 9.44)                      | (536.22, 371.65)             |
| 39                            | (13.62, 8.54)                      | (536.22, 336.22)             |
| 40                            | (13.62, 7.63)                      | (536.22, 300.39)             |
| 41                            | (13.62, 6.73)                      | (536.22, 264.96)             |
| 42                            | (13.62, 5.83)                      | (536.22, 229.53)             |
| 43                            | (13.62, 4.93)                      | (536.22, 194.09)             |



**Figure 17**      **Solder pad reference location**

## 5 Digital and analog capabilities and connections

**Table 10** and **Table 11** detail the solder pad connection definitions and available functions for each connection pad. **Table 10** lists the solder pads on CYBLE-416070-02, the Bluetooth® LE device port-pin, and denotes whether the digital function shown is available for each solder pad. **Table 11** denotes whether the analog function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

**Table 10 Digital peripheral capabilities**

| Pad number | Device port pin     | UART  | SPI          | I <sup>2</sup> C | TCPWM <sup>[3, 4]</sup>                           | EXT_-CLK_IN | Audio     | SWD/JTAG    | GPIO |
|------------|---------------------|---|--------------|------------------|---|-------------|-----------|-------------|------|
| 1          | GND <sup>[5]</sup>  | Ground connection                                     |              |                  |   |             |           |             |      |
| 2          | P0.5                | –   | –            | –                | tcpwm[0].line_compl[2]<br>tcpwm[1].line_compl[2]  | ✓           | –         | –           | ✓    |
| 3          | V <sub>BACKUP</sub> | Battery backup domain input voltage (1.71 V to 3.6 V) |              |                  |   |             |           |             |      |
| 4          | V <sub>DD</sub>     | Power supply input voltage (1.71 V to 3.6 V)          |              |                  |   |             |           |             |      |
| 5          | P0.0                | –   | –            | –                | tcpwm[0].line[0]<br>tcpwm[1].line[0]              | ✓           | –         | –           | ✓    |
| 6          | P0.1                | –   | –            | –                | tcpwm[0].line_compl[0]<br>tcpwm[1].line_compl[0]  | –           | –         | ✓(JTAG RST) | ✓    |
| 7          | P10.3               | ✓(scb1_CTS)   | ✓(scb1_SS0)  | –                | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[23] | –           | –         | –           | ✓    |
| 8          | P10.4               | –   | ✓(scb1_SS1)  | –                | tcpwm[0].line[0]<br>tcpwm[1].line[0]              | –           | ✓PDM_CLK  | –           | ✓    |
| 9          | P9.3                | ✓(scb2_CTS)   | ✓(scb2_SS0)  | –                | tcpwm[0].line_compl[5]<br>tcpwm[1].line_compl[21] | –           | –         | –           | ✓    |
| 10         | P10.6               | –   | ✓(scb1_SS3)  | –                | tcpwm[0].line[1]<br>tcpwm[1].line[2]              | –           | –         | –           | ✓    |
| 11         | P10.5               | –   | ✓(scb1_SS2)  | –                | tcpwm[0].line_compl[0]<br>tcpwm[1].line_compl[0]  | –           | ✓PDM_DATA | –           | ✓    |
| 12         | P10.1               | ✓(scb1_TX)  | ✓(scb1_MISO) | ✓(scb1_SDA)      | tcpwm[0].line_compl[6]<br>tcpwm[1].line_compl[22] | –           | –         | –           | ✓    |

### Notes

- TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
- TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity.
- The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.

**Table 10** Digital peripheral capabilities (continued)

| Pad number | Device port pin  | UART                               | SPI                          | I <sup>2</sup> C          | TCPWM <sup>[3, 4]</sup>                           | EXT_-CLK_IN | Audio | SWD/JTAG    | GPIO |
|------------|------------------|------------------------------------|------------------------------|---------------------------|---|-------------|-------|-------------|------|
| 13         | P10.0            | ✓(scb1_RX)                         | ✓(scb1_MO SI)                | ✓(scb1_SCL)               | tcpwm[0].line[6]<br>tcpwm[1].line[22]             | -           | -     | -           | ✓    |
| 14         | P9.4             | -                                  | ✓(scb2_SS1)                  | -                         | tcpwm[0].line[7]<br>tcpwm[1].line[0]              | -           | -     | -           | ✓    |
| 15         | GND              | Ground connection                  |                              |                           |   |             |       |             |      |
| 16         | V <sub>REF</sub> | Voltage reference input (Optional) |                              |                           |   |             |       |             |      |
| 17         | P9.0             | ✓(scb2_RX)                         | ✓(scb2_MO SI)                | ✓(scb2_SCL)               | tcpwm[0].line[4]<br>tcpwm[1].line[20]             | -           | -     | -           | ✓    |
| 18         | P9.1             | ✓(scb2_TX)                         | ✓(scb2_MIS O)                | ✓(scb2_SDA)               | tcpwm[0].line_compl[4]<br>tcpwm[1].line_compl[20] | -           | -     | -           | ✓    |
| 19         | P9.5             | -                                  | ✓(scb2_SS2)                  | -                         | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[0]  | -           | -     | -           | ✓    |
| 20         | P9.6             | -                                  | ✓(scb2_SS3)                  | -                         | tcpwm[0].line[0]<br>tcpwm[1].line[1]              | -           | -     | -           | ✓    |
| 21         | P9.2             | ✓(scb2_RTS)                        | ✓(scb2_SCL K)                | -                         | tcpwm[0].line[5]<br>tcpwm[1].line[21]             | -           | -     | -           | ✓    |
| 22         | P7.2             | -                                  | -                            | -                         | tcpwm[0].line[5]<br>tcpwm[1].line[13]             | -           | -     | -           | ✓    |
| 23         | P7.1             | -                                  | -                            | -                         | tcpwm[0].line_compl[4]<br>tcpwm[1].line_compl[12] | -           | -     | -           | ✓    |
| 24         | P6.4             | ✓(scb6_RX)                         | ✓(scb6_MO SI)<br>(scb8_MOSI) | ✓(scb8_SCL)<br>(scb6_SCL) | tcpwm[0].line[2]<br>tcpwm[1].line[10]             | -           | -     | ✓(JTAG TDO) | ✓    |

**Notes**

- TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
- TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity.
- The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.

**Table 10** Digital peripheral capabilities (continued)

| Pad number | Device port pin | UART        | SPI                          | I <sup>2</sup> C           | TCPWM <sup>[3, 4]</sup>                           | EXT_-CLK_IN | Audio                    | SWD/JTAG                 | GPIO |
|------------|-----------------|-------------|------------------------------|----------------------------|---|-------------|--------------------------|--------------------------|------|
| 25         | P5.4            | –           | ✓(scb5_SS1)                  | –                          | tcpwm[0].line[6]<br>tcpwm[1].line[6]              | –           | ✓I <sup>2</sup> S_SCK_RX | –                        | ✓    |
| 26         | P6.7            | ✓(scb6_CTS) | ✓(scb6_SS0)<br>(scb8_SS0)    | –                          | tcpwm[0].line_compl[3]<br>tcpwm[1].line_compl[11] | –           | –                        | ✓(SWDCLK)<br>(JTAG TCLK) | ✓    |
| 27         | P6.6            | ✓(scb6_RTS) | ✓(scb6_SCL_K)<br>(scb8_SCLK) | –                          | tcpwm[0].line[3]<br>tcpwm[1].line[11]             | –           | –                        | ✓(SWDIO)<br>(JTAG TMS)   | ✓    |
| 28         | P6.2            |             | ✓(scb8_SCL_K)                | –                          | tcpwm[0].line[1]<br>tcpwm[1].line[9]              | –           | –                        | –                        | ✓    |
| 29         | P6.5            | ✓(scb6_TX)  | ✓(scb6_MISO)<br>(scb8_MISO)  | ✓(scb8_SDA)<br>✓(scb6_SDA) | tcpwm[0].line_compl[2]<br>tcpwm[1].line_compl[10] | –           | –                        | ✓(JTAG TDI)              | ✓    |
| 30         | P6.3            | –           | ✓(scb8_SS0)                  | –                          | tcpwm[0].line_compl[1]<br>tcpwm[1].line_compl[9]  | –           | –                        | –                        | ✓    |
| 31         | P7.7            | –           | –                            | –                          | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[15] | –           | –                        | –                        | ✓    |
| 32         | P5.6            | –           | ✓(scb5_SS3)                  | –                          | tcpwm[0].line[7]<br>tcpwm[1].line[7]              | –           | ✓I <sup>2</sup> S_SDI_RX | –                        | ✓    |
| 33         | P10.2           | ✓(scb1_RTS) | ✓(scb1_SCL_K)                | –                          | tcpwm[0].line[7]<br>tcpwm[1].line[23]             | –           | –                        | –                        | ✓    |
| 34         | P12.6           | –           | ✓(scb6_SS3)                  | –                          | tcpwm[0].line[7]<br>tcpwm[1].line[7]              | –           | –                        | –                        | ✓    |

**Notes**

- TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
- TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity.
- The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.



**Table 10** Digital peripheral capabilities (continued)

| Pad number | Device port pin    | UART                        | SPI             | I <sup>2</sup> C | TCPWM <sup>[3, 4]</sup>                          | EXT_-CLK_IN | Audio                    | SWD/JTAG | GPIO |
|------------|--------------------|-----------------------------|-----------------|------------------|--|-------------|--------------------------|----------|------|
| 35         | P12.7              | –                           | –               | –                | tcpwm[0].line_compl[7]<br>tcpwm[1].line_compl[7] | –           | –                        | –        | ✓    |
| 36         | P5.5               | –                           | ✓(scb5_5_SS2)   | –                | tcpwm[0].line_compl[6]<br>tcpwm[1].line_compl[6] | –           | ✓I <sup>2</sup> S_WS_RX  | –        | ✓    |
| 37         | P5.3               | ✓(scb5_5_CTS)               | ✓(scb5_5_SS0)   | –                | cpwm[0].line_compl[5]<br>tcpwm[1].line_compl[5]  | –           | ✓I <sup>2</sup> S_SDO_TX | –        | ✓    |
| 38         | P5.2               | ✓(scb5_5_RTS)               | ✓(scb5_5_SCL_K) | –                | tcpwm[0].line[5]<br>tcpwm[1].line[5]             | –           | ✓I2S_WS_TX               | –        | ✓    |
| 39         | P5.0               | ✓(scb5_5_RX)                | ✓(scb5_5_MO_Sl) | ✓(scb5_SCL)      | tcpwm[0].line[4]<br>tcpwm[1].line[4]             | –           | ✓I2S_EXT_CLK             | –        | ✓    |
| 40         | P5.1               | ✓(scb5_5_TX)                | ✓(scb5_5_MISO)  | ✓(scb5_SDA)      | tcpwm[0].line_compl[4]<br>tcpwm[1].line_compl[4] | –           | ✓I2S_CLK_TX              | –        | ✓    |
| 41         | P0.4               | –                           | –               | –                | tcpwm[0].line[2]<br>tcpwm[1].line[2]             | –           | –                        | –        | ✓    |
| 42         | XRES               | External reset (Active Low) |                 |                  |  |             |                          |          |      |
| 43         | GND <sup>[5]</sup> | Ground connection           |                 |                  |  |             |                          |          |      |

**Notes**

- TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
- TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity.
- The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.

**Table 11 Additional analog and digital capabilities**

| Pad number | Device port pin     | Analog functionality                                  | Universal digital block (UDB) | CAPSENSE™ | Smart IO     |
|------------|---------------------|---|-------------------------------|-----------|--------------|
| 1          | GND                 | Ground connection                                     |                               |           |              |
| 2          | P0.5                | –   | ✓                             | ✓         | –            |
| 3          | V <sub>BACKUP</sub> | Battery backup domain input voltage (1.71 V to 3.6 V) |                               |           |              |
| 4          | VDD                 | Power supply input voltage (1.71 V to 3.6 V)          |                               |           |              |
| 5          | P0.0                | wco_in  | ✓                             | ✓         | –            |
| 6          | P0.1                | wco_out   | ✓                             | ✓         | –            |
| 7          | P10.3               | sarmux[3]   | ✓                             | ✓         | –            |
| 8          | P10.4               | sarmux[4]   | ✓                             | ✓         | –            |
| 9          | P9.3                | ctb_oa1_out   | ✓                             | ✓         | SMARTIO10[3] |
| 10         | P10.6               | sarmux[6]   | ✓                             | ✓         | –            |
| 11         | P10.5               | sarmux[5]   | ✓                             | ✓         | –            |
| 12         | P10.1               | sarmux[1]   | ✓                             | ✓         | –            |
| 13         | P10.0               | sarmux[0]   | ✓                             | ✓         | –            |
| 14         | P9.4                | ctb_oa1-  | ✓                             | ✓         | SMARTIO9[4]  |
| 15         | GND                 | Ground connection                                     |                               |           |              |
| 16         | V <sub>REF</sub>    | Reference voltage input (Optional)                    |                               |           |              |
| 17         | P9.0                | ctb_oa0+  | ✓                             | ✓         | SMARTIO9[0]  |
| 18         | P9.1                | ctb_oa0-  | ✓                             | ✓         | SMARTIO9[1]  |
| 19         | P9.5                | ctb_oa1+  | ✓                             | ✓         | SMARTIO9[5]  |
| 20         | P9.6                | ctb_oa0+  | ✓                             | ✓         | SMARTIO9[6]  |
| 21         | P9.2                | ctb_oa0_out   | ✓                             | ✓         | SMARTIO9[2]  |
| 22         | P7.2                | csd.csh_tankpadd<br>csd.csh_tankpads                  | ✓                             | ✓         | –            |
| 23         | P7.1                | csd.cmodpadd<br>csd.cmodpads                          | ✓                             | ✓         | –            |
| 24         | P6.4                | –   | ✓                             | ✓         | –            |
| 25         | P5.4                | –   | ✓                             | ✓         | –            |
| 26         | P6.7                | –   | ✓                             | ✓         | –            |
| 27         | P6.6                | –   | ✓                             | ✓         | –            |
| 28         | P6.2                | lpcomp.inp_comp1                                      | ✓                             | ✓         | –            |
| 29         | P6.5                |   | ✓                             | ✓         | –            |
| 30         | P6.3                | lpcomp.inn_comp1                                      | ✓                             | ✓         | –            |
| 31         | P7.7                | csd.cshieldpads                                       | ✓                             | ✓         | –            |
| 32         | P5.6                | lpcomp.inp_comp0                                      | ✓                             | ✓         | –            |
| 33         | P10.2               | sarmux[2]   | ✓                             | ✓         | –            |
| 34         | P12.6               | –   | ✓                             | ✓         | –            |
| 35         | P12.7               | –   | ✓                             | ✓         | –            |
| 36         | P5.5                | –   | ✓                             | ✓         | –            |
| 37         | P5.3                | –   |                               |           | –            |

**Table 11**      **Additional analog and digital capabilities** *(continued)*

| Pad number | Device port pin | Analog functionality        | Universal digital block (UDB) | CAPSENSE™ | Smart IO |
|------------|-----------------|-----------------------------|-------------------------------|-----------|----------|
| 38         | P5.2            | –                           | ✓                             | ✓         | –        |
| 39         | P5.0            | –                           | ✓                             | ✓         | –        |
| 40         | P5.1            | –                           | ✓                             | ✓         | –        |
| 41         | P0.4            | –                           | ✓                             | ✓         | –        |
| 42         | XRES            | External reset (Active Low) |                               |           |          |
| 43         | GND             | Ground connection           |                               |           |          |

## 6 Power

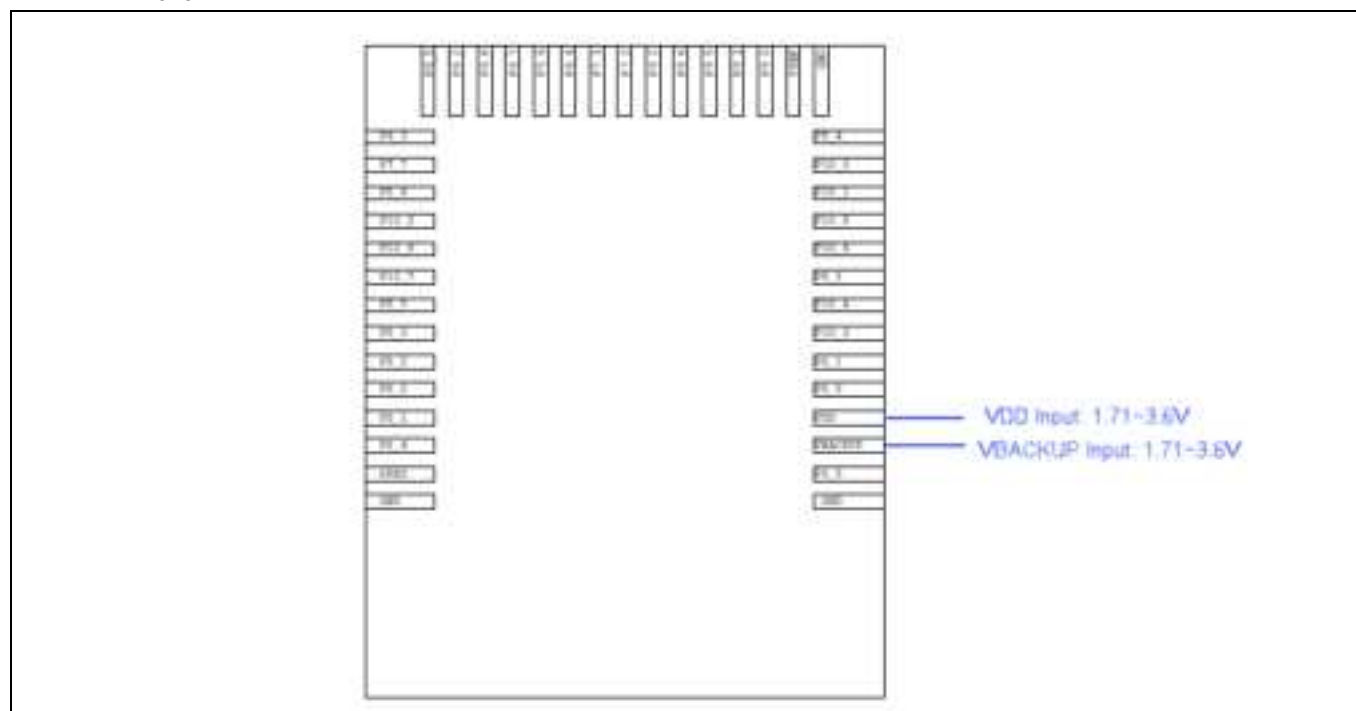
The power connection diagram (see [Figure 18](#)) shows the general requirements for power pins on the CYBLE-416070-02. The CYBLE-416070-02 contains a single power supply connection ( $V_{DD}$ ) and a backup voltage input ( $V_{BACKUP}$ ).

Description of the power pins is as follows:

- $V_{BACKUP}$  is the supply to the backup domain. The backup domain includes the 32-kHz WCO, real-time clock (RTC), and backup registers. It can generate a wakeup interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDD when not used as a separate battery backup domain.  $V_{BACKUP}$  provides the supply for Port 0.
- $V_{DD}$  is the main power supply input (1.71 V to 3.6 V). It provides the power input to the digital, analog, and radio domains. Isolation required for these domains is integrated on-module; therefore, no additional isolation is required for the CYBLE-416070-02.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All ground connections specified must be connected to system ground.

$V_{DD}$  and  $V_{BACKUP}$  may be shorted together externally. They are not required to be separate input voltages.

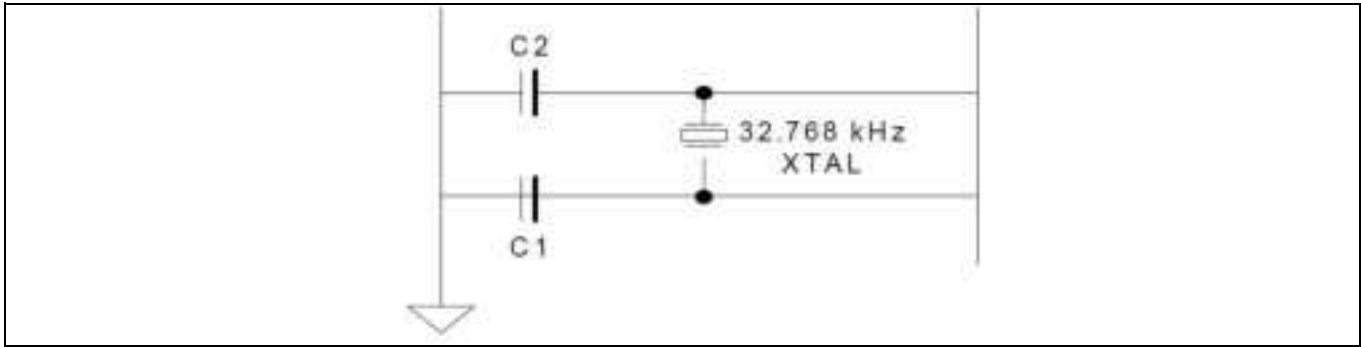


**Figure 18** CYBLE-416070-02 power connections

### 6.1 32-kHz crystal oscillator

The CYBLE-416070-02 includes connections for a 32-kHz oscillator to provide accurate timing during low-power operations. [Figure 19](#) shows the 32-kHz XTAL oscillator with external components and [Table 12](#) lists the oscillators characteristics. This oscillator can be operated with a 32-kHz or 32.768-kHz crystal oscillator, or be driven with a clock input at similar frequency. The XTAL must have an accuracy of  $\pm 250$  ppm or better according to the Bluetooth® LE specification over temperature and including aging. The values for C1 and C2 are used to fine-tune the oscillator. The external 32-kHz XTAL is optional, and the precision internal low-speed oscillator (PILO) can be used if precise timing is not required. Precise timing will improve overall system power consumption, as shown in [Table 17](#).

Power



**Figure 19** 32-kHz oscillator block diagram

**Table 12** XTAL oscillator characteristics

| Parameter   | Description                  | Minimum | Typical | Maximum | Unit       | Details/conditions |
|-------------|------------------------------|---------|---------|---------|------------|--------------------|
| $F_{WCO}$   | Crystal frequency            | –       | 32.768  | –       | kHz        |                    |
| $F_{TOL}$   | Frequency tolerance          | –       | 50      | –       | ppm        |                    |
| ESR         | Equivalent series resistance | –       | 70      | –       | k $\Omega$ |                    |
| PD          | Drive level                  | –       | –       | 1       | $\mu$ W    |                    |
| $T_{START}$ | Startup time                 | –       | –       | 500     | ms         |                    |
| $C_L$       | Crystal load capacitance     | 6       | –       | 12.5    | pF         |                    |
| $C_0$       | Crystal shunt capacitance    | –       | 1.35    | –       | pF         |                    |

Power

The CYBLE-416070-02 schematic is shown in [Figure 20](#).

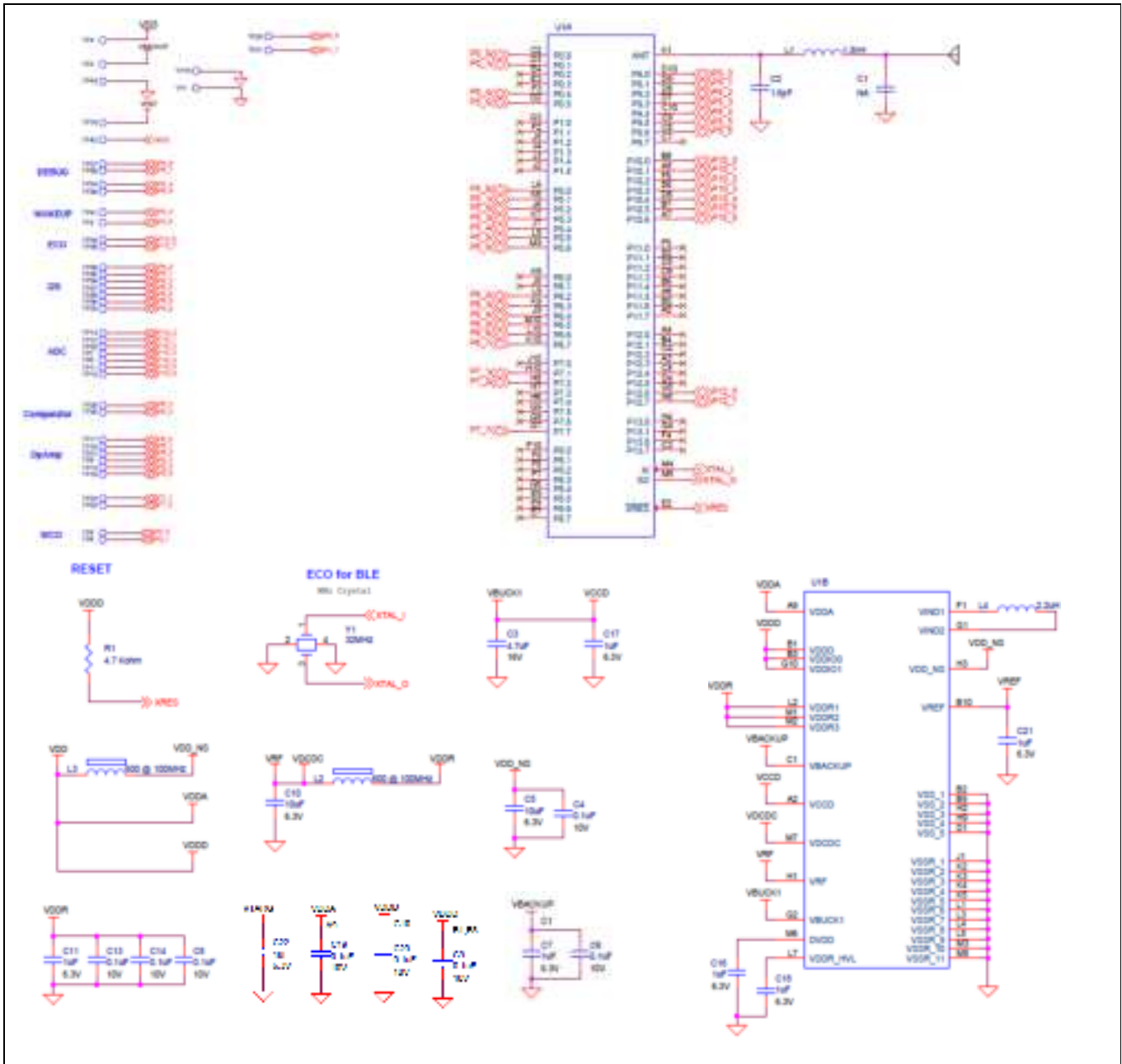


Figure 20 CYBLE-416070-02 schematic diagram

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 Power

## 6.2 Critical components list

**Table 13** details the critical components used in the CYBLE-416070-02 module.

**Table 13 Critical component list**

| Component | Reference designator | Description  |
|-----------|----------------------|--|
| Silicon   | U1                   | 116-pin BGA Programmable system-on-chip (PSoC™ 6 MCU) with Bluetooth® LE |
| Crystal   | Y1                   | 32.000 MHz, 10 PF  |

## 6.3 Antenna design

**Table 14** details the PCB trace antenna used on the CYBLE-416070-02 module.

**Table 14 Trace antenna specifications**

| Item            | Description      |
|-----------------|------------------|
| Frequency range | 2400 – 2500 MHz  |
| Peak gain       | –0.5 dBi typical |
| Return loss     | 10 dB minimum    |



## 7 Electrical specification

**Table 15** details the absolute maximum electrical characteristics for the Infineon Bluetooth® LE module.

**Table 15 CYBLE-416070-02 absolute maximum ratings<sup>[6]</sup>**

| Parameter                   | Description   | Min  | Typ | Max                     | Unit | Details/conditions                                     |
|-----------------------------|---|------|-----|-------------------------|------|--|
| V <sub>DDD_ABS</sub>        | V <sub>DD</sub> , V <sub>DDA</sub> , and V <sub>DDR</sub> supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> ) | −0.5 | –   | 4                       | V    | Absolute maximum                                       |
| V <sub>CCD_ABS</sub>        | Direct digital core voltage input relative to V <sub>SSD</sub>  | −0.5 | –   | 1.2                     | V    | Absolute maximum                                       |
| V <sub>DDD_RIPPLE</sub>     | Maximum power supply ripple for V <sub>DD</sub> , V <sub>DDA</sub> , and V <sub>DDR</sub> input voltage                             | –    | –   | 100                     | mV   | 3.0 V supply<br>Ripple frequency of 100 kHz to 750 kHz |
| V <sub>GPIO_ABS</sub>       | GPIO voltage  | −0.5 | –   | V <sub>DD</sub><br>+0.5 | V    | Absolute maximum                                       |
| I <sub>GPIO_ABS</sub>       | Maximum current per GPIO  | −25  | –   | 25                      | mA   | Absolute maximum                                       |
| I <sub>GPIO_injection</sub> | GPIO injection current per pin  | −0.5 | –   | 0.5                     | mA   | Absolute maximum<br>current injected per pin           |
| LU                          | Pin current for latch up  | −100 |     | 100                     | mA   | Absolute maximum                                       |

### Note

6. Usage above the absolute maximum conditions listed in **Table 15** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

### 7.1 Device-level specifications

All specifications are valid for −40°C ≤ TA ≤ 85°C and for 1.71 V to 3.6 V except where noted.

**Table 16 Power supply range, CPU current, and transition time specifications**

| Parameter                | Description   | Min  | Typ | Max  | Unit | Details/conditions                                  |
|--------------------------|---|------|-----|------|------|---|
| <b>DC specifications</b> |   |      |     |      |      |   |
| V <sub>DDD</sub>         | Internal regulator and Port 1 GPIO supply                         | 1.71 | –   | 3.6  | V    | –   |
| V <sub>DDA</sub>         | Analog power supply voltage. Shorted to V <sub>DDIOA</sub> on PCB | 1.71 | –   | 3.6  | V    | Internally unregulated supply                       |
| V <sub>DDIO1</sub>       | GPIO supply for Ports 5 to 8 when present                         | 1.71 | –   | 3.6  | V    | V <sub>DDIO_1</sub> must be ≥ to V <sub>DDA</sub> . |
| V <sub>DDIO0</sub>       | GPIO supply for Ports 11 to 13 when present                       | 1.71 | –   | 3.6  | V    |   |
| V <sub>DDIO0</sub>       | Supply for eFuse programming                                      | 2.38 | 2.5 | 2.62 | V    | eFuse programming voltage                           |
| V <sub>DDIOR</sub>       | GPIO supply for Ports 2 to 4 on BGA 124 only                      | 1.71 | –   | 3.6  | V    | –   |
| V <sub>DDIOA</sub>       | GPIO supply for Ports 9 to 10. Shorted to V <sub>DDA</sub> on PCB | 1.71 | –   | 3.6  | V    | –   |
| V <sub>BACKUP</sub>      | Backup power and GPIO Port 0 supply when present                  | 1.71 | –   | 3.6  | V    | Minimum is 1.4 V in Backup mode                     |
| V <sub>CCD1</sub>        | Output voltage (for core logic bypass)                            | –    | 1.1 | –    | V    | High-speed mode                                     |

## Electrical specification

**Table 16 Power supply range, CPU current, and transition time specifications** (continued)

| Parameter         | Description   | Min | Typ | Max | Unit | Details/conditions              |
|-------------------|---|-----|-----|-----|------|---------------------------------|
| V <sub>CCD2</sub> | Output voltage (for core logic bypass)                | –   | 0.9 | –   |      | ULP mode. Valid for –20 to 85°C |
| C <sub>EFC</sub>  | External regulator voltage (V <sub>CCD</sub> ) bypass | 3.8 | 4.7 | 5.6 | μF   | X5R ceramic or better           |
| C <sub>EXC</sub>  | Power supply decoupling capacitor                     | –   | 10  | –   | μF   | X5R ceramic or better           |

**LP range power specifications (for V<sub>CCD</sub> = 1.1 V with buck and LDO)**
**Cortex®-M4 - Active mode**
**Execute with cache disabled (Flash)**

|                  |  |   |     |     |    |  |
|------------------|--|---|-----|-----|----|--|
| I <sub>DD1</sub> | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. While(1) | – | 2.3 | 3.2 | mA | V <sub>DD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                  |  | – | 3.1 | 3.6 |    | V <sub>DD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                  |  | – | 4.2 | 5.1 |    | V <sub>DD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD2</sub> | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1)           | – | 0.9 | 1.5 | mA | V <sub>DD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                  |  | – | 1.2 | 1.6 |    | V <sub>DD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                  |  | – | 1.6 | 2.4 |    | V <sub>DD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |

**Execute with cache enabled**

|                  |  |   |      |      |    |  |
|------------------|--|---|------|------|----|--|
| I <sub>DD3</sub> | Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO and FLL. Dhrystone  | – | 6.3  | 7    | mA | V <sub>DD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                  |  | – | 9.7  | 11.2 |    | V <sub>DD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                  |  | – | 13.2 | 13.7 |    | V <sub>DD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD4</sub> | Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100 MHz. IMO and FLL. Dhrystone | – | 4.8  | 5.8  | mA | V <sub>DD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                  |  | – | 7.4  | 8.4  |    | V <sub>DD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                  |  | – | 10.1 | 10.7 |    | V <sub>DD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD5</sub> | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. IMO and FLL. Dhrystone   | – | 2.4  | 3.4  | mA | V <sub>DD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                  |  | – | 3.7  | 4.1  |    | V <sub>DD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                  |  | – | 5.1  | 5.8  |    | V <sub>DD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD6</sub> | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone             | – | 0.90 | 1.5  | mA | V <sub>DD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                  |  | – | 1.27 | 1.75 |    | V <sub>DD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                  |  | – | 1.8  | 2.6  |    | V <sub>DD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |

**Cortex®-M0+. Active mode**

## Electrical specification

**Table 16 Power supply range, CPU current, and transition time specifications** (continued)

| Parameter                           | Description  | Min | Typ  | Max | Unit | Details/conditions                                |
|-------------------------------------|--|-----|------|-----|------|---|
| Execute with cache disabled (Flash) |  |     |      |     |      |   |
| I <sub>DD7</sub>                    | Execute from Flash;CM4 OFF, CM0+ Active 50 MHz. With IMO and FLL. While (1). | –   | 2.4  | 3.3 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 3.2  | 3.7 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 4.1  | 4.8 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD8</sub>                    | Execute from Flash;CM4 OFF, CM0+ Active 8 MHz. With IMO. While (1)           | –   | 0.8  | 1.5 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 1.1  | 1.6 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 1.45 | 1.9 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| Execute with cache enabled          |  |     |      |     |      |   |
| I <sub>DD9</sub>                    | Execute from Cache;CM4 OFF, CM0+ Active 100 MHz. With IMO and FLL. Dhrystone | –   | 3.8  | 4.5 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 5.9  | 6.5 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 7.7  | 8.2 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD10</sub>                   | Execute from Cache;CM4 OFF, CM0+ Active 8 MHz. With IMO. Dhrystone           | –   | 0.80 | 1.3 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 1.2  | 1.7 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 1.41 | 2   |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| Cortex®-M4. Sleep mode              |  |     |      |     |      |   |
| I <sub>DD11</sub>                   | CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO and FLL                       | –   | 1.5  | 2.2 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 2.2  | 2.7 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 2.9  | 3.5 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD12</sub>                   | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL                        | –   | 1.20 | 1.9 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 1.70 | 2.2 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 2.20 | 2.8 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD13</sub>                   | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO                                  | –   | 0.7  | 1.3 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                                     |  | –   | 0.96 | 1.5 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                                     |  | –   | 1.22 | 2   |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |

## Electrical specification

**Table 16 Power supply range, CPU current, and transition time specifications** (continued)

| Parameter                                | Description  | Min | Typ  | Max  | Unit | Details/conditions                                |
|--|--|-----|------|------|------|---|
| Cortex®-M0+. Sleep mode                  |  |     |      |      |      |   |
| I <sub>DD14</sub>                        | CM4 Off, CM0+ Sleep 50 MHz. With IMO and FLL                             | –   | 1.3  | 2    | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|  |  | –   | 1.94 | 2.4  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|  |  | –   | 2.57 | 3.2  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD15</sub>                        | CM4 Off, CM0+ Sleep 8 MHz. With IMO                                      | –   | 0.7  | 1.3  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|  |  | –   | 0.95 | 1.5  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|  |  | –   | 1.25 | 2    |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| Cortex®-M4. Low-Power Active (LPA) mode  |  |     |      |      |      |   |
| I <sub>DD16</sub>                        | Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1) | –   | 0.85 | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|  |  | –   | 1.18 | 1.65 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|  |  | –   | 1.63 | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD17</sub>                        | Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone | –   | 0.90 | 1.5  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|  |  | –   | 1.27 | 1.75 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|  |  | –   | 1.77 | 2.5  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| Cortex®-M0+. Low-Power Active (LPA) mode |  |     |      |      |      |   |
| I <sub>DD18</sub>                        | Execute from Flash; CM4 Off, CM0+ LPA 8 MHz. With IMO. While (1)         | –   | 0.8  | 1.4  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|  |  | –   | 1.14 | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|  |  | –   | 1.6  | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| I <sub>DD19</sub>                        | Execute from Cache; CM4 Off, CM0+ LPA 8 MHz. With IMO. Dhrystone         | –   | 0.8  | 1.4  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|  |  | –   | 1.15 | 1.65 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|  |  | –   | 1.62 | 2.4  |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |
| Cortex®-M4. Low-Power Sleep (LPS) mode   |  |     |      |      |      |   |

## Electrical specification

**Table 16 Power supply range, CPU current, and transition time specifications (continued)**

| Parameter         | Description                             | Min | Typ  | Max | Unit | Details/conditions                                |
|-------------------|---|-----|------|-----|------|---|
| I <sub>DD20</sub> | CM4 LPS 8 MHz, CM0+ LPS 8 MHz. With IMO | –   | 0.65 | 1.1 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                   |   | –   | 0.95 | 1.5 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                   |   | –   | 1.31 | 2.1 |      | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |

**Cortex®-M0+. Low-Power Sleep (LPS) Mode**

|                   |                                   |   |      |      |    |   |
|-------------------|-----------------------------------|---|------|------|----|---|
| I <sub>DD22</sub> | CM4 OFF, CM0+ LPS 8 MHz. With IMO | – | 0.64 | 1.1  | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C    |
|                   |                                   | – | 0.93 | 1.45 |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C    |
|                   |                                   | – | 1.29 | 2    |    | V <sub>DDD</sub> = 1.8 to 3.3 V, LDO, max at 60°C |

**ULP range power specifications (for V<sub>CCD</sub> = 0.9 V using the Buck). ULP Mode is valid from -20 to +85°C.**
**Cortex®-M4. Active mode**
**Execute with cache disabled (Flash)**

|                  |  |   |      |     |    |  |
|------------------|--|---|------|-----|----|--|
| I <sub>DD3</sub> | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. While(1) | – | 1.7  | 2.2 | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|                  |  | – | 2.1  | 2.4 |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD4</sub> | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1)          | – | 0.56 | 0.8 | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|                  |  | – | 0.75 | 1   |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |

**Execute with cache enabled**

|                   |   |   |      |     |    |  |
|-------------------|---|---|------|-----|----|--|
| I <sub>DD10</sub> | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. Dhrystone | – | 1.6  | 2.2 | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|                   |   | – | 2.4  | 2.7 |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD11</sub> | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone           | – | 0.65 | 0.8 | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|                   |   | – | 0.8  | 1.1 |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |

**Cortex®-M0+. Active mode**
**Execute with cache disabled (Flash)**

|                   |   |   |      |      |    |  |
|-------------------|---|---|------|------|----|--|
| I <sub>DD16</sub> | Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO and FLL. Write(1) | – | 1.00 | 1.4  | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|                   |   | – | 1.34 | 1.6  |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD17</sub> | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1)          | – | 0.54 | 0.75 | mA | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|                   |   | – | 0.73 | 1    |    | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |

## Electrical specification

**Table 16 Power supply range, CPU current, and transition time specifications** (continued)

| Parameter                                       | Description  | Min | Typ  | Max  | Unit | Details/conditions                             |
|---|--|-----|------|------|------|--|
| Execute with cache enabled                      |  |     |      |      |      |  |
| I <sub>DD18</sub>                               | Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO and FLL. Dhrystone | –   | 0.91 | 1.25 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 1.34 | 1.6  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD19</sub>                               | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone          | –   | 0.51 | 0.72 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.73 | 0.95 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| Cortex®-M4. Sleep mode                          |  |     |      |      |      |  |
| I <sub>DD21</sub>                               | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL                        | –   | 0.76 | 1.1  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 1.1  | 1.4  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD22</sub>                               | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO                                  | –   | 0.42 | 0.65 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.59 | 0.8  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| Cortex®-M0+. Sleep mode                         |  |     |      |      |      |  |
| I <sub>DD23</sub>                               | CM4 Off, CM0+ Sleep 25 MHz. With IMO and FLL                                 | –   | 0.62 | 0.9  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.88 | 1.1  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD24</sub>                               | CM4 Off, CM0+ Sleep 8 MHz. With IMO  | –   | 0.41 | 0.6  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.58 | 0.8  |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| Cortex®-M4. Ultra Low-Power Active (ULPA) mode  |  |     |      |      |      |  |
| I <sub>DD25</sub>                               | Execute from Flash. CM4 ULPA 8 MHz, CM0+ ULPS 8 MHz. With IMO. While(1)      | –   | 0.52 | 0.75 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.76 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD26</sub>                               | Execute from Cache. CM4 ULPA 8 MHz, CM0+ ULPS 8 MHz. With IMO. Dhrystone     | –   | 0.54 | 0.76 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.78 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| Cortex®-M0+. Ultra Low-Power Active (ULPA) mode |  |     |      |      |      |  |
| I <sub>DD27</sub>                               | Execute from Flash. CM4 OFF, CM0+ ULPA 8 MHz. With IMO. While (1)            | –   | 0.51 | 0.75 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.75 | 1    |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| I <sub>DD28</sub>                               | Execute from Cache. CM4 OFF, CM0+ ULPA 8 MHz. With IMO. Dhrystone            | –   | 0.48 | 0.7  | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|   |  | –   | 0.7  | 0.95 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |

## Electrical specification

**Table 16 Power supply range, CPU current, and transition time specifications (continued)**

| Parameter                                      | Description  | Min | Typ  | Max | Unit | Details/conditions                             |
|--|--|-----|------|-----|------|--|
| Cortex®-M4. Ultra Low-Power Sleep (ULPS) mode  |  |     |      |     |      |  |
| I <sub>DD29</sub>                              | CM4 ULPS 8 MHz, CM0 ULPS 8 MHz. With IMO           | –   | 0.4  | 0.6 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|  |  | –   | 0.57 | 0.8 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| Cortex®-M0+. Ultra Low-Power Sleep (ULPS) mode |  |     |      |     |      |  |
| I <sub>DD31</sub>                              | CM4 Off, CM0+ ULPS 8 MHz. With IMO.                | –   | 0.39 | 0.6 | mA   | V <sub>DDD</sub> = 3.3 V, Buck ON, max at 60°C |
|  |  | –   | 0.56 | 0.8 |      | V <sub>DDD</sub> = 1.8 V, Buck ON, max at 60°C |
| Deep Sleep mode                                |  |     |      |     |      |  |
| I <sub>DD33A</sub>                             | With internal Buck enabled and 64K SRAM retention  | –   | 7    | –   | μA   | Max value is at 85°C                           |
| I <sub>DD33A_B</sub>                           | With internal Buck enabled and 64K SRAM retention  | –   | 7    | –   | μA   | Max value is at 60°C                           |
| I <sub>DD33B</sub>                             | With internal Buck enabled and 256K SRAM retention | –   | 9    | –   | μA   | Max value is at 85°C                           |
| I <sub>DD33B_B</sub>                           | With internal Buck enabled and 256K SRAM retention | –   | 9    | –   | μA   | Max value is at 60°C                           |
| Hibernate mode                                 |  |     |      |     |      |  |
| I <sub>DD34</sub>                              | V <sub>DDD</sub> = 1.8 V                           | –   | 300  | –   | nA   | No clocks running                              |
| I <sub>DD34A</sub>                             | V <sub>DDD</sub> = 3.3 V                           | –   | 800  | –   | nA   | No clocks running                              |
| Power mode transition times                    |  |     |      |     |      |  |
| T <sub>LPACT_ACT</sub>                         | Low-Power Active to Active transition time         | –   | –    | 35  | μs   | Including PLL lock time                        |
| T <sub>DS_LPACT</sub>                          | Deep Sleep to LP Active transition time            | –   | –    | 25  | μs   | Guaranteed by design                           |
| T <sub>DS_ACT</sub>                            | Deep Sleep to Active transition time               | –   | –    | 25  | μs   | Guaranteed by design                           |
| T <sub>HIB_ACT</sub>                           | Hibernate to Active transition time                | –   | 500  | –   | μs   | Including PLL lock time                        |

### 7.1.1 Module level power consumption

Test condition: V<sub>DDD</sub> = 3.3 V, Execute from Cache, WCO Enable

**Table 17 Module level power consumption**

| Test items                | Specification (1.1 V LDO) |        | Specification (1.1 V Buck) |        | Condition                    |
|---------------------------|---------------------------|--------|----------------------------|--------|------------------------------|
|                           | Typ                       | Max    | Typ                        | Max    |                              |
| CM0 Power mode transition |                           |        |                            |        |                              |
| Active                    | 7.7 mA                    | 8.2 mA | 3.8 mA                     | 4.5 mA | CM4 Off, CM0+ Active 100 MHz |
| Sleep                     | 2.57 mA                   | 3.2 mA | 1.3 mA                     | 2 mA   | CM4 Off, CM0+ Sleep 50 MHz   |
| Low-Power Active          | 1.62 mA                   | 2.4 mA | 0.8 mA                     | 1.4 mA | CM4 Off, CM0+ LPA 8 MHz      |
| Low-Power Sleep           | 1.29 mA                   | 2 mA   | 0.64 mA                    | 1.1 mA | CM4 Off, CM0+ LPS 8 MHz      |
| CM4 Power mode transition |                           |        |                            |        |                              |



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Electrical specification

**Table 17**      **Module level power consumption** *(continued)*

| Test items       | Specification (1.1 V LDO) |         | Specification (1.1 V Buck) |        | Condition                              |
|------------------|---------------------------|---------|----------------------------|--------|--|
|                  | Typ                       | Max     | Typ                        | Max    |  |
| Active           | 10.1 mA                   | 10.7 mA | 4.8 mA                     | 5.8 mA | CM4 Active 100 MHz, CM0+ Sleep 100 MHz |
| Sleep            | 2.9 mA                    | 3.5 mA  | 1.5 mA                     | 2.2 mA | CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz   |
| Low-Power Active | 1.77 mA                   | 2.5 mA  | 0.9 mA                     | 1.5 mA | CM4 LPA 8 MHz, CM0+ Sleep 8 MHz        |
| Low-Power Sleep  | 1.31 mA                   | 2.1 mA  | 0.65 mA                    | 1.1 mA | CM4 LPS 8 MHz, CM0+ LPS 8 MHz          |

**Bluetooth® LE RF current (DIRECT\_TEST\_MODE)**

|                   |         |  |        |  |             |
|-------------------|---------|--|--------|--|-------------|
| TX (0dBm, 1 Mbps) | 10 mA   |  | 5.7 mA |  | HCI Command |
| TX (0dBm, 2 Mbps) | 10 mA   |  | 5.7 mA |  |             |
| RX (1 Mbps)       | 11 mA   |  | 6.7 mA |  | HCI Command |
| RX (2 Mbps)       | 11.3 mA |  | 7 mA   |  |             |

**System level Bluetooth® LE (System\_Level)**

| Test items                 | PILO (1.1 V Buck) |        | WCO (1.1 V Buck) |        | Condition                    |
|----------------------------|-------------------|--------|------------------|--------|------------------------------|
|                            | Typ               | Max    | Typ              | Max    |                              |
| Deep Sleep                 | 90 µA             | 120 µA | 7 µA             | 14 µA  |                              |
| Adv 1.28s interval         | 80 µA             | 121 µA | 21 µA            | 28 µA  | 32 bytes, 0 dBm, 3.3 V, Buck |
| 300 ms connection interval | 170 µA            | 305 µA | 28 µA            | 34 µA  | 0 byte, 0 dBm, 3.3 V, Buck   |
| 1s connection interval     | 75 µA             | 106 µA | 18 µA            | 23 µA  |                              |
| 4s connection interval     | 75 µA             | 106 µA | 14 µA            | 19 µA  |                              |
| Hibernate                  | 1.2 µA            | 1.8 µA | 2.0 µA           | 2.3 µA |                              |

## Electrical specification

### 7.1.2 XRES

**Table 18 XRES**

| Parameter                               | Description   | Min                | Typ | Max                | Unit    | Details/conditions      |
|---|---|--------------------|-----|--------------------|---------|-------------------------|
| <b>XRES (Active Low) specifications</b> |   |                    |     |                    |         |                         |
| <b>XRES AC specifications</b>           |   |                    |     |                    |         |                         |
| $T_{XRES\_ACT}$                         | POR or XRES release to active transition time       | –                  | 750 | –                  | $\mu s$ | Normal mode, 50 MHz M0+ |
| $T_{XRES\_PW}$                          | XRES Pulse width                                    | 5                  | –   | –                  | $\mu s$ | –                       |
| <b>XRES DC specifications</b>           |   |                    |     |                    |         |                         |
| $T_{XRES\_IDD}$                         | $I_{DD}$ when XRES asserted                         | –                  | 300 | –                  | nA      | $V_{DDD} = 1.8 V$       |
| $T_{XRES\_IDD\_1}$                      | $I_{DD}$ when XRES asserted                         | –                  | 800 | –                  | nA      | $V_{DDD} = 3.3 V$       |
| $V_{IH}$                                | Input voltage high threshold                        | $0.7 \cdot V_{DD}$ | –   | –                  | V       | CMOS Input              |
| $V_{IL}$                                | Input voltage low threshold                         | –                  | –   | $0.3 \cdot V_{DD}$ | V       | CMOS Input              |
| $C_{IN}$                                | Input capacitance                                   | –                  | 3   | –                  | pF      | –                       |
| $V_{HYSXRES}$                           | Input voltage hysteresis                            | –                  | 100 | –                  | mV      | –                       |
| $I_{DIODE}$                             | Current through protection diode to $V_{DD}/V_{SS}$ | –                  | –   | 100                | $\mu A$ | –                       |

#### Notes

- Infineon-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25  $\mu s$ ) before transition to Application code. With an 8-MHz CPU clock (LP Active), the time before user code executes is  $25 + 12.5 = 37.5 \mu s$ .
- Infineon-supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25  $\mu s$ ) before transition to Application code. With a 25-MHz CPU clock (FLL), the time before user code executes is  $25 + 4 = 29 \mu s$ . With a 100-MHz CPU clock, the time is  $25 + 1 = 26 \mu s$ .

## Electrical specification

### 7.1.3 GPIO

**Table 19 GPIO specifications**

| Parameter                     | Description   | Min             | Typ | Max            | Unit | Details/conditions   |
|-------------------------------|---|-----------------|-----|----------------|------|--|
| <b>GPIO DC specifications</b> |   |                 |     |                |      |  |
| $V_{IH}$                      | Input voltage high threshold                          | $0.7 * V_{DD}$  | –   | –              | V    | CMOS Input   |
| $I_{IHS}$                     | Input current when Pad > VDDIO for OVT inputs         | –               | –   | 10             | μA   | Per I <sup>2</sup> C Spec  |
| $V_{IL}$                      | Input voltage low threshold                           | –               | –   | $0.3 * V_{DD}$ | V    | CMOS Input   |
| $V_{IH}$                      | LVTTL input, $V_{DD} < 2.7$ V                         | $0.7 * V_{DD}$  | –   | –              | V    | –  |
| $V_{IL}$                      | LVTTL input, $V_{DD} < 2.7$ V                         | –               | –   | $0.3 * V_{DD}$ | V    | –  |
| $V_{IH}$                      | LVTTL input, $V_{DD} \geq 2.7$ V                      | 2.0             | –   | –              | V    | –  |
| $V_{IL}$                      | LVTTL input, $V_{DD} \geq 2.7$ V                      | –               | –   | 0.8            | V    | –  |
| $V_{OH}$                      | Output voltage high level                             | $V_{DD} - 0.5$  | –   | –              | V    | $I_{OH} = 8$ mA  |
| $V_{OL}$                      | Output voltage low level                              | –               | –   | 0.4            | V    | $I_{OL} = 8$ mA  |
| $R_{PULLUP}$                  | Pull-up resistor                                      | 3.5             | 5.6 | 8.5            | kΩ   | –  |
| $R_{PULLDOWN}$                | Pull-down resistor                                    | 3.5             | 5.6 | 8.5            | kΩ   | –  |
| $I_{IL}$                      | Input leakage current (absolute value)                | –               | –   | 2              | nA   | 25 °C, $V_{DD} = 3.0$ V  |
| $I_{IL\_CTBM}$                | Input leakage on CTBm input pins                      | –               | –   | 4              | nA   | –  |
| $C_{IN}$                      | Input Capacitance                                     | –               | –   | 5              | pF   | –  |
| $V_{HYSTTL}$                  | Input hysteresis LVTTL $V_{DD} > 2.7$ V               | 100             | 0   | –              | mV   | –  |
| $V_{HYSCMOS}$                 | Input hysteresis CMOS                                 | $0.05 * V_{DD}$ | –   | –              | mV   | –  |
| $I_{DIODE}$                   | Current through protection diode to $V_{DD}/V_{SS}$   | –               | –   | 100            | μA   | –  |
| $I_{TOT\_GPIO}$               | Maximum Total Source or Sink Chip Current             | –               | –   | 200            | mA   | –  |
| <b>GPIO AC specifications</b> |   |                 |     |                |      |  |
| $T_{RISEF}$                   | Rise time in Fast Strong mode. 10% to 90% of $V_{DD}$ | –               | –   | 2.5            | ns   | $C_{load} = 15$ pF, 8 mA drive strength                                |
| $T_{FALLF}$                   | Fall time in Fast Strong mode. 10% to 90% of $V_{DD}$ | –               | –   | 2.5            | ns   | $C_{load} = 15$ pF, 8 mA drive strength                                |
| $T_{RISES\_1}$                | Rise time in Slow Strong mode. 10% to 90% of $V_{DD}$ | 52              | –   | 142            | ns   | $C_{load} = 15$ pF, 8 mA drive strength, $V_{DD} \leq 2.7$ V           |
| $T_{RISES\_2}$                | Rise time in Slow Strong mode. 10% to 90% of $V_{DD}$ | 48              | –   | 102            | ns   | $C_{load} = 15$ pF, 8 mA drive strength, $2.7$ V < $V_{DD} \leq 3.6$ V |
| $T_{FALLS\_1}$                | Fall time in Slow Strong mode. 10% to 90% of $V_{DD}$ | 44              | –   | 211            | ns   | $C_{load} = 15$ pF, 8 mA drive strength, $V_{DD} \leq 2.7$ V           |
| $T_{FALLS\_2}$                | Fall time in Slow Strong mode. 10% to 90% of $V_{DD}$ | 42              | –   | 93             | ns   | $C_{load} = 15$ pF, 8 mA drive strength, $2.7$ V < $V_{DD} \leq 3.6$ V |

## Electrical specification

**Table 19** GPIO specifications (continued)

| Parameter       | Description   | Min                   | Typ | Max  | Unit | Details/conditions                                |
|-----------------|---|-----------------------|-----|------|------|---|
| $T_{FALL\_I2C}$ | Fall time (30% to 70% of $V_{DD}$ ) in Slow Strong mode                         | $20 \cdot V_{DDIO}/5$ | –   | 250  | ns   | $C_{load} = 10$ pF to 400 pF, 8-mA drive strength |
| $F_{GPIOOUT1}$  | GPIO $F_{out}$ , Fast Strong mode   | –                     | –   | 100  | MHz  | 90/10%, 15-pF load, 60/40 duty cycle              |
| $F_{GPIOOUT2}$  | GPIO $F_{out}$ ; Slow Strong mode   | –                     | –   | 16.7 | MHz  | 90/10%, 15-pF load, 60/40 duty cycle              |
| $F_{GPIOOUT3}$  | GPIO $F_{out}$ ; Fast Strong mode   | –                     | –   | 7    | MHz  | 90/10%, 25-pF load, 60/40 duty cycle              |
| $F_{GPIOOUT4}$  | GPIO $F_{out}$ ; Slow Strong mode   | –                     | –   | 3.5  | MHz  | 90/10%, 25-pF load, 60/40 duty cycle              |
| $F_{GPIOIN}$    | GPIO input operating frequency; $1.71 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ | –                     | –   | 100  | MHz  | 90/10% $V_{IO}$                                   |

## 7.2 Analog peripherals

### 7.2.1 Opamp

**Table 20** Opamp specifications

| Parameter           | Description                                       | Min | Typ  | Max           | Unit          | Details/conditions |
|---------------------|---|-----|------|---------------|---------------|--------------------|
| $I_{DD}$            | Opamp block current. No load.                     | –   | –    | –             | –             | –                  |
| $I_{DD\_HI}$        | Power = HI  | –   | 1300 | 1500          | $\mu\text{A}$ | –                  |
| $I_{DD\_MED}$       | Power = MED                                       | –   | 450  | 600           | $\mu\text{A}$ | –                  |
| $I_{DD\_LOW}$       | Power = LO  | –   | 250  | 350           | $\mu\text{A}$ | –                  |
| GBW                 | Load = 20 pF, 0.1 mA<br>$V_{DDA} = 2.7 \text{ V}$ | –   | –    | –             | –             | –                  |
| $G_{BW\_HI}$        | Power = HI  | 6   | –    | –             | MHz           | –                  |
| $G_{BW\_MED}$       | Power = MED                                       | 4   | –    | –             | MHz           | –                  |
| $G_{BW\_LO}$        | Power = LO  | –   | 1    | –             | MHz           | –                  |
| $I_{OUT\_MAX}$      | $V_{DDA} \geq 2.7 \text{ V}$ , 500 mV from rail   | –   | –    | –             | –             | –                  |
| $I_{OUT\_MAX\_HI}$  | Power = HI  | –   | –    | –             | mA            | –                  |
| $I_{OUT\_MAX\_MID}$ | Power = MID                                       | 10  | –    | –             | mA            | –                  |
| $I_{OUT\_MAX\_LO}$  | Power = LO  | –   | 5    | –             | mA            | –                  |
| $I_{OUT}$           | $V_{DDA} = 1.71 \text{ V}$ , 500 mV from rail     | –   | –    | –             | –             | –                  |
| $I_{OUT\_MAX\_HI}$  | Power = HI  | 4   | –    | –             | mA            | –                  |
| $I_{OUT\_MAX\_MID}$ | Power = MID                                       | 4   | –    | –             | mA            | –                  |
| $I_{OUT\_MAX\_LO}$  | Power = LO  | –   | 2    | –             | mA            | –                  |
| $V_{IN}$            | Input voltage range                               | 0   | –    | $V_{DDA}-0.2$ | V             | –                  |
| $V_{CM}$            | Input common mode voltage                         | 0   | –    | $V_{DDA}-0.2$ | V             | –                  |
| $V_{OUT}$           | $V_{DDA} \geq 2.7 \text{ V}$                      | –   | –    | –             | –             | –                  |
| $V_{OUT\_1}$        | Power = HI, $I_{load} = 10 \text{ mA}$            | 0.5 | –    | $V_{DDA}-0.5$ | V             | –                  |
| $V_{OUT\_2}$        | Power = HI, $I_{load} = 1 \text{ mA}$             | 0.2 | –    | $V_{DDA}-0.2$ | V             | –                  |

## Electrical specification

**Table 20 Opamp specifications** (continued)

| Parameter                           | Description   | Min | Typ  | Max                   | Unit       | Details/conditions   |
|-------------------------------------|---|-----|------|-----------------------|------------|--|
| V <sub>OUT_3</sub>                  | Power = MED, I <sub>load</sub> = 1 mA   | 0.2 | –    | V <sub>DDA</sub> -0.2 | V          | –  |
| V <sub>OUT_4</sub>                  | Power = LO, I <sub>load</sub> = 0.1 mA  | 0.2 | –    | V <sub>DDA</sub> -0.2 | V          | –  |
| V <sub>OS_UNTR</sub>                | Offset voltage, untrimmed   | –   | –    | –                     | mV         | –  |
| V <sub>OS_TR</sub>                  | Offset voltage, trimmed   | –   | ±0.5 | –                     | mV         | High mode, 0.2 to V <sub>DDA</sub> - 0.2   |
| V <sub>OS_TR</sub>                  | Offset voltage, trimmed   | –   | ±1   | –                     | mV         | Medium mode  |
| V <sub>OS_TR</sub>                  | Offset voltage, trimmed   | –   | ±2   | –                     | mV         | Low mode   |
| V <sub>OS_DR_UNTR</sub>             | Offset voltage drift, untrimmed   | –   | –    | –                     | μV/°C      | –  |
| V <sub>OS_DR_TR</sub>               | Offset voltage drift, trimmed   | –10 | ±3   | 10                    | μV/°C      | High mode, 0.2 to V <sub>DDA</sub> - 0.2   |
| V <sub>OS_DR_TR</sub>               | Offset voltage drift, trimmed   | –   | ±10  | –                     | μV/°C      | Medium mode  |
| V <sub>OS_DR_TR</sub>               | Offset voltage drift, trimmed   | –   | ±10  | –                     | μV/°C      | Low mode   |
| common-mode rejection ratio (CMRR)  | DC common mode rejection ratio  | 67  | 80   | –                     | dB         | V <sub>DD</sub> = 3.3 V  |
| power supply rejection ratio (PSRR) | Power supply rejection ratio at 1 kHz, 10-mV ripple                               | 70  | 85   | –                     | dB         | V <sub>DD</sub> = 3.3 V  |
| Noise                               | –   | –   | –    | –                     | –          | –  |
| VN1                                 | Input-referred, 1 Hz - 1 GHz, power = HI  | –   | 100  | –                     | μVrms      | –  |
| VN2                                 | Input-referred, 1 kHz, power = HI   | –   | 180  | –                     | nV/root Hz | –  |
| VN3                                 | Input-referred, 10 kHz, power = HI  | –   | 70   | –                     | nV/root Hz | –  |
| VN4                                 | Input-referred, 100 kHz, power = HI   | –   | 38   | –                     | nV/root Hz | –  |
| CLOAD                               | Stable up to maximum load<br>Performance specs at 50 pF                           | –   | –    | 125                   | pF         | –  |
| SLEW_RATE                           | Output slew rate  | 6   | –    | –                     | V/μs       | C <sub>load</sub> = 50 pF, Power = High, V <sub>DDA</sub> ≥ 2.7 V                                      |
| T <sub>OP_WAKE</sub>                | From disable to enable, no external RC dominating                                 | –   | 25   | –                     | μs         | –  |
| COMP_MODE                           | Comparator mode; 50-mV overdrive, T <sub>rise</sub> = T <sub>fall</sub> (approx.) | –   | –    | –                     | –          | –  |
| T <sub>PD1</sub>                    | Response time; power = HI   | –   | 150  | –                     | ns         | –  |
| T <sub>PD2</sub>                    | Response time; power = MED  | –   | 400  | –                     | ns         | –  |
| T <sub>PD3</sub>                    | Response time; power = LO   | –   | 2000 | –                     | ns         | –  |
| V <sub>HYST_OP</sub>                | Hysteresis  | –   | 10   | –                     | mV         | –  |
| Deep Sleep mode                     | Mode 2 is lowest current range<br>Mode 1 has higher GBW                           | –   | –    | –                     | –          | Deep Sleep mode operation: V <sub>DDA</sub> ≥ 2.7 V<br>V <sub>IN</sub> is 0.2 to V <sub>DDA</sub> -1.5 |
| I <sub>DD_HI_M1</sub>               | Mode 1, High current  | –   | 1300 | 1500                  | μA         | Typ at 25°C  |
| I <sub>DD_MED_M1</sub>              | Mode 1, Medium current  | –   | 460  | 600                   | μA         | Typ at 25°C  |

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Electrical specification

**Table 20**      **Opamp specifications** *(continued)*

| Parameter               | Description            | Min | Typ | Max | Unit | Details/conditions   |
|-------------------------|------------------------|-----|-----|-----|------|--|
| I <sub>DD_LOW_M1</sub>  | Mode 1, Low current    | –   | 230 | 350 | μA   | Typ at 25°C  |
| I <sub>DD_HI_M2</sub>   | Mode 2, High current   | –   | 120 | –   | μA   | 25°C   |
| I <sub>DD_MED_M2</sub>  | Mode 2, Medium current | –   | 60  | –   | μA   | 25°C   |
| I <sub>DD_LOW_M2</sub>  | Mode 2, Low current    | –   | 15  | –   | μA   | 25°C   |
| GBW_HI_M1               | Mode 1, High current   | –   | 4   | –   | MHz  | 25°C   |
| GBW_MED_M1              | Mode 1, Medium current | –   | 2   | –   | MHz  | 25°C   |
| GBW_LOW_M1              | Mode 1, Low current    | –   | 0.5 | –   | MHz  | 25°C   |
| GBW_HI_M2               | Mode 2, High current   | –   | 0.5 | –   | MHz  | 20-pF load, no DC load<br>0.2 V to V <sub>DDA</sub> -1.5 V |
| GBW_MED_M2              | Mode 2, Medium current | –   | 0.2 | –   | MHz  | 20-pF load, no DC load<br>0.2 V to V <sub>DDA</sub> -1.5 V |
| GBW_LOW_M2              | Mode 2, Low current    | –   | 0.1 | –   | MHz  | 20-pF load, no DC load<br>0.2 V to V <sub>DDA</sub> -1.5 V |
| V <sub>OS_HI_M1</sub>   | Mode 1, High current   | –   | 5   | –   | mV   | With trim 25°C, 0.2 V to<br>V <sub>DDA</sub> -1.5 V        |
| V <sub>OS_MED_M1</sub>  | Mode 1, Medium current | –   | 5   | –   | mV   | With trim 25°C, 0.2 V to<br>V <sub>DDA</sub> -1.5 V        |
| V <sub>OS_LOW_M1</sub>  | Mode 1, Low current    | –   | 5   | –   | mV   | With trim 25°C, 0.2 V to<br>V <sub>DDA</sub> -1.5 V        |
| V <sub>OS_HI_M2</sub>   | Mode 2, High current   | –   | 5   | –   | mV   | With trim 25°C, 0.2 V to<br>V <sub>DDA</sub> -1.5 V        |
| V <sub>OS_MED_M2</sub>  | Mode 2, Medium current | –   | 5   | –   | mV   | With trim 25°C, 0.2 V to<br>V <sub>DDA</sub> -1.5 V        |
| V <sub>OS_LOW_M2</sub>  | Mode 2, Low current    | –   | 5   | –   | mV   | With trim 25°C, 0.2 V to<br>V <sub>DDA</sub> -1.5 V        |
| I <sub>OUT_HI_M1</sub>  | Mode 1, High current   | –   | 10  | –   | mA   | Output is 0.5 V to V <sub>DDA</sub><br>-0.5 V              |
| I <sub>OUT_MED_M1</sub> | Mode 1, Medium current | –   | 10  | –   | mA   | Output is 0.5 V to V <sub>DDA</sub><br>-0.5 V              |
| I <sub>OUT_LOW_M1</sub> | Mode 1, Low current    | –   | 4   | –   | mA   | Output is 0.5 V to V <sub>DDA</sub><br>-0.5 V              |
| I <sub>OUT_HI_M2</sub>  | Mode 2, High current   | –   | 1   | –   | mA   | Output is 0.5 V to V <sub>DDA</sub><br>-0.5 V              |
| I <sub>OUT_MED_M2</sub> | Mode 2, Medium current | –   | 1   | –   | mA   | Output is 0.5 V to V <sub>DDA</sub><br>-0.5 V              |
| I <sub>OUT_LOW_M2</sub> | Mode 2, Low current    | –   | 0.5 | –   | mA   | Output is 0.5 V to V <sub>DDA</sub><br>-0.5 V              |

## Electrical specification

**Table 21 Low-Power (LP) comparator specifications**

| Parameter                              | Description   | Min | Typ | Max                     | Unit | Details/conditions         |
|--|---|-----|-----|-------------------------|------|----------------------------|
| <b>LP comparator DC specifications</b> |   |     |     |                         |      |                            |
| V <sub>OFFSET1</sub>                   | Input offset voltage for COMP1. Normal power mode     | -10 | -   | 10                      | mV   | COMP0 offset is ±25 mV     |
| V <sub>OFFSET2</sub>                   | Input offset voltage. Low-power mode                  | -25 | ±12 | 25                      | mV   | -                          |
| V <sub>OFFSET3</sub>                   | Input offset voltage. Ultra low-power mode            | -25 | ±12 | 25                      | mV   | -                          |
| V <sub>HYST1</sub>                     | Hysteresis when enabled in Normal mode                | -   | -   | 60                      | mV   | -                          |
| V <sub>HYST2</sub>                     | Hysteresis when enabled in Low-power mode             | -   | -   | 80                      | mV   | -                          |
| V <sub>ICM1</sub>                      | Input common mode voltage in Normal mode              | 0   | -   | V <sub>DDIO1</sub> -0.1 | V    | -                          |
| V <sub>ICM2</sub>                      | Input common mode voltage in Low-power mode           | 0   | -   | V <sub>DDIO1</sub> -0.1 | V    | -                          |
| V <sub>ICM3</sub>                      | Input common mode voltage in Ultra low-power mode     | 0   | -   | V <sub>DDIO1</sub> -0.1 | V    | -                          |
| CMRR                                   | Common mode rejection ratio in Normal power mode      | 50  | -   | -                       | dB   | -                          |
| I <sub>CMP1</sub>                      | Block current, Normal mode                            | -   | -   | 150                     | μA   | -                          |
| I <sub>CMP2</sub>                      | Block current, Low-power mode                         | -   | -   | 10                      | μA   | -                          |
| I <sub>CMP3</sub>                      | Block current in Ultra low-power mode                 | -   | 0.3 | 0.85                    | μA   | -                          |
| ZCMP                                   | DC input impedance of comparator                      | 35  | -   | -                       | MΩ   | -                          |
| <b>LP comparator AC specifications</b> |   |     |     |                         |      |                            |
| T <sub>RESP1</sub>                     | Response time, Normal mode, 100 mV overdrive          | -   | -   | 100                     | ns   | -                          |
| T <sub>RESP2</sub>                     | Response time, Low-power mode, 100 mV overdrive       | -   | -   | 1000                    | ns   | -                          |
| T <sub>RESP3</sub>                     | Response time, Ultra low-power mode, 100 mV overdrive | -   | -   | 20                      | μs   | -                          |
| T <sub>CMP_EN1</sub>                   | Time from enabling to operation                       | -   | -   | 10                      | μs   | Normal and Low-power modes |
| T <sub>CMP_EN2</sub>                   | Time from enabling to operation                       | -   | -   | 50                      | μs   | Ultra low-power mode       |

**Table 22 Temperature sensor specifications**

| Parameter            | Description                 | Min | Typ | Max | Unit | Details/conditions |
|----------------------|-----------------------------|-----|-----|-----|------|--------------------|
| T <sub>SENSACC</sub> | Temperature sensor accuracy | -   | ±1  | 5   | °C   | -40 to +85°C       |

**Table 23 Internal reference specification**

| Parameter          | Description | Min   | Typ | Max   | Unit | Details/conditions |
|--------------------|-------------|-------|-----|-------|------|--------------------|
| V <sub>REFBG</sub> | -           | 1.188 | 1.2 | 1.212 | V    | -                  |



## Electrical specification

### 7.2.2 SAR ADC

**Table 24 12-bit SAR ADC DC specifications**

| Parameter | Description   | Min      | Typ | Max       | Unit       | Details/conditions                      |
|-----------|---|----------|-----|-----------|------------|---|
| A_RES     | SAR ADC resolution                                  | –        | –   | 12        | bits       | –                                       |
| A_CHNLS_S | Number of channels - single ended                   | –        | –   | 16        | –          | 8 full speed                            |
| A-CHNKS_D | Number of channels - differential                   | –        | –   | 8         | –          | Differential inputs use neighboring I/O |
| A-MONO    | Monotonicity  | –        | –   | –         | –          | Yes                                     |
| A_GAINERR | Gain error  | –        | –   | ±0.2      | %          | With external reference                 |
| A_OFFSET  | Input offset voltage                                | –        | –   | 2         | mV         | Measured with 1-V reference             |
| A_ISAR_1  | Current consumption at 1 Msps                       | –        | –   | 1         | mA         | At 1 Msps. External bypass capacitor    |
| A_ISAR_2  | Current consumption at 1 Msps. Reference = $V_{DD}$ | –        | –   | 1.25      | mA         | At 1 Msps. External bypass capacitor    |
| A_VINS    | Input voltage range - single-ended                  | $V_{SS}$ | –   | $V_{DDA}$ | V          | –                                       |
| A_VIND    | Input voltage range - differential                  | $V_{SS}$ | –   | $V_{DDA}$ | V          | –                                       |
| A_INRES   | Input resistance                                    | –        | –   | 2.2       | k $\Omega$ | –                                       |
| A_INCAP   | Input capacitance                                   | –        | –   | 10        | pF         | –                                       |

**Table 25 12-bit SAR ADC AC specifications**

| Parameter                               | Description  | Min | Typ | Max | Unit | Details/conditions   |
|---|--|-----|-----|-----|------|--|
| <b>12-bit SAR ADC AC specifications</b> |  |     |     |     |      |  |
| A_PSR                                   | Power supply rejection ratio   | 70  | –   | –   | dB   | –  |
| A_CMRR                                  | Common mode rejection ratio  | 66  | –   | –   | dB   | Measured at 1 V  |
| <b>One Msp per second mode:</b>         |  |     |     |     |      |  |
| A_SAMP_1                                | Sample rate with external reference bypass capacitor                           | –   | –   | 1   | Msps | –  |
| A_SAMP_2                                | Sample rate with no bypass capacitor; Reference = $V_{DD}$                     | –   | –   | 250 | Ksps | –  |
| A_SAMP_3                                | Sample rate with no bypass capacitor; Internal reference                       | –   | –   | 100 | Ksps | –  |
| A_SINAD                                 | Signal-to-noise and Distortion ratio (SINAD). $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps | 64  | –   | –   | dB   | $F_{in}$ = 10 kHz  |
| A_INL                                   | Integral Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps                       | –2  | –   | 2   | LSB  | Measured with internal $V_{REF}$ = 1.2 V and bypass capacitor                      |
| A_INL                                   | Integral Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps                       | –4  | –   | 4   | LSB  | Measured with external $V_{REF} \geq 1$ V and $V_{IN}$ common mode < 2 * $V_{REF}$ |
| A_DNL                                   | Differential Non Linearity. $V_{DDA}$ = 2.7 to 3.6 V, 1 Msps                   | –1  | –   | 1.4 | LSB  | Measured with internal $V_{REF}$ = 1.2 V and bypass capacitor                      |

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**Table 25**      **12-bit SAR ADC AC specifications** *(continued)*

| Parameter | Description   | Min | Typ | Max | Unit | Details/conditions   |
|-----------|---|-----|-----|-----|------|--|
| A_DNL     | Differential Non Linearity.<br>$V_{DDA} = 2.7$ to $3.6$ V, 1 Msps | -1  | -   | 1.7 | LSB  | Measured with external $V_{REF} \geq 1$ V and $V_{IN}$ common mode $< 2 * V_{REF}$ |
| A_THD     | Total harmonic distortion.<br>$V_{DDA} = 2.7$ to $3.6$ V, 1 Msps  | -   | -   | -65 | dB   | $F_{in} = 10$ kHz  |

**Table 26**      **12-bit DAC Specifications**

| Parameter                           | Description                                | Min | Typ | Max | Unit       | Details/Conditions                      |
|-------------------------------------|--|-----|-----|-----|------------|---|
| <b>12-bit DAC DC specifications</b> |  |     |     |     |            |   |
| DAC_RES                             | DAC resolution                             | -   | -   | 12  | bits       | -                                       |
| DAC_INL                             | Integral nonlinearity                      | -4  | -   | 4   | LSB        | -                                       |
| DAC_DNL                             | Differential nonlinearity                  | -2  | -   | 2   | LSB        | Monotonic to 11 bits.                   |
| DAC_OFFSET                          | Output Voltage zero offset error           | -10 | -   | 10  | mV         | For 000 (hex)                           |
| DAC_OUT_RES                         | DAC Output resistance                      | -   | 15  | -   | k $\Omega$ | -                                       |
| DAC_IDD                             | DAC Current                                | -   | -   | 125 | $\mu$ A    | -                                       |
| DAC_QIDD                            | DAC Current when DAC stopped               | -   | -   | 1   | $\mu$ A    | -                                       |
| <b>12-bit DAC AC specifications</b> |  |     |     |     |            |   |
| DAC_CONV                            | DAC Settling time                          | -   | -   | 2   | $\mu$ s    | Driving through CTBm buffer; 25 pF load |
| DAC_WAKEUP                          | Time from Enabling to ready for conversion | -   | -   | 10  | $\mu$ s    | -                                       |

## Electrical specification

### 7.2.3 CSD

**Table 27 CAPSENSE™ Sigma-Delta (CSD) specifications**

| Parameter  | Description  | Min  | Typ | Max             | Unit  | Details/conditions  |
|--|--|------|-----|-----------------|-------|---|
| <b>CSD V2 specifications</b>   |  |      |     |                 |       |   |
| $V_{DD\_RIPPLE}$   | Max allowed ripple on power supply, DC to 10 MHz           | –    | –   | ±50             | mV    | $V_{DDA} > 2\text{ V}$ (with ripple), 25°C $T_A$ , Sensitivity = 0.1 pF   |
| $V_{DD\_RIPPLE\_1.8}$  | Max allowed ripple on power supply, DC to 10 MHz           | –    | –   | ±25             | mV    | $V_{DDA} > 1.75\text{ V}$ (with ripple), 25°C $T_A$ , Parasitic Capacitance ( $C_P$ ) < 20 pF, Sensitivity ≥ 0.4 pF |
| $I_{CSD}$  | Maximum block current                                      |      |     | 4500            | μA    |   |
| $V_{REF}$  | Voltage reference for CSD and comparator                   | 0.6  | 1.2 | $V_{DDA} - 0.6$ | V     | $V_{DDA} - V_{REF} \geq 0.6\text{ V}$   |
| $V_{REF\_EXT}$   | External voltage reference for CSD and comparator          | 0.6  |     | $V_{DDA} - 0.6$ | V     | $V_{DDA} - V_{REF} \geq 0.6\text{ V}$   |
| $I_{DAC1IDD}$  | IDAC1 (7-bits) block current                               | –    | –   | 1900            | μA    |   |
| $I_{DAC2IDD}$  | IDAC2 (7-bits) block current                               | –    | –   | 1900            | μA    |   |
| $V_{CSD}$  | Voltage range of operation                                 | 1.71 | –   | 3.6             | V     | 1.71 to 3.6 V   |
| $V_{COMPIDAC}$   | Voltage compliance range of IDAC                           | 0.6  | –   | $V_{DDA} - 0.6$ | V     | $V_{DDA} - V_{REF} \geq 0.6\text{ V}$   |
| $I_{DAC1DNL}$  | DNL  | –1   | –   | 1               | LSB   |   |
| $I_{DAC1INL}$  | INL  | –3   | –   | 3               | LSB   | If $V_{DDA} < 2\text{ V}$ then for LSB of 2.4 μA or less  |
| $I_{DAC2DNL}$  | DNL  | –1   | –   | 1               | LSB   |   |
| $I_{DAC2INL}$  | INL  | –3   | –   | 3               | LSB   | If $V_{DDA} < 2\text{ V}$ then for LSB of 2.4 μA or less  |
| <b>SNRC of the following is ratio of counts of finger to noise. Guaranteed by characterization</b> |  |      |     |                 |       |   |
| SNRC_1   | SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5    | –   | –               | Ratio | 9.5-pF maximum capacitance  |
| SNRC_2   | SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5    | –   | –               | Ratio | 31-pF maximum capacitance   |
| SNRC_3   | SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5    | –   | –               | Ratio | 61-pF maximum capacitance   |
| SNRC_4   | PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5    | –   | –               | Ratio | 12-pF maximum capacitance   |
| SNRC_5   | PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5    | –   | –               | Ratio | 47-pF maximum capacitance   |
| SNRC_6   | PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5    | –   | –               | Ratio | 86-pF maximum capacitance   |
| SNRC_7   | PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity | 5    | –   | –               | Ratio | 27-pF maximum capacitance   |
| SNRC_8   | PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity | 5    | –   | –               | Ratio | 86-pF maximum capacitance   |
| SNRC_9   | PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity | 5    | –   | –               | Ratio | 168-pF maximum capacitance  |

## Electrical specification

**Table 27 CAPSENSE™ Sigma-Delta (CSD) specifications** *(continued)*

| Parameter                 | Description   | Min  | Typ | Max  | Unit | Details/conditions                      |
|---------------------------|---|------|-----|------|------|---|
| I <sub>DAC1CRT1</sub>     | Output current of IDAC1 (7 bits) in low range                                   | 4.2  |     | 5.7  | μA   | LSB = 37.5 nA typical                   |
| I <sub>DAC1CRT2</sub>     | Output current of IDAC1 (7 bits) in medium range                                | 33.7 |     | 45.6 | μA   | LSB = 300 nA typical                    |
| I <sub>DAC1CRT3</sub>     | Output current of IDAC1 (7 bits) in high range                                  | 270  |     | 365  | μA   | LSB = 2.4 μA typical                    |
| I <sub>DAC1CRT12</sub>    | Output current of IDAC1 (7 bits) in low range, 2X mode                          | 8    |     | 11.4 | μA   | LSB = 37.5 nA typical 2X output stage   |
| I <sub>DAC1CRT22</sub>    | Output current of IDAC1 (7 bits) in medium range, 2X mode                       | 67   |     | 91   | μA   | LSB = 300 nA typical 2X output stage    |
| I <sub>DAC1CRT32</sub>    | Output current of IDAC1 (7 bits) in high range, 2X mode. V <sub>DDA</sub> > 2 V | 540  |     | 730  | μA   | LSB = 2.4 μA typical 2X output stage    |
| I <sub>DAC2CRT1</sub>     | Output current of IDAC2 (7 bits) in low range                                   | 4.2  |     | 5.7  | μA   | LSB = 37.5 nA typical                   |
| I <sub>DAC2CRT2</sub>     | Output current of IDAC2 (7 bits) in medium range                                | 33.7 |     | 45.6 | μA   | LSB = 300 nA typical                    |
| I <sub>DAC2CRT3</sub>     | Output current of IDAC2 (7 bits) in high range                                  | 270  |     | 365  | μA   | LSB = 2.4 μA typical                    |
| I <sub>DAC2CRT12</sub>    | Output current of IDAC2 (7 bits) in low range, 2X mode                          | 8    |     | 11.4 | μA   | LSB = 37.5 nA typical 2X output stage   |
| I <sub>DAC2CRT22</sub>    | Output current of IDAC2 (7 bits) in medium range, 2X mode                       | 67   |     | 91   | μA   | LSB = 300 nA typical 2X output stage    |
| I <sub>DAC2CRT32</sub>    | Output current of IDAC2 (7 bits) in high range, 2X mode. V <sub>DDA</sub> > 2 V | 540  |     | 730  | μA   | LSB = 2.4 μA typical 2X output stage    |
| I <sub>DAC3CRT13</sub>    | Output current of IDAC in 8-bit mode in low range                               | 8    |     | 11.4 | μA   | LSB = 37.5 nA typical                   |
| I <sub>DAC3CRT23</sub>    | Output current of IDAC in 8-bit mode in medium range                            | 67   |     | 91   | μA   | LSB = 300 nA typical                    |
| I <sub>DAC3CRT33</sub>    | Output current of IDAC in 8-bit mode in high range. V <sub>DDA</sub> > 2 V      | 540  |     | 730  | μA   | LSB = 2.4 μA typical                    |
| I <sub>DACOFFSET</sub>    | All zeros input   | –    | –   | 1    | LSB  | Polarity set by Source or Sink          |
| I <sub>DACGAIN</sub>      | Full-scale error less offset  | –    | –   | ±15  | %    | LSB = 2.4 μA typical                    |
| I <sub>DACMISMATCH1</sub> | Mismatch between IDAC1 and IDAC2 in Low mode                                    | –    | –   | 9.2  | LSB  | LSB = 37.5 nA typical                   |
| I <sub>DACMISMATCH2</sub> | Mismatch between IDAC1 and IDAC2 in Medium mode                                 | –    | –   | 6    | LSB  | LSB = 300 nA typical                    |
| I <sub>DACMISMATCH3</sub> | Mismatch between IDAC1 and IDAC2 in High mode                                   | –    | –   | 5.8  | LSB  | LSB = 2.4 μA typical                    |
| I <sub>DACSET8</sub>      | Settling time to 0.5 LSB for 8-bit IDAC   | –    | –   | 10   | μs   | Full-scale transition. No external load |
| I <sub>DACSET7</sub>      | Settling time to 0.5 LSB for 7-bit IDAC   | –    | –   | 10   | μs   | Full-scale transition. No external load |
| C <sub>MOD</sub>          | External modulator capacitor  | –    | 2.2 | –    | nF   | 5-V rating, X7R or NP0 capacitor        |

## Electrical specification

**Table 28 CSD ADC specifications**

| Parameter                       | Description   | Min              | Typ | Max              | Unit | Details/conditions   |
|---------------------------------|---|------------------|-----|------------------|------|--|
| <b>CSDv2 ADC specifications</b> |   |                  |     |                  |      |  |
| A_RES                           | Resolution  | –                | –   | 10               | bits | Auto-zeroing is required every milli-second  |
| A_CHNLS_S                       | Number of channels - single ended   | –                | –   | –                | 16   |  |
| A-MONO                          | Monotonicity  | –                | –   | Yes              | –    | V <sub>REF</sub> mode  |
| A_GAINERR_VREF                  | Gain error  | –                | 0.6 | –                | %    | Reference Source: SRSS<br>(V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V),<br>(V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)                  |
| A_GAINERR_VDDA                  | Gain error  | –                | 0.2 | –                | %    | Reference Source: SRSS<br>(V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V),<br>(V <sub>REF</sub> = 1.6 V, 2.2 V < V <sub>DDA</sub> < 2.7 V),<br>(V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)               |
| A_OFFSET_VREF                   | Input offset voltage  | –                | 0.5 | –                | LSB  | After ADC calibration, Ref. SRC = SRSS,<br>(V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V,<br>2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V) |
| A_OFFSET_VDDA                   | Input offset voltage  | –                | 0.5 | –                | LSB  | After ADC calibration, Ref. SRC = SRSS,<br>(V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V,<br>2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V) |
| A_ISAR_VREF                     | Current consumption   | –                | 0.3 | –                | mA   | CSD ADC Block current  |
| A_ISAR_VDDA                     | Current consumption   | –                | 0.3 | –                | mA   | CSD ADC Block current  |
| A_VINS_VREF                     | Input voltage range - single ended  | V <sub>SSA</sub> | –   | V <sub>REF</sub> | V    | (V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V,<br>2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)  |
| A_VINS_VDDA                     | Input voltage range - single ended  | V <sub>SSA</sub> | –   | V <sub>DDA</sub> | V    | (V <sub>REF</sub> = 1.20 V, V <sub>DDA</sub> < 2.2 V), (V <sub>REF</sub> = 1.6 V,<br>2.2 V < V <sub>DDA</sub> < 2.7 V), (V <sub>REF</sub> = 2.13 V, V <sub>DDA</sub> > 2.7 V)  |
| A_INRES                         | Input charging resistance   | –                | 15  | –                | kΩ   | –  |
| A_INCAP                         | Input capacitance   | –                | 41  | –                | pF   | –  |
| A_PSRR                          | Power supply rejection ratio (DC)   | –                | 60  | –                | dB   | –  |
| A_TACQ                          | Sample acquisition time   | –                | 10  | –                | μs   | Measured with 50 Ω source impedance.<br>10 μs is default software driver acquisition time setting. Settling to within 0.05%.   |
| A_CONV8                         | Conversion time for 8-bit resolution at conversion rate = F <sub>hclk</sub> /(2 × (N+2)). Clock frequency = 50 MHz. | –                | 25  | –                | μs   | Does not include acquisition time  |

## Electrical specification

**Table 28 CSD ADC specifications (continued)**

| Parameter  | Description   | Min | Typ | Max | Unit | Details/conditions                  |
|------------|---|-----|-----|-----|------|-------------------------------------|
| A_CONV10   | Conversion time for 10-bit resolution at conversion rate = $F_{\text{hclk}}/(2 \times (N + 2))$ . Clock frequency = 50 MHz. | –   | 60  | –   | μs   | Does not include acquisition time   |
| A_SND_VRE  | Signal-to-noise and Distortion ratio (SINAD)  | –   | 57  | –   | dB   | Measured with 50 Ω source impedance |
| A_SND_VDDA | SINAD   | –   | 52  | –   | dB   | Measured with 50 Ω source impedance |
| A_INL_VREF | Integral nonlinearity – 11.6 ksps   | –   | –   | 2   | LSB  | Measured with 50 Ω source impedance |
| A_INL_VDDA | Integral nonlinearity – 11.6 ksps   | –   | –   | 2   | LSB  | Measured with 50 Ω source impedance |
| A_DNL_VREF | Differential nonlinearity – 11.6 ksps   | –   | –   | 1   | LSB  | Measured with 50 Ω source impedance |
| A_DNL_VDDA | Differential nonlinearity – 11.6 ksps   | –   | –   | 1   | LSB  | Measured with 50 Ω source impedance |

## 7.3 Digital peripherals

**Table 29 Timer/Counter/PWM (TCPWM) specifications**

| Parameter                      | Description                                      | Min       | Typ | Max | Unit | Details/conditions  |
|--------------------------------|--|-----------|-----|-----|------|---|
| $I_{\text{TCPWM1}}$            | Block current consumption at 8 MHz               | –         | –   | 70  | μA   | All modes (TCPWM)   |
| $I_{\text{TCPWM2}}$            | Block current consumption at 24 MHz              | –         | –   | 180 | μA   | All modes (TCPWM)   |
| $I_{\text{TCPWM3}}$            | Block current consumption at 50 MHz              | –         | –   | 270 | μA   | All modes (TCPWM)   |
| $I_{\text{TCPWM4}}$            | Block current consumption at 100 MHz             | –         | –   | 540 | μA   | All modes (TCPWM)   |
| $\text{TCPWM}_{\text{FRE Q}}$  | Operating frequency                              | –         | –   | 100 | MHz  | $F_{\text{cmax}} = F_{\text{cpu}}$<br>Maximum = 100 MHz   |
| $\text{TPWM}_{\text{ENEXT T}}$ | Input trigger pulse width for all trigger events | $2/F_c$   | –   | –   | ns   | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected |
| $\text{TPWM}_{\text{EXT}}$     | Output trigger pulse widths                      | $1.5/F_c$ | –   | –   | ns   | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs                |
| $\text{TC}_{\text{RES}}$       | Resolution of counter                            | $1/F_c$   | –   | –   | ns   | Minimum time between successive counts  |
| $\text{PWM}_{\text{RES}}$      | PWM resolution                                   | $1/F_c$   | –   | –   | ns   | Minimum pulse width of PWM output   |
| $\text{Q}_{\text{RES}}$        | Quadrature inputs resolution                     | $2/F_c$   | –   | –   | ns   | Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar                             |

# Electrical specification

**Table 30 Serial Communication Block (SCB) specifications**

| Parameter  | Description  | Min | Typ | Max   | Unit | Details/conditions                                    |
|--|--|-----|-----|---|------|---|
| Fixed I <sup>2</sup> C DC specifications   |  |     |     |   |      |   |
| I <sub>I2C1</sub>  | Block current consumption at 100 kHz   | –   | –   | 30  | μA   | –   |
| I <sub>I2C2</sub>  | Block current consumption at 400 kHz   | –   | –   | 80  | μA   | –   |
| I <sub>I2C3</sub>  | Block current consumption at 1 Mbps  | –   | –   | 180   | μA   | –   |
| I <sub>I2C4</sub>  | I <sup>2</sup> C enabled in Deep Sleep mode  | –   | –   | 1.7   | μA   | At 60°C   |
| Fixed I <sup>2</sup> C AC specifications   |  |     |     |   |      |   |
| F <sub>I2C1</sub>  | Bit Rate   | –   | –   | 1   | Mbps | –   |
| Fixed UART DC specifications   |  |     |     |   |      |   |
| I <sub>UART1</sub>   | Block current consumption at 100 Kbps  | –   | –   | 30  | μA   | –   |
| I <sub>UART2</sub>   | Block current consumption at 1000 Kbps   | –   | –   | 180   | μA   | –   |
| Fixed UART AC specifications   |  |     |     |   |      |   |
| F <sub>UART1</sub>   | Bit Rate   | –   | –   | 3   | Mbps | ULP mode  |
| F <sub>UART2</sub>   |  | –   | –   | 8   |      | LP mode   |
| Fixed SPI DC specifications  |  |     |     |   |      |   |
| I <sub>SPI1</sub>  | Block current consumption at 1 Mbps  | –   | –   | 220   | μA   | –   |
| I <sub>SPI2</sub>  | Block current consumption at 4 Mbps  | –   | –   | 340   | μA   | –   |
| I <sub>SPI3</sub>  | Block current consumption at 8 Mbps  | –   | –   | 360   | μA   | –   |
| I <sub>SP14</sub>  | Block current consumption at 25 Mbps   | –   | –   | 800   | μA   | –   |
| Fixed SPI AC specifications for LP Mode (1.1 V) unless noted otherwise             |  |     |     |   |      |   |
| F <sub>SPI</sub>   | SPI operating frequency Master and externally clocked slave                            | –   | –   | 25  | MHz  | 14-MHz maximum for ULP (0.9 V) mode                   |
| F <sub>SPI_IC</sub>  | SPI Slave internally clocked   | –   | –   | 15  | MHz  | 5 MHz maximum for ULP (0.9 V) mode                    |
| Fixed SPI Master mode AC specifications for LP Mode (1.1 V) unless noted otherwise |  |     |     |   |      |   |
| T <sub>DMO</sub>   | master out, slave in (MOSI) valid after SClock driving edge                            | –   | –   | 12  | ns   | 20 ns maximum for ULP (0.9 V) mode                    |
| T <sub>DSI</sub>   | MISO valid before SClock capturing edge  | 5   | –   | –   | ns   | Full clock, late master in, slave out (MISO) sampling |
| T <sub>HMO</sub>   | MOSI data hold time  | 0   | –   | –   | ns   | Referred to slave capturing edge                      |
| Fixed SPI Slave mode AC specifications for LP Mode (1.1 V) unless noted otherwise  |  |     |     |   |      |   |
| T <sub>DMI</sub>   | MOSI valid before Sclock capturing edge  | 5   | –   | –   | ns   | –   |
| T <sub>DSO_EXT</sub>   | MISO valid after Sclock driving edge in external clock mode                            | –   | –   | 20  | ns   | 35 ns maximum for ULP (0.9 V) mode                    |
| T <sub>DSO</sub>   | MISO valid after Sclock driving edge in internal clock mode                            | –   | –   | T <sub>DSO_EXT</sub> + 3 * T <sub>scb</sub> | ns   | T <sub>scb</sub> is SCB clock period                  |
| T <sub>DSO</sub>   | MISO valid after Sclock driving edge in internal clock mode with median filter enabled | –   | –   | T <sub>DSO_EXT</sub> + 4 * T <sub>scb</sub> | ns   | T <sub>scb</sub> is SCB clock period                  |
| T <sub>HSO</sub>   | Previous MISO data hold time   | 5   | –   | –   | ns   | –   |



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Electrical specification

**Table 30**      **Serial Communication Block (SCB) specifications** *(continued)*

| Parameter             | Description                         | Min | Typ | Max | Unit | Details/conditions |
|-----------------------|-------------------------------------|-----|-----|-----|------|--------------------|
| TSSEL <sub>SCK1</sub> | SSEL valid to first SCK valid edge  | 65  | –   | –   | ns   | –                  |
| TSSEL <sub>SCK2</sub> | SSEL hold after Last SCK valid edge | 65  | –   | –   | ns   | –                  |

**7.3.1**      **LCD specifications**
**Table 31**      **LCD direct drive DC specifications**

| Parameter             | Description                                       | Min | Typ | Max  | Unit | Details/conditions                    |
|-----------------------|---|-----|-----|------|------|---------------------------------------|
| I <sub>LCDLOW</sub>   | Operating current in low-power mode               | –   | 5   | –    | μA   | 16 x 4 small segment display at 50 Hz |
| C <sub>LCDCAP</sub>   | LCD capacitance per segment/common driver         | –   | 500 | 5000 | pF   | –                                     |
| LCD <sub>OFFSET</sub> | Long-term segment offset                          | –   | 20  | –    | mV   | –                                     |
| I <sub>LCDOP1</sub>   | PWM mode current.<br>3.3-V bias, 8-MHz IMO, 25°C. | –   | 0.6 | –    | mA   | 32 x 4 segments 50 Hz                 |
| I <sub>LCDOP2</sub>   | PWM mode current.<br>3.3-V bias, 8-MHz IMO, 25°C. | –   | 0.5 | –    | mA   | 32 x 4 segments 50 Hz                 |

**Table 32**      **LCD direct drive AC specifications**

| Parameter        | Description    | Min | Typ | Max | Unit | Details/conditions |
|------------------|----------------|-----|-----|-----|------|--------------------|
| F <sub>LCD</sub> | LCD frame rate | 10  | 50  | 150 | Hz   | –                  |

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Electrical specification

## 7.4 Memory

**Table 33 Flash specifications**

| Parameter                      | Description   | Min   | Typ | Max | Unit    | Details/conditions      |
|--------------------------------|---|-------|-----|-----|---------|-------------------------|
| <b>Flash DC specifications</b> |   |       |     |     |         |                         |
| VPE                            | Erase and program voltage                           | 1.71  | –   | 3.6 | V       | –                       |
| <b>Flash AC specifications</b> |   |       |     |     |         |                         |
| T <sub>ROWWRITE</sub>          | Row (Block) write time (erase & program)            | –     | –   | 16  | ms      | Row (Block) = 512 bytes |
| T <sub>ROWERASE</sub>          | Row erase time                                      | –     | –   | 11  | ms      | –                       |
| T <sub>ROWPROGRAM</sub>        | Row program time after erase                        | –     | –   | 5   | ms      | –                       |
| T <sub>BULKERASE</sub>         | Bulk erase time (1024 KB)                           | –     | –   | 11  | ms      | –                       |
| T <sub>SECTORERASE</sub>       | Sector erase time (256 KB)                          | –     | –   | 11  | ms      | 512 rows per sector     |
| T <sub>SSERIAE</sub>           | Sub-sector erase time                               | –     | –   | 11  | ms      | 8 rows per sub-sector   |
| T <sub>SSWRITE</sub>           | Sub-sector write time; 1 erase plus 8 program times | –     | –   | 51  | ms      | –                       |
| T <sub>SWRITE</sub>            | Sector write time; 1 erase plus 512 program times   | –     | –   | 2.6 | seconds | –                       |
| T <sub>DEVPROG</sub>           | Total device program time                           | –     | –   | 15  | seconds | –                       |
| F <sub>END</sub>               | Flash Endurance                                     | 100 K | –   | –   | cycles  | –                       |
| F <sub>RET1</sub>              | Flash Retention. Ta ≤ 25°C, 100 K P/E cycles        | 10    | –   | –   | years   | –                       |
| F <sub>RET2</sub>              | Flash Retention. Ta ≤ 85°C, 10 K P/E cycles         | 10    | –   | –   | years   | –                       |
| F <sub>RET3</sub>              | Flash Retention. Ta ≤ 55°C, 20 K P/E cycles         | 20    | –   | –   | years   | –                       |
| T <sub>WS100</sub>             | Number of Wait states at 100 MHz                    | 3     | –   | –   | –       | –                       |
| T <sub>WS50</sub>              | Number of Wait states at 50 MHz                     | 2     | –   | –   | –       | –                       |

**Note**

9. It can take as much as 16 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watch-dog. Make certain that these are not inadvertently activated.

## Electrical specification

### 7.5 System resources

**Table 34 CYBLE-416070-02 system resources**

| Parameter                                  | Description   | Min  | Typ  | Max  | Unit        | Details/conditions                           |
|--|---|------|------|------|-------------|--|
| <b>POR with brownout DC specifications</b> |   |      |      |      |             |  |
| <b>Precise POR (PPOR)</b>                  |   |      |      |      |             |  |
| $V_{FALLPPOR}$                             | BOD trip voltage in Active and Sleep modes, $V_{DDD}$     | 1.54 | –    | –    | V           | BOD Reset guaranteed for levels below 1.54 V |
| $V_{FALLDPSLP}$                            | BOD trip voltage in Deep Sleep, $V_{DDD}$                 | 1.54 | –    | –    | V           | –  |
| $V_{DDRAMP}$                               | Maximum power supply ramp rate (any supply)               | –    | –    | 100  | mV/ $\mu$ s | Active mode                                  |
| <b>POR with brownout AC specification</b>  |   |      |      |      |             |  |
| $V_{DDRAMP\_DS}$                           | Maximum power supply ramp rate (any supply) in Deep Sleep | –    | –    | 10   | mV/ $\mu$ s | BOD operation guaranteed                     |
| <b>Voltage monitors DC specifications</b>  |   |      |      |      |             |  |
| $V_{HVD0}$                                 | –   | 1.18 | 1.23 | 1.27 | V           | –  |
| $V_{HVDI1}$                                | –   | 1.38 | 1.43 | 1.47 | V           | –  |
| $V_{HVDI2}$                                | –   | 1.57 | 1.63 | 1.68 | V           | –  |
| $V_{HVDI3}$                                | –   | 1.76 | 1.83 | 1.89 | V           | –  |
| $V_{HVDI4}$                                | –   | 1.95 | 2.03 | 2.1  | V           | –  |
| $V_{HVDI5}$                                | –   | 2.05 | 2.13 | 2.2  | V           | –  |
| $V_{HVDI6}$                                | –   | 2.15 | 2.23 | 2.3  | V           | –  |
| $V_{HVDI7}$                                | –   | 2.24 | 2.33 | 2.41 | V           | –  |
| $V_{HVDI8}$                                | –   | 2.34 | 2.43 | 2.51 | V           | –  |
| $V_{HVDI9}$                                | –   | 2.44 | 2.53 | 2.61 | V           | –  |
| $V_{HVDI10}$                               | –   | 2.53 | 2.63 | 2.72 | V           | –  |
| $V_{HVDI11}$                               | –   | 2.63 | 2.73 | 2.82 | V           | –  |
| $V_{HVDI12}$                               | –   | 2.73 | 2.83 | 2.92 | V           | –  |
| $V_{HVDI13}$                               | –   | 2.82 | 2.93 | 3.03 | V           | –  |
| $V_{HVDI14}$                               | –   | 2.92 | 3.03 | 3.13 | V           | –  |
| $V_{HVDI15}$                               | –   | 3.02 | 3.13 | 3.23 | V           | –  |
| $LVI\_IDD$                                 | Block current   | –    | 5    | 15   | $\mu$ A     | –  |
| <b>Voltage monitors AC specification</b>   |   |      |      |      |             |  |
| $T_{MONTRIP}$                              | Voltage monitor trip time                                 | –    | –    | 170  | ns          | –  |

## Electrical specification

### 7.5.1 SWD interface

**Table 35 SWD and trace specifications**

| Parameter                      | Description   | Min        | Typ | Max       | Unit | Details/conditions                   |
|--------------------------------|---|------------|-----|-----------|------|--------------------------------------|
| <b>SWD and trace interface</b> |   |            |     |           |      |                                      |
| F_SWCLK2                       | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$           | –          | –   | 25        | MHz  | LP mode. $V_{CCD} = 1.1\text{ V}$    |
| F_SWCLK2L                      | $1.71\text{ V} \leq V_{DD} \leq 3.6\text{ V}$           | –          | –   | 12        | MHz  | ULP mode. $V_{CCD} = 0.9\text{ V}$ . |
| T_SWDI_SETUP                   | $T = 1/f_{\text{SWCLK}}$                                | $0.25 * T$ | –   | –         | ns   | –                                    |
| T_SWDI_HOLD                    | $T = 1/f_{\text{SWCLK}}$                                | $0.25 * T$ | –   | –         | ns   | –                                    |
| T_SWDO_VALID                   | $T = 1/f_{\text{SWCLK}}$                                | –          | –   | $0.5 * T$ | ns   | –                                    |
| T_SWDO_HOLD                    | $T = 1/f_{\text{SWCLK}}$                                | 1          | –   | –         | ns   | –                                    |
| F_TRCLK_LP1                    | With Trace Data setup/hold times of 2/1 ns respectively | –          | –   | 75        | MHz  | LP mode. $V_{DD} = 1.1\text{ V}$     |
| F_TRCLK_LP2                    | With Trace Data setup/hold times of 3/2 ns respectively | –          | –   | 70        | MHz  | LP mode. $V_{DD} = 1.1\text{ V}$     |
| F_TRCLK_ULP                    | With Trace Data setup/hold times of 3/2 ns respectively | –          | –   | 25        | MHz  | ULP mode. $V_{DD} = 0.9\text{ V}$    |

### 7.5.2 Internal main oscillator

**Table 36 IMO DC specifications**

| Parameter  | Description                    | Min | Typ | Max | Unit | Details/conditions |
|------------|--------------------------------|-----|-----|-----|------|--------------------|
| $I_{IMO1}$ | IMO operating current at 8 MHz | –   | 9   | 15  | μA   | –                  |

**Table 37 IMO AC specifications**

| Parameter     | Description                           | Min | Typ | Max | Unit | Details/conditions |
|---------------|---------------------------------------|-----|-----|-----|------|--------------------|
| $F_{IMOTOL1}$ | Frequency variation centered on 8 MHz | –   | –   | ±2  | %    | –                  |
| $T_{JITR}$    | Cycle-to-Cycle and Period jitter      | –   | 250 | –   | ps   | –                  |

### 7.5.3 Internal low-speed oscillator

**Table 38 ILO DC specification**

| Parameter  | Description                     | Min | Typ | Max | Unit | Details/conditions |
|------------|---------------------------------|-----|-----|-----|------|--------------------|
| $I_{ILO2}$ | ILO operating current at 32 kHz | –   | 0.3 | 0.7 | μA   | –                  |

**Table 39 ILO AC specifications**

| Parameter       | Description              | Min  | Typ | Max  | Unit | Details/conditions                     |
|-----------------|--------------------------|------|-----|------|------|--|
| $T_{STARTILO1}$ | ILO startup time         | –    | –   | 7    | μs   | Startup time to 95% of final frequency |
| $T_{LIODUTY}$   | ILO duty cycle           | 45   | 50  | 55   | %    | –                                      |
| $F_{ILOTRIM1}$  | 32-kHz trimmed frequency | 28.8 | 32  | 35.2 | kHz  | ±10% variation                         |

## Electrical specification

**Table 40 UDB AC specifications**

| Parameter   | Description  | Min | Typ | Max | Unit | Details/conditions |
|---|--|-----|-----|-----|------|--------------------|
| <b>Data path performance</b>  |  |     |     |     |      |                    |
| F <sub>MAX-TIMER</sub>  | Maximum frequency of 16-bit timer in a UDB pair        | –   | –   | 100 | MHz  | –                  |
| F <sub>MAX-ADDER</sub>  | Maximum frequency of 16-bit adder in a UDB pair        | –   | –   | 100 | MHz  | –                  |
| F <sub>MAX_CRC</sub>  | Maximum frequency of 16-bit CRC/PRS in a UDB pair      | –   | –   | 100 | MHz  | –                  |
| <b>PLD performance in UDB</b>   |  |     |     |     |      |                    |
| F <sub>MAX_PLD</sub>  | Maximum frequency of 2-pass PLD function in a UDB pair | –   | –   | 100 | MHz  | –                  |
| <b>Clock to output performance</b>                                      |  |     |     |     |      |                    |
| T <sub>CLK_OUT_UBD1</sub>   | Propagation delay for clock in to data out             | –   | 5   | –   | ns   | –                  |
| <b>UDB port adapter specifications</b>                                  |  |     |     |     |      |                    |
| <i>Conditions: 10-pF load, 3-V V<sub>DDIO</sub> and V<sub>DDD</sub></i> |  |     |     |     |      |                    |
| T <sub>LCLKDO</sub>   | L <sub>CLK</sub> to output delay                       | –   | –   | 11  | ns   | –                  |
| T <sub>DINLCLK</sub>  | Input setup time to L <sub>CLK</sub> rising edge       | –   | –   | 7   | ns   | –                  |
| T <sub>DINLCLKHLD</sub>   | Input hold time from L <sub>CLK</sub> rising edge      | 5   | –   | –   | ns   | –                  |
| T <sub>LCLKHIZ</sub>  | L <sub>CLK</sub> to output tristate                    | –   | –   | 28  | ns   | –                  |
| T <sub>FLCLK</sub>  | L <sub>CLK</sub> frequency                             | –   | –   | 33  | MHz  | –                  |
| T <sub>LCLKDUTY</sub>   | L <sub>CLK</sub> duty cycle (percentage high)          | 40% | –   | 60% | %    | –                  |

**Table 41 Audio subsystem specifications**

| Parameter                             | Description                                       | Min   | Typ | Max    | Unit | Details/conditions      |
|---------------------------------------|---|-------|-----|--------|------|-------------------------|
| <b>Audio subsystem specifications</b> |   |       |     |        |      |                         |
| <b>PDM specifications</b>             |   |       |     |        |      |                         |
| PDM_IDD1                              | PDM active current, Stereo operation, 1-MHz clock | –     | 175 | –      | μA   | 16-bit audio at 16 ksps |
| PDM_IDD2                              | PDM active current, Stereo operation, 3-MHz clock | –     | 600 | –      | μA   | 24-bit audio at 48 ksps |
| PDM_JITTER                            | RMS jitter in PDM clock                           | –200  | –   | 200    | ps   |                         |
| PDM_CLK                               | PDM clock speed                                   | 0.384 | –   | 3.072  | MHz  |                         |
| PDM_BLK_CLK                           | PDM block input clock                             | 1.024 | –   | 49.152 | MHz  |                         |
| PDM_SETUP                             | Data input setup time to PDM_CLK edge             | 10    | –   | –      | ns   |                         |
| PDM_HOLD                              | Data input hold time to PDM_CLK edge              | 10    | –   | –      | ns   |                         |
| PDM_OUT                               | Audio sample rate                                 | 8     | –   | 48     | ksps |                         |
| PDM_WL                                | Word length                                       | 16    | –   | 24     | bits |                         |

## Electrical specification

**Table 41 Audio subsystem specifications (continued)**

| Parameter | Description                        | Min  | Typ       | Max  | Unit | Details/conditions                 |
|-----------|------------------------------------|------|-----------|------|------|------------------------------------|
| PDM_SNR   | Signal-to-noise ratio (A-weighted) | –    | 100       | –    | dB   | PDM input, 20 Hz to 20 kHz BW      |
| PDM_DR    | Dynamic range (A-weighted)         | –    | 100       | –    | dB   | 20 Hz to 20 kHz BW, -60 dB FS      |
| PDM_FR    | Frequency response                 | -0.2 | –         | 0.2  | dB   | DC to 0.45. DC Blocking filter OFF |
| PDM_SB    | Stop band                          | –    | 0.56<br>6 | –    | f    | –                                  |
| PDM_SBA   | Stop band attenuation              | –    | 60        | –    | dB   | –                                  |
| PDM_GAIN  | Adjustable gain                    | -12  | –         | 10.5 | dB   | PDM to PCM, 1.5 dB/step            |
| PDM_ST    | Startup time                       | –    | 48        | –    | –    | Word Select (WS) cycles            |

**I2S specifications (same for LP and ULP modes unless stated otherwise)**

|                           |  |   |   |     |      |                                       |
|---------------------------|--|---|---|-----|------|---------------------------------------|
| I <sup>2</sup> S_WORD     | Length of I <sup>2</sup> S word          | 8 | – | 32  | bits | –                                     |
| I <sup>2</sup> S_WS       | Word clock frequency in LP mode          | – | – | 192 | kHz  | 12.288 MHz bit clock with 32-bit word |
| I <sup>2</sup> S_WS_U     | Word clock frequency in ULP mode         | – | – | 48  | kHz  | 3.072 MHz bit clock with 32-bit word  |
| I <sup>2</sup> S_WS_TDM   | Word clock frequency in TDM mode for LP  | – | – | 48  | kHz  | 8 32-bit channels                     |
| I <sup>2</sup> S_WS_TDM_U | Word clock frequency in TDM mode for ULP | – | – | 12  | kHz  | 8 32-bit channels                     |

**I2S Slave mode**

|         |  |                   |   |                |    |  |
|---------|--|-------------------|---|----------------|----|--|
| TS_WS   | WS setup time to the following rising edge of SCK for LP mode    | 5                 | – | –              | ns | –  |
| TS_WS   | WS setup time to the following rising edge of SCK for ULP mode   | 11                | – | –              | ns | –  |
| TH_WS   | WS hold time to the following edge of SCK                        | TMCLK_SOC + 5     | – | –              | ns | –  |
| TD_SDO  | Delay time of TX_SDO transition from edge of TX_SCK for LP mode  | -(TMCLK_SOC + 25) | – | TMCLK_SOC + 25 | ns | Associated clock edge depends on selected polarity |
| TD_SDO  | Delay time of TX_SDO transition from edge of TX_SCK for ULP mode | -(TMCLK_SOC + 70) | – | TMCLK_SOC + 70 | ns | Associated clock edge depends on selected polarity |
| TS_SDI  | RX_SDI setup time to the following edge of RX_SCK in LP mode     | 5                 | – | –              | ns | –  |
| TS_SDI  | RX_SDI setup time to the following edge of RX_SCK in ULP mode    | 11                | – | –              | ns | –  |
| TH_SDI  | RX_SDI hold time to the rising edge of RX_SCK                    | TMCLK_SOC + 5     | – | –              | ns | –  |
| T_SCKCY | TX/RX_SCK bit clock duty cycle                                   | 45                | – | 55             | %  | –  |

**I<sup>2</sup>S Master mode**

## Electrical specification

**Table 41 Audio subsystem specifications (continued)**

| Parameter   | Description   | Min           | Typ | Max    | Unit | Details/conditions  |
|-------------|---|---------------|-----|--------|------|---|
| TD_WS       | WS transition delay from falling edge of SCK in LP mode   | -10           | -   | 20     | ns   | -   |
| TD_WS_U     | WS transition delay from falling edge of SCK in ULP mode  | -10           | -   | 40     | ns   | -   |
| TD_SDO      | SDO transition delay from falling edge of SCK in LP mode  | -10           | -   | 20     | ns   | -   |
| TD_SDO      | SDO transition delay from falling edge of SCK in ULP mode | -10           | -   | 40     | ns   | -   |
| TS_SDI      | SDI setup time to the associated edge of SCK              | 5             | -   | -      | ns   | Associated clock edge depends on selected polarity                                  |
| TH_SDI      | SDI hold time to the associated edge of SCK               | TMCLK_SOC + 5 | -   | -      | ns   | T is TX/RX_SCK bit clock period. Associated clock edge depends on selected polarity |
| T_SCKCY     | SCK bit clock duty cycle                                  | 45            | -   | 55     | %    | -   |
| FMCLK_SOC   | MCLK_SOC frequency in LP mode                             | 1.024         | -   | 98.304 | MHz  | FMCLK_SOC = 8 * Bit-clock   |
| FMCLK_SOC_U | MCLK_SOC frequency in ULP mode                            | 1.024         | -   | 24.576 | MHz  | FMCLK_SOC_U = 8 * Bit-clock   |
| T_MCLKCY    | MCLK_SOC duty cycle                                       | 45            | -   | 55     | %    | -   |
| T_JITTER    | MCLK_SOC input jitter                                     | -100          | -   | 100    | ps   | -   |

**Table 42 Smart I/O specifications**

| Parameter | Description              | Min | Typ | Max | Unit | Details/Conditions |
|-----------|--------------------------|-----|-----|-----|------|--------------------|
| SMIO_BYP  | Smart I/O bypass delay   | -   | -   | 2   | ns   | -                  |
| SMIO_LUT  | Smart I/O LUT prop delay | -   | TBD | -   | ns   | -                  |

**Table 43 Bluetooth® LE subsystem specifications**

| Parameter                                     | Description   | Min | Typ | Max | Unit | Details/conditions                             |
|---|---|-----|-----|-----|------|--|
| <b>Bluetooth® LE subsystem specifications</b> |   |     |     |     |      |  |
| <b>RF receiver specifications (1 Mbps)</b>    |   |     |     |     |      |  |
| RXS, IDLE                                     | RX Sensitivity with Ideal Transmitter                                   | -   | -95 | -   | dBm  | Across RF operating frequency range            |
| RXS, IDLE                                     | RX Sensitivity with Ideal Transmitter                                   | -   | -93 | -   | dBm  | 255-byte packet length, across frequency range |
| RXS, DIRTY                                    | RX Sensitivity with Dirty Transmitter                                   | -   | -92 | -   | dBm  | RF-PHY Specification (RCV-LE/CA/01/C)          |
| PRX <sub>MAX</sub>                            | Maximum received signal strength at < 0.1% PER                          | -   | 0   | -   | dBm  | RF-PHY Specification (RCV-LE/CA/06/C)          |
| CI1   | Co-channel interference, Wanted Signal at -67 dBm and Interferer at FRX | -   | 9   | 21  | dB   | RF-PHY Specification (RCV-LE/CA/03/C)          |

## Electrical specification

**Table 43 Bluetooth® LE subsystem specifications (continued)**

| Parameter | Description  | Min | Typ | Max | Unit | Details/conditions                    |
|-----------|--|-----|-----|-----|------|---------------------------------------|
| CI2       | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at $FRX \pm 1$ MHz                      | -   | 3   | 15  | dB   | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI3       | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at $FRX \pm 2$ MHz                      | -   | -26 | -17 | dB   | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI4       | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at $\geq FRX \pm 3$ MHz                 | -   | -33 | -27 | dB   | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI5       | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at Image frequency (FIMAGE)             | -   | -20 | -9  | dB   | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI6       | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at Image frequency (FIMAGE $\pm 1$ MHz) | -   | -28 | -15 | dB   | RF-PHY Specification (RCV-LE/CA/03/C) |

**RF receiver specifications (2 Mbps)**

|                    |  |   |     |     |     |  |
|--------------------|--|---|-----|-----|-----|--|
| RXS, IDLE          | RX Sensitivity with Ideal Transmitter  | - | -92 | -   | dBm | Across RF operating frequency range            |
| RXS, IDLE          | RX Sensitivity with Ideal Transmitter  | - | -90 | -   | dBm | 255-byte packet length, across frequency range |
| RXS, DIRTY         | RX Sensitivity with Dirty Transmitter  | - | -89 | -   | dBm | RF-PHY Specification (RCV-LE/CA/01/C)          |
| PRX <sub>MAX</sub> | Maximum received signal strength at < 0.1% PER   | - | 0   | -   | dBm | RF-PHY Specification (RCV-LE/CA/06/C)          |
| CI1                | Co-channel interference,<br>Wanted Signal at -67 dBm and Interferer at FRX                                       | - | 9   | 21  | dB  | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI2                | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at $FRX \pm 2$ MHz                      | - | 3   | 15  | dB  | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI3                | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at $FRX \pm 4$ MHz                      | - | -26 | -17 | dB  | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI4                | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at $\geq FRX \pm 6$ MHz                 | - | -33 | -27 | dB  | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI5                | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at Image frequency (FIMAGE)             | - | -20 | -9  | dB  | RF-PHY Specification (RCV-LE/CA/03/C)          |
| CI6                | Adjacent channel interference<br>Wanted Signal at -67 dBm and Interferer at Image frequency (FIMAGE $\pm 2$ MHz) | - | -28 | -15 | dB  | RF-PHY Specification (RCV-LE/CA/03/C)          |

**RF receiver specification (1 and 2 Mbps)**



## Electrical specification

**Table 43 Bluetooth® LE subsystem specifications (continued)**

| Parameter | Description   | Min | Typ | Max | Unit | Details/conditions  |
|-----------|---|-----|-----|-----|------|---|
| OBB1      | Out of Band blocking<br>Wanted Signal at –67 dBm and Interferer at<br>F = 30 -2000 MHz                                  | –30 | –27 | –   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| OBB2      | Out of Band blocking<br>Wanted Signal at –67 dBm and Interferer at<br>F = 2003 -2399 MHz                                | –35 | –27 | –   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| OBB3      | Out of Band blocking<br>Wanted Signal at –67 dBm and Interferer at<br>F= 2484-2997 MHz                                  | –35 | –27 | –   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| OBB4      | Out of Band blocking<br>Wanted Signal at –67 dBm and Interferer at<br>F= 3000-12750 MHz                                 | –30 | –27 | –   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/04/C)                  |
| IMD       | Intermodulation performance<br>Wanted Signal at –64 dBm and 1 Mbps<br>Bluetooth® LE, 3rd, 4th and 5th offset<br>channel | –50 | –   | –   | dBm  | RF-PHY Specification<br>(RCV-LE/CA/05/C)                  |
| RXSE1     | Receiver Spurious emission<br>30 MHz to 1.0 GHz   | –   | –   | –57 | dBm  | 100 kHz measurement<br>bandwidth<br>ETSI EN300 328 V2.1.1 |
| RXSE2     | Receiver Spurious emission<br>1.0 GHz to 12.75 GHz  | –   | –   | –53 | dBm  | 1 MHz measurement<br>bandwidth<br>ETSI EN300 328 V2.1.1   |

**RF transmitter specifications**

|            |  |      |     |     |     |  |
|------------|--|------|-----|-----|-----|--|
| TXP, ACC   | RF Power Accuracy  | –    | –   | 1   | dB  | –  |
| TXP, RANGE | Frequency Accuracy   | –    | 24  | –   | dB  | –20 dBm to +4 dBm                        |
| TXP, 0 dBm | Output Power, 0 dB Gain Setting                                | –    | 0   | –   | dBm | –  |
| TXP, MAX   | Output Power, Maximum Power Setting                            | –    | 4   | –   | dBm | –  |
| TXP, MIN   | Output Power, Minimum Power Setting                            | –    | –20 | –   | dBm | –  |
| F2AVG      | Average Frequency Deviation for<br>10101010 pattern            | 185  | –   | –   | kHz | RF-PHY Specification<br>(TRM-LE/CA/05/C) |
| F2AVG_2M   | Average Frequency Deviation for<br>10101010 pattern for 2 Mbps | 370  | –   | –   | kHz | RF-PHY Specification<br>(TRM-LE/CA/05/C) |
| F1AVG      | Average Frequency Deviation for<br>11110000 pattern            | 225  | 250 | 275 | kHz | RF-PHY Specification<br>(TRM-LE/CA/05/C) |
| F1AVG_2M   | Average Frequency Deviation for<br>11110000 pattern for 2 Mbps | 450  | 500 | 550 | kHz | RF-PHY Specification<br>(TRM-LE/CA/05/C) |
| EO         | Eye opening = $\Delta F_{2AVG} / \Delta F_{1AVG}$              | 0.8  | –   | –   | –   | RF-PHY Specification<br>(TRM-LE/CA/05/C) |
| FTX, ACC   | Frequency Accuracy   | –150 | –   | 150 | kHz | RF-PHY Specification<br>(TRM-LE/CA/06/C) |

## Electrical specification

**Table 43 Bluetooth® LE subsystem specifications (continued)**

| Parameter   | Description  | Min | Typ | Max   | Unit          | Details/conditions                    |
|-------------|--|-----|-----|-------|---------------|---------------------------------------|
| FTX, MAXDR  | Maximum Frequency Drift  | -50 | -   | 50    | kHz           | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, INITDR | Initial Frequency Drift  | -20 | -   | 20    | kHz           | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, DR     | Maximum Drift Rate   | -20 | -   | 20    | kHz/<br>50 µs | RF-PHY Specification (TRM-LE/CA/06/C) |
| IBSE1       | In Band Spurious Emission at 2 MHz offset (1 Mbps)<br>In Band Spurious Emission at 4 MHz offset (2 Mbps) | -   | -   | -20   | dBm           | RF-PHY Specification (TRM-LE/CA/03/C) |
| IBSE2       | In Band Spurious Emission at 3 MHz offset (1 Mbps)<br>In Band Spurious Emission at 6 MHz offset (2 Mbps) | -   | -   | -30   | dBm           | RF-PHY Specification (TRM-LE/CA/03/C) |
| TXSE1       | Transmitter Spurious Emissions (Averaging), < 1.0 GHz  | -   | -   | -55.5 | dBm           | FCC-15.247                            |
| TXSE2       | Transmitter Spurious Emissions (Averaging), > 1.0 GHz  |     |     | -41.5 | dBm           | FCC-15.247                            |

### General RF specification

|       |                           |      |      |      |      |   |
|-------|---------------------------|------|------|------|------|---|
| FREQ  | RF Operating Frequency    | 2400 | -    | 2482 | MHz  | - |
| CHBW  | Channel Spacing           | -    | 2    | -    | MHz  | - |
| DR1   | On-air Data Rate (1 Mbps) | -    | 1000 | -    | Kbps | - |
| DR2   | On-air Data Rate (2 Mbps) | -    | 2000 | -    | Kbps | - |
| TXSUP | Transmitter Startup time  | -    | 80   | 82   | µs   | - |
| RXSUP | Receiver Startup time     | -    | 80   | 82   | µs   | - |

### RSSI specification

|           |                    |    |   |   |    |                                      |
|-----------|--------------------|----|---|---|----|--------------------------------------|
| RSSI, ACC | RSSI Accuracy      | -4 | - | 4 | dB | -95 dBm to -20 dBm measurement range |
| RSSI, RES | RSSI Resolution    | -  | 1 | - | dB | -                                    |
| RSSI, PER | RSSI Sample Period | -  | 6 | - | µs | -                                    |

**Table 44 Precision ILO (PILO) specifications**

| Parameter         | Description                             | Min  | Typ   | Max | Unit | Details/conditions           |
|-------------------|---|------|-------|-----|------|------------------------------|
| I <sub>PILO</sub> | Operating current                       | -    | 1.2   | 4   | µA   | -                            |
| F <sub>PILO</sub> | PILO nominal frequency                  | -    | 32768 | -   | Hz   | T = 25°C with 20 ppm crystal |
| ACC_PILO          | PILO accuracy with periodic calibration | -500 | -     | 500 | ppm  | -                            |

## 8 Environmental specifications

### 8.1 Environmental compliance

This Infineon Bluetooth® LE module is built in compliance with RoHS and Halogen Free (HF) directives. The Infineon module and components used to produce this module are RoHS and HF compliant.

### 8.2 RF certification

The CYBLE-416070-02 module is certified under the following RF certification standards:

- FCC ID: WAP6045
- CE
- ISED: 7922A-6045
- MIC: 201-180370

### 8.3 Environmental conditions

**Table 45** describes the operating and storage conditions for the Infineon Bluetooth® LE module.

**Table 45 Environmental conditions for CYBLE-416070-02**

| Description   | Minimum specification | Maximum specification       |
|---|-----------------------|-----------------------------|
| Operating temperature   | –40°C                 | 85°C                        |
| Operating humidity (relative, non-condensation)               | 5%                    | 85%                         |
| Thermal ramp rate   | –                     | 3°C/minute                  |
| Storage temperature   | –40°C                 | 85°C                        |
| Storage temperature and humidity                              | –                     | 85° C at 85%                |
| ESD: Module integrated into system components <sup>[10]</sup> | –                     | 15 kV Air<br>2.2 KV Contact |

### 8.4 ESD and EMI protection

Exposed components require special attention to ESD and EMI.

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device handling:** Proper ESD protocol must be followed in manufacturing to ensure component reliability.

#### Note

10. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500 V HBM.

## 9 Regulatory information

### 9.1 FCC

#### FCC NOTICE:

The device CYBLE-416070-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. Transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Infineon may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instruction may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP6045.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP6045".

#### ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed in [Table 14](#). When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

#### RF EXPOSURE:

To comply with FCC RF Exposure requirements, the OEM must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in [Table 14](#), to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-416070-02 is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-416070-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

## 9.2 ISED

### Innovation, Science and Economic Development (ISED) Canada Certification

CYBLE-416070-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada.

License: IC: 7922A-6045

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from [www.ic.gc.ca](http://www.ic.gc.ca).

This device has been designed to operate with the antennas listed in **Table 14**, having a maximum gain of -0.5 dBi. Antennas not included in **Table 14** or having a gain greater than -0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### ISED NOTICE:

The device CYBLE-416070-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBLE-416070-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

#### ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé.

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-6045. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-6045".

## Regulatory information

Le fabricant d'équipement d'origine (OEM) doit s'assurer que les exigences d'étiquetage ISED sont respectées. Cela comprend une étiquette clairement visible à l'extérieur de l'enceinte OEM spécifiant l'identifiant Infineon IC approprié pour ce produit ainsi que l'avis ISED ci-dessus. L'identificateur IC est 7922A-6045. En tout cas, le produit final doit être étiqueté dans son extérieur avec "Contient IC: 7922A-6045".

### 9.3 European Declaration of Conformity

Hereby, Infineon declares that the Bluetooth® module CYBLE-416070-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

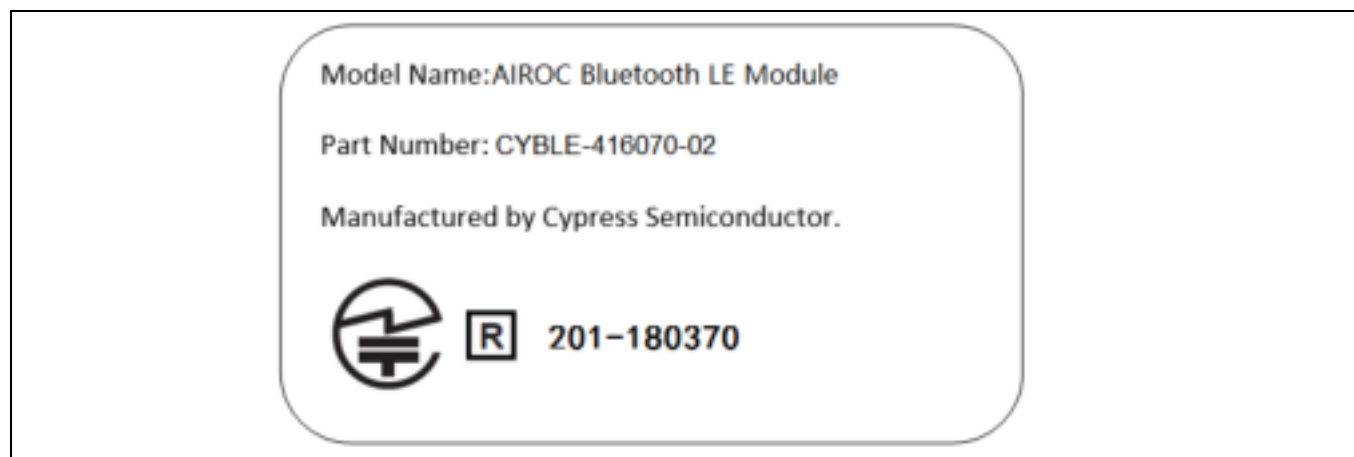


All versions of the CYBLE-416070-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

### 9.4 MIC Japan

CYBLE-416070-02 is certified as a module with type certification number 201-180370. End products that integrate CYBLE-416070-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.



Packaging

# 10 Packaging

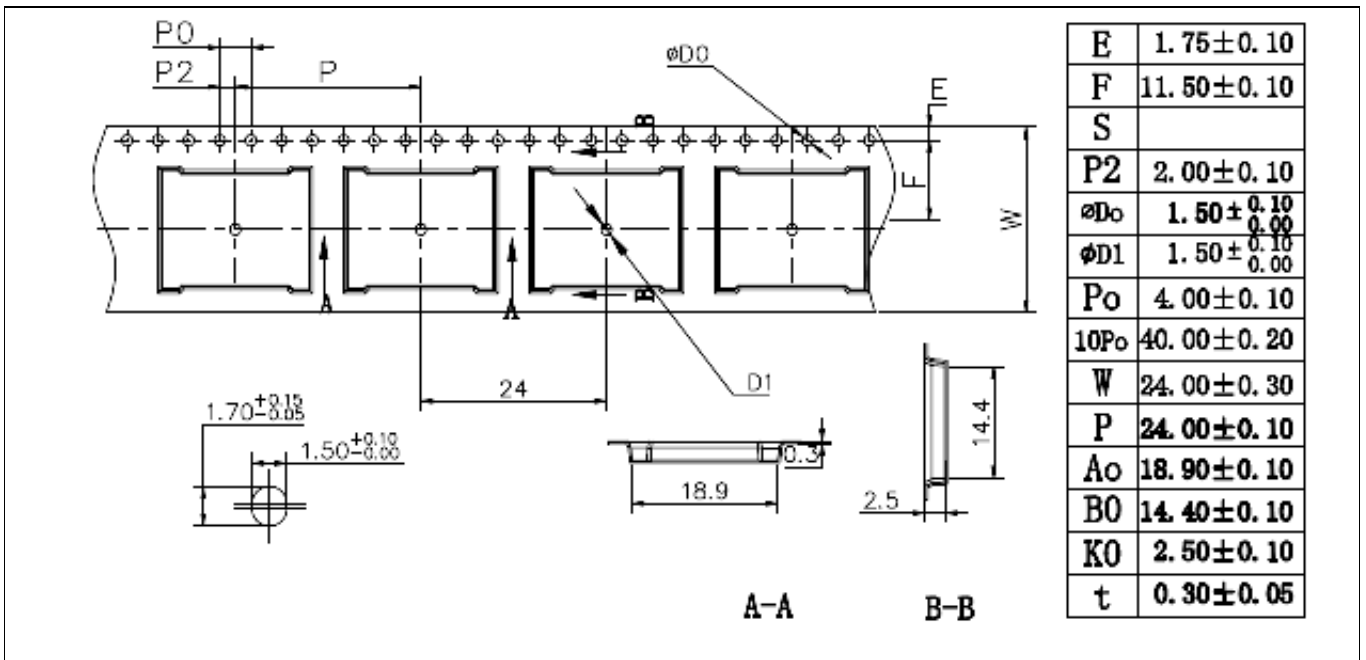
**Table 46 Solder reflow peak temperature**

| Module part number | Package    | Maximum peak temperature | Maximum time at peak temperature | No. of cycles |
|--------------------|------------|--------------------------|----------------------------------|---------------|
| CYBLE-416070-02    | 43-pad SMT | 260 °C                   | 30 seconds                       | 2             |

**Table 47 Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

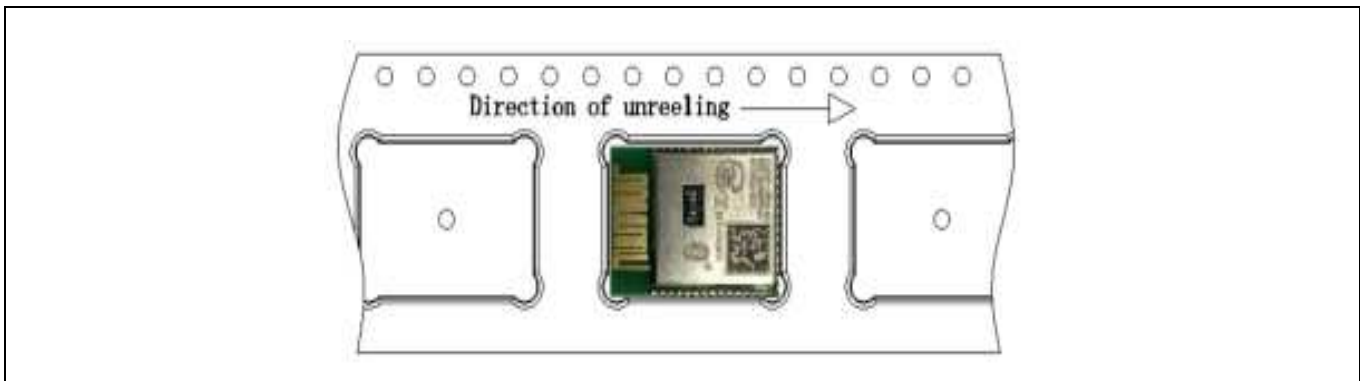
| Module part number | Package    | MSL   |
|--------------------|------------|-------|
| CYBLE-416070-02    | 43-pad SMT | MSL 3 |

The CYBLE-416070-02 is offered in tape and reel packaging. **Figure 21** details the tape dimensions used for the CYBLE-416070-02.



**Figure 21 CYBLE-416070-02 tape dimensions**

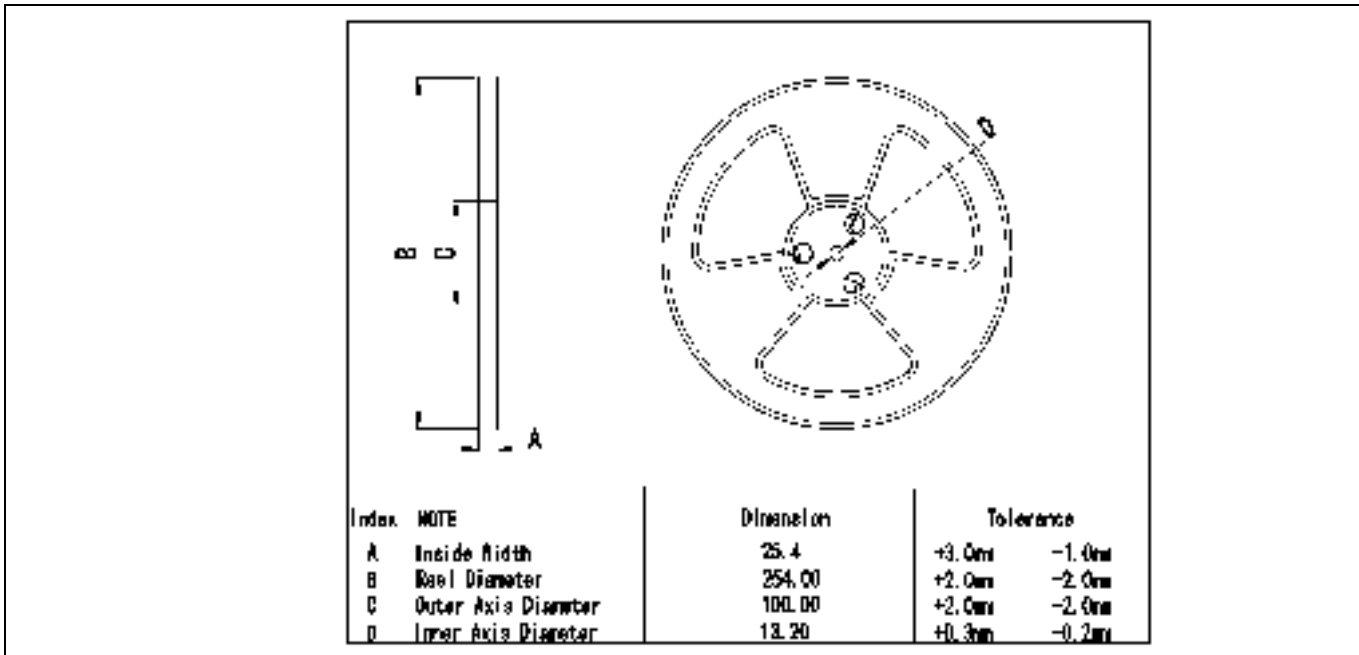
**Figure 22** details the orientation of the CYBLE-416070-02 in the tape as well as the direction for unreeling.



**Figure 22 Component orientation in tape and unreeling direction**

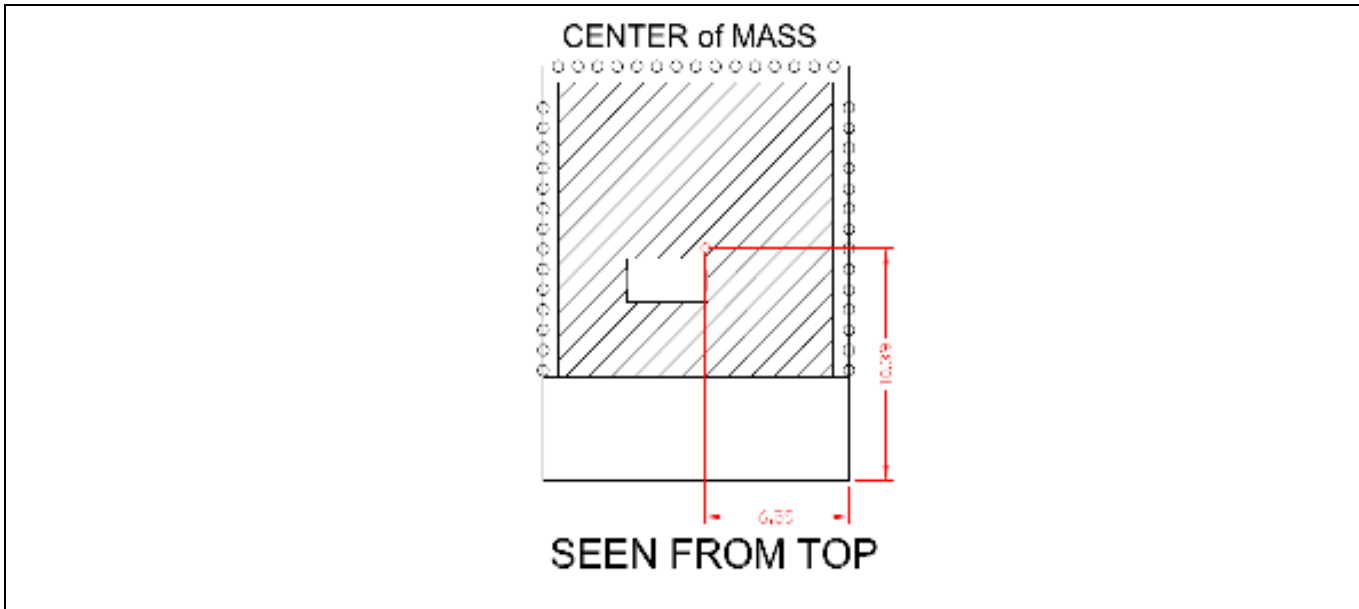


**Figure 23** details reel dimensions used for the CYBLE-416070-02.



**Figure 23** Reel dimensions

The CYBLE-416070-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-416070-02 is detailed in [Figure 24](#).



**Figure 24** CYBLE-416070-02 center of mass



## Ordering information

## 11 Ordering information

**Table 48** lists the CYBLE-416070-02 part number and features. **Table 49** lists the reel shipment quantities for the CYBLE-416070-02.

**Table 48 Ordering information**

| MPN             | Features       |                 |            |           |     |           |                  |                |                |            |         |      | Package |
|-----------------|----------------|-----------------|------------|-----------|-----|-----------|------------------|----------------|----------------|------------|---------|------|---------|
|                 | CPU speed (M4) | CPU speed (M0+) | Flash (KB) | SRAM (KB) | UDB | CAPSENSE™ | Direct LCD Drive | 12-bit SAR ADC | LP Comparators | SCB Blocks | I2S/PDM | GPIO |         |
| CYBLE-416070-02 | 150/50         | 100/25          | 1024       | 288       | 12  | ✓         | ✓                | 1 Msps         | 2              | 5          | ✓       | 36   | 43-SMT  |

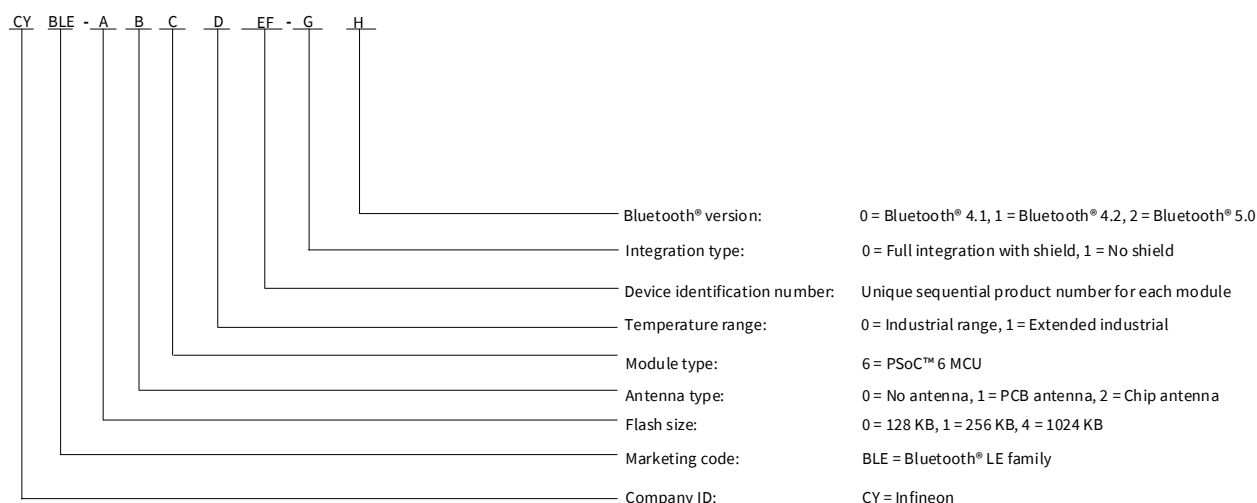
**Table 49 Tape and reel package quantity and minimum order amount**

| Description                  | Minimum reel quantity | Maximum reel quantity | Comments                           |
|------------------------------|-----------------------|-----------------------|------------------------------------|
| Reel Quantity                | 500                   | 500                   | Ships in 500 unit reel quantities. |
| Minimum Order Quantity (MOQ) | 500                   | –                     |                                    |
| Order Increment (OI)         | 500                   | –                     |                                    |

The CYBLE-416070-02 is offered in tape and reel packaging. The CYBLE-416070-02 ships with a maximum of 500 Unit/reel.

### 11.1 Part numbering convention

The part numbers are of the form CYBLE-ABCDEF-GH where the fields are defined as follows.



For additional information and a complete list of Infineon Bluetooth® LE products, contact your local Infineon sales representative. To locate the nearest Infineon office, visit our [website](#).

## 12 Acronyms

**Table 50 Acronyms used in this document**

| Acronym | Description  |
|---------|--|
| 3DES    | Triple Data Encryption Standard  |
| abus    | analog local bus   |
| ADC     | analog-to-digital converter  |
| AES     | Advanced Encryption Standard   |
| AG      | analog global  |
| AHB     | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus |
| ALU     | arithmetic logic unit  |
| AMUXBUS | analog multiplexer bus   |
| API     | application programming interface  |
| APSR    | application program status register  |
| Arm®    | advanced RISC machine, a CPU architecture  |
| ATM     | automatic thump mode   |
| BW      | bandwidth  |
| CAN     | Controller Area Network, a communications protocol   |
| CMRR    | common-mode rejection ratio  |
| CPU     | central processing unit  |
| CTBm    | Continuous Time Block mini   |
| CRC     | cyclic redundancy check, an error-checking protocol  |
| DAC     | digital-to-analog converter, see also IDAC, VDAC   |
| DFB     | digital filter block   |
| DIO     | digital input/output, GPIO with only digital capabilities, no analog. See GPIO.                  |
| DMIPS   | Dhrystone million instructions per second  |
| DMA     | direct memory access, see also TD  |
| DNL     | differential nonlinearity, see also INL  |
| DNU     | do not use   |
| DR      | port write data registers  |
| DSI     | digital system interconnect  |
| DWT     | data watchpoint and trace  |
| ECC     | error correcting code or Elliptic Curve Cryptography   |
| ECO     | external crystal oscillator  |
| EEPROM  | electrically erasable programmable read-only memory  |
| EMI     | electromagnetic interference   |
| EMIF    | external memory interface  |
| EOC     | end of conversion  |
| EOF     | end of frame   |
| EPSR    | execution program status register  |

## Acronyms

**Table 50**      **Acronyms used in this document** *(continued)*

| Acronym                  | Description  |
|--------------------------|--|
| ESD                      | electrostatic discharge                                |
| ETM                      | embedded trace macrocell                               |
| FIR                      | finite impulse response, see also IIR                  |
| FPB                      | flash patch and breakpoint                             |
| FS                       | full-speed   |
| GPIO                     | general-purpose input/output, applies to a PSoC™ pin   |
| HVI                      | high-voltage interrupt, see also LVI, LVD              |
| IC                       | integrated circuit                                     |
| IDAC                     | current DAC, see also DAC, VDAC                        |
| IDE                      | integrated development environment                     |
| I <sup>2</sup> C, or IIC | Inter-Integrated Circuit, a communications protocol    |
| IIR                      | infinite impulse response, see also FIR                |
| ILO                      | internal low-speed oscillator, see also IMO            |
| IMO                      | internal main oscillator, see also ILO                 |
| INL                      | integral nonlinearity, see also DNL                    |
| I/O                      | input/output, see also GPIO, DIO, SIO, USBIO           |
| IPOR                     | initial power-on reset                                 |
| IPSR                     | interrupt program status register                      |
| IRQ                      | interrupt request                                      |
| ITM                      | instrumentation trace macrocell                        |
| LCD                      | liquid crystal display                                 |
| LIN                      | Local Interconnect Network, a communications protocol. |
| LR                       | link register  |
| LUT                      | lookup table   |
| LVD                      | low-voltage detect, see also LVI                       |
| LVI                      | low-voltage interrupt, see also HVI                    |
| LVTTL                    | low-voltage transistor-transistor logic                |
| MAC                      | multiply-accumulate                                    |
| MCU                      | microcontroller unit                                   |
| MISO                     | master-in slave-out                                    |
| NC                       | no connect   |
| NMI                      | nonmaskable interrupt                                  |
| NRZ                      | non-return-to-zero                                     |
| NVIC                     | nested vectored interrupt controller                   |
| NVL                      | nonvolatile latch, see also WOL                        |
| opamp                    | operational amplifier                                  |
| PAL                      | programmable array logic, see also PLD                 |
| PC                       | program counter  |
| PCB                      | printed circuit board                                  |
| PDM                      | Pulse-Density Modulation                               |

## Acronyms

**Table 50**      **Acronyms used in this document** *(continued)*

| Acronym | Description  |
|---------|--|
| P/E     | Program/Erase  |
| PGA     | programmable gain amplifier                                  |
| PHUB    | peripheral hub   |
| PHY     | physical layer   |
| PICU    | port interrupt control unit                                  |
| PLA     | programmable logic array                                     |
| PLD     | programmable logic device, see also PAL                      |
| PLL     | phase-locked loop  |
| PMDD    | package material declaration data sheet                      |
| POR     | power-on reset   |
| PRES    | precise power-on reset                                       |
| PRS     | pseudo random sequence                                       |
| PS      | port read data register                                      |
| PSoC™   | Programmable System-on-Chip                                  |
| PSRR    | power supply rejection ratio                                 |
| PWM     | pulse-width modulator  |
| RAM     | random-access memory   |
| RMS     | root-mean-square   |
| RISC    | reduced-instruction-set computing                            |
| RSA     | Rivest–Shamir–Adleman  |
| RTC     | real-time clock  |
| RTL     | register transfer language                                   |
| RTR     | remote transmission request                                  |
| RX      | receive  |
| SAR     | successive approximation register                            |
| SC/CT   | switched capacitor/continuous time                           |
| SCL     | I <sup>2</sup> C serial clock                                |
| SDA     | I <sup>2</sup> C serial data                                 |
| S/H     | sample and hold  |
| SIG     | Special Interest Group                                       |
| SINAD   | signal to noise and distortion ratio                         |
| SIO     | special input/output, GPIO with advanced features. See GPIO. |
| SOC     | start of conversion  |
| SOF     | start of frame   |
| S/PDIF  | Sony/Philips Digital Interface                               |
| SPI     | Serial Peripheral Interface, a communications protocol       |
| SR      | slew rate  |
| SRAM    | static random access memory                                  |
| SRES    | software reset   |
| SRSS    | System Resources Subsystem                                   |

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 Acronyms

**Table 50**      **Acronyms used in this document** *(continued)*

| Acronym | Description  |
|---------|--|
| SWD     | serial wire debug, a test protocol                                     |
| SWV     | single-wire viewer   |
| TD      | transaction descriptor, see also DMA                                   |
| THD     | total harmonic distortion  |
| TIA     | transimpedance amplifier   |
| TRM     | technical reference manual   |
| TRNG    | True Random Number Generator   |
| TTL     | transistor-transistor logic  |
| TX      | transmit   |
| UART    | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB     | universal digital block  |
| ULP     | Ultra-low power  |
| USB     | Universal Serial Bus   |
| USBIO   | USB input/output, PSoC™ pins used to connect to a USB port             |
| VDAC    | voltage DAC, see also DAC, IDAC  |
| WDT     | watchdog timer   |
| WOL     | write once latch, see also NVL   |
| WRES    | watchdog timer reset   |
| XRES    | external reset I/O pin   |
| XTAL    | crystal  |

## 13 Document conventions

### 13.1 Unit of measure

**Table 51 Unit of measure**

| Symbol | Unit of Measure        |
|--------|------------------------|
| °C     | degrees Celsius        |
| dB     | decibel                |
| dBm    | decibel-milliwatts     |
| fF     | femtofarads            |
| Hz     | hertz                  |
| KB     | 1024 bytes             |
| kbps   | kilobits per second    |
| Khr    | kilohour               |
| kHz    | kilohertz              |
| kΩ     | kilo ohm               |
| ksps   | kilosamples per second |
| LSB    | least significant bit  |
| Mbps   | megabits per second    |
| MHz    | megahertz              |
| MΩ     | mega-ohm               |
| Msp    | megasamples per second |
| μA     | microampere            |
| μF     | microfarad             |
| μH     | microhenry             |
| μs     | microsecond            |
| μV     | microvolt              |
| μW     | microwatt              |
| mA     | milliampere            |
| ms     | millisecond            |
| mV     | millivolt              |
| nA     | nanoampere             |
| ns     | nanosecond             |
| nV     | nanovolt               |
| Ω      | ohm                    |
| pF     | picofarad              |
| ppm    | parts per million      |
| ps     | picosecond             |
| s      | second                 |
| sps    | samples per second     |
| sqrtHz | square root of hertz   |
| V      | volt                   |



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Revision history

**Revision history**

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| **               | 2022-01-13      | Initial release        |

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