DS-52832-02

Datasheet

Version：V1.0.0

SHEZHEN DEASINO TECHNOLOGY.,LTD

VERSION HISTORY

REVISION	AMENDMENT	DATA	
0.01	Dimension Chang		

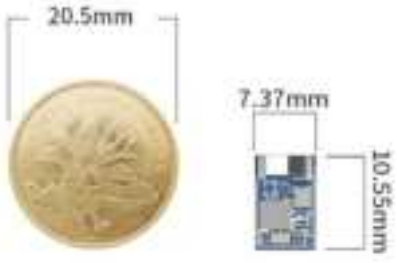
DESCRIPTION

DS-52832-02 is an external antenna Bluetooth low power module. DS-52832-02 integrates all features of Bluetooth radio,software stack,GATT based profiles,antenna and host end user applications,which means no external micro controller. It provides a Bluetooth Low Energy fully compliant system for a data communication. At +4 dBm TX Power and -93dBm RX Sensitivity DS-52832-02 has best RF performance.

APPLICATIONFEATURE

-Commercial
-Sports and fitness
-Healthcare
-Medical sensors
-Home entertainment
- Watch
- Human interface devices

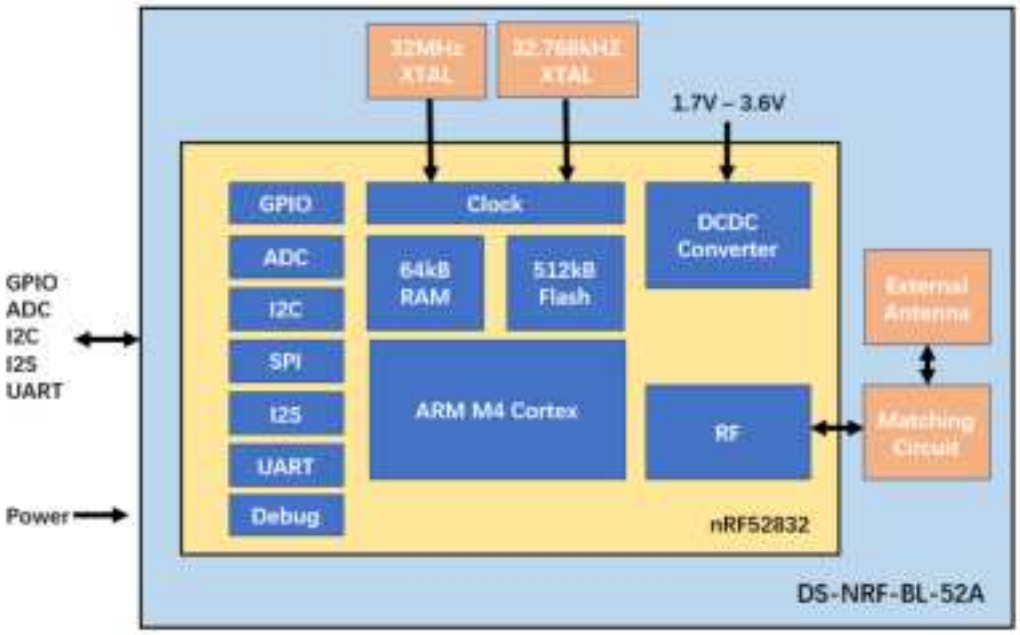
-Bluetooth v5.0 Single Mode Compliant
-Integrated Bluetooth Smart Stack
  .GAP, GATT,L2CAP and SMP
  .Bluetooth Smart profiles
- RF Performance
  .Transmit power:+4dBm(-20 dBm to +4 dBm)
  .Receiver sensitivity:-96 dBm
- Low Power Consumption
  .Transmit:7.5 mA peak
  .Receiver:12.9 mA peak
  .Sleep mode:0.5uA
- Peripheral Interfaces
  .UART/SPI(Master/Slave)/I2C
  .GPIO
  .12-bit ADC
  .I2S and PDM
  .Temperature Sensor
- Power supply:1.7 to 3.6V
- Dimension:7.37x10.5x2.3 mm(W x L x H)



<Figure 1.DS-52832-02>

1.Block Diagram

DS-52832-02 block diagram is illustrated in figure 2 below.



<Figure 2.Simplified block diagram of DS-52832-02>

CPU and Memory

The Main core is **ARM Cortex-M4.**The processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including"digital signal processing" ,"Single-cycle multiply and accumulate instructions", "hardware divide", "8 and 16-bit single instruction multiple data instructions" and " Single-precision floating-point unit"

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handing events at configurable priority levels via the Nested Vectored Interrupt Controller(NVIC).

The floating point unit (FPU) may generate exceptions when sed due to e.g. overflow or underflow. These exceptions will trigger the FPU interrupt.

The **64-KB SRAM**of 1024 byte page size and **512-KB flash**of 8-KB block size memory are provided

Power management

DS-52832-02supporttwodifferentpowersupplyalternativesof Internal LDO mode and Low voltage mode. In **internal LDO mode**, the system power is generated directly from the supply voltage VDD. In **low voltage mode**, the system power is supplied by 1.8V.

The module's power management features are System OFF mode and System ON mode. In **system OFF mode**, the module is in deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated.

In system ON mode, the module is fully operational and CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected by Low power or Constant latency.

Clock management

The module has a 32MHz main crystal oscillator and 32.768kHz RTC crystal oscillator.

Peripherals

The **general GPIO** is organized as one port with up to 30 I/Os enabling access and control of up to 28 pins through one port. Each GPIO can be accessed individually with the following user configurable features.

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system. The maximum number of pins that canbe interfaced through the PPI at the same time is limited by the number of GPIOTEchannels
- All pins can be individually configured to carry serial interface orquadrature demodulator signals.

The **transceiver** receives and transmits data directly to and from system memory for flexible andefficient packet data management. The module's transceiver has the following features.

- General modulation features

.GFSK modulation

.Data whitening

.On-air data rates(250 kbps/1 Mbps/2 Mbps)

- Transmitter with programmable output power of +4 dBm to-20 dBm, in 4 dB step
- RSSI function(1 dB resolution)
- Receiver with integrated channel filters achieving maximum sensitivity
- Baseband controller

.EasyDMA RX and TX packet transfer directly to and from RAM

.Dynamic payload length

.On-the-fly packet assembly/disassembly and AES CCM payload encryption

. 8 bit, 16 bit and 24 bit CRC check

The **timer** runs on the high-frequency clock source(HFCLK) and includes a four-bit (1/2X)prescalerthat can divide the timer input clock from the HFCLK controller Clock source selectionbetween PCLK16M and PCLKlM is automatic according to timer base frequency set by theprescaler. The timer base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral ofdevice. The PPI system also enables the TIMER task/event features to generate periodic outputand PWM signals to any GPIO. The number of input/outputs used at the same time is limited bythe number of GPIOTE channels.

The **temperature sensor** measures die temperature over the temperature range of the device with0. 25 degree resolution.

The **SPI** is implemented with Easy DMA support for ultra low power serial communication from anexternal SPI master. Easy DMA in conjunction with hardware-based semaphore mechanismsremoves all real-time requirements associated with controlling the SPI slave from a low priority
CPU execution context.

The **TWI** slave with EasyDMA(TWIS) is compatible with I2C operating at 100 kHz and 400 kHz.The TWI transmitter and receiver implement Easy DMA.

The Universal asynchronous receiver/transmitter with Easy DMA (**UART**) offers fast, full-duplex,asynchronous serial communication with built-in flow control (CTS, RTS)support in hardware at arate up to l Mbps, and Easy DMA data transfer from/to RAM.

The **ADC** supports up to eight external analog input channels, depending on package variant. Itan be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate. The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select AINO to AIN7 pins, or the VDD pin. Channels can be sampled individually inone-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampledin sequence. Channels can also be oversampled to improve noise performance.

The I2S (Inter-IC Sound)module, supports the original two-channel I2S format, and left or right-aligned formats. It implements Easy DMA for sample transfer directly to and from RAM withoutCPU intervention. The I2S peripheral has the following main features

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

2.Electrical Characteristic

2.1 Absolute Maximum rating

Rating	Min	Max	Unit
Storage Temperature	-40	+120	Degree
VDD, VDD_RF	-0.3	3.9	V
Other Terminal Voltages	-0.3	VDD+0.3	V

<Table1:Absolutes Maximum Ratings>

2.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating Temperature	-40	+85	Degree
VDD, VDD_RF*	1.7	3.6	V

<Table2: Recommended Operating Conditions>

*)normal supply voltage is 3.0 to 3.3V

2.3 Current consumption

Power mode	Condition	Min	Typ	Max	Unit
Transmit(DCDC,3V)	Pout = +4 dBm		7.5		mA
	Pout = 0 dBm		5.3		mA
Receive(DCDC,3V)	At 1 Mbps		11.7		mA
	At 2 Mbps		12.9		mA

<Table3: Current consumption>

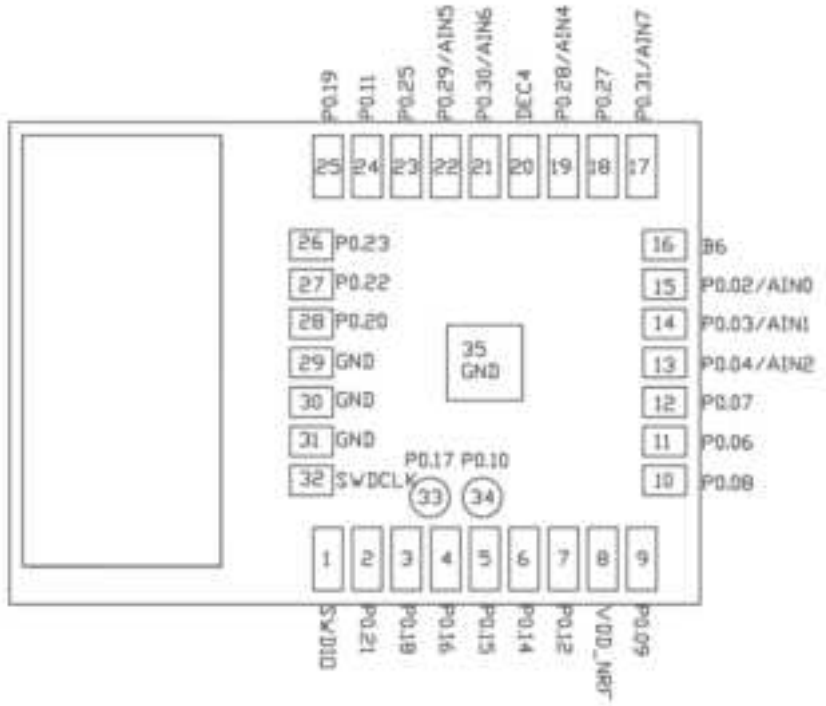
2.4 RF Characteristics

Data obtained using the official onboard antenna. Figure 3 below.

<Figure 3.Development board>

3. Pin Description

DS-52832-02 PIN descriptions are summarized in Figure 4 and Table 5 below.



<Figure 4. PIN descriptions>

.Bottom View(Bottom Pad)

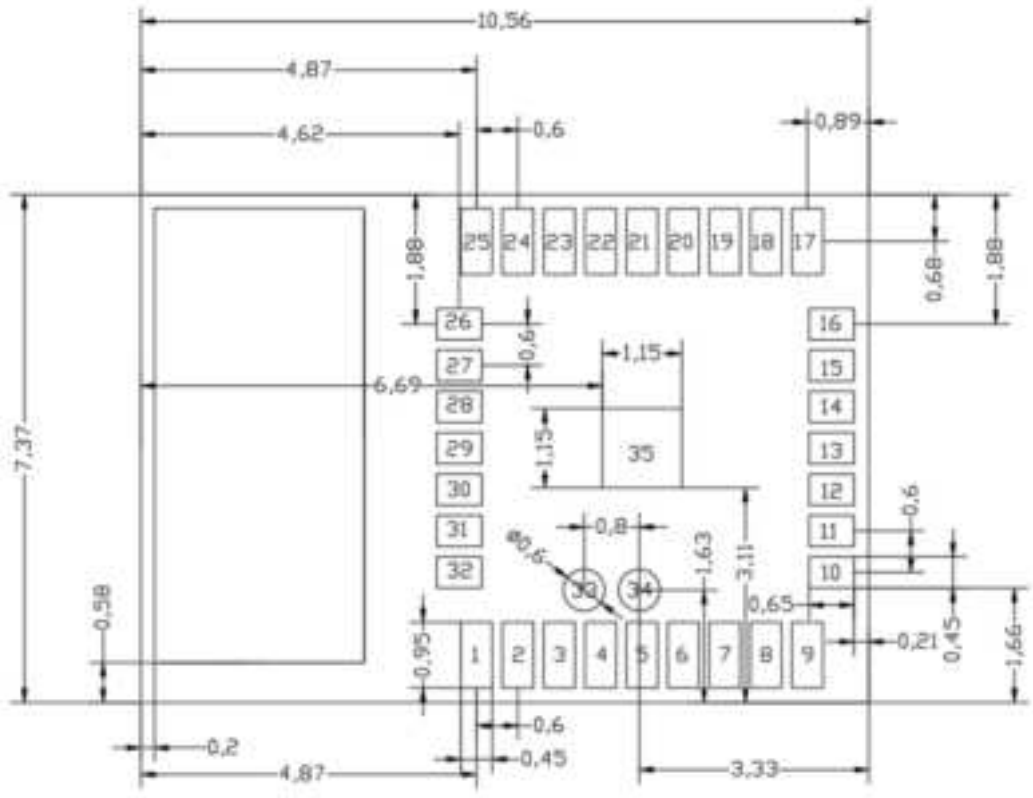
Pin	Name	Type	Description
1	SWDIO	Digital input	Serial Wire debug IO for debug and Programming.
2	P0.21	Digital I/O or REST	General purpose I/O pin. Configurable as pin reset.
3	P0.18	Digital I/O	General purpose I/O pin. Single Wire Output. Trace port output.
4	P0.16	Digital I/O	General purpose I/O pin. Trace port output
5	P0.15	Digital I/O	General purpose I/O pin.
6	P0.14	Digital I/O	General purpose I/O pin. Trace port output.
7	P0.12	Digital I/O	General purpose I/O pin.
8	VDD	Power	Power-supply pin.
9	P0.09	Digital I/O	General purpose I/O pin.
10	P0.08	Digital I/O	General purpose I/O pin.
11	P0.06	Digital I/O	General purpose I/O pin.
12	P0.07	Digital I/O	General purpose I/O pin.
13	P0.04 AIN2	Digital I/O Analog input	General purpose I/O pin. SAADC/COMP/LPCOMP input.

14	P0.03 AIN1	Digital I/O Analog input	General purpose I/O pin. SAADC/COMP/LPCOMP input.
15	P0.02 AIN0	Digital I/O Analog input	General purpose I/O pin. SAADC/COMP/LPCOMP input.
16	DCC	Power	DC/DC regulator output pin.
17	P0.31 AIN7	Digital I/O Analog input	General purpose I/O pin. SAADC/COMP/LPCOMP input.
18	P0.27	Digital I/O	General purpose I/O pin[2].
19	P0.28 AIN4	Digital I/O Analog input	General purpose I/O pin[2]. SAADC/COMP/LPCOMP input.
20	DEC4	Power	1V3 regulator supply decoupling. Input from DC/DC regulator. output from 1.3V LDO.
21	P0.30 AIN6	Digital I/O Analog input	General purpose I/O pin[2]. SAADC/COMP/LPCOMP input.
22	P0.29 AIN5	Digital I/O Analog input	General purpose I/O pin[2]. SAADC/COMP/LPCOMP input.
23	P0.25	Digital I/O	General purpose I/O pin[2].
24	P0.11	Digital I/O	General purpose I/O pin.
25	P0.19	Digital I/O	General purpose I/O pin.
26	P0.23	Digital I/O	General purpose I/O pin[2].
27	P0.22	Digital I/O	General purpose I/O pin[2].
28	P0.20 RRACECLK	Digital I/O	General purpose I/O pin. Trace port clock output.
29	GND	Power	Ground Pin
30	GND	Power	Ground Pin
31	GND	Power	Ground Pin
32	SWCLK	Digital input	Serial Wire debug IO for debug and Programming.
33	P0.17	Digital I/O	General purpose I/O pin.
34	P0.10	Digital I/O	General purpose I/O pin[1].
39	GND	Power	Ground Pin.
40	RF	Antenna	External antenna.

<Table 5: PIN descriptions>

4. Physical Dimensions

UINT : mm

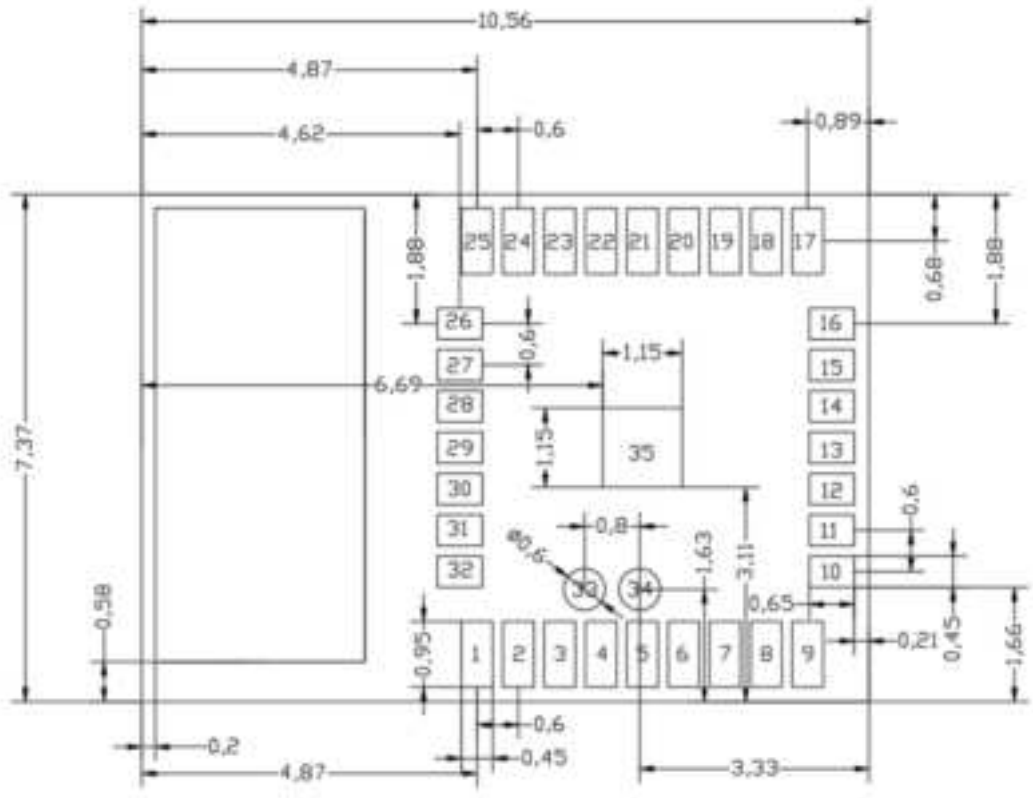


<Figure5.Phsical dimension>

·Top View(Bottom pad)

5.Layout

UINT : mm

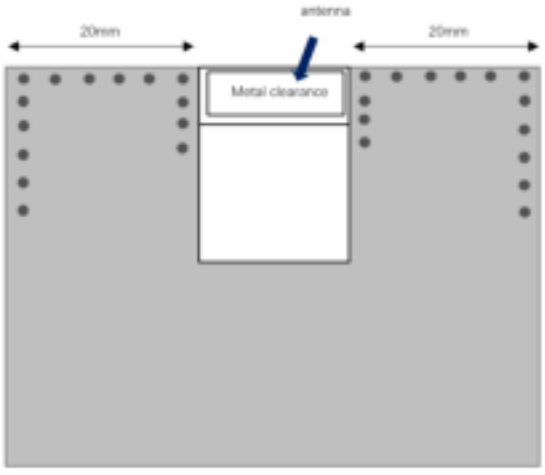


<Figure6.Layout>

·Top View(Bottom pad)

4.1 PCB design suggestion

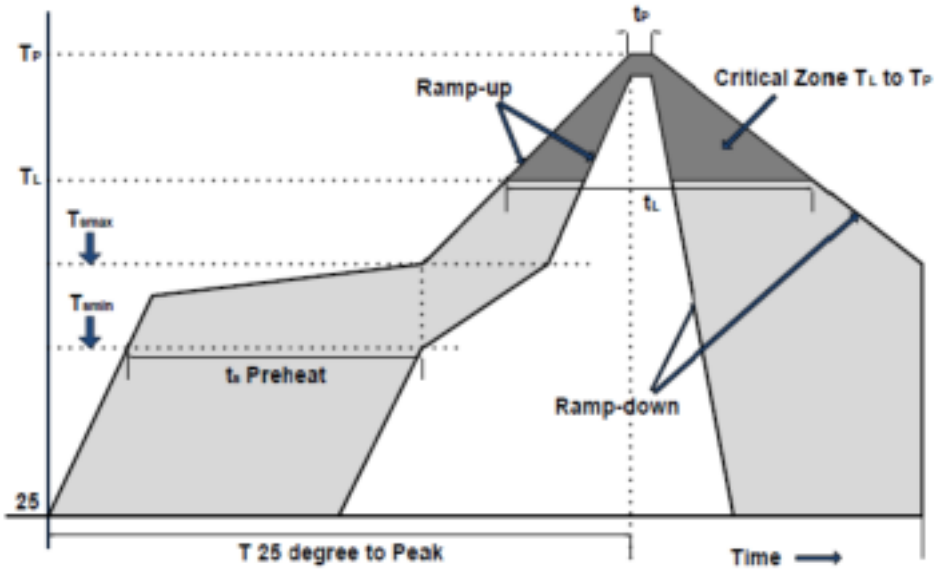
For the best performance of theDS-52810-03 module, do not place any metal or other obstacles in the clear area of the antenna, do not allow any plastic or insulating materials to touch the antenna, and make the PCBA design follow the design shown in figure 7



<Figure 7. PCBA design drawing>

6.Re-flow Temperature time profile

The data here is given only for guidance on solder and has to be adapted to your process and other re-flow parameters for example the used solder paste. The paste manufacturer provides a re-flow profile recommendation for his product.



<Figure10. Soldering Temperature time profile>

Preheat		Main Heat		Peak	
Tsmax		TLmax		tpmax	
Temperature	Time	Temperature	Time	Temperature	Time
Degree	sec	Degree	sec	Degree	sec
150	10	220	90	258	9
		230	40		
Parameter				Value	Unit
Average ramp-up rate				3	Degree/sec
Average ramp-down rate				6	Degree/sec
Max. Time 25degree to Peak Temperature				8	Min.

<Table 6: Soldering temperature parameters>

7.Contact information

COMPANY: SHEZHEN DEASINO TECHNOLOGY .,LTD (深圳市鼎欣茂科技有限公司)

ADDRESS: Floor3B. 4Building. YongQi Technology Park. YinTian Industrial Zone. XiXiang.Baoan District Shenzhen

TEL:0755-83418691-801

FAX:0755-83418691-803

Addendum

FCCID: 2AV9TDS-52832-02

(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module. For 15 B (§15.107 and if applicable §15.107) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101.

Integrator is reminded to assure that these installation instructions
will not be made available to the end user of the final host device.

The final host device, into which this RF Module isintegrated" hasto be labelled
with an auxilliary lable stating the FCC IDofthe RF Module,
such as "Contains FCC ID: 2AV9TDS-52832-02

"This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1)this devicemay not cause harmful interference, and
(2)this devicemust accept any interference received, including
interference thatmay cause undesired operation."

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection
against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
--Reorient or relocate the receiving antenna.
--Increase the separation between the equipment and receiver.
--Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
--Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Module statement

The single-modular transmitter is a self-contained, physically delineated, component for which compliance can be demonstrated independent of the host operating conditions, and which complies with all eight requirements of § 15.212(a)(1) as summarized below.
1) The radio elements have the radio frequency circuitry shielded.
2) The module has buffered modulation/data inputs to ensure that the device will comply with Part 15 requirements with any type of input signal.
3) The module contains power supply regulation on the module.
4) The module contains a permanently attached antenna.
5) The module demonstrates compliance in a stand-alone configuration.
6) The module is labeled with its permanently affixed FCC ID label
7) The module complies with all specific rules applicable to the transmitter, including all the conditions provided in the integration instructions by the grantee.
8) The module complies with RF exposure requirements.

This transmitter/module must not be collocated or operating in conjunction with any other antenna or transmitter

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15.247.

2.3 Specific operational use conditions

his transmitter/module and its antenna(s) must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer's instruction manual.

2.4 Limited module procedures

not applicable.

2.5 Trace antenna designs

It is "not applicable" as trace antenna which is not used on the module.

2.6 RF exposure considerations

This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This compliance to FCC radiation exposure limits for an uncontrolled environment, and minimum of 20cm separation between antenna and body.

The host product manufacturer would provide the above information to end users in their end-product manuals.

2.7 Antennas

Ceramic antenna; 0dBi;2.402 GHz～2.480GHz.

2.8 Label and compliance information

The end product must carry a physical label or shall use e-labeling followed KDB784748D01 and KDB 784748 stating "Contains Transmitter Module FCC ID: 2AV9TDS-52832-02".

2.9 Information on test modes and additional testing requirements

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Programming " direct test mode software " and use TI "Nordic nRFgo studio" driver to control fixed frequency for testing requirements. And programming application software for radiate test.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.