

# **AW-HM581**

## **IEEE 802.11ah Wireless LAN Module**

### **Datasheet**

**Rev. B**

**DF**

**(For STD)**

## Features

### General

- Support 902 ~ 928MHz frequency band
- Support single-stream data rate up to 32.5Mbps @8MHz or 15 Mbps @4MHz channel
- Support channel width options of 1/2/4/8 MHz
- Support Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
- Modulation: BPSK & QPSK, 16-QAM & 64 - QAM
- Support for 1 MHz and 2 MHz duplicate modes

### Host interface

- SDIO 2.0 (slave) Default Speed (DS) at 25MHz
- SDIO 2.0 (slave) High Speed (HS) at 50MHz
- Support for both 1-bit and 4-bit data mode
- Support for SPI mode operation

### Standards Supported

- IEEE Std 802.11ah-2016 compliant

### Security Features

- AES encryption engine
- Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- WPA3 including protected management

frames (PMF)

- Opportunistic Wireless Encryption (OWE)

### Peripheral Interfaces

- SDIO/SPI, I2C and UART
- Support for STA and AP roles



## Revision History

**Document NO: R2-2581-DST-01**

[illegible]

## Table of Contents

Features .....	2
Revision History .....	3
Table of Contents .....	4
1. Introduction .....	5
1.1 Product Overview .....	5
1.2 Block Diagram .....	6
1.3 Specifications Table .....	7
1.3.1 General .....	7
1.3.2 WLAN .....	7
1.3.3 Operating Conditions .....	8
2. Pin Definition .....	9
2.1 Pin Map .....	9
3. Electrical Characteristics .....	12
3.1 Absolute Maximum Ratings .....	12
3.2 Recommended Operating Conditions .....	12
3.3 Timing Sequence .....	13
3.3.1 SDIO Bus Timing .....	13
3.3.2 SPI Bus .....	14
3.3.3 UART Bus .....	14
3.3.4 I2C Bus Timing .....	15
3.4 Power Consumption .....	16
3.4.1 Transmit Power Consumption .....	16
3.4.2 Receive Power Consumption .....	16
4. Mechanical Information .....	17
4.1 Mechanical Drawing .....	17
5. Package information .....	18

## 1. Introduction

### 1.1 Product Overview

**AzureWave Technologies, Inc.** introduces the pioneer of the IEEE 802.11ah WIFI LGA module --- **AW-HM581**. The **AW-HM581** is an IEEE 802.11ah Wi-Fi module designed in compliance with the IEEE 802.11ah standard, supporting data rates up to 32.5 Mbps that operates in the Sub 1GHz license-exempt band, offering longer range and higher data rate for internet of things (IoT) applications. The **AW-HM581** enables streamlined data transfer interoperability with existing Wi-Fi networks while meeting up to 1Km long range data transfer with low power consumption requirements.

The **AW-HM581** integrated IEEE 802.11ah Sub-1G 8MHz Single-chip MAC/PHY/Radio SoC Morse Micro MM6108, ultra-long-reach PA, high linearity LNA, T/R switch, 32 MHz crystal and it has been designed for a simplified Wi-Fi HaLow connection to an external host for applications in which a customer wants to merely replace their prior RF technology with a Wi-Fi HaLow connection while leveraging the latest WPA3 security protocol. **AW-HM581** supports SDIO 2.0 compliant slave interface and SPI mode operation, and many peripherals such as general I2C, UART and GPIOs. In addition, its MAC supports for STA and AP roles.



## 1.2 Block Diagram

TBD

## 1.3 Specifications Table

### 1.3.1 General

Features	Description
<b>Product Description</b>	IEEE 802.11ah Wireless LAN Module
<b>Major Chipset</b>	Morse Micro MM6108 (48-pin QFN)
<b>Host Interface</b>	SDIO/SPI
<b>Dimension</b>	13mm x 13mm x 2.1mm (Tolerance remarked in mechanical drawing)
<b>Form Factor</b>	LGA module, 44 pins
<b>Antenna</b>	<ul style="list-style-type: none"> <li>For Stamp Module, “1T1R, external”</li> </ul> ANT Main: TX/RX
<b>Weight</b>	0.7g

### 1.3.2 WLAN

Features	Description					
WLAN Standard	IEEE 802.11ah					
WLAN VID/PID	TBD					
WLAN SVID/SPID	TBD					
Frequency Rage	USA 902 - 928 MHz					
Modulation	OFDM, BPSK, QPSK, 16-QAM, 64-QAM					
Channel Bandwidth	1/2/4/8 MHz					
Output Power (Board Level Limit)*		Min	Typ	Max	Unit	
	MCS0 (1/2/4/8 MHz) @EVM ≦ -5dB	21.5	23	24.5	dBm	
	MCS7 (1/2/4/8 MHz) @EVM ≦ -27dB	15.5	17	18.5	dBm	

<b>Receiver Sensitivity</b>		Min	Typ	Max	Unit
	MCS0 (1 MHz)		-100dBm	-95dBm	dBm
	MCS0 (2 MHz)		-97dBm	-92dBm	dBm
	MCS0 (4 MHz)		-94dBm	-89dBm	dBm
	MCS0 (8 MHz)		-91dBm	-86dBm	dBm
	MCS7 (1 MHz)		-82dBm	-77dBm	dBm
	MCS7 (2 MHz)		-79dBm	-74dBm	dBm
	MCS7 (4 MHz)		-76dBm	-71dBm	dBm
	MCS7 (8 MHz)		-73dBm	-68dBm	dBm
<b>Data Rate</b>	<ul style="list-style-type: none"> <li>■ 1 MHz Bandwidth: up to 3.333Mbps</li> <li>■ 2 MHz Bandwidth: up to 7.222Mbps</li> <li>■ 4 MHz Bandwidth: up to 15Mbps</li> <li>■ 8 MHz Bandwidth: up to 32.5Mbps</li> </ul>				
<b>Security</b>	<ul style="list-style-type: none"> <li>■ AES encryption engine</li> <li>■ Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)</li> <li>■ WPA3 including protected management frames (PMF)</li> <li>■ Opportunistic Wireless Encryption (OWE)</li> </ul>				

**\* If you have any certification questions about output power please contact FAE directly.**

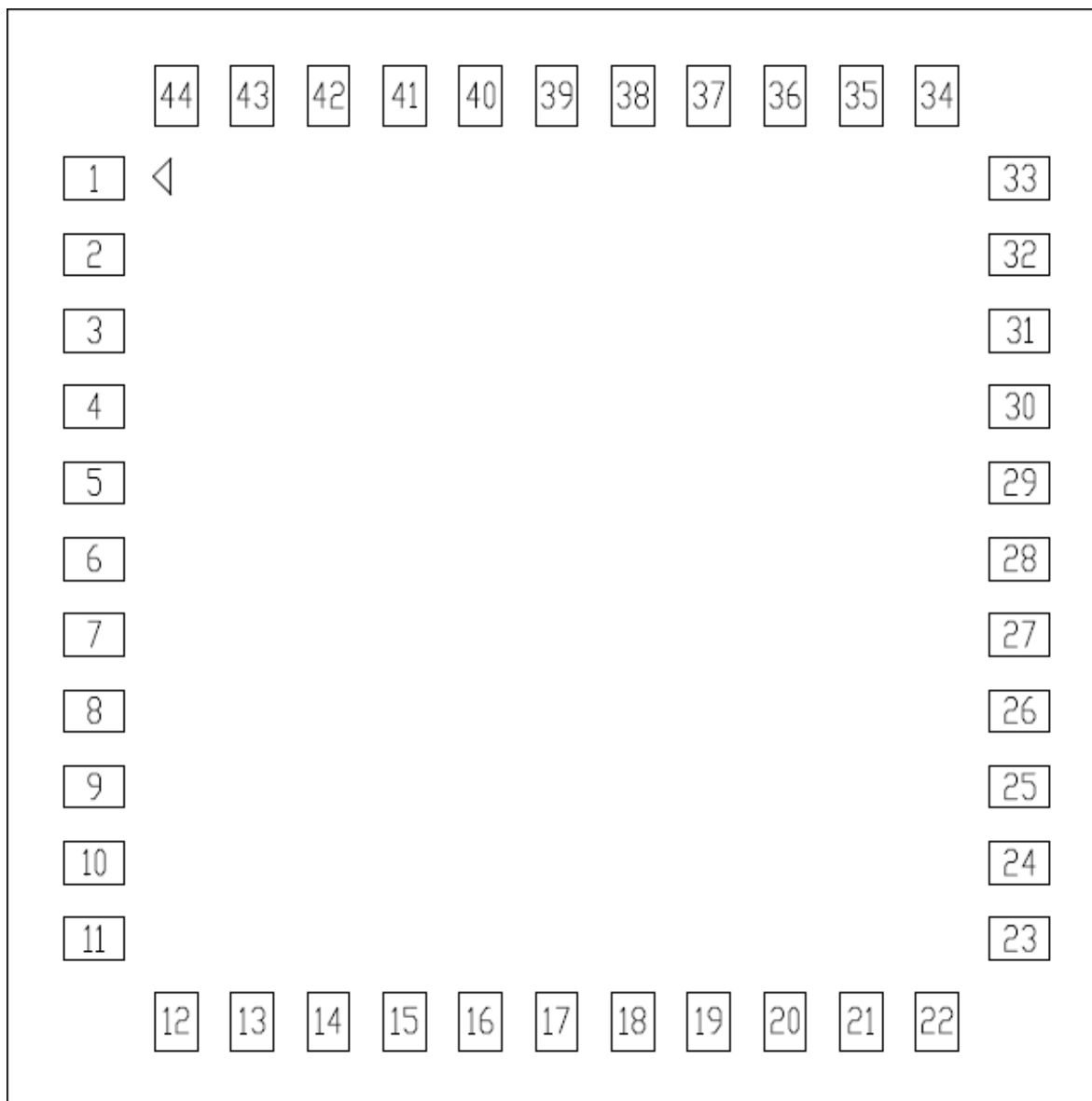
### 1.3.3 Operating Conditions

Features	Description
<b>Operating Conditions</b>	
<b>Voltage</b>	VBAT: 3.3V VDDIO: 3.3V
<b>Operating Temperature</b>	-40°C~85 °C
<b>Operating Humidity</b>	less than 85%R.H
<b>Storage Temperature</b>	-40°C~90 °C
<b>Storage Humidity</b>	less than 60%R.H
<b>ESD Protection</b>	
<b>Human Body Model</b>	TBD
<b>Changed Device Model</b>	TBD



## 2. Pin Definition

### 2.1 Pin Map



**AW-HM581 Pin Map (Top View)**

## 2.2 Pin Table

Pin No.	Definition	Basic Description	Voltage	Type
1	GND	GROUND		GND
2	ANT	RF IN/OUT		I/O
3	GND	GROUND		GND
4	NC	No Connection		
5	NC	No Connection		
6	MM_WAKE	WAKE from sleep		I
7	NC	No Connection		
8	NC	No Connection		
9	VBAT	3.3V power supply	3.3V	Power
10	GND	GROUND		GND
11	GND	GROUND		GND
12	MM_RESET_N	Reset (active low)		I/O
13	NC	No Connection		
14	MM_SD_D2	SDIO Data pin 2		I/O
15	MM_SD_D3	SDIO Data pin 3		I/O
16	MM_SD_CMD	SDIO Command pin		I/O
17	MM_SD_CLK	SDIO Clock pin (input)		I
18	MM_SD_D0	SDIO Data pin 0		I/O
19	MM_SD_D1	SDIO Data pin 1		I/O
20	GND	GROUND		GND
21	NC	No Connection		
22	VDDIO	I/O supply Input		Power
23	NC	No Connection		

24	NC	No Connection		I
25	MM_GPIO6	General purpose I/O		I/O
26	MM_GPIO5	General purpose I/O		I/O
27	MM_GPIO4	General purpose I/O		I/O
28	MM_GPIO3	General purpose I/O		I/O
29	MM_GPIO2	General purpose I/O		I/O
30	MM_GPIO1	General purpose I/O		I/O
31	GND	GROUND		GND
32	MM_GPIO7	General purpose I/O		I/O
33	GND	GROUND		GND
34	MM_GPIO11	General purpose I/O		I/O
35	MM_GPIO10	General purpose I/O		I/O
36	GND	GROUND		GND
37	MM_GPIO9	General purpose I/O		I/O
38	MM_GPIO8	General purpose I/O		I/O
39	MM_JTAG_TDO	JTAG data output		O
40	MM_GPIO0	General purpose I/O		I/O
41	MM_JTAG_TMS	JTAG mode selection		I
42	MM_JTAG_TDI	JTAG data input		I
43	MM_JTAG_TRST	JTAG reset		I
44	MM_JTAG_TCK	JTAG clock		I

### 3. Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.3V power supply	-0.5	-	4.3	V
VDDIO	I/O supply Input	-0.5	-	4.3	V
T <sub>stg</sub>	Storage temperature	-40	-	90	°C

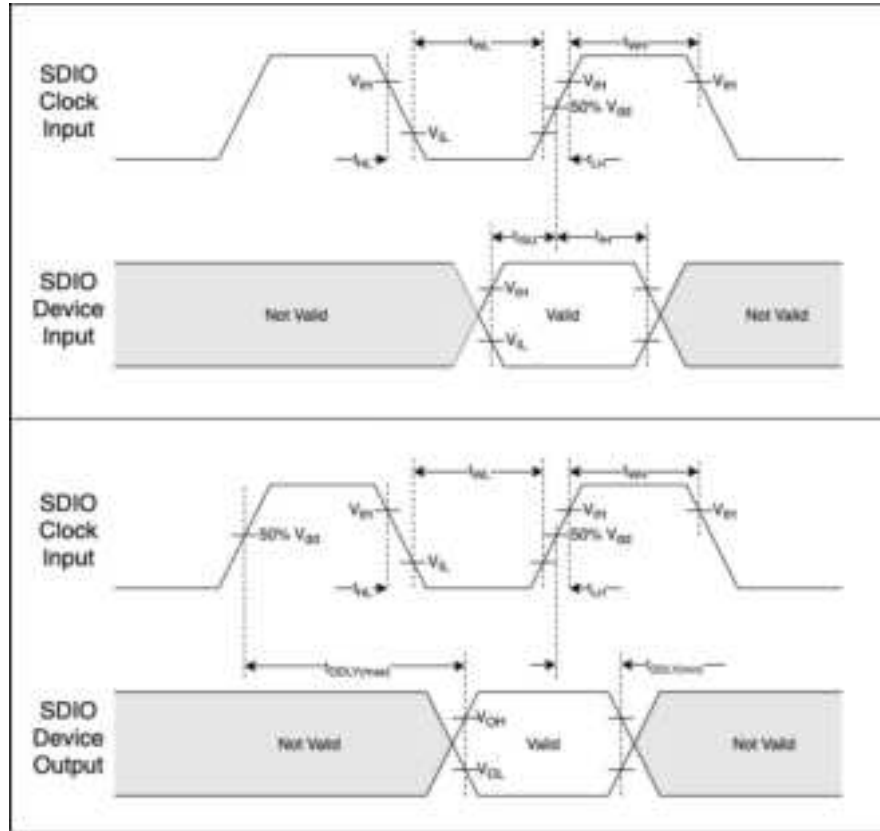
#### 3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.3V power supply	3.0	3.3	3.6	V
VDDIO	3.3V I/O supply Input	1.8	3.3	VBAT	V
T <sub>AMBIENT</sub>	Ambient temperature	-40	25	85	°C

### 3.3 Timing Sequence

#### 3.3.1 SDIO Bus Timing

The SDIO clock rate supports up to 50MHz. The device always operates in SD high speed mode.



Parameter	Min	Max
Clock parameters		
Clock frequency	0MHz	50MHz
Clock low time ( $t_{LCL}$ )	7ns	
Clock high time ( $t_{HCL}$ )	7ns	
Clock rise time ( $t_{LCL}$ )		3ns
Clock fall time ( $t_{HCL}$ )		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time ( $t_{SU}$ )	5ns	
Input hold time ( $t_{HD}$ )	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ( $t_{OZD}$ )		14ns
Output hold time ( $t_{OHD}$ )	2.5ns	
Total system capacitance for each line		40pF

### 3.3.2 SPI Bus

The SPI clock rate supports up to 50MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge) after being initialized.

### 3.3.3 UART Bus

Two universal asynchronous receiver/transmitter (UARTs) are available and provide a means for serial communication to off-chip devices. The UART cores are as-provided by the SiFive IP repository. The UART peripheral does not support hardware flow control or other modem control signals, or synchronous serial data transfers.

We will clock the UARTs with a maximum clock speed of 30MHz (TBD), meaning maximum baud of the UART will be around 30Mbaud or 30Mbits/s if a divisor of 0 is specified.

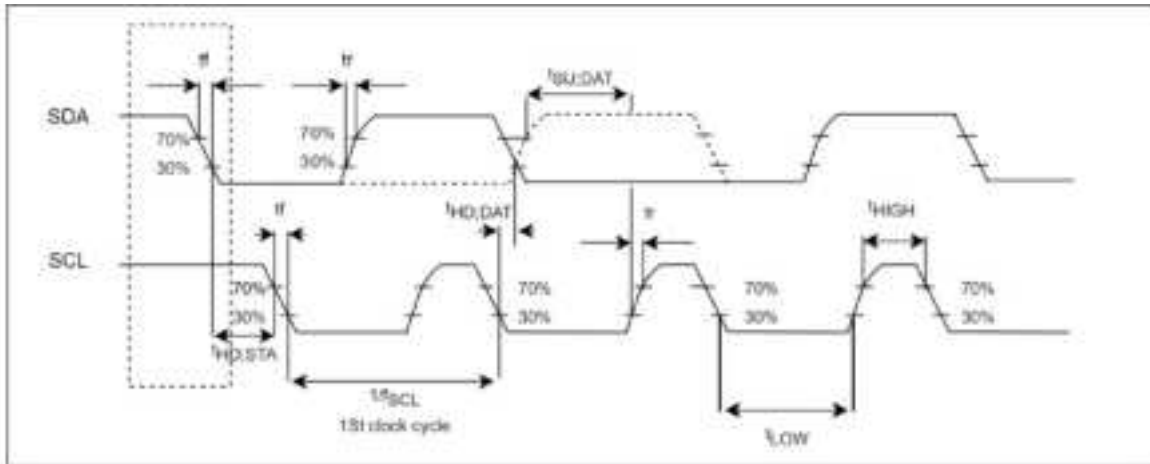
Pin	Name	Default Function	I/O Function
32	MM_GPIO7	GPIO	UART1 Tx
25	MM_GPIO6	GPIO	UART1 Rx
28	MM_GPIO3	GPIO	UART0 Tx
29	MM_GPIO2	GPIO	UART0 Rx

### 3.3.4 I2C Bus Timing

An I2C master interface is available. It consists of two lines, SDA and SCL, which are bidirectional, connected to a positive supply voltage via a current-source or pull-up resistor.

Pin	Name	Default Function	I/O Function
27	MM_GPIO4	GPIO	I2C SDA
26	MM_GPIO5	GPIO	I2C SCL

Definition of timing for F/S-mode devices on the I2C-bus. All values referred to



$V_{H(min)}$  (0.3V<sub>DD</sub>) and  $V_{L(max)}$  (0.7V<sub>DD</sub>) levels.

Parameter	Standard-mode		Fast-mode	
	Min	Max	Min	Max
Clock frequency (f <sub>SCL</sub> )	0	100kHz	0	400kHz
Fall time of both SDA and SCL (t <sub>f</sub> )	-	300ns	20x (V <sub>DD</sub> /5.5V)	300ns
Rise time of both SDA and SCL signals (t <sub>r</sub> )	-	1000ns	20ns	300ns
Data hold time (t <sub>HD,DAT</sub> )	5.0us	-	-	-
Data set-up time (t <sub>SU,DAT</sub> )	250ns	-	100ns	-
LOW period of the SCL clock	4.7us	-	1.3us	-
HIGH period of the SCL clock	4.0us	-	0.6us	-
Hold time- START, first clock is generated after this (t <sub>HD,STA</sub> )	4us	-	0.6us	-

### 3.4 Power Consumption

#### 3.4.1 Transmit Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V	
				VBAT (mA)	
				Max.	Avg.
915	MCS0	1	Tx @ 23 dBm	305mA	301mA
		2		278mA	274mA
		4		249mA	247mA
		8		230mA	227mA
	MCS7	1	Tx @ 17 dBm	189mA	188mA
		2		151mA	150mA
		4		143mA	141mA
		8		143mA	142mA

\* The power consumption is based on AzureWave test environment, these data for reference only.

#### 3.4.2 Receive Power Consumption

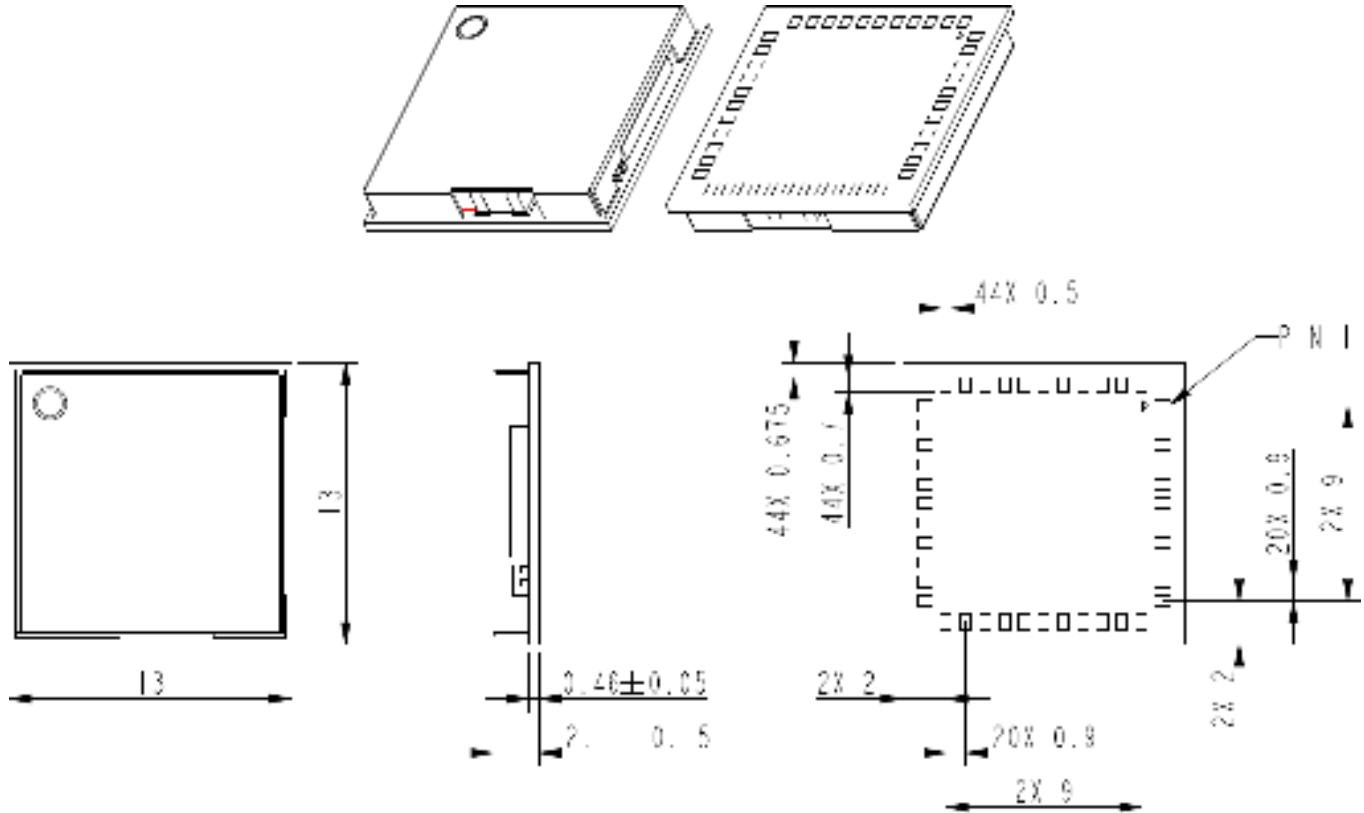
Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V	
				VBAT (mA)	
				Max.	Avg.
915	MCS0	1	Continuous Rx @ -95 dBm	32.3mA	32.3mA
		2	Continuous Rx @ -92 dBm	34.3mA	34.2mA
		4	Continuous Rx @ -89 dBm	43.0mA	42.8mA
		8	Continuous Rx @ -86 dBm	55.8mA	55.5mA
	MCS7	1	Continuous Rx @ -77 dBm	32.8mA	32.7mA
		2	Continuous Rx @ -74 dBm	36.3mA	36.2mA
		4	Continuous Rx @ -71 dBm	43.1mA	43mA
		8	Continuous Rx @ -68 dBm	52.8mA	52.6mA

\* The power consumption is based on AzureWave test environment, these data for reference only.



## 4. Mechanical Information

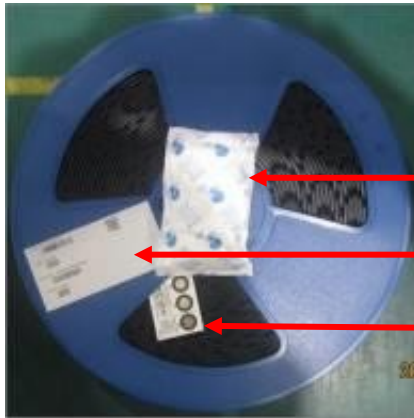
### 4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:  $\pm 0.1\text{mm}$

## 5. Package information

1. One reel can pack 1000pcs
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



One desiccant

One production label

One humidity indicator card

3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



One production label

4. A bag is put into the anti-static pink bubble wrap



One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box



One production label

6. **5 inner boxes** could be put into one carton



7. Sealing the carton by AzureWave tape



8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton



Example of carton label	
Example of box label	

Example of production label	 <p>AW-HM581        LOT 1005    FORM NO. FR201500000007    QTY 204  BAG SEAL DATE:</p>
Example of balance label	 <p>尾数 Balance</p>

# **AW-HM581**

## **IEEE 802.11ah Wireless LAN Module**

### **Layout Guide**

**Rev. 0.1**

**(For Standard)**

## Revision History

Document NO:

Version	Revision Date	DCN NO.	Description	Initials	Approved
0.1	2022/9/27		● Initial Version	Daniel Lee	NC Chen

## Table of Contents

Revision History	23
Table of Contents	24
1 Overview	25
1.1 Device supported	25
2 GENERAL RF GUIDELINES	26
3 Ground Layout	27
4 Power Layout	27
5 Digital Interface	27
6 RF Trace	27
7 Antenna	28
8 Antenna Matching	28
9 SHIELDING CASE	30
10 GENERAL LAYOUT GUIDELINES	30
11 The other layout guide Information	30
12 LGA module layout footprint recommend	32
12.1 LGA Module stencil and Pad opening Suggestion	32





# 1 Overview

## 1.1 Device supported

This document provides key guidelines and recommendations to be followed when creating AW-HM581 (13 x 13 mm LGA Module) layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

## 2 GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:
  - Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
  - Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
  - Keep all trace routing inside the ground plane area by at least the width of a trace.
  - Check for RF trace stubs, particularly when bypassing a circuit.
2. Keep RF traces properly isolated by doing the following:
  - Do not route any digital or analog signal traces between the RF traces and the reference ground.
  - Keep the pins and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
  - Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.
3. Consider the following RF design practices:
  - Verify that the RF path is short, smooth, and neat. Use curved traces for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
  - Do not use thermals on RF traces because of their high loss.
  - The RF traces between AW-HM581 RF\_ANT pin and antenna must be made using 50 $\Omega$  controlled-impedance transmission line.

### 3 Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

### 4 Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 10uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

### 5 Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

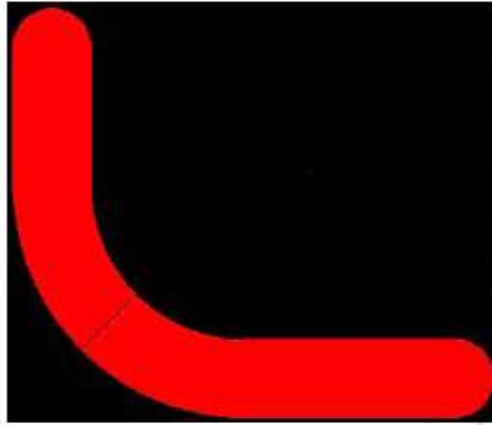
- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

### 6 RF Trace

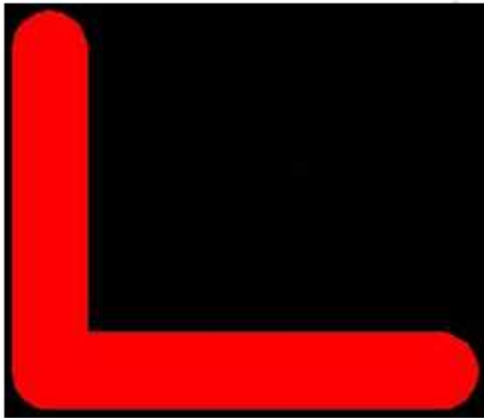
The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should be laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with a ground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

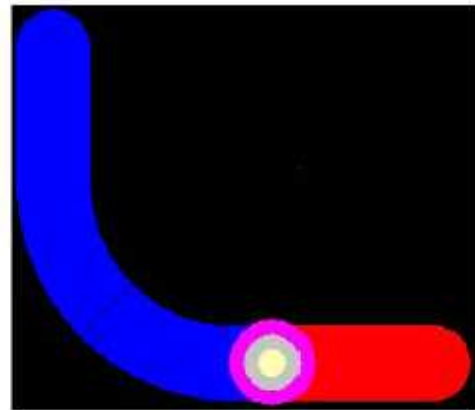
If the customers have any problem in calculation of trace impedance, please contact AzureWave.



**Correct RF trace**



Right-angled corner



Via on RF trace

**Incorrect RF trace**

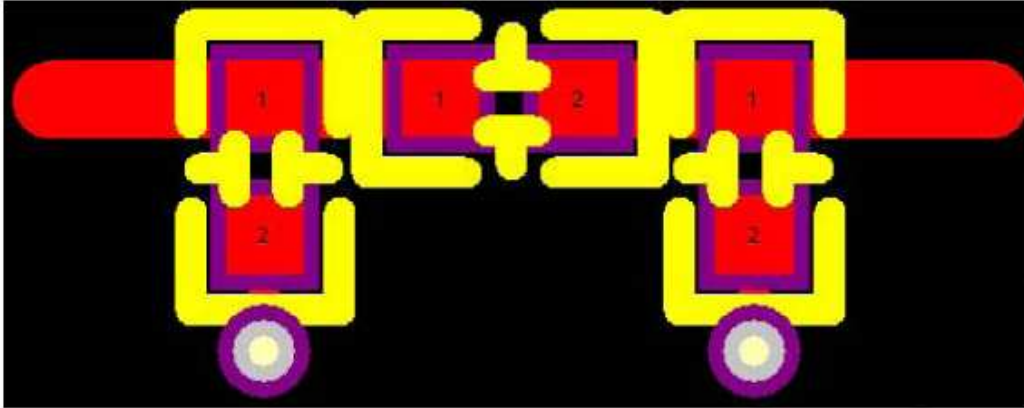
## 7 Antenna

All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

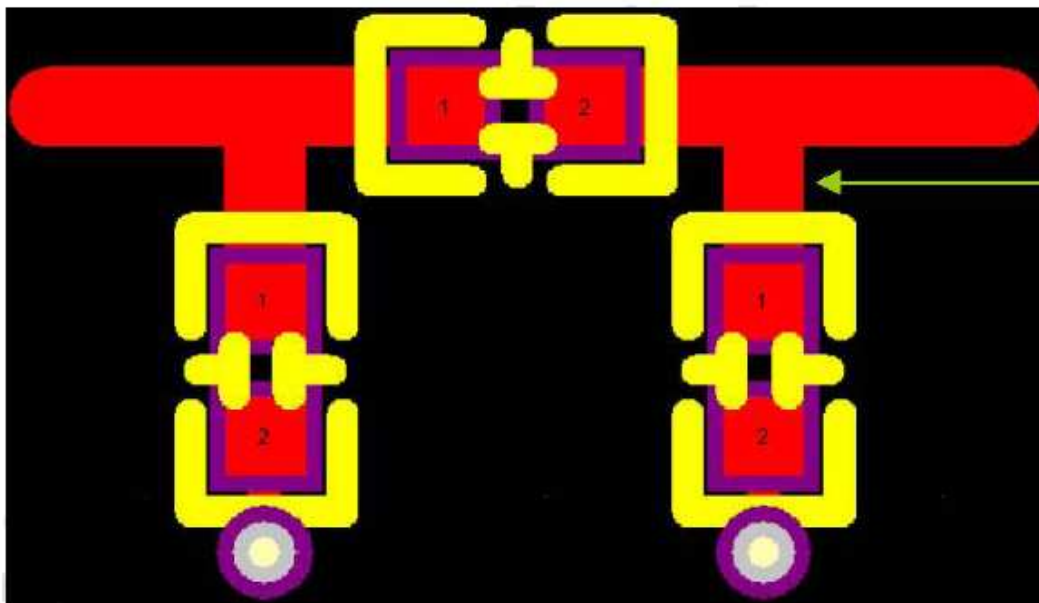
## 8 Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in

different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



It will be a stub if a shunt component is not necessary.

Incorrect layout for antenna matching

## 9 SHIELDING CASE

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

## 10 GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
  - Keep analog and digital circuits in separate areas.
  - Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
  - Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise. However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
  - Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.
2. Consider the following with respect to ground and power supply planes:
  - Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
  - Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
  - Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
3. Consider these power supply decoupling practices:
  - Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance.
  - Use appropriate capacitance values for the target circuit.

## 11 The other layout guide Information

- High speed interface (i.e. UART/SPI) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDDIO will improve the signal integrity of digital interfaces.
- Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
- RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from



port to port.

- Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).
- Discuss with AzureWave Engineer after you finish schematic and layout job.

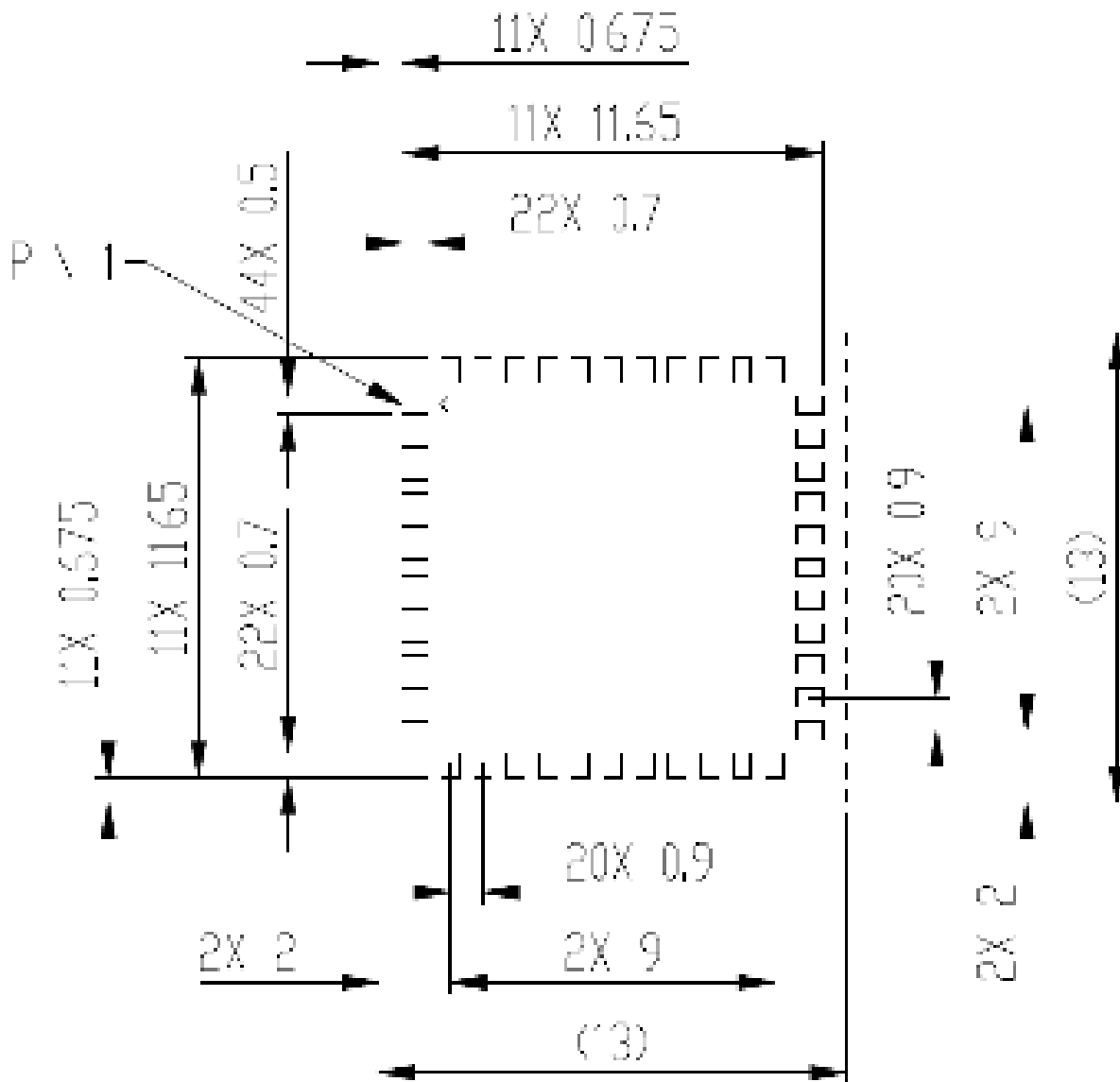
## 12 LGA module layout footprint recommend

### 12.1 LGA Module stencil and Pad opening Suggestion

- Stencil thickness : 0.08~0.1mm
- Function Pad opening size suggestion: Max. 1:1

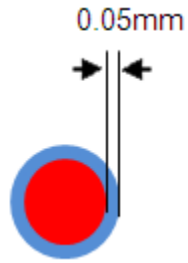
PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

- Solder Paste: Need to use type 5 paste (powder 5).
- 13 x 13 mm Solder Printer Opening Reference:





- IF Cu Pad size : 0.85mm
- Pad opening suggestion: 0.75mm



## FCC Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

The OEM or integrator is obligated to adhere to these requirements and restrictions as a condition for using the module's certification. The OEM or integrator is responsible to perform the required additional host regulatory testing and/or obtaining the required host approvals for compliance.

**Per KDB 996369 D03 v01r01 OEM Manual, this module is intended for OEM integrators under the following conditions:**

Ensure that the end-user has no manual instructions to remove or install module.

### 2.2 List of applicable FCC and ISSED rules

This module is certified pursuant to Part 15 rule section 15.247 and RSS-247.

### 2.3 Summarize the specific operational use conditions

This module has been approved to operate with the antenna types listed below, with the maximum permissible gain indicated.

Frequency Band	Model Number	Antenna Type	Gain(dBi)
902-928MHz	AN0915-5001BSM	Diople	2

### 2.4 Limited module procedures

**Not applicable.**

### 2.6 RF exposure considerations

This module is restricted to installation in products for use only in mobile and fixed applications.

The host product manufacturer must provide following statement in end-product manuals.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance **20cm** between the radiator & your body.

### 2.7 Antennas

This module has been approved to operate with the antenna types listed below, with the maximum permissible gain indicated.

Frequency Band	Model Number	Antenna Type	Gain(dBi)
902-928MHz	AN0915-5001BSM	Diople	2



## 2.8 Label and compliance information

### **Label of the end product:**

#### **FCC:**

The host product must be labeled in a visible area with the following "Contains FCC ID: TLZ-HM581".

The end product shall bear the following 15.19 statement: This device complies with part 15 of the FCC Rules.

Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

#### **ISED:**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains transmitter module IC: 6100A-HM581" or "Contains IC: 6100A-HM581"

Contient le module d'émission IC: 6100A-HM581

The Host Model Number (HMN) must be indicated at any location on the exterior of the end product or product packaging or product literature which shall be available with the end product or online.

## 2.9 Information on test modes and additional testing requirements

This module has been approved under stand-alone configuration.

The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093/RSS-102 and different antenna configurations.

The information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host can be found at KDB Publication 996369 D04.

OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**IMPORTANT NOTE:** In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/ISED authorization is no longer considered valid and the FCC/IC No. cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/ISED authorization.

## 2.10 Additional testing, Part 15 Subpart B and ICES-003 disclaimer

Appropriate measurements (e.g. Part 15 Subpart B compliance) and if applicable additional equipment authorizations (e.g. SDoC) of the host product to be addressed by the integrator/manufacturer.

This module is only FCC/ISED authorized for the specific rule parts 15.247, RSS-247 listed on the grant, and the host product manufacturer is responsible for compliance to any other FCC/ISED rules that apply to the host product as being Part 15 Subpart B/ICES-003 compliant.

## 2.11 Note EMI Considerations

Note that a host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties

For standalone mode, reference the guidance in D04 Module Integration Guide and for simultaneous mode; see D02 Module Q&A Question 12, which permits the host manufacturer to confirm compliance.

## 2.12 How to make changes

If any changes or modifications need to be made to the integrated product, such as adding or adjusting the antenna or cable, follow the guidelines provided by Grantee.

For further assistance, please contact: [patrick.lin@azurewave.com](mailto:patrick.lin@azurewave.com)

### **The user manual of the end product should include (information for OEMs):**



The module must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.

**Information To Be Supplied to the End User by the OEM or Integrator**

**FCC:**

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

The antenna(s) used for this transmitter must not transmit simultaneously with any other antenna or transmitter.

**ISED:**

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**ISED Radiation Exposure Statement:**

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

The transmitter module may not be co-located with any other transmitter or antenna.

Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

The end user manual shall include all required regulatory information/warning as shown in this document.