WT5010-S2 Datasheet

V1.0.1

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About this document

This document provides users with WT5010-S2 specifications.

Document version

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Revision history

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Document Revision History

No.	Version	Changes	Change (+ / -) description	Author	Date
1	V1.0.0	C	First release	Fiona	Nov 17, 2020
2	V1.0.1	M	Modified BLE name	Fiona	Dec 14, 2020

*Changes: C——Create, A——Add, M——Modify, D——Delete

Contents

1 Overview

- BLE5.0 / BLE5.1
  - Support 125Kbps/500Kbps/1Mbps
  - Receiving sensitivity: -99.7dBm@1Mbps
    -105dBm@125Kbps
  - Transmit power: +12 dBm（Max.）
  - Link gain: 117dBm@125Kbps（Max.）
  - Support Single-Ended Antenna Output
- BLE MESH
  - Support BLE SIG Mesh
  - Support private MESH
- MCU core
  - 32-bit CPU core
  - Frequency up to 64MHZ
  - Max. 64KB Data SRAM memory
  - Max. 512KB Data Flash memory
  - Support two-wire debugging protocol
- System power consumption
  - RX mode: 4.5mA @3.3V
  - TX mode: 4.3 mA @3.3V 0dBm
  - Deep sleep mode: 1.1 μA（RTC wake-up+GPIO wake-up）
  - ShutDown mode: 700nA（GPIO wake-up）
- Power, reset
  - Main power domain（VDD33）
  - Operating voltage range: 1.7V≤VDD33≤3.6 V
  - POR, PDR, PVD
- Clock
  - External high-speed crystal oscillator: 16MHz
  - Internal high-speed RC oscillator: 24 MHz
  - External low-speed crystal oscillator: 32.768KHz
  - Internal low-speed RC oscillator: 32.768KHz
- System peripherals

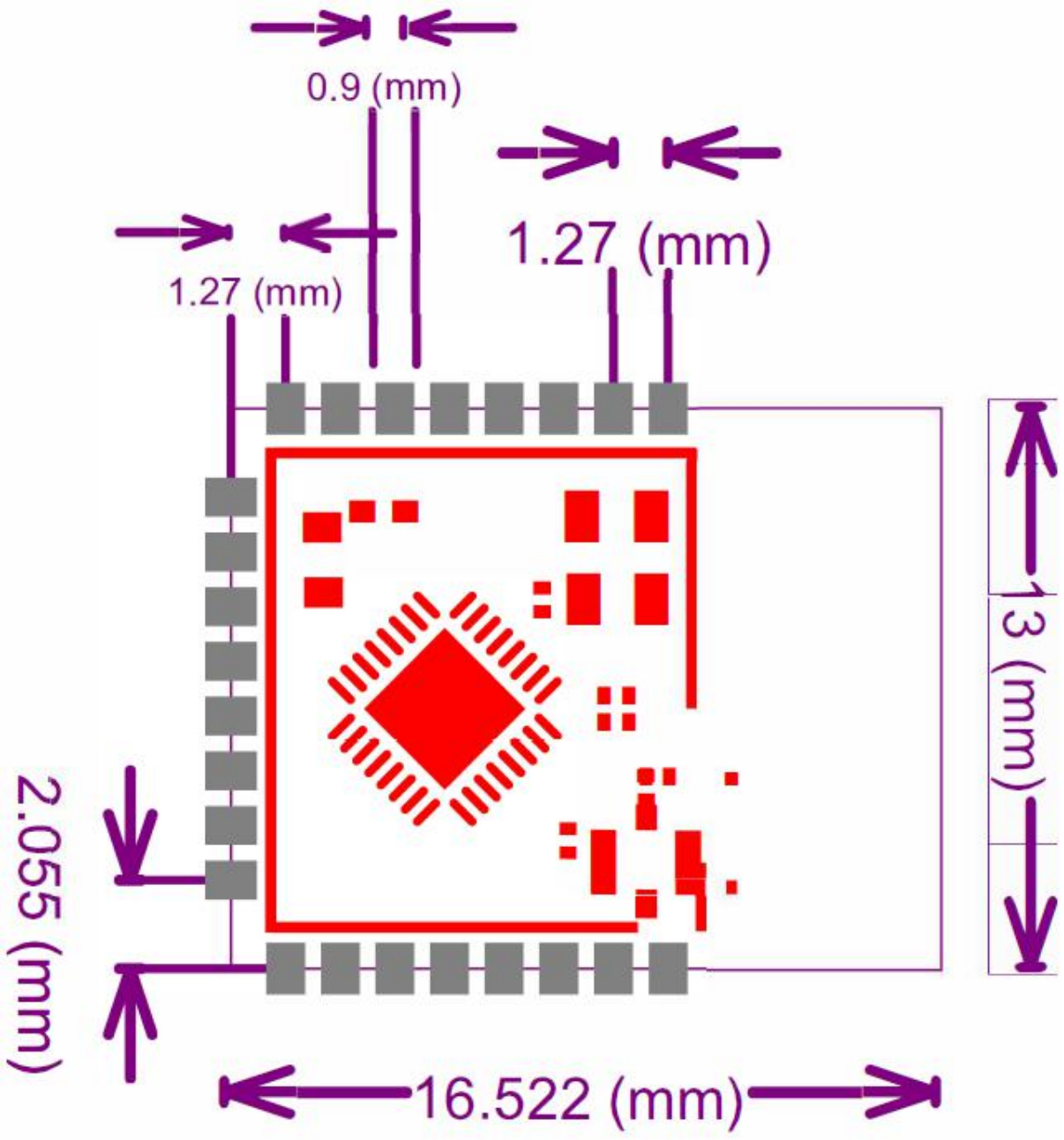
- DMA: support 8 multiplex channels
- Watchdog timer: IWDG and WWDG
- Peripheral interconnection PIS
- System tick timer

- Security and computing acceleration unit
  - ECC elliptic curve cryptography (256)
  - AES advanced encryption (256/192/128)
  - T/DES advanced encryption (192/128/64)
  - True random number generator (TRNG)
  - Calculating accelerator (CALC)
- Timer
  - One advanced 16-bit timer (ADTIM), support 4-channel PWM, 3 of which support dead-zone complementary
  - One general-purpose 32-bit timer A (GPTIMA), support 4-channel PWM
  - One general-purpose 16-bit timer B (GPTIMB), support 4-channel PWM
  - One general-purpose 16-bit timer C (GPTIMC), support 2-channel PWM, one of which supports dead zone complementary
  - One basic timer (BSTIM)
  - One low power timer (LPTIM)
- RTC (Real time clock)
  - Support high precision hardware temperature compensation
- ADC (Analog to digital conversion)
  - 12-bit high precision SAR ADC
  - Support up to 9 external channels
  - Support 3 internal channels
    - ✓ Built-in temperature sensor
    - ✓ 1/8, 1/4, 1/2, 3/8VDD
    - ✓ Internal reference voltage of 1.4V
- Communication interface
  - 2 x I2C (support bus arbitration)
  - 2 x SPI
  - 3 x UART (support ISO7816, LIN, IrDA, etc.)
- Audio interface
  - 2 x PDM, support digital MIC
  - 1 x I2S

- General-purpose IO

2 Chip Dimensions

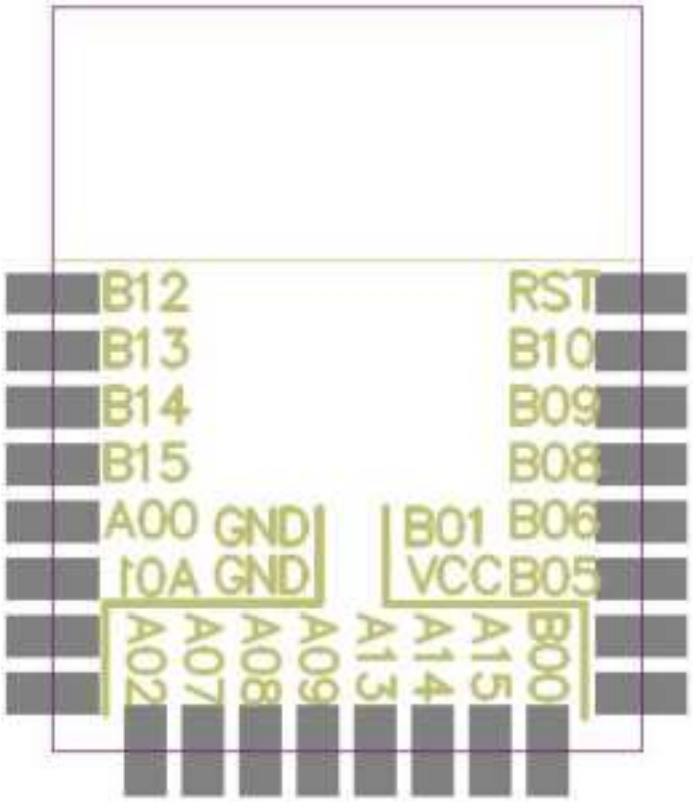
Figure 1 Chip Dimensions



3 Pin Definition

3.1 Pin Layout

Figure 2 Top View



3.2 Pin Description

The module has a total of 24 pins. See Table 1 for specific descriptions.

Table 1 Pin Definition

Pin No.	Pin Name	Description
1	B12	GPIO/ADC Channel 0
2	B13	GPIO/ADC Channel 1
3	B14	GPIO (BOOT pin, high level is required when programming)
4	B15	GPIO/Wake-up
5	A00	GPIO/ADC Channel 4/Wake-up
6	A01	GPIO/ADC Channel 5

Pin No.	Pin Name	Description
7	GND	Module power negative
8	GND	Module power negative
9	A02	GPIO/ADC Channel 6
10	A07	GPIO/Wake-up
11	A08	GPIO
12	A09	GPIO
13	A13	GPIO
14	A14	GPIO
15	A15	GPIO
16	B00	GPIO
17	VCC	Module power positive 3.3V
18	B01	GPIO
19	B05	GPIO(debug interface data by default)
20	B06	GPIO(debug interface clock by default)
21	B08	GPIO
22	B09	GPIO
23	B10	GPIO
24	RST	Reset input pin, active low

4 Functional Description

4.1 Direct Memory Access Controller (DMA)

The Direct memory access (DMA) is used to provide high-speed data transfer between peripheral and memory or between memory and memory, without intervention from CPU, data can be transferred quickly by DMA, which frees up CPU resources for other operations.

The features are described as follows:

- Support 8 independent DMA channels
- Each DMA channel has an independent handshake signal
- The priority of each DMA channel is programmable
- Each priority arbitration uses a fixed priority determined by the DMA channel number
- Support various transfer modes
  - Memory to memory
  - Memory to peripheral
  - Peripheral to memory
- Support various DMA cycle modes
- Support various DMA transfer data bit width
- Each DMA channel can access the primary and alternate channel controlled data structure
- All channel controlled data is stored in system memory in little endian format
- The number of data transferred in a single DMA cycle can be programmed (from 1 to 1024)
- The transfer address increment can be greater than the data width
- It can indicate errors on the bus

4.2 Independent Watchdog(IWDG)

The independent watchdog IWDG can be used to detect software and hardware abnormalities, such as the main clock stops oscillating, the program becomes out of control and no longer refreshes the watchdog.

The features are described as follows:

- Free running down counter
  - Writing to the IWDG_RLR register will reload the watchdog
  - After the watchdog is activated, a reset occurs when the counter reaches 0
- IWDG interrupt can wake up from sleep mode 0 and sleep mode 2

4.3 Window Watchdog(WWDG)

Window Watchdog(WWDG)will generate a WWDG reset if it is refreshed too early or too late. It can be used to detect whether the software fails to refresh the watchdog or it refreshes the watchdog in the refresh prohibited area to prevent the program from running into an uncontrollable state.

The features are described as follows:

- Support setting a watchdog refresh prohibited area
  - Set a watchdog refresh prohibited period through WIN
    - ✓ When WIN register is set to 11, refreshing the watchdog in any area will not generate a reset.
  - Refreshing the watchdog in the refresh prohibited area will generate a WWDG reset.
  - WWDG interrupt occurs after the watchdog refresh prohibited area
    - ✓ WWDG interrupt can be used as a watchdog refresh request
- WWDG overflow length can be set
  - It can be set by WWDG_RLR register
  - WWDG reset generated on overflow
- WWDG interrupt can be used as a watchdog refresh request

4.4 General Purpose and Alternate Function(GPIO and AFIO)

Each GPIO port contains 16 independent pins, which can be individually configured as input or output. Each pin can be additionally configured as an open-drain output mode or a filtered input mode, and the drive strength of each pin can be selected when configured as an output pin.

GPIO pins can be multiplexed as peripheral function ports, such as PWM output port or UART communication port, and each peripheral can be multiplexed onto multiple pins. The GPIO port supports up to 13 asynchronous external interrupts, which can be configured to any IO pin. And the GPIO port supports triggering other peripherals through PIS.

The features are described as follows:

- It can be configured as input or output
- Output mode
  - Push-pull/open drain
  - Pull-up/pull-down
- Input mode
  - Floating
  - Pull-up/pull-down

- Analog port

- Support reset/set of port output data, bitwise operation
- Support multiplexing as peripheral functions port
- Configurable output drive capacity: four drive capacity options
- Support 16 external input interrupts
- Support write protection of port configuration

4.5 Peripheral Interconnection

PIS is used as a bridge interface for the interconnection of peripherals in the microcontroller. The use of PIS can achieve the mutual triggering, control and automation of the peripherals, improve the real-time performance and rapid response ability of the system, avoid occupying excessive CPU resources and simplify software work to provide convenience for various applications.

The features are described as follows:

- Support up to 8 PIS channel selection
- Support synchronous and asynchronous channel selection
- Support signal effective edge selection
- Support channel output to pin

4.6 Elliptic Curve Cryptography(ECC)

Elliptic Curve Cryptography, ECC for short, is an asymmetric encryption algorithm based on the mathematical theory of elliptic curve. Compared with RSA, ECC has the advantage of using shorter keys to achieve security equivalent to or higher than RSA.

4.7 Encryption(AES/DES)

The hardware encryption module is mainly used to encrypt or decrypt data by hardware, and supports AES and DES standards.

AES (Advanced Encryption Standard) is the latest block symmetric cipher algorithm, compatible with the Advanced Encryption Standard (AES) specified by the Federal Information Processing Standards Publication (FIPS PUB 197, November 26, 2001).

DES (Data Encryption Standard) is a widely used symmetric encryption algorithm, compatible with the Data Encryption Standard (DES) and Triple DES (TDES) specified in the Federal Information Processing Standards Publication (FIPS PUB 46-3, October 25, 1999) , and complies with the American National Standards Institute (ANSI) 9.52 standard.

The features are described as follows:

- Suitable for AES, DES and TEDS encryption and decryption operations
- AES
  - Support 128/192/256-bit keys
  - Support ECB/CBC modes
  - Support 1/8/16/32-bit data exchange
- DES(TDES)
  - Support ECB/CBC modes
  - Support 64/128/192-bit keys
  - Support 4x32-bit initialization vector (IV) used in CBC mode
  - Support 1/8/16/32-bit data exchange
- Support Direct Memory Access (DMA) (used to transfer data and read processed data)
- Support to generate CPU interrupt requests

4.8 True Random Number Generator(TRNG)

True random number generator (TRNG) can produce 1-bit serial true random numbers or 8/16/32-bit parallel true random numbers.

The features are described as follows:

- Support programmable random bit width
- Support programmable seed value
- Support random correction mode
- Support random sequence error detection

4.9 Calculating Accelerator(CALC)

The calculating accelerator (CALC) can perform calculation acceleration of square root and division.

The features are described as follows:

- Support up to 32-bit unsigned square root operation
- Support division of up to 32-bit signed and unsigned numbers
- Support the use of DMA write data to perform calculating operations

4.10 Advanced Timer(ADTIM)

The advanced-control timer (ADTIM) consists of a 16-bit auto-load counter driven by a programmable Prescaler. It may be used for a variety of purposes, including measuring the pulse widths of input signals (input capture), or generating output waveforms (output compare, PWM, complementary PWM with

dead-time insertion).

Pulse widths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer Prescaler and the RCC clock controller Prescaler.

The advanced-control timers (ADTIM), general-purpose timers (GPTIMA, GPTIMB, GPTIMC) and basic timers (BSTIM) are completely independent and do not share any clock sources. They can be synchronized together as well.

The features are described as follows:

- 16-bit up, down, up/down auto-reload counter.
- 16-bit programmable Prescaler allowing dividing (on the fly) the counter clock frequency by any factor between 1 and 65536.
- Up to 4 independent channels for:
  - Input Capture
  - Output Compare
  - PWM generation (Edge and Center-aligned Mode)
  - One-pulse mode output
- Synchronization circuit can control the timer with external signals and interconnect several timers.
- Interrupt/DMA request is generated when the following events occur:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger events (counter start, stop, initialization or count by internal trigger)
  - Input capture (capture register)
  - Output compare (count register paired with compare register)
- Support incremental (quadrature) encoder and Hall sensor circuits for positioning purposes.
- Trigger input for an external clock or cycle-by-cycle current management

4.11 General-Purpose Timer(GPTIMC)

The general-purpose timer (GPTIMC) consists of a 16-bit auto-reload counter driven by a programmable Prescaler.

It may also be used for multiple purposes, including measuring the pulse lengths of input signals (input capture), or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds by using the timer Prescaler and the APB clock controller Prescaler.

The advanced-control timers (ADTIM1), general-purpose timers (GPTIMA1, GPTIMB1, GPTIMC1) and

basic timers (BSTIM1) are completely independent and do not share any clock sources.

The features are described as follows:

- 16-bit auto-reload up-counter
- 16-bit programmable Prescaler allows the counter clock frequency to be divided by any factor between 1 and 65536 (on the fly)
- Up to 2 independent channels
  - Input capture
  - Output compare
  - PWM generation (Edge-aligned and Center-aligned modes)
  - One-pulse mode output
- Complementary output programmable dead-time register
- Synchronization circuit can control the timer with external signal and interconnect several timers
- The repeat counter is used to update the timing register and only works after the definition number of the counter period
- Pause input to put timer output signal in reset state or known state
- Interrupt/DMA generation on the following events:
  - Update: Counter overflow/underflow, counter initialization (through software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture (capture register)
  - Output compare (count register paired with compare register)
  - Brake signal input
- Trigger input for an external clock or cycle-by-cycle current management

4.12 Basic Timer(BSTIM)

The basic timer consists of a 16-bit auto-reload counter driven by a programmable Prescaler. It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds by using the timer Prescaler and the APB clock controller Prescaler.

The advanced-control timers (ADTIM), general-purpose timers (GPTIMA, GPTIMB, GPTIMC) and basic timers (BSTIM) are completely independent and do not share any clock source.

The features are described as follows:

- 16-bit auto-reload up-counter

- 16-bit programmable Prescaler used to divide (on the fly) the counter clock frequency by any factor between 1 and 65536
- Synchronization circuit can control the timer with external signal and interconnect several timers
- Interrupt/DMA request is generated when the following event occurs:
  - Update: Counter overflow/underflow, counter initialization (by software or internal/external trigger)
- Trigger input for an external clock or cycle-by-cycle current management

4.13 Low-Power Timer(LPTIM)

The LPTIM is a 16-bit timer that is designed for low-power applications. Thanks to its multiple clock sources, the LPTIM supports the use of external input as a clock source, and can also count when the internal clock source is stopped.

The features are described as follows:

- 16-bit up-counter
- 3-bit Prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
- Clock sources
  - Internal clock sources: HSE, HIS, LSI, LSE, HSE, PLL
  - External clock source: external port input
- 16-bit ARR auto-reload register
- 16-bit compare register
- Continuous or one-shot mode optional
- Selectable software or hardware trigger
- Programmable filter
- Configurable output: Pulse, PWM, Flip
- Configurable I/O polarity

4.14 Analog-to-Digital Converter(ADC)

The ADC module is a 12-bit precision successive approximation analog-to-digital converter. It has up to 8 multiplexed channels allowing it to measure 8 external signals, two internal signals and BVAT voltage signals. The A/D conversion of the various channels can be performed in a single, continuous, scan, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined high or low thresholds.The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined high or low thresholds.

The features are described as follows:

- Configurable conversion accuracy (6/8/10/12)
- Interrupt generation at the end of conversion, the end of injected conversion, analog watchdog or overrun events.
- Support single and continuous conversion modes
- Scan mode for automatic conversion of channel 0 to channel “n”
- Configurable data alignment
- Programmable sampling time of each channel
- External trigger option to configure polarity for both regular and injected conversion
- Support discontinuous sampling mode
- Configurable conversion clock divider
- DMA request generation during regular channel conversion

4.15 Real Time Clock(RTC)

Real Time Clock (RTC) can provide users with accurate time and date information. These keywords are stored in the RTC control register in BCD format to provide users with the alarm function. There are two RTC CLK sources for users to choose from, which are an external 32.768K Hz crystal oscillator and an internal 32.768K Hz RC oscillator. When the MCU is in low power consumption mode, the RTC can still continue to provide accurate time information.

The features are described as follows:

- Support calendar display: year, month, day
- Support time display: week, hour, minute, second
- The calendar and time are stored in BCD format
- Support leap year detection capability
- Support users to set the RTC counter correction function
- Support users to set the alarm interrupt function
- Support rollover interrupt of year, month, day, week, hour, minute, and second
- Support MCU to keep counting in sleep mode
- Support users to configure the sleep counter
- Support a sleep counting up to 16777216 seconds (194 days).
- Support a sleep counting as short as 1/16 second.
- Support to detect whether the calendar and time have been cleared.

4.16 Inter-Integrated Circuit Interface(I2C)

The I2C (Inter-chip) bus interface connects the microcontroller and the serial I2C bus. It provides the multi-master capability and controls all I2C bus-specified sequencing, protocol, arbitration and timing. It supports standard mode, fast mode and super ultra-fast mode. At the same time, it is compatible with SMBus (System Management Bus) and PMBus (Power Management Bus). DMA can be used to reduce the burden on the CPU.

The features are described as follows:

- Slave mode and master mode
- Multi-master mode
- Standard mode (up to 100KHz)
- Fast mode (up to 400KHz)
- Ultra-fast mode (up to 1MHz)
- 7-bit and 10-bit addressing modes
- Multiple 7-bit slave addressing (2 addresses, one of which can be masked)
- All 7-bit addressing response mode
- Broadcast call
- Programmable setup and hold time
- Optional clock stretching
- Programmable digital noise filter
- Transmit/receive FIFOs of depth 8
- DMA function
- SMBus specification
- Generation and verification hardware PEC (Packet Error Checking) , with ACK control
- Command and data response control
- Support address resolution protocol (ARP)
- Master and device supporting
- SMBus alert
- Timeout and idle state detection
- Compatible with PMBus version 1.1 specification

4.17 Serial Peripheral Interface 1(LSSPI)

SPI1 is a full-duplex master/slave synchronous serial interface. The master processor accesses data, control and status information on LSSPI through a bus interface. LSSPI is connected to a DMA controller through a set of DMA signals. LSSPI can be set to one of the two operating modes: serial master mode or serial

slave mode. LSSPI can be connected to any serial master or serial slave peripheral device using one of the following interfaces.

The features are described as follows:

- Support SPI serial peripheral interface
- Support SSP protocol
- Support national semiconductor ray

4.18 Serial Peripheral Interface 2(SPI2)

The SPI/I2S interface can be used to communicate with external devices based on the SPI protocol and the I2S audio protocol. SPI or I2S mode is selected by software. SPI mode is selected by default after device reset.

Serial Peripheral Interface (SPI) protocol supports serial communication with external devices in half-duplex, full-duplex and simplex synchronization modes. This interface can be configured as master mode, in this case, it provides communication clock (SCK) to external slave device. The interface can also be operated in multiple configurations.

I2S audio protocol, also a synchronous serial communication interface, uses three external signals. It supports four different audio standards, including Philips' I2S standard, MSB and LSB alignment standards and PCM standard. It can achieve half-duplex communication in master-slave mode. When I2S is used as a master device, it can provide a communication clock to an external slave device.

The features are described as follows:

- SPI main features
  - Master device and slave device modes
  - Three-wire full-duplex synchronous transmission
  - Two-wire half-duplex synchronous transmission (two-way data line)
  - Two-wire simplex synchronous transmission (one-way data line)
  - 8-bit to 16-bit data size selection
  - Multiple modes capability
  - 8-bit master mode baud rate divider
  - Slave mode frequency up to $f_{pclk}/2$
  - In both master and slave modes, you can manage NSS by hardware or software: dynamic changes of master/slave mode operation
  - Programmable clock polarity and phase
  - High-order or low-order can be set
  - Special sending and receiving status flags, all support interrupt triggering
  - SPI bus busy status flag

- Support SPI Motorola mode
- Hardware CRC can achieve reliable communication
  - ✓ CRC value can be transmitted as the last byte of TX mode
  - ✓ CRC automatically performs an error check to the last received byte.
- Support Rx and TxFIFO, depth is 16
- Support DMA transfer
- Support SPI TI mode

- I2S features
  - Simplex communication (only send or receive)
  - Master or slave operation
  - 8-bit linear programmable frequency divider to achieve accurate audio sampling frequency (from 8kHz to 968kHz)
  - The data format is 16-bit, 24-bit or 32-bit
  - Fixed data frame of audio channel is 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit, 32-bit data frame)
  - Programmable clock polarity (steady state)
  - Underflow flag for slave transmission mode and overflow flag for receiving function (master or slave)
  - 16-bit transmit and receive registers, with one register at each end of the channel
  - I2S protocol supported:
    - ✓ I2S Philips standard
    - ✓ MSB alignment standard (left alignment)
    - ✓ LSB alignment standard (right alignment)
    - ✓ PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extended to 32-bit channel frame)
  - Data direction is always MSB first
  - Support sending and receiving DMA (16 bits wide)
  - The main clock can be output to an external audio component. The rate is fixed at 256 times FS (where FS is the audio sampling frequency)
  - Support TX and RX FIFO, depth is 16
  - Provides 2-channel external clock inputs

4.19 Universal Asynchronous Receiver Transmitter(UART)

The Universal Asynchronous Receiver Transmitter (UART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry-standard NRZ asynchronous serial data format.

The UART offers a wide range of baud rates using a fractional baud rate generator.

UART supports asynchronous communication and half-duplex single-wire communication. It also supports the LIN (local interconnection network), Smart Card Protocol and IrDA (infrared Data Association) SIR ENDEC specifications, and modem operations (CTSn/RTSn). It also supports multiprocessor communication. High-speed data communication is possible by using the DMA for multibuffer settings.

The features are described as follows:

- Full duplex asynchronous communications
- 16-byte receive and transmit FIFO
- Compatible with 16C550 standard
- Programmable receiving buffer trigger point
- Support independent baud rate programmable for each channel
- Support automatic baud rate detection
- 12 interrupt sources
- Can use DMA
  - Buffering the received/transmitted bytes in the reserved SRAM using DMA
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values
  - Programmable transmit and receive baud rates up to 3MHz, min. 732Hz (clock frequency 48MHz)
- Support hardware automatic flow control/flow control (CTSn, RTSn), RTSn control flow trigger point can be programmed
  - Modem hardware automatic control
  - RS485 transmit enable control
- Support CTS wake-up function
- Support IrDASIR mode
  - Support 3/16 bit periodic modulation
- Support RS485
  - Support 9-bit mode
  - Multiprocessor communication
- Fully programmable serial interface features
  - Programmable data bit number, namely 5-, 6-, 7-, 8-, 9-bit
  - Parity control, odd, even, no parity or fixed parity generation and detection can be programmed
  - Stop bit length can be programmed: 1, 2 bits; 0.5, 1.5 bits supported in Smartcard mode

- Programmable bit order with MSB or LSB first
- Simple half duplex communication
- Switch TX / RX pin configuration
- Disconnection signal transmission ability of LIN master and disconnection signal detection ability of LIN slave
  - When the UART is set to LIN mode, there are a 13-bit disconnect signal generator and disconnect signal detection functions
- Smartcard mode
  - Support T=0 and T=1 Smartcard asynchronous protocol declared by ISO/IEC7816-3 standard
  - 1.5 stop bit length used in Smartcard
- Support ModBus communication
  - Timeout detection function
  - CR/LF character recognition
- Noise detection

4.20 Audio Interface (PDM)

PDM (Pulse Density Modulation) is a modulation technique that uses digital signals to represent analog signals. PCM, also as a technique of converting analog to digital by taking regular samples at uniform intervals, expresses the amplitude of each sampled analog signal as N-bit digital component (N=quantization depth). So the result of each sample in PCM method is always data of N-bit word length. PDM uses a clock with a sampling rate much higher than PCM's to sample and modulate the analog components, and only one bit is output, either 0 or 1. Therefore, digital audio expressed by PDM is also called Oversampled 1-bit Audio. Compared with a series of 0 and 1 in PDM, the quantization result of PCM is more intuitive and simple.

4.21 BLE

BLE5.0/5.1 protocol.

Federal Communication Commission Statement (FCC, U.S.)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTES

Co-location warning:

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

OEM integration instructions:

This device is intended only for OEM integrators under the following conditions:
The transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.
As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End product labeling:

The final end product must be labeled in a visible area with the following: “Contains Transmitter Module FCC ID: 2AFOS-WT5010-S2”.

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Integration instructions for host product manufactures according to KDB 996369

D03 OEM

Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.247 & 15.207 & 15.209

2.3 Specific operational use conditions

The module is a Bluetooth module with BLE 2.4G function.

BLE Specification:

Operation Frequency: 2402~2480MHz
Number of Channel: 40
Modulation: GFSK
Type: PCB Antenna
Gain: 2 dBi
The module can be used for mobile or applications with a maximum 2dBi antenna. The host manufacturer installing this module into their product must ensure that the final composit product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operaition. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Not applicable.

2.5 Trace antenna designs

Not applicable. The module has its own antenna, and doesn’t need a host’s printed board microstrip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users’ body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization

2.7 Antennas

Antenna Specification are as follows:
Type: PCB Antenna
Gain: 2 dBi
This device is intended only for host manufacturers under the following conditions:
The transmitter module may not be co-located with any other transmitter or antenna;
The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a ‘unique’ antenna coupler.
As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating “Contains Transmitter Module FCC ID: 2AFOS-WT5010-S2” with their finished product.

2.9 Information on test modes and additional testing requirements

BLE

Operation Frequency: 2402~2480MHz
Number of Channel: 40
Modulation: GFSK

Host manufacturer must perfom test of radiated & conducted emission and spurious emission, etc

according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.
Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15.207 & 15.209 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.