

KG200Z Hardware Design

LoRa Module Series

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⊕	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
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	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio signals. RF interference can occur if it is used close to TV sets, radios, computers, or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phones or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-12-05	Paul YU/ Quentin QIU	Creation of the document
1.0.0	2023-12-05	Paul YU/Quentin QIU	Preliminary

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1 Introduction

QuecOpen[®] is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Enhance product competitiveness and price-performance ratio

This document defines KG200Z in QuecOpen[®] solution and describes its air interfaces and hardware interfaces, which are connected with your applications.

With this document, you can quickly understand module interface specifications, RF performance, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

KG200Z is a low power, cost-effective LoRa module supporting LoRaWAN protocol. It features built-in power management unit, power amplifier, low noise amplifier and RF transceiver switch. The module provides multiple interfaces including UART, SPI*, I2C* and SWD for various applications.

KG200Z is an SMD module with compact packaging. The general features of the module are as follow:

- 48 MHz and 32-bit MCU processor
- Built-in 64 KB RAM and 256 KB Flash
- Support for secondary development

Table 2: Basic Information

KG200Z	
Packaging type	LGA
Pin counts	73
Dimensions	(12.0 ±0.2) mm × (12.0 ±0.2) mm × (1.8 ±0.2) mm
Weight	Approx. 0.56 g

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocols and	LoRa protocol: LoRaWAN
Standards	All hardware components are fully compliant with EU RoHS directive
	VBAT Power Supply:
	• 1.8–3.6 V
	• Typ.: 3.3 V
	VDD_IO Power Supply:
Power Supply	• 1.8–3.6 V
	• Typ.: 3.3 V
	VDDA Power Supply:
	• 1.8–3.6 V
	• Typ.: 3.3 V
Temperature Ranges	Operating temperature ¹ : -40 to +85 °C
	Storage temperature: -45 to +95 °C
TE-B Kit	KG200Z-TE-B ²
Antenna Interface	
Antenna Interface	 Pin antenna interface (ANT_LORA)
	 50 Ω characteristic impedance
Application Interfaces	3
Application Interfaces	UART, SPI*, I2C*, SWD

¹ Within the operating temperature range, the module's related performance meets LoRa specification requirements. ² For more details about the TE-B, see *document [1]*.

³ For more details about the interfaces, see **Chapter 0** and **Chapter 1.1**.

3 Application Interfaces

3.1. Pin Assignment

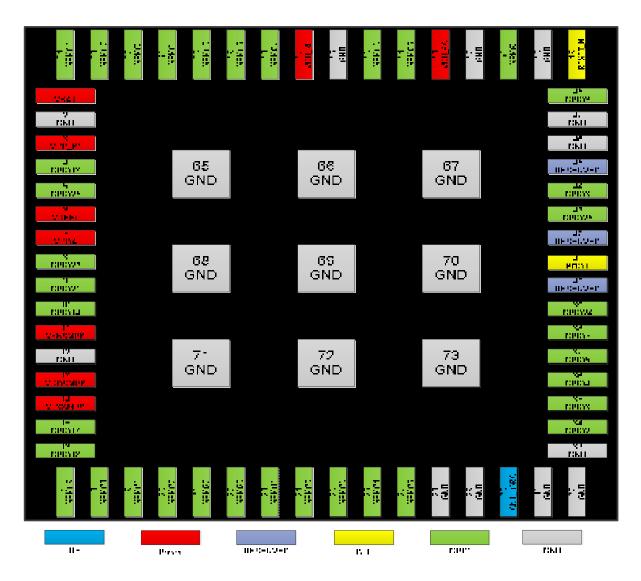


Figure 1: Pin Assignment (Top View)

NOTE

- 1. Keep all RESERVED and unused pins unconnected.
- 2. All GND pins should be connected to ground.
- 3. The module has 37 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including UART, SPI*, I2C*, SWD. For more details, see *Chapter 3.3* and *Chapter 3.4*.

3.2. Pin Description

Table 4: Parameter Description

Parameter	Description
AIO	Analog Input/Output
DI	Digital Input
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT	1	ΡI	Power supply for the module	Vmin = 1.8 V Vnom = 3.3 V Vmax = 3.6 V	It must be provided with sufficient current of at least 0.3 A.
VDD_IO	3	ΡI	Power supply for I/O pins	Vmin = 1.8 V Vnom = 3.3 V Vmax = 3.6 V	
VREF+	6	ΡI	Power supply for the ADC/DAC	Vmin = 1.8V Vnom = 3.3 V Vmax = 3.6	

VDDA	7	PI	External analog power supply for	Vmin = 1.8V Vnom = 3.3 V	
			A/D converters	Vmax = 3.6 V	
			DC-DC switching	Vmin = 1.45 V	
VFBSMPS	11	ΡI	power feedback	Vnom =1.55V	
			F	Vmax = 1.62 V	
			DC-DC switching	Vmin = 1.8 V	
VDDSMPS	13	ΡI	power input	Vnom = 3.3 V	
			power input	Vmax = 3.6 V	
			DC-DC switching	Vmin = 1.8 V	
VLXSMPS	14	PO	Ū.	Vnom = 3.3 V	
			power output	Vmax = 3.6 V	
				Vmin = 1.8 V	
VDD_PA	53	ΡI	Power supply for	Vnom = 3.3 V	
—			the PA	Vmax = 3.6 V	
				Vmin = 1.8 V	
VDD_RF	57	ΡI	Power supply for	Vnom = 3.3 V	
			the RF	Vmax = 3.6 V	
	0.40				
GND	Ζ, ΙΖ, Ι	28, 29, 3	31, 32, 33, 46, 47, 50,	52, 50, 65-73	
Control Signa	als				
_					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
Pin Name	Pin	I/O DI	Description Reset the module	Characteristics	Hardware reset.
	Pin No.				Hardware reset. Internally pulled up to 3.3 V.
	Pin No.		Reset the module	Characteristics	Hardware reset. Internally pulled up to 3.3 V.
RESET_N	Pin No . 49	DI	Reset the module Make the module	Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low.
RESET_N	Pin No. 49 41	DI	Reset the module Make the module into download	Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low.
RESET_N BOOT GPIO Interfac	Pin No. 49 41 ees	DI	Reset the module Make the module into download mode	Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT	Pin No. 49 41	DI	Reset the module Make the module into download	Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low.
RESET_N BOOT GPIO Interfac Pin Name	Pin No. 49 41 es Pin No.	DI DI I/O	Reset the module Make the module into download mode Description	Characteristics Characteristics VDD_IO DC	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac	Pin No. 49 41 ees Pin	DI	Reset the module Make the module into download mode Description General-purpose	Characteristics Characteristics VDD_IO DC	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name	Pin No. 49 41 es Pin No.	DI DI I/O	Reset the module Make the module into download mode Description General-purpose input/output	Characteristics Characteristics VDD_IO DC	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name	Pin No. 49 41 es Pin No.	DI DI I/O	Reset the module Make the module into download mode Description General-purpose input/output General-purpose	Characteristics Characteristics VDD_IO DC	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name GPIO13	Pin No. 49 41 es Pin No. 4	DI DI I/O DIO	Reset the module Make the module into download mode Description General-purpose input/output General-purpose input/output	Characteristics Characteristics VDD_IO DC	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name GPIO13	Pin No. 49 41 es Pin No. 4	DI DI I/O DIO	Reset the module Make the module into download mode Description General-purpose input/output General-purpose input/output General-purpose	Characteristics Characteristics VDD_IO DC	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name GPIO13 GPIO28	Pin A9 41 es Pin No. 4 5	DI DI I/O DIO DIO	Reset the module Make the module into download mode Description General-purpose input/output General-purpose input/output General-purpose input/output	Characteristics Characteristics DC Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name GPIO13 GPIO28 GPIO23	Pin A9 41 es Pin No. 4 5 8	DI DI I/O DIO DIO DIO	Reset the module Make the module into download mode Description General-purpose input/output General-purpose input/output General-purpose input/output	Characteristics Characteristics DC Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name GPIO13 GPIO28	Pin A9 41 es Pin No. 4 5	DI DI I/O DIO DIO	Reset the module Make the module into download mode Description General-purpose input/output General-purpose input/output General-purpose input/output	Characteristics Characteristics DC Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode
RESET_N BOOT GPIO Interfac Pin Name GPIO13 GPIO28 GPIO23	Pin A9 41 es Pin No. 4 5 8	DI DI I/O DIO DIO DIO	Reset the module Make the module into download mode Description General-purpose input/output General-purpose input/output General-purpose input/output	Characteristics Characteristics DC Characteristics	Hardware reset. Internally pulled up to 3.3 V. Active low. Select download mode

			input/output
GPIO17	15	DIO	General-purpose input/output
GPIO18	16	DIO	General-purpose input/output
GPIO19	17	DIO	General-purpose input/output
GPIO33	18	DIO	General-purpose input/output
GPIO21	19	DIO	General-purpose input/output
GPIO32	20	DIO	General-purpose input/output
GPIO22	21	DIO	General-purpose input/output
GPIO20	22	DIO	General-purpose input/output
GPIO31	23	DIO	General-purpose input/output
GPIO30	24	DIO	General-purpose input/output
GPIO35	25	DIO	General-purpose input/output
GPIO34	26	DIO	General-purpose input/output
GPIO36	27	DIO	General-purpose input/output
GPIO2	34	DIO	General-purpose input/output
GPIO3	35	DIO	General-purpose input/output
GPIO4	36	DIO	General-purpose input/output
GPIO5	37	DIO	General-purpose input/output
GPIO7	38	DIO	General-purpose input/output
GPIO24	39	DIO	General-purpose input/output
GPIO25	43	DIO	General-purpose input/output

GPIO8	44	DIO	General-purpose input/output		
GPIO6	48	DIO	General-purpose input/output	-	
GPIO9	51	DIO	General-purpose input/output	-	
GPIO26	54	DIO	General-purpose input/output	-	
GPIO15	55	DIO	General-purpose input/output	-	
GPIO27	58	DIO	General-purpose input/output	-	
GPIO16	59	DIO	General-purpose input/output	-	
GPIO10	60	DIO	General-purpose input/output	-	
GPIO1	61	DIO	General-purpose input/output		
GPIO0	62	DIO	General-purpose input/output		
GPIO12	63	DIO	General-purpose input/output		
GPIO11	64	DIO	General-purpose input/output		
Antenna Interfa	ace				
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
	NO.				
ANT_LORA	30	AIO	LoRa antenna interface		50 Ω characteristic impedance.
ANT_LORA	30	AIO			
_	30				

3.3. GPIO Multiplexing

The module has 37 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including UART, SPI*, I2C*, SWD. Pins are defined as follows:

Table 6: GPIO Multiplexing

Pin Name	Pin No.	Alternate Function 0 (GPIO No.)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4
GPIO0	62	PA0	USART2_CTS	-	I2C3_SMBA	-
GPIO1	61	PA1	USART2_RTS	LPUART_RTS	I2C1_SMBA	SPI1_SCK
GPIO2	34	PA2	USART2_TXD	LPUART_TXD	-	-
GPIO3	35	PA3	USART2_RXD	LPUART_RXD	-	-
GPIO4	36	PA4	-	-	-	SPI1_CS
GPIO5	37	PA5	-	-	-	SPI1_CLK
GPIO6	48	PA6	-	LPUART_CTS	I2C2_SMBA	SPI1_MISO
GPI07	38	PA7	-	-	I2C3_SCL	SPI1_MOSI
GPIO8	44	PA8	-	-	-	SPI2_CLK



GPIO9	51	PA9	USART1_TXD	-	I2C1_SCL	SPI2_CS
GPIO10	60	PA10	USART1_RXD	-	I2C1_SDA	SPI2_MOSI
GPIO11	64	PA12	USART1_RTS	-	I2C2_SCL	SPI1_MOSI
GPIO12	63	PA13	SWDIO	-	I2C2_SMBA	-
GPIO13	4	PA14	SWCLK	-	I2C1_SMBA	-
GPIO14	10	PA15	-	-	I2C2_SDA	SPI1_CS
GPIO15	55	PB1	-	-	-	-
GPIO16	59	PB2	-	-	I2C3_SMBA	SPI1_CS
GPIO17	15	PB3	USART1_RTS	-	-	SPI1_CLK
GPIO18	16	PB4	USART1_CTS	-	I2C3_SDA	SPI1_MISO
GPIO19	17	PB5	-	-	I2C1_SMBA	SPI1_MOSI
GPIO20	22	PB6	USART1_TXD	-	I2C1_SCL	-
GPIO21	19	PB7	USART1_RXD	-	I2C1_SDA	-
GPIO22	21	PB8	-	-	I2C1_SCL	-
GPIO23	8	PB9	-	-	I2C1_SDA	SPI2_CS
GPIO24	39	PB10	-	LPUART_RXD	I2C3_SCL	SPI2_CLK



GPIO25	43	PB11	-	LPUART_TXD	I2C3_SDA	-
GPIO26	54	PB12	-	LPUART_RTS	I2C3_SMBA	SPI2_CS
GPIO27	58	PB13	-	LPUART_CTS	I2C3_SCL	SPI2_CLK
GPIO28	5	PB14	-	-	I2C3_SDA	SPI2_MISO
GPIO29	9	PB15	-	-	I2C2_SCL	SPI2_MOSI
GPIO30	24	PC0	-	LPUART_RXD	I2C3_SCL	-
GPIO31	23	PC1	-	LPUART_TXD	I2C3_SDA	-
GPIO32	20	PC2	-	-	-	SPI2_MISO
GPIO33	18	PC3	-	-	-	SPI2_MOSI
GPIO34	26	PC4	-	-	-	-
GPIO35	25	PC5	-	-	-	-
GPIO36	27	PC6	-	-	-	-

3.4. Interface Definition

3.4.1. UART

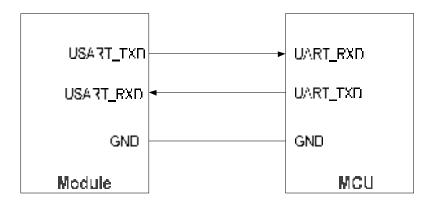
In the case of multiplexing, the module supports two USARTs (USART1 and USART2) and one LPUART.

3.4.1.1. USART

Table 7: Pin Definition of USART Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIO2	34	USART2_TXD	DO	USART2 transmit	Other configurations for USART interfaces, see Table 6 .
GPIO3	35	USART2_RXD	DI	USART2 receive	
GPIO20	22	USART1_TXD	DO	USART1 transmit	
GPIO21	19	USART1_RXD	DI	USART1 receive	

USART clock is independent of the CPU clock, allowing it to wake up the MCU from stop mode, using a baud rate of up to 200 kbps. The USART interfaces can be supported by the DMA controller. The USART interfaces connection between the module and the MCU is shown below:







The reference design of USART interfaces is shown below:

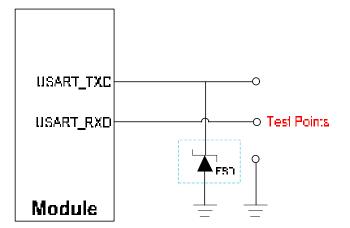


Figure 3: Reference Design of USART Interfaces

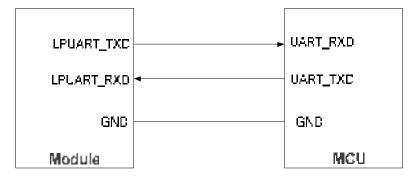
3.4.1.2. LPUART

KG200Z has one low-power UART (LPUART) that enables asynchronous serial communication with minimum power consumption. The LPUART supports half-duplex single-wire communication and modem operations (CTS/RTS), allowing multiprocessor communication.

Table 8: Pin Definition of LPUART Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIO2	34	LPUART_TXD	DO	LPUART transmit	Other configurations for USART interfaces. see
GPIO3	35	LPUART_RXD	DI	LPUART receive	USART interfaces, see Table 6 .

The LPUART can be used for AT command communication and data transmission. The LPUART connection between the module and the MCU is illustrated below.





3.4.2. SPI*

In the case of multiplexing, the module supports two SPIs (SPI1 and SPI2) which can operate in master or slave mode. The maximum clock frequency of the interface can reach 24 MHz.

Table 9: Pin Definition of SPI

Pin name	Pin No.	Alternate Function	I/O	Description	Comment
GPIO4	36	SPI1_CS	DIO	SPI chip select	
GPIO5	37	SPI1_CLK	DIO	SPI clock	
GPIO6	48	SPI1_MISO	DIO	SPI master-in slave-out	
GPIO7	38	SPI1_MOSI	DIO	SPI master-out slave-in	Other configurations
GPIO26	54	SPI2_CS	DIO	SPI chip select	for SPI interfaces, see Table 6 .
GPIO27	58	SPI2_CLK	DIO	SPI clock	
GPIO28	5	SPI2_MISO	DIO	SPI master-in slave-out	_
GPIO29	9	SPI2_MOSI	DIO	SPI master-out slave-in	_

The following figure shows the connection between the host and the slave:

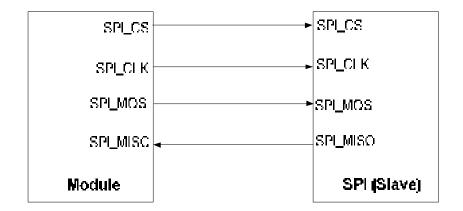


Figure 5: SPI Connection (Master Mode)

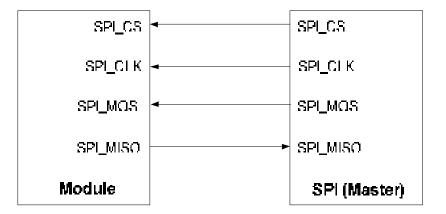


Figure 6: SPI Connection (Slave Mode)

3.4.3. I2C Interface*

In the case of multiplexing, the module supports three I2C interfaces (I2C1, I2C2, and I2C3) which can operate in master or slave mode, supporting SMBus/PMBus and I2C bus specifications.

Table 10:	Pin	Definition	of	I2C	Interface
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Pin name	Pin No.	Alternate Function	I/O	Description	Comment
GPIO9	51	I2C1_SCL	OD	I2C1 serial clock	
GPIO10	60	I2C1_SDA	OD	I2C1 serial data	Other configurations for I2C interfaces,
GPIO11	64	I2C2_SCL	OD	I2C2 serial clock	 for I2C interfaces, see <i>Table 6</i>.
GPIO14	10	I2C2_SDA	OD	I2C2 serial data	

GPIO30	24	I2C3_SCL	OD	I2C3 serial clock
GPIO31	23	I2C3_SDA	OD	I2C3 serial data

3.4.4. SWD Interface

In the case of multiplexing, the module supports one SWD interface for module debugging and testing. SWD serves as a serial download and debugging port, and only two pins need to be connected to the serial debugger during debugging.

Table 11: Pin Definition of SWD Interface

Pin name	Pin No.	Alternate Function	I/O	Description	Comment
GPIO12	63	SWDIO	DIO	Serial wire debugging input/output	Other configurations
GPIO13	4	SWCLK	DIO	Serial wire debugging clock	for SWD interfaces, see <i>Table</i> 6.

4 Operating Characteristics

4.1. Power Supply

Power supply pin and ground pins of the module are defined in the following table.

Pin Name	Pin No.	I/O	Description	Min.	Тур.	Max.
VBAT	1	ΡI	Power supply for the module	1.8	3.3	3.6
VDD_IO	3	ΡI	Power supply for the I/O	1.8	3.3	3.6
VREF+	6	ΡI	Power supply for the ADC/DAC	1.8	3.3	3.6
VDDA	7	ΡI	External analog power supply for A/D converters	1.8	3.3	3.6
VFBSMPS	11	ΡI	DC-DC switching power feedback	1.45	1.55	1.62
VDDSMPS	13	ΡI	DC-DC switching power input	1.8	3.3	3.6
VLXSMPS	14	PO	DC-DC switching power output	1.8	3.3	3.6
VDD_PA	53	ΡI	Power supply for the PA	1.8	3.3	3.6
VDD_RF	57	ΡI	Power supply for the RF	1.8	3.3	3.6
GND	GND 2, 12, 28, 29, 31, 32, 33, 46, 47, 50, 52, 56, 65–73					

Table 12: Pin Definition of Power Supply and GND Pins (Unit: V)

4.1.1. Reference Design for Power Supply

The module supports two power supply modes: LDO and DC-DC (SMPS). SMPS is optional and can be turned on internally by software to improve power efficiency. When LDO and SMPS are running simultaneously, the power supply of the module should be able to provide sufficient current of at least 0.3 A. For better power supply performance, it is recommended to parallel a 22 μ F decoupling capacitor, and two filter capacitors (1 μ F and 100 nF) near the module's VBAT pin. And C4 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to

improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VBAT reference circuit is shown below:

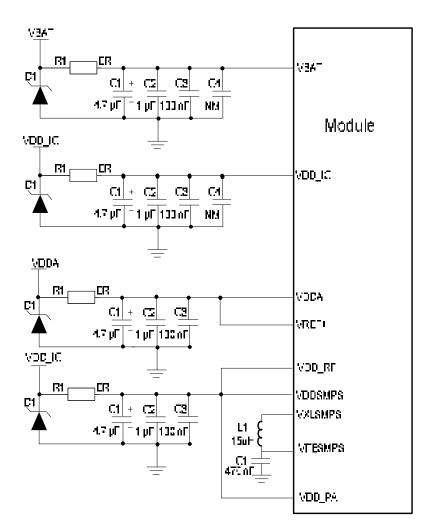


Figure 7: VBAT Reference Circuit

4.2. Turn On

After the module is powered on, it can be automatically powered on.

4.3. Reset

Drive RESET_N low for at least 100 ms and then release it to reset the module. In order to avoid module

restart due to abnormal interference, it is recommended to route the trace as short as possible and surround it with ground.

Table 13: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	49	DI	Reset the module	Hardware reset; Internally pulled up to 3.3 V; Active low.

The reference design for resetting the module is shown below. You can use an open collector driving circuit to control RESET_N.

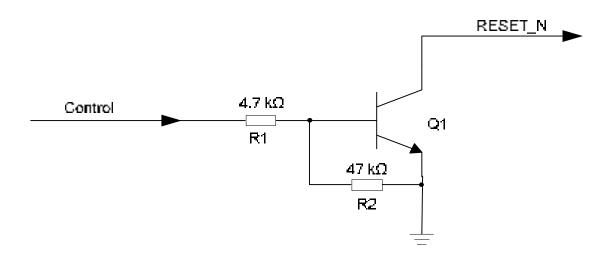


Figure 8: Reference Circuit of Reset by Using Driving Circuit

Another way to control RESET_N is by using a button directly. When pressing the button, an electrostatic strike may generate from finger. Therefore, a TVS component shall be placed near the button for ESD protection.

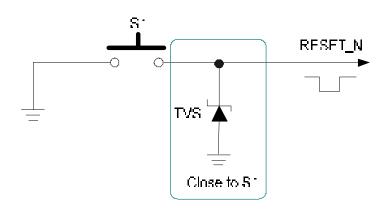


Figure 9: Reference Circuit of Reset with A Button

The module reset timing is illustrated in the following figure.

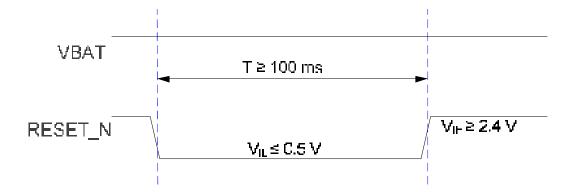


Figure 10: Reset Timing

5 RF Performances

5.1. LoRa Performances

Operating Frequency

902–928 MHz

Modulation

LORA, DTS, FHSS, FSK

Encryption Mode

AES, RNG, PCROP, RDP, WRP, CRC, PKA

Operating Mode

- Class A
- Class B
- Class C

Transmission Data Rate

- LoRa BR: 0.013–17.4 kbps
- (G)FSK BR: 0.6–300 kbps

LoRa 902–928 MHz	BW = 125 kHz, SF = 7,8,9	21dBm	
	BW = 500 kHz, SF =5,6,7,8,9,10,1		
Frequency	Tx Power (Max.)	BR (Тур.)	
FSK	21dBm	BR@ 50 kbps	
902–928 MHz		BR@ 150 kbps	



BR@ 250 kbps

5.2. Antenna/Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides a pin antenna interface designs (ANT_LoRa). And the RF port of the module requires 50 Ω characteristic impedance.

5.2.1. Pin Antenna Interface (ANT_LoRa)

Pin Name	Pin No.	I/O	Description	Comment
ANT_LORA	30	AIO	LORA antenna interface	50 Ω characteristic impedance.

Table 15: ANT_LORA Pin Definition

5.2.1.1. Reference Design

For better RF performance, it is necessary to reserve a π -type matching circuit and add an ESD protection component. Matching components such as R1, C1, C2, and D1 should be placed as close to the antenna as possible. C1, C2, and D1 are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF and R1 is recommended to be 0 Ω .

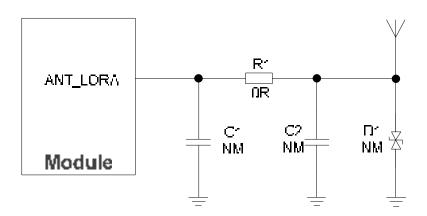


Figure 11: Antenna Reference Design

5.2.1.2. Antenna Design Requirements

Table 16: Antenna Design Requirements

Parameter	Requirement
Frequency Range (MHz)	863–928 MHz
Cable Insertion Loss (dB)	< 1
VSWR	≤ 2
Gain (dBi)	2.5 (Тур.)
Max. input power (W)	50
Input impedance (Ω)	50
Polarization type	Vertical

5.2.1.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω . The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

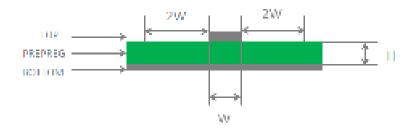


Figure 12: Microstrip Design on a 2-layer PCB



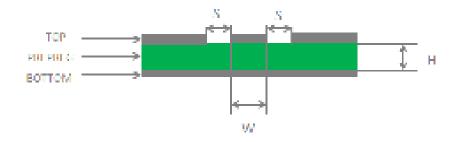


Figure 13: Coplanar Waveguide Design on a 2-layer PCB

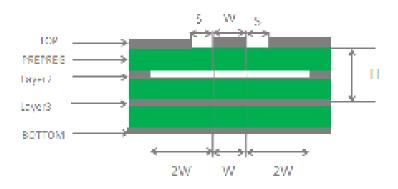


Figure 14: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

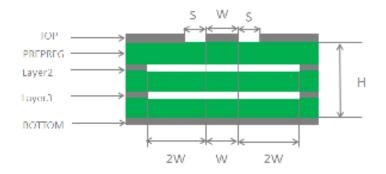


Figure 15: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to the ground.
- The distance between the RF pins and the RF connector should be as short as possible and all right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. In addition, adding some ground vias

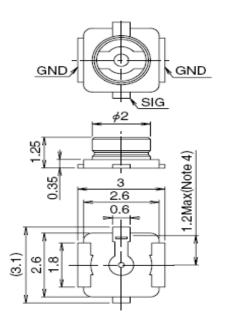
around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 \times W).

• Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see *document [2]*.

5.2.1.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.



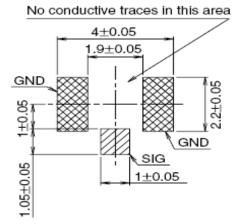


Figure 16: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

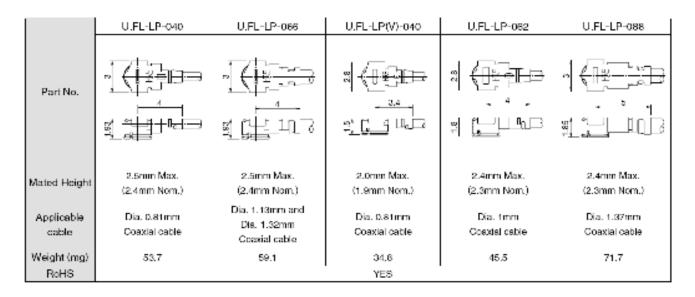


Figure 17: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

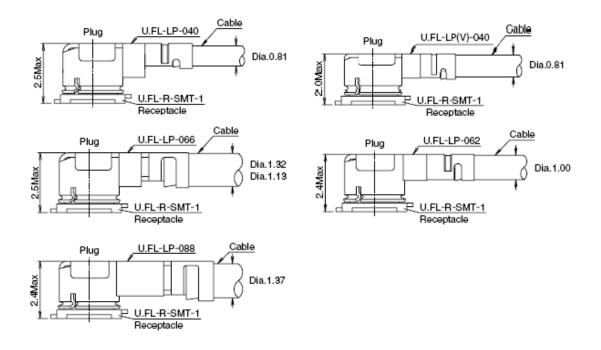


Figure 18: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit <u>http://www.hirose.com</u>.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 17: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	3.9
VDD_IO	-0.3	3.9

6.2. Power Supply Ratings

Parameter	Description	Condition	Min.	Тур.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	1.8	3.3	3.6
VDD_IO	Power supply for I/O pins	-	1.8	3.3	3.6

Table 18: Module Power Supply Ratings (Unit: V)

6.3. LoRa Power Consumption

Table 19: LoRa Power Consumption (Typ.; Unit: mA)

Condition	I
Tx @ 20 dBm	120

6.4. Digital I/O Characteristics

Table 20: VDD_IO I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V _{IH}	High-level input voltage	0.7 × VDD_IO	VDD_IO + 0.3
V _{IL}	Low-level input voltage	-0.3	0.3 × VDD_IO
V _{OH}	High-level output voltage	0.9 × VDD_IO	-
V _{OL}	Low-level output voltage	-	0.1 × VDD_IO

6.5. ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 21: ESD Characteristics (Unit: kV)

Model	Test Result	Standard
Human Body Model (HBM)	TBD	ANSI/ESDA/JEDEC JS-001-2017
Charged Device Model (CDM)	TBD	ANSI/ESDA/JEDEC JS-002-2018

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

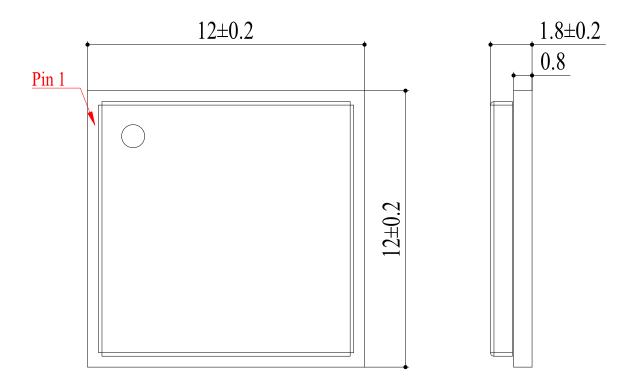


Figure 19: Top and Side Dimensions

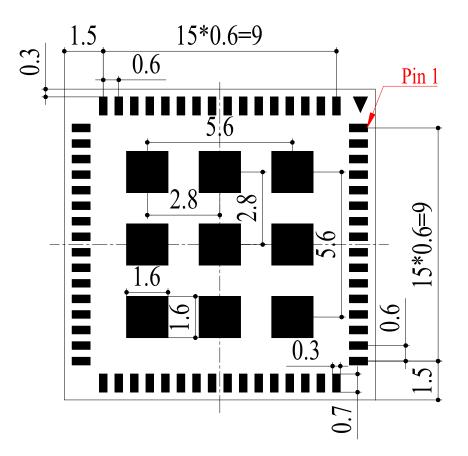


Figure 20: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

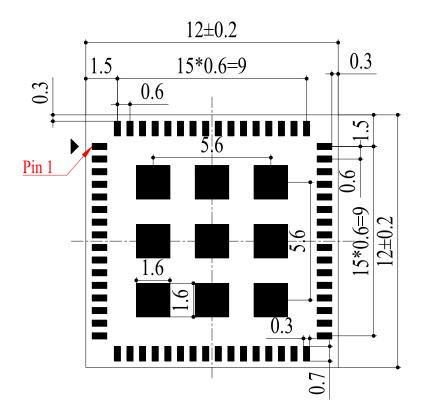


Figure 21: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

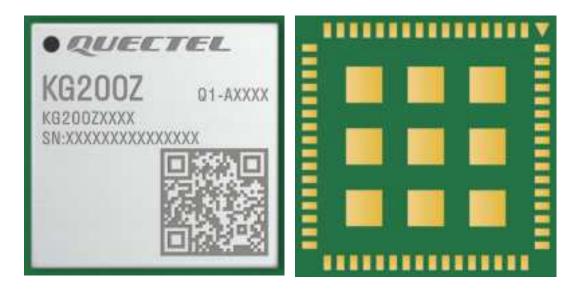


Figure 22: Top and Bottom Views

NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

- 1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.
- 2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
- 3. Floor life: 168 hours ⁴ in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
- 4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
- 5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 8 hours at 120 ±5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

⁴ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

QUECTEL

NOTE

- 1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
- 2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
- 3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see *document [3]*.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

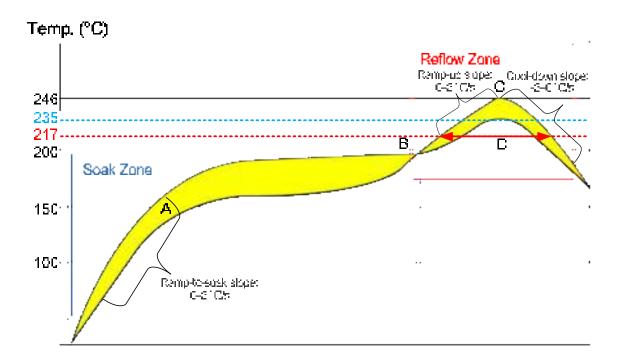


Figure 23: Recommended Reflow Soldering Thermal Profile

Table 22: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

- 1. The above profile parameter requirements are for the measured temperature of solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
- 2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
- 3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
- 4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
- 5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
- 6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
- 7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in *document [3]*.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

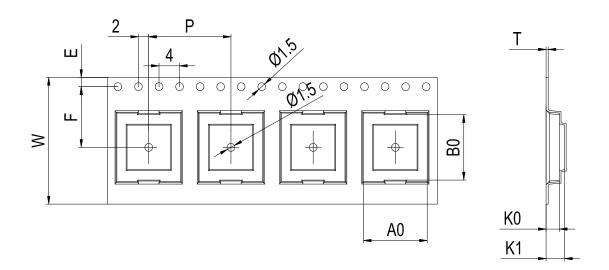


Figure 24: Carrier Tape Dimension Drawing (Unit: mm)

Table 23: Carrier Tape Dimension Table (Unit: mm)

W	Р	т	A0	B0	K0	K1	F	Е
24	16	0.35	12.4	12.4	2.6	3.6	11.5	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

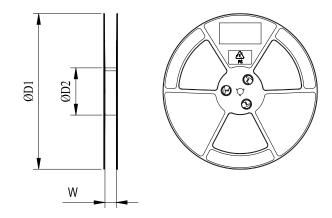


Figure 25: Plastic Reel Dimension Drawing

Table 24: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	24.5

8.3.3. Mounting Direction

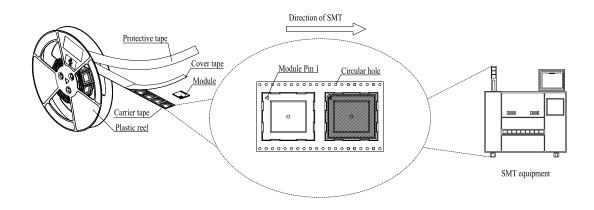
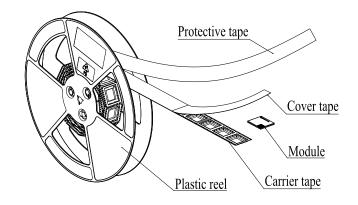


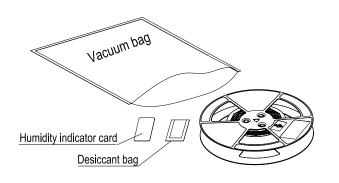
Figure 26: Mounting Direction

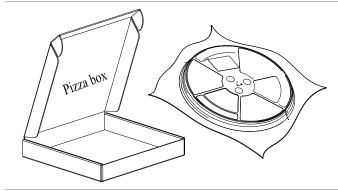
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

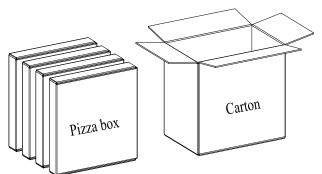


Figure 27: Packaging Process

9 Appendix References

Table 25: Reference Documents

Document Name

- [1] Quectel_KG200Z_TE-B_User_Guide
- [2] Quectel_RF_Layout_Application_Note
- [3] Quectel_Module_SMT_Application_Note

Table 26: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
BPSK	Binary Phase Shift Keying
BR	Basic Rate
BW	Band Width
CDM	Charged Device Model
CRC	Cyclic Redundancy Check
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
ESD	Electrostatic Discharge
FSK	Frequency Shift Keying

GFSK	Gauss Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GND	Ground
НВМ	Human Body Model
I/O	Input/Output
12C	Inter-Integrated Circuit
kbps	Kilobits Per Second
LDO	Low-dropout Regulator
LGA	Land Grid Array
LoRa	Long Range
LPUART	Low Power Universal Asynchronous Receiver/Transmitter
Mbps	Megabits per second
MCU	Microcontroller Unit
MSK	Minimum Shift Keying
MSL	Moisture Sensitivity Level
РСВ	Printed Circuit Board
PCROP	Proprietary Code Read Out Protection
РКА	Public Key Accelerator
PMBus	Power Management Bus
RAM	Random Access Memory
RDP	Read Protection
RF	Radio Frequency
RNG	Random Number Generators
RoHS	Restriction of Hazardous Substances
RTS	Request to Send

RXD	Receive Data
SF	Spreading Factor
SMBus	System Management Bus
SMD	Surface Mounted Devices
SMPS	Switched-Mode Power Supply
SMT	Surface Mount Technology
SPDT	Single-Pole Double-Throw
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
ТСХО	Temperature Compensate X'tal (crystal) Oscillator
TVS	Transient Voltage Suppressor
Тх	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
V _{IH}	High-level Input Voltage
VIL	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage Value
V _{OH}	High-level Output Voltage
V _{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WRP	Write Protection

Important Notice to OEM integrators

- 1. This module is limited to OEM installation ONLY.
- 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (XMR2024KG200Z) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: XMR2024KG200Z"

"Contains IC: 10224A-2024KG200Z"

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	863MHz band		915MHz band		928MHz band	
	Peak	Gain	Peak	Gain	Peak	Gain

	(dBi)	(dBi)	(dBi)
Dipole	0.95	2.5	1.88

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with 15.247 requirements for Modular Approval. The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following

conditions: (For module device use)

The antenna must be installed such that 20 cm is maintained between the antenna and users, and
 The transmitter module may not be co-located with any other transmitter or antenna.
 As long as 2 conditions above are met, further transmitter test will not be required. However, the
 OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following

conditions: (For module device use)

The antenna must be installed such that 20 cm is maintained between the antenna and users, and
 The transmitter module may not be co-located with any other transmitter or antenna.
 As long as 2 conditions above are met, further transmitter test will not be required. However, the
 OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les

conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC:10224A-2024KG200Z".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-2024KG200Z".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à

la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

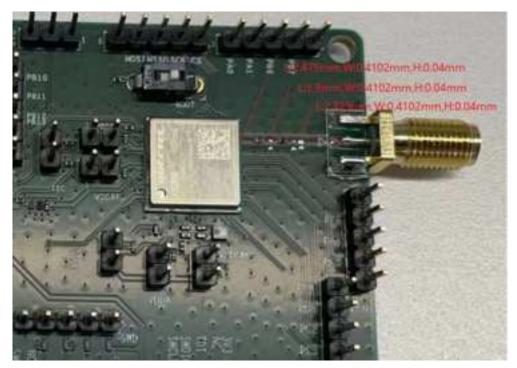
Label



FCC ID: XMR2024KG200Z

IC: 10224A-2024KG200Z

Trace design



Dielectric constant, and Impedance

4 Layer 1.0	+/-10%mm		S1150G		
Layer	Mother Board	Typical loyer thickness	Tolerance(um]	Dielectric Constant	ы
	Solder Mask	20		3.5	
11	1/Boz (plating	40	ı/-6		
	Prepreg (2116-56%*2)	250	+/ 10%	4.15	0.013
12	copper	16	i/-5		
	Core 0.96mm	960	+/ 75	4,4	0.011
13	copper	16	1/-5		
	Prepreg (2116-56%*2)	250	+/ 10%	4.15	0.013
14	1/3oz (plating	40	i/-6		
	Solder Mask	20		3.5	
	Lotal thickness	1612			

Impedance Meter											
	Туре	Control layer	Reference layer	Customer Line Width (mm)		Linished product impedance	Adjusting Line Weights (mm)	Adjust line	control	Green oil front impedance	Original to copper sheet distance
	Single ended	L1	L2	0.4102	1	50	0.439	1	(/ 5.0	49.9	/