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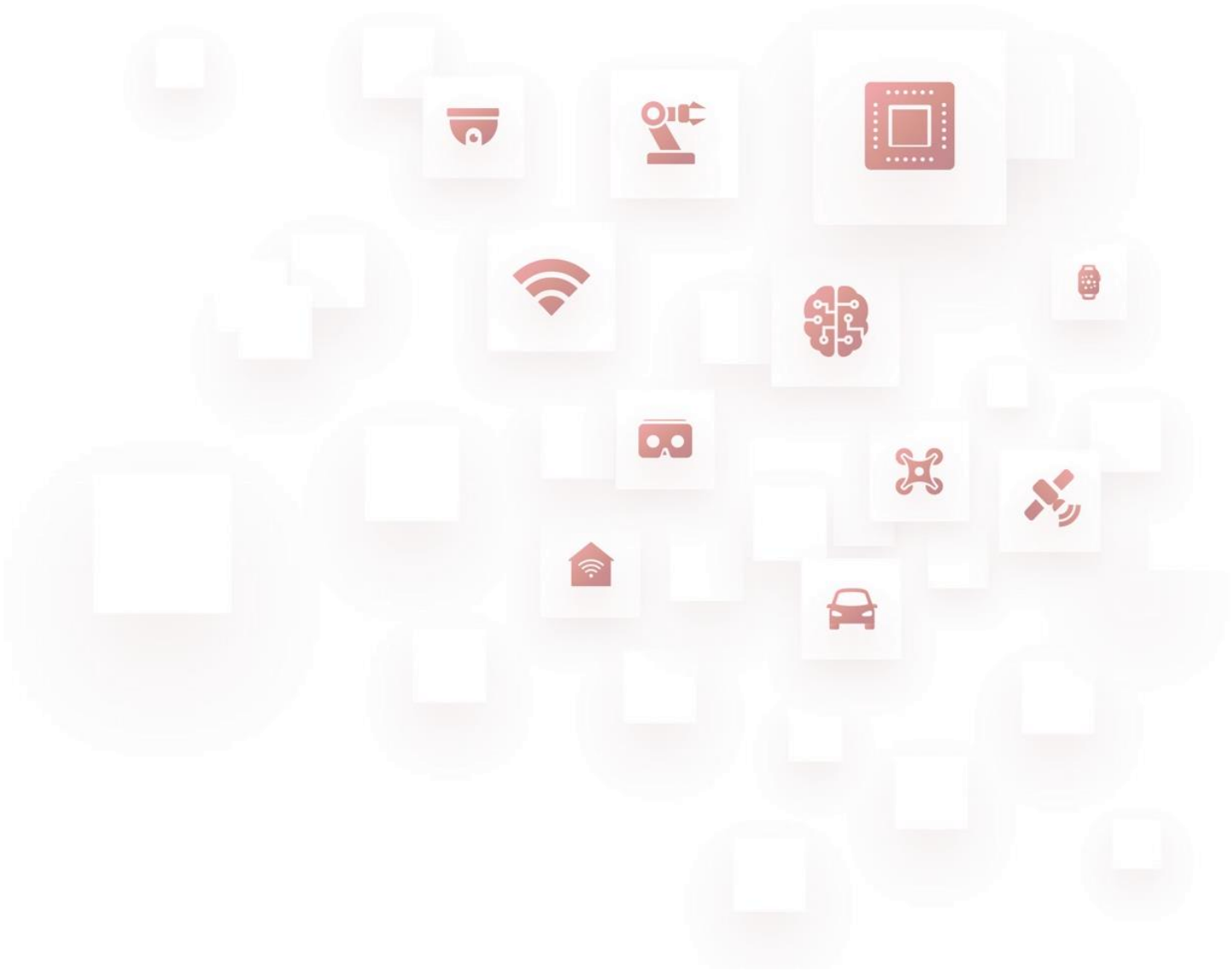

Thundercomm TurboX
C610 SOM DATASHEET

Rev V1.0
Oct 12, 2020

Revision History

Revision	Date	Description
1.0	Oct 12，2020	Initial release

Applications

TurboX C610 SOM is ideal for many applications including (but not limited to): AI, Robotics, Virtual Reality (VR), Augmented Reality (AR), Drones and Medical Devices.

Reference Documents

Document
80-pl052-1_a_qcs610_qcs410_data_sheet
80-pl052-41_b_qcs610_qcs410_+_pm6150_+_pm6150l_reference_schematic
80-ph856-1_j_pm6150_pm6250_pm7150_power_management_ic_device_specification
80-pg281-1_k_pm6150a_pm6150l_and_pm7150a_pm7150l_device_specification
80-ph856-5a_g_pm6150_pm6250_pm7150_power_management_ic_design_guidelines_training_slides
80-wl022-1_j_wcn3980_wireless_connectivity_ic_device_specification

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TurboX C610 System on Module

A high performance SOM (System On Module) based on Qualcomm® Snapdragon™ QCS610 processor

Description

Thundercomm TurboX C610 System on Module (SOM) is a high performance intelligent module, integrating Android, based on Qualcomm® Snapdragon™ 610 processor to boast a 64-bit capable Octa-core CPU architecture with Wi-Fi to balance power and performance in high-tier products.

C610 SOM supports 1x1 Wi-Fi 802.11 a/b/g/n/ac and BT5.1. It supports 2520 × 1080p 60 (Built-in) + 1920 × 1200 at 60 (external) with one 4-lane DSI and Display port 1.4; supports three 4-lane CSIs (4/4/4 or 4/4/2/1) with 2 ISP +1 lite ISP(16M+16M+2MP). It integrates multiple audio and video input/output interfaces, provides a variety of GPIO, I2C, UART and SPI standard interfaces. It support RGMII interface. In addition, it supports SOM common standard protocol interfaces such as USB3.1 gen1, USB2.0, DMIC and I2S.

C610 SOM provides convenient and stable system solution for IOT field, it can be embedded into the device on AI camera, Video Conference, Surveillance camera, Panorama camera, Dash Camera and Edge Computing, and any other connecting fields. The size of module is 38x38mm x 2.6mm, with LGA pads.

Features

The following table shows the detail features of QCS610 and C610 SOM.

QCS610	
Applications Processor	64-bit Arm v-8 compliant applications processor, Qualcomm® Kryo™ 460 CPU ■ Kryo Gold: Dual high-performance cores 2.2 GHz ■ Kryo Silver: Hexa low-power cores 1.8 GHz
DSP	Qualcomm® Hexagon™ DSP with dual Qualcomm® Hexagon™ Vector eXtensions (HVX), 1.1 GHz
Always-on system	Always-on subsystem with RPMh for hardware-based resource and power management
Graphics	■ Adreno 612; 845 MHz, 3D graphics accelerator with 64-bit addressing ■ OpenGL ES 3.2, Vulkan, DX12FL9.3

	■OpenCL 2.0
Display support	■ One 4-lane; DSI D-PHY 1.2 with split link; VESA DSC 1.1 supporting resolutions up to QHD+ ■ Display port 1.4 ■ Color depth – 30-bit pp; TFT, LTPS, CSTN ■ 2520 × 1080p 60 (Built-in) + 1920 × 1200 at 60 (external)
Camera support	■ Three 4-lane CSIs (4/4/4 or 4/4/2/1) D-DPHY is 2.1 Gbps, CPHY – 5.7 Gbps per trio ■ Three (two IFEs + one IFE Lite); 16 + 16 +2 MP ■ One IPE and one BPS
Video Encode	■ Multi-format codec up to 4K30 video encode. Multi-stream codec (4K30 + 720p + VA (YUV)) ■ Dual 14-bit image signal processing (ISP) + Lite ISP: 24 MP ■ (2x IFE + 1x IFE Lite, 16 + 16 + 2 MP), 4K30, MCTF, SHDR, C-PHY, DPHY ■ 4K30 8-bit HEVC
Video Decode	4K30 10-bit HEVC/VP9

C610 SOM	
Processor	Snapdragon™ QCS610
Memory	LPDDR4x + eMMC5.1, 16Gb + 16GB
WLAN	WCN3980, Support 1 x 1, 802.11 a/b/g/n/ac, support Bluetooth + LE5.x + HS
Display Interfaces	1x 4-lane MIPI-DSI
Camera Interfaces	3x 4-lane MIPI CSI
Audio Interface	■ SLIMbus for codec ■ SoundWire interface for codec ■ SoundWire interface for smart speaker amplifier ■ 2x MI2S ■ 2x DMIC ports supports up to 4 DMICs
USB	■ 1x USB 3.1 GEN1 ■ 1x USB 2.0 port
Display Port	Display port 1.4
RGMII	One RGMII interface with MDIO for Ethernet with AVB (1.8 V only for RGMII and MDIO)
Other Interfaces	■ 2x RF connector for Wi-Fi /BT, 1 x SDC for SD card ■ 14x QUPs (eight serial engines available in GPIOs and six serial engines available in LPI GPIOs. Only one protocol can be selected in one QUP engine at a time) ■ 2x camera dedicated I2Cs ■ 2x sensor dedicated I2Cs
Charger & Power	■ High-efficiency switch-mode Li-Ion battery charger ■ WLED and LCD bias ■ Power rail for Codec other peripherals

Operating Environment	■ Operation Temperature: -20℃ ~ 70℃ ■ Operation Humidity: 5%~95%, non-condensing
Power supply	3.2V ~ 4.8V, typ. 3.8V
Dimension	38mm x 38mm LGA
RoHS	All hardware components are fully compliant with EU RoHS 2.0 directive

1 Physical Description

1.1 Hardware Block Diagram

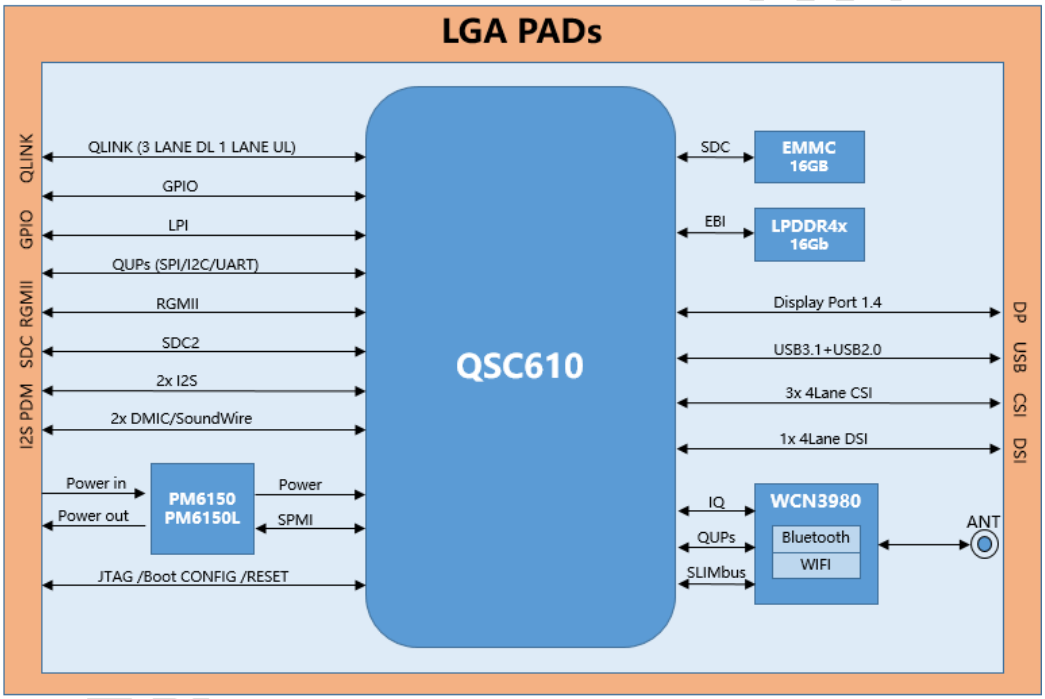


Figure 1.1-1 TurboX C610 SOM Hardware System Block Diagram

1.2 Major Components Location

TurboX C610 SOM's major components is shown as below.

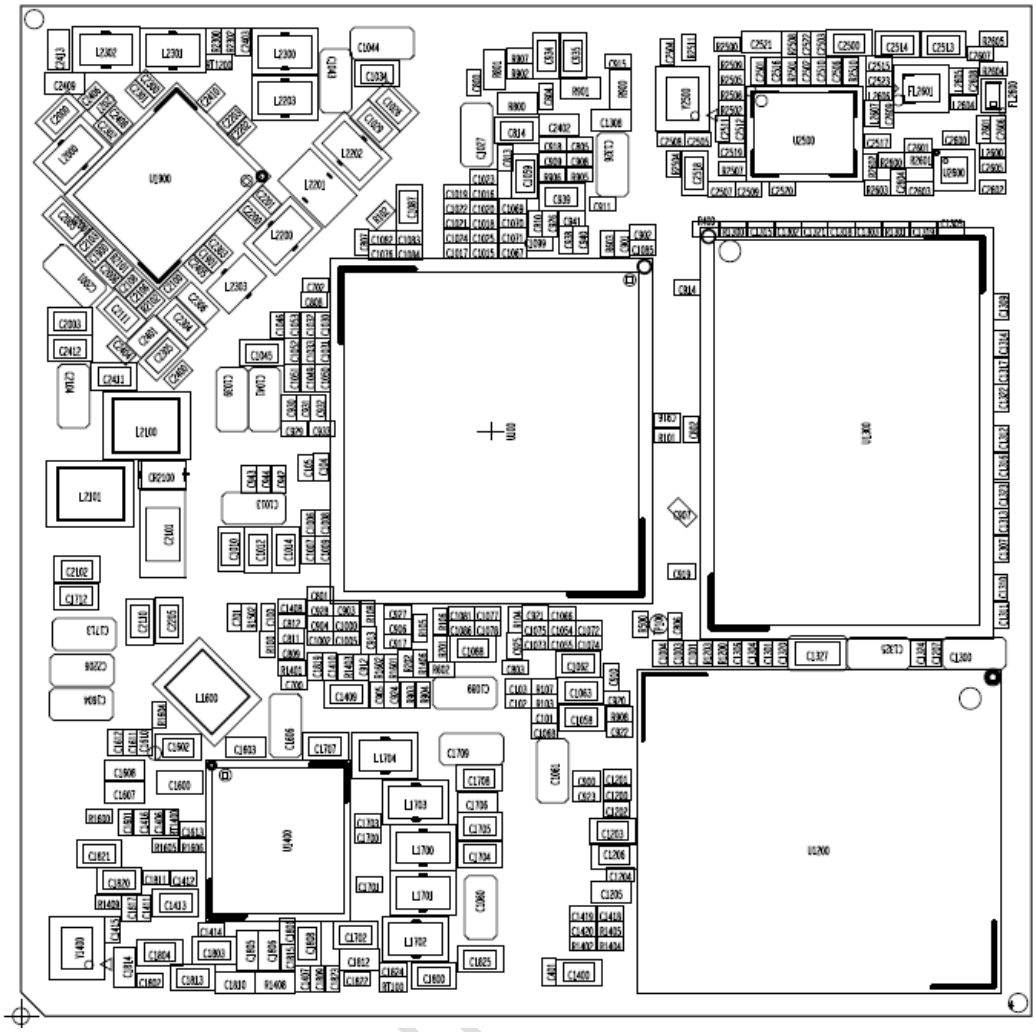


Figure 1.2-1 TurboX C610 SOM Key component Location

1.3 Package Drawing and Dimensions

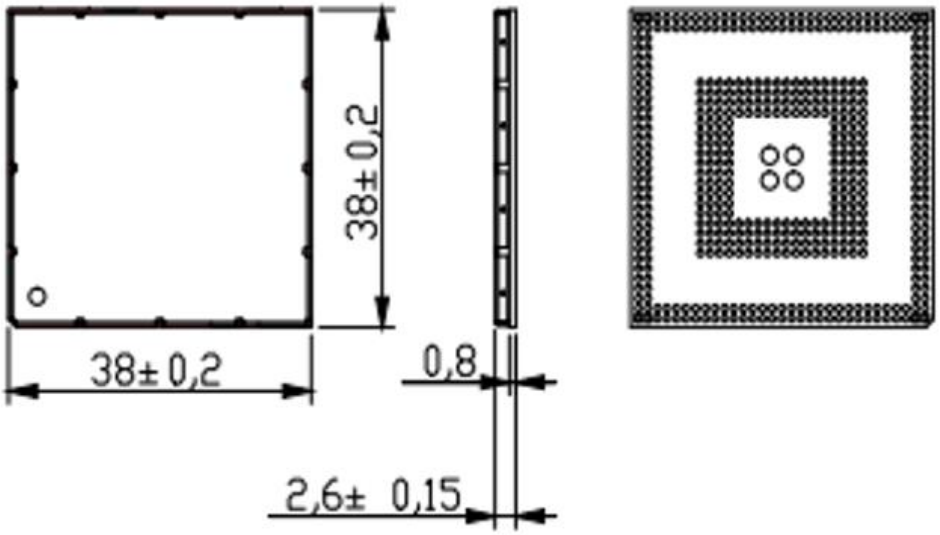


Figure 1.3-1 TurboX C610 SOM Drawing and Dimensions

2 Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on Thundercomm TurboX C610 SOM.

2.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DI	Digital input(CMOS)
DSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DO	Digital output(CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and

	is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, it is 1.8V.
P2	SDC Power group 2, it is 1.8V or 2.95V.
MV	VPH_PWR
LV	1.8V

Table 0-1 Interfaces parameter definitions

2.2 Pin Description

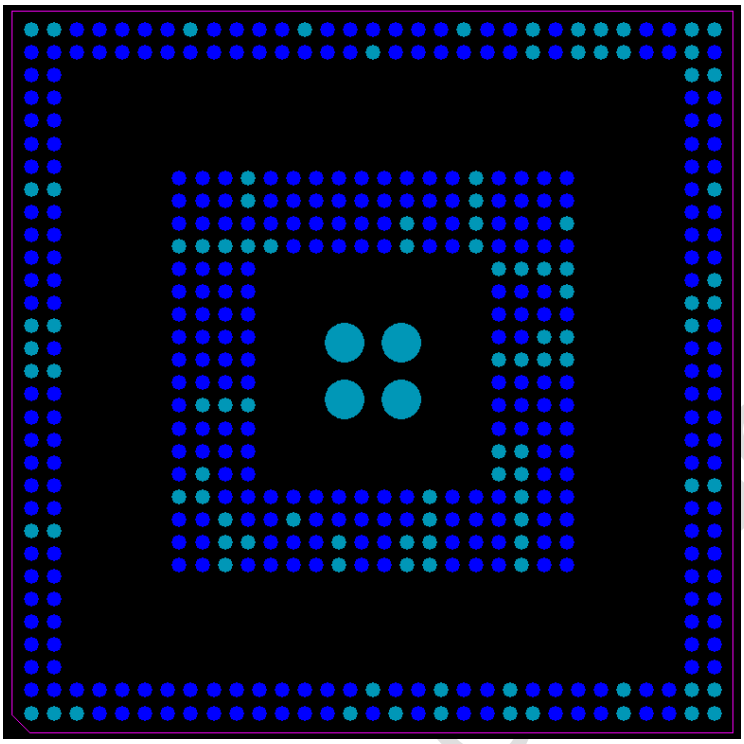
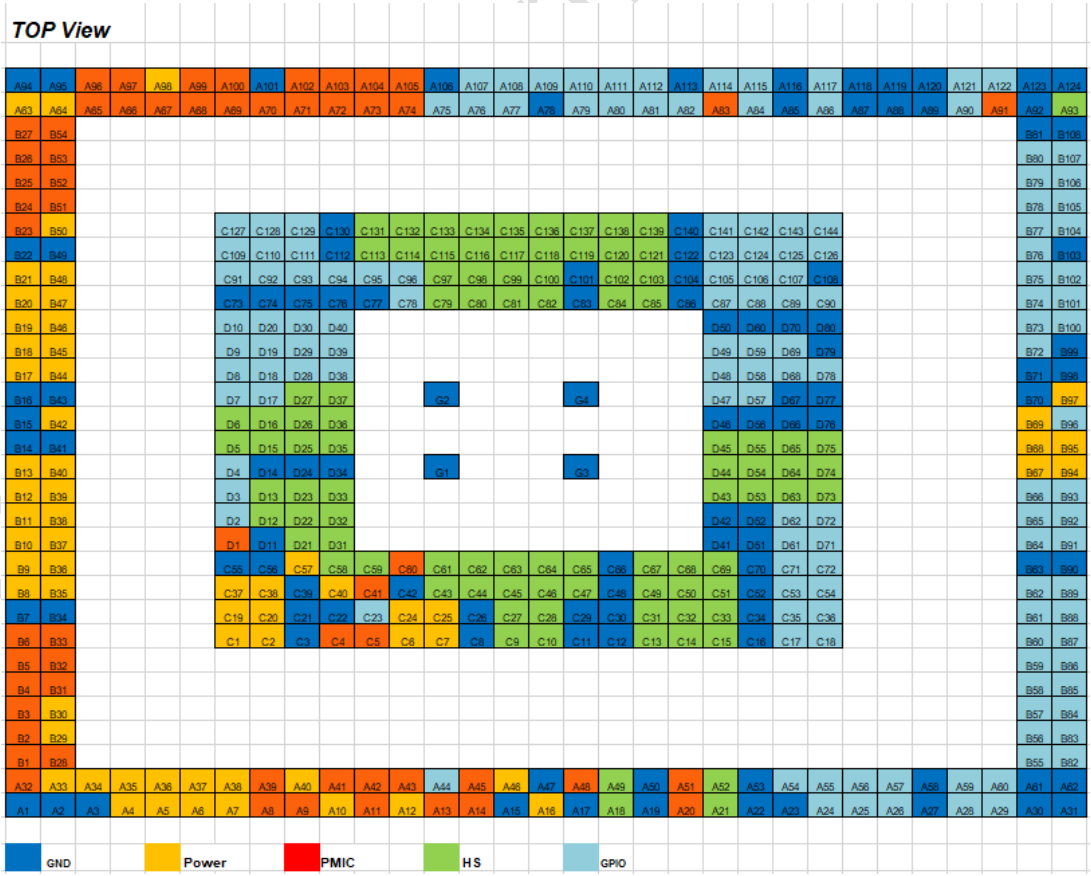


Figure 0-1 TurboX C610 SOM pin Top view



2.3 Pin Assignment

2.3.1 Power Supply Interface

Pad#	Function	Type	Function description
A1 A2 A3 A15 A17 A19 A22 A23 A27 A30 A31 A47 A50 A53 A58 A61 A62 A78 A85 A87 A88 A89 A92 A94 A95 A101 A106 A113 A116 A118 A119 A120 A123 A124 B7 B14 B15 B16 B22 B34 B41 B43 B49 B63 B70 B71 B81 B90 B98 B99 B103 B108 C3 C8 C11 C12 C16 C21 C22 C26 C29 C30 C34 C39 C42 C48 C52 C55 C56 C66 C70 C73 C74 C75 C76 C77 C83 C86 C101 C104 C108 C112 C122 C130 C140 D11 D14 D24 D34 D41 D42 D46 D50 D51 D52 D56 D60 D66 D67 D70 D76 D77 D79 D80 G1 G2 G3 G4	GND	GND	Ground

Pad#	Function	Type	Expected use
C1 C2 C19 C20 C37 C38	VBAT	PI	Battery voltage node
B12 B13 B39 B40	VPH_PWR	PI,PO	Primary system supply node
B10 B11 B37 B38	USB_IN_MID	PI	Midpoint of the charger
B8 B9 B35 B36	USB_VBUS_CONN	PO	USB VBUS OTG output
A6 A7	VREG_S4A_1P056	PO	LV sub regulation
C6 C7 C24 C25	VREG_S5A_2P04	PO	HV sub regulation
A37 A38	VREG_L1A_1P2	PO	WTR 1.2V
A35 A36	VREG_L2A_1P0	PO	WTR 1.0V analog
A4 A5	VREG_L3A_1P0	PO	WTR 1.0V digital
A40	VREG_L5A_2P7	PO	RFFE 2.7V
A33 A34	VREG_L10A_1P8	PO	1.8V PX3 LDO
C57	VREG_L13A_1P8	PO	1.8V camera IO, USB Retimer
B29	VREG_L14A_1P8	PO	WTR 1.8V analog
B30	VREG_L15A_1P8	PO	WCD93xx Codec 1.8V，600mA
A10	VREG_L16A_3P3	PO	RFFE 2.7V
A12	VREG_L18A_3P3	PO	AMOLED 3V
A46	VREG_L19A_2P85	PO	2.848v camera AFVDD rails
B17 B18 B44 B45	VREG_S8C_1P3	PO	MV sub regulation
B20 B21 B47 B48	VREG_BOB	PO	3.3V BoB
A63	VREG_L6C_SDC2	PO	SD Card IO PX2
A64	VREG_L7C_3P0	PO	Sensor, 3V

A98	VREG_L8C_1P8	PO	Sensor 1.8V
B46	VREG_L9C_2P95	PO	SD/MMC card, 2.95V
B42	VREG_WLED	PO	LCD Backlight Power
B50	VREG_DISP_P	PO	LCDB positive output voltage， 5.5V
B19	VREG_DISP_N	PO	LCDB negative output voltage，-5.5V
C40	VIB_DRV_P	PO	Power supply for haptics driver
A16	VCOIN	AI, AO	Coin-cell battery/capacitor

2.3.2 Control Signal

Pad#	Function	Voltage	Type	Function description
A57	QSC_MODE_0	1.8	DIS-PD:nppukp	Mode control bit 0
A26	QSC_MODE_1	1.8	DIS-PD:nppukp	Mode control bit 0
D48	SDM_RESOUT_N	1.8	DO	Reset output
A44	SDM_PS_HOLD	1.8	DO	Power supply hold signal to PMIC
C23	SDM_RESIN_N	1.8	DI	Used for generating a stage 2 and/or stage 3 reset
B92	FORCED_USB_BOOT	1.8	DI	SDM_GPIO_101, force USB boot
A45	PHONE_ON_N	-	DI	Connected to a keypad power-on button
A51	PM_RESIN_N	-	DI	Reset input
A14	CBLPWR_N	-	DI	Used to initiate the power-on sequence when grounded
B1	WTR_CLK	-	DO	RF clock 1, 38.4 MHz RF (low-noise) XO clock buffer output
A8	RF_CLK3	-	-	RF clock 3, NC
A39	NFC_LNBBCLK3	-	DO	19.2 MHz, NFC clock
C41	SLEEP_CLK	-	DO	Sleep clock
D1	FAULT_N	-	DO	PMIC fault signal
A103	CABC	-	DI	Content-adaptive backlight control
B23	DISP_HW_EN	1.8	DO	Hardware enable pin for LCDB
B31	SMB_EN	1.8	DO	Enable/disable control pin for parallel SMB (slave) charger.
B3	DC_IN_EN	-	DO	DC barrel jack charging power source enable/disable pin. Keeps DC charger input disabled during USB charging.
B4	DC_IN_PON	-	AO	DC charging power-on trigger
B5	DC_IN_PSNS	-	AO	DC charging power sense input
B32	IUSB_OUT	-	AO	Buffered voltage signal proportional to USB input current
B6	VBATT_CONN_VSNS_M	-	AI	Battery voltage sense input minus
B33	VBATT_CONN_VSNS_P	-	AI	Battery voltage sense input plus
A32	PACK_SNS_M	-	AI	Battery voltage sense input minus

B2	BATT_ID	-	AI	Battery ID input
B28	BATT_THERM	-	AI	Battery temperature input
C4	BA_N	-	DO	Battery alarm
A66	SPMI_CLK	1.8V	DO	SPMI communication bus clock
A67	SPMI_DATA	1.8V	B	SPMI communication bus
C60	TYPEC_uUSB_SEL	-	AO	AUX1, 560Kohm to GND if use USB Type_C connector on USB port 0. Float, If use Micro USB connector,
A48	USB_THERM	-	AI	AMUX 4
A97	EMMC/UFS_THERM	-	AI	6150L AMUX1
A69	RF_PA0_THERM	-	AI	6150L AMUX2
A68	RF_PA1_THERM	-	AI	6150L AMUX3

2.3.3 USB DisplayPort

Pad#	Function	Voltage	Type	Function description
C65	USB1_DP_LANE1_P	-	AO	Display port lane 0 pair plus
C47	USB1_DP_LANE1_M	-	AO	Display port lane 0 pair minus
C27	USB1_DP_LANE2_P	-	AO	Display port lane 1 pair plus
C9	USB1_DP_LANE2_M	-	AO	Display port lane 1 pair minus
C64	USB1_DP_LANE3_P	-	AO	Display port lane 2 pair plus
C46	USB1_DP_LANE3_M	-	AO	Display port lane 2 pair minus
C63	USB1_DP_LANE4_P	-	AO	Display port lane 3 pair plus
C45	USB1_DP_LANE4_M	-	AO	Display port lane 3 pair minus
C28	USB1_DP_AUX_P	-	AI, AO	Display port auxiliary pair plus
C10	USB1_DP_AUX_M	-	AI, AO	Display port auxiliary pair minus
C62	USB1_HS_DP	-	AO	USB1 high-speed data - plus
C44	USB1_HS_DM	-	AO	USB1 high-speed data - minus
C59	USB0_HS_DP	-	AI, AO	USB0 high-speed data - plus
C58	USB0_HS_DM	-	AI, AO	USB0 high-speed data - minus
D23	USB0_SS_RX0_P	-	AI	USB super-speed receive 0 - plus
D33	USB0_SS_RX0_M	-	AI	USB super-speed receive 0 - minus
D13	USB0_SS_RX1_P	-	AI	USB super-speed receive 1 - plus
D12	USB0_SS_RX1_M	-	AI	USB super-speed receive 1 - minus
D21	USB0_SS_TX0_P	-	AO	USB super-speed transmit 0 - plus
D31	USB0_SS_TX0_M	-	AO	USB super-speed transmit 0 - minus
D22	USB0_SS_TX1_P	-	AO	USB super-speed transmit 1 - plus
D32	USB0_SS_TX1_M	-	AO	USB super-speed transmit 1 - minus
A21	USB_SBU1	-	DI	Type-C side band signal SBU1
A52	USB_SBU2	-	DI	Type-C side band signal SBU2
A49	USB_CC1	-	AI/PO	CC1 pin for the USB Type-C connector

A18	USB_CC2	-	AI/PO	CC2 pin for the USB Type-C connector

2.3.4 MIPI

Pad#	Function	Voltage	Type	Function description
C84	MIPI_CSI0_L0_P	CSI	AI	MIPI CSI 0 (DPHY) differential lane 0 - plus
C85	MIPI_CSI0_L0_N	CSI	AI	MIPI CSI 0 (DPHY) differential lane 0 - minus
C138	MIPI_CSI0_L1_P	CSI	AI	MIPI CSI 0 (DPHY) differential lane 1 - plus
C139	MIPI_CSI0_L1_N	CSI	AI	MIPI CSI 0 (DPHY) differential lane 1 - minus
C120	MIPI_CSI0_L2_P	CSI	AI	MIPI CSI 0 (DPHY) differential lane 2 - plus
C121	MIPI_CSI0_L2_N	CSI	AI	MIPI CSI 0 (DPHY) differential lane 2 - minus
C119	MIPI_CSI0_L3_P	CSI	AI	MIPI CSI 0 (DPHY) differential lane 3 - plus
C137	MIPI_CSI0_L3_N	CSI	AI	MIPI CSI 0 (DPHY) differential lane 3 - minus
C102	MIPI_CSI0_CLK_P	CSI	AI	MIPI CSI 0 (DPHY) differential clock - plus
C103	MIPI_CSI0_CLK_N	CSI	AI	MIPI CSI 0 (DPHY) differential clock - minus
C99	MIPI_CSI1_L0_P	CSI	AI	MIPI CSI 1 (DPHY) differential lane 0 - plus
C81	MIPI_CSI1_L0_N	CSI	AI	MIPI CSI 1 (DPHY) differential lane 0 - minus
C118	MIPI_CSI1_L1_P	CSI	AI	MIPI CSI 1 (DPHY) differential lane 1 - plus
C136	MIPI_CSI1_L1_N	CSI	AI	MIPI CSI 1 (DPHY) differential lane 1 - minus
C117	MIPI_CSI1_L2_P	CSI	AI	MIPI CSI 1 (DPHY) differential lane 2 - plus
C135	MIPI_CSI1_L2_N	CSI	AI	MIPI CSI 1 (DPHY) differential lane 2 - minus
C98	MIPI_CSI1_L3_P	CSI	AI	MIPI CSI 1 (DPHY) differential lane 3 - plus
C80	MIPI_CSI1_L3_N	CSI	AI	MIPI CSI 1 (DPHY) differential lane 3 - minus
C100	MIPI_CSI1_CLK_P	CSI	AI	MIPI CSI 1 (DPHY) differential clock - plus
C82	MIPI_CSI1_CLK_N	CSI	AI	MIPI CSI 1 (DPHY) differential clock - minus
C132	MIPI_CSI2_L0_P	CSI	AI	MIPI CSI 2 (DPHY) differential lane 0 - plus
C114	MIPI_CSI2_L0_N	CSI	AI	MIPI CSI 2 (DPHY) differential lane 0 - minus
C131	MIPI_CSI2_L1_P	CSI	AI	MIPI CSI 2 (DPHY) differential lane 1 - plus
C113	MIPI_CSI2_L1_N	CSI	AI	MIPI CSI 2 (DPHY) differential lane 1 - minus
C134	MIPI_CSI2_L2_P	CSI	AI	MIPI CSI 2 (DPHY) differential lane 2 - plus
C116	MIPI_CSI2_L2_N	CSI	AI	MIPI CSI 2 (DPHY) differential lane 2 - minus
C133	MIPI_CSI2_L3_P	CSI	AI	MIPI CSI 2 (DPHY) differential lane 3 - plus
C115	MIPI_CSI2_L3_N	CSI	AI	MIPI CSI 2 (DPHY) differential lane 3 - minus
C97	MIPI_CSI2_CLK_P	CSI	AI	MIPI CSI 2 (DPHY) differential clock - plus
C79	MIPI_CSI2_CLK_N	CSI	AI	MIPI CSI 2 (DPHY) differential clock - minus
C14	MIPI_DSI0_L0_P	DSI	AO	MIPI DSI lane 0 pair plus
C32	MIPI_DSI0_L0_N	DSI	AO	MIPI DSI lane 0 pair minus
C49	MIPI_DSI0_L1_P	DSI	AO	MIPI DSI lane 1 pair plus
C67	MIPI_DSI0_L1_N	DSI	AO	MIPI DSI lane 1 pair minus
C50	MIPI_DSI0_L2_P	DSI	AO	MIPI DSI lane 2 pair plus
C68	MIPI_DSI0_L2_N	DSI	AO	MIPI DSI lane 2 pair minus
C15	MIPI_DSI0_L3_P	DSI	AO	MIPI DSI lane 3 pair plus

C33	MIPI_DSI0_L3_N	DSI	AO	MIPI DSI lane 3 pair minus
C13	MIPI_DSI0_CLK_P	DSI	AO	MIPI DSI clock pair plus
C31	MIPI_DSI0_CLK_N	DSI	AO	MIPI DSI clock pair minus
C51	MIPI_DSI1_CLK_P	DSI	AO	MIPI DSI clock 1 pair plus
C69	MIPI_DSI1_CLK_N	DSI	AO	MIPI DSI clock 1 pair minus

2.3.5 PMIC IO

Pad#	Function	Voltage	Type	Function description
A41	PM_GPIO1	MV	-	PM6150 GPIO1
A83	PM_GPIO2	MV	-	PM6150 GPIO2
A13	PM_GPIO3	MV	-	PM6150 GPIO3
A20	PM_GPIO4	MV	-	PM6150 GPIO4
A42	PM_GPIO6	LV	-	PM6150 GPIO6
C5	PM_GPIO7	LV	-	PM6150 GPIO7
A43	PM_GPIO8	LV	-	PM6150 GPIO8
A9	PM_GPIO9	LV	-	PM6150 GPIO9
A11	PM_GPIO10	LV	-	PM6150 GPIO10
B26	PML_GPIO1	LV	-	Reserved
B27	KEY_VOLP_N	LV	-	PM6150L GPIO2
A96	CAM_DVDD0_1P2_EN	LV	-	PM6150L GPIO3
B54	SDM_DP_EN	LV	-	PM6150L GPIO4
B53	CAMERA_FLASH_THERM	LV	-	PM6150L GPIO5
A65	IR_LED_PWM	LV	-	PM6150L GPIO6
A99	PML_GPIO8	MV	-	PM6150L GPIO8
A70	DBU2_ETH_PHY_3P3_EN	MV	-	PM6150L GPIO9
A91	QUIET_THERM	MV	-	PM6150L GPIO10
A100	PML_GPIO11	MV	-	PM6150L GPIO11
B24	PML_GPIO12	LV	-	PM6150L GPIO12
A71	BLUE_LED	-	AO	RGB LED high-side current source for the blue LED
A105	GREEN_LED	-	AO	RGB LED high-side current source for the green LED
A74	RED_LED	-	AO	RGB LED high-side current source for the red LED
B51	FLASH_LED1	-	AO	Flash high-side current source for LED1
B25	FLASH_LED2	-	AO	Flash high-side current source for LED2
B52	FLASH_LED3	-	AO	Flash high-side current source for LED3
A102	WLED_SINK1	-	PI	WLED low-side current sink input, string 1
A72	WLED_SINK2	-	PI	WLED low-side current sink input, string 2
A73	WLED_SINK3	-	PI	WLED low-side current sink input, string 3

A104	WLED_SINK4	-	PI	WLED low-side current sink input, string 4

2.3.6 LPI GPIO

Pad#	Function	Voltage	Type	Function description
B82	SSC_I2C_1_SDA	1.8V	B	LPI_GPIO00
B55	SSC_I2C_1_SCL		B	LPI_GPIO01
A59	SSC_SPI_1_MISO		DI	LPI_GPIO02
A28	SSC_SPI_1_MOSI		DO	LPI_GPIO03
B56	SSC_SPI_1_CLK		DO	LPI_GPIO04
A60	SSC_SPI_1_CS_N		DO	LPI_GPIO05
B83	LPI_GPIO_6		B-PD:nppukp	LPI_GPIO06
A29	LPI_GPIO_7		B-PD:nppukp	LPI_GPIO07
D69	BT_PCM_IN		B	LPI_GPIO08
D59	BT_PCM_OUT		B	LPI_GPIO09
D78	BT_PCM_CLK		B	LPI_GPIO10
D68	BT_PCM_SYNC		B	LPI_GPIO11
B86	SSC_UART_2_TX		DO	LPI_GPIO14
B65	SSC_UART_2_RX		DI	LPI_GPIO15
B91	LPI_GPIO_16		B-PD:nppukp	LPI_GPIO16
D49	LPI_GPIO_17		B-PD:nppukp	LPI_GPIO17
D8	SWR_TX_CLK		DO	LPI_GPIO18
D20	SWR_TX_DATA1		DO	LPI_GPIO19
D19	SWR_TX_DATA2		DO	LPI_GPIO20
D9	SWR_RX_CLK		DO	LPI_GPIO21
D29	SWR_RX_DATA1		DI	LPI_GPIO22
D28	SWR_RX_DATA2		DI	LPI_GPIO23
D18	SWR_CODE_RST_N		DO	LPI_GPIO24
D10	LPI_GPIO_25		B-PD:nppukp	LPI_GPIO25
D30	SDM_DMIC_CLK1		DO	LPI_GPIO26
D40	SDM_DMIC_DATA1		DO	LPI_GPIO27
D38	SDM_DMIC_CLK2		DO	LPI_GPIO28
D39	SDM_DMIC_DATA2		DO	LPI_GPIO29

2.3.7 QCS GPIO

Pad#	Function	Voltage	Type	Function description
D62	SDM_GPIO_0	1.8V	B-PD:nppukp	GPIO_00
C53	SDM_GPIO_1		B-PD:nppukp	GPIO_01
D61	SDM_GPIO_2		B-PD:nppukp	GPIO_02
C71	SDM_GPIO_3		B-PD:nppukp	GPIO_03

B62	QUP0_1_I2C_SDA		B	GPIO_04
B89	QUP0_1_I2C_SCL		B	GPIO_05
C94	QUP1_2_SPI_MISO		DI	GPIO_06
C111	QUP1_2_SPI_MOSI		DO	GPIO_07
C93	QUP1_2_SPI_CLK		DO	GPIO_08
C129	QUP1_2_SPI_CS_N		DO	GPIO_09
B73	SDM_GPIO_14		B-PD:nppukp	GPIO_14
B72	SDM_GPIO_15		B-PD:nppukp	GPIO_15
B66	QUP0_0_UART_TX		DO	GPIO_16
B96	QUP0_0_UART_RX		DI	GPIO_17
D57	QUP0_3_I2C_SDA		B	GPIO_18
D47	QUP0_3_I2C_SDL		B	GPIO_19
B104	HDMI_RSTN		B-PD:nppukp	GPIO_20
C107	SDM_GPIO_21		B-PD:nppukp	GPIO_21
C90	IR_LED_PWM_CAM2		B-PD:nppukp	GPIO_22
C89	IR_LED_FLASH_CAM2		B-PD:nppukp	GPIO_23
B102	SDM_GPIO_24		B-PD:nppukp	GPIO_24
B101	SDM_GPIO_25		B-PD:nppukp	GPIO_25
B80	HDMI_INT		B-PD:nppukp	GPIO_26
C141	BOOT_CONFIG_2		DI	GPIO_27
C96	CAM_MCLK0		DO	GPIO_28
C95	CAM_MCLK1_CONN2		DO	GPIO_29
C78	CAM_MCLK2_CONN2		DO	GPIO_30
A81	CAM_MCLK3_CONN2		DO	GPIO_31
A117	CCI_I2C_SDA0		B	GPIO_32
A86	CCI_I2C_SCL0		B	GPIO_33
A79	CCI_I2C_SDA1		B	GPIO_34
A110	CCI_I2C_SCL1		B	GPIO_35
B75	EPHY_RST_N		B-PD:nppukp	GPIO_36
A114	CAM2_RST_N_CONN2/IRIS_DRV1_M		B-PD:nppukp	GPIO_37
A107	FRONT_FL_EN/IMX334_IRIS_DRV1_P		B-PD:nppukp	GPIO_38
A75	FLASH_STROBE		B-PD:nppukp	GPIO_39
A112	CAM3_RST_N/IRIS_DRV2_P		B-PD:nppukp	GPIO_40
A76	IRIS_DRV2_M/CAM_IRQ		B-PD:nppukp	GPIO_41
C123	OIS_SYNC		DI	GPIO_42
A108	FORCE_USB_BOOT_POL_SEL		DI	GPIO_43
C124	SDM_GPIO_44		B-PD:nppukp	GPIO_44
A111	CAM1_RST_N_CONN2		B-PD:nppukp	GPIO_45

A77	IMX290_DVDD_eLDO5_EN		B-PD:nppukp	GPIO_46
A82	CAM0_RST_N		B-PD:nppukp	GPIO_47
A80	USB_DP_GPU_SEL		B-PD:nppukp	GPIO_49
A109	SDM_GPIO_50		B-PD:nppukp	GPIO_50
D2	QLINK_REQUEST		DI	GPIO_51
D3	QLINK_ENABLE		DO	GPIO_52
D71	PA_INDICATOR		DO	GPIO_53
C17	SDM_GPIO_54		B-PD:nppukp	GPIO_54
D72	SDM_GPIO_55		B-PD:nppukp	GPIO_55
C36	SDM_GPIO_56		B-PD:nppukp	GPIO_56
C35	BOOT_CONFIG_0		DI	GPIO_57
C54	SDM_GPIO_58		B-PD:nppukp	GPIO_58
C18	SDM_GPIO_59		B-PD:nppukp	GPIO_59
C72	SDM_GPIO_60		B-PD:nppukp	GPIO_60
D7	RFFE1_DATA		B-PD:nppukp	GPIO_61
D17	RFFE1_CLK		B-PD:nppukp	GPIO_62
A25	BOOT_CONFIG_11		DI	GPIO_63
B58	SDM_GPIO_64		B-PD:nppukp	GPIO_64
A54	BOOT_CONFIG_8		DI	GPIO_65
B85	SDM_GPIO_66		B-PD:nppukp	GPIO_66
A55	BOOT_CONFIG_9		DI	GPIO_67
B84	SDM_GPIO_68		B-PD:nppukp	GPIO_68
A56	BOOT_CONFIG_12		DI	GPIO_69
B59	SDM_GPIO_70		B-PD:nppukp	GPIO_70
B57	SDM_GPIO_71		B-PD:nppukp	GPIO_71
A24	BOOT_CONFIG_7		DI	GPIO_72
A115	IR_CUT_FILTER_P		B-PD:nppukp	GPIO_73
A84	CAM0_STANDBY_N/IRCUT_FILTER_M		B-PD:nppukp	GPIO_74
C143	IR_LED_FLASH		B-PD:nppukp	GPIO_75
B100	EPHY_INT_N		B-PD:nppukp	GPIO_76
C106	SDM_GPIO_77		B-PD:nppukp	GPIO_77
C87	SDM_GPIO_78		B-PD:nppukp	GPIO_78
B76	HDMI_ELDO_EN		B-PD:nppukp	GPIO_79
B74	ALPS_INT_N		B-PD:nppukp	GPIO_84
C142	ACCL_GYRO_DRDY_INT		B-PD:nppukp	GPIO_85
C144	ACCL_GYRO_EVENT_INT		B-PD:nppukp	GPIO_86
C105	MAG_INT_N		B-PD:nppukp	GPIO_87
B61	BOOT_CONFIG_1		DI	GPIO_88
B88	SDM_GPIO_89		B-PD:nppukp	GPIO_89
B87	MDP_VSYNC_P		DI	GPIO_90
B60	LCD0_RST_N		B-PD:nppukp	GPIO_91

B93	KEY_SNAPSHOT_N		B-PD:nppukp	GPIO_98
C125	SDM_GPIO_99		B-PD:nppukp	GPIO_99
B64	KEY_FOCUS_N		B-PD:nppukp	GPIO_100
D4	WMSS_RST_N		B-PD:nppukp	GPIO_105
C88	WCD_WSA_EN1		B-PD:nppukp	GPIO_108
A122	SDM_WSA_EN2		B-PD:nppukp	GPIO_109
A90	SDM_SWR_DATA		B	GPIO_110
A121	SDM_SWR_CLK		B	GPIO_111
B78	I2S_SCK		BI	GPIO_115
B107	I3S_WS		B	GPIO_116
B79	I2S_DATA0		B	GPIO_117
B106	I2S_DATA1		B	GPIO_118
B77	HDMI_DET_N		B-PD:nppukp	GPIO_119
C126	BOOT_CONFIG_3		DI	GPIO_120
B105	I2S_MCLK		DO	GPIO_121
D58	WCD_INT1		B-PD:nppukp	GPIO_122

2.3.8 RGMII

Pad#	Function	Voltage	Type	GPIO	Function description
D43	RGMII_RXD0	1.8V	DI	GPIO_83	RGMII receive data 0
D53	RGMII_RXD1		DI	GPIO_82	RGMII receive data 1
D63	RGMII_RXD2		DI	GPIO_81	RGMII receive data 2
D73	RGMII_RXD3		DI	GPIO_103	RGMII receive data 3
D55	RGMII_RX_CTL		DI	GPIO_112	RGMII receive Control
C43	RGMII_RX_CLK		DO		RGMII Receiver Clock
D44	RGMII_TXD0		DO	GPIO_96	RGMII transmit data 0
D54	RGMII_TXD1		DO	GPIO_95	RGMII transmit data 1
D64	RGMII_TXD2		DO	GPIO_94	RGMII transmit data 2
D74	RGMII_TXD3		DO	GPIO_93	RGMII transmit data 3
D75	RGMII_TX_EN		DO	GPIO_97	RGMII transmit enable
C61	RGMII_TX_CLK		DO	GPIO_92	RGMII transmit clock
D65	RGMII_MDC		DI	GPIO_113	RGMII management interface clock
D45	RGMII_MDIO		-	GPIO_114	RGMII management interface IO

2.3.9 QLINK

Pad#	Function	Voltage	Type	Function description

D26	QLINK_RX1_P	-	AI	QLink downlink lane 0 - plus
D36	QLINK_RX1_M	-	AI	QLink downlink lane 0 - minus
D27	QLINK_RX2_P	-	AI	QLink downlink lane 1 - plus
D37	QLINK_RX2_M	-	AI	QLink downlink lane 1 - minus
D6	QLINK_RX3_P	-	AI	QLink downlink lane 2 - plus
D16	QLINK_RX3_M	-	AI	QLink downlink lane 2 - minus
D25	QLINK_TX1_P	-	AO	QLink uplink lane 0 - plus
D35	QLINK_TX1_M	-	AO	QLink uplink lane 0 - minus
D5	QLINK_CLK_P	-	AO	QLink clock - plus
D15	QLINK_CLK_M	-	AO	QLink clock - minus

2.3.10SDC2

Pad#	Function	Voltage	Type	Function description
C128	SDC2_CLK	1.8/2.95	BH-NP: dpukp	Secure digital controller 2 clock
C127	SDC2_CMD		BH-NP: dpukp	Secure digital controller 2 command
C109	SDC2_DATA_0		BH-NP: dpukp	Secure digital controller 2 data bit 0
C110	SDC2_DATA_1		BH-NP: dpukp	Secure digital controller 2 data bit 1
C92	SDC2_DATA_2		BH-NP: dpukp	Secure digital controller 2 data bit 2
C91	SDC2_DATA_3		BH-NP: dpukp	Secure digital controller 2 data bit 3

2.3.11 JTAG

Pad#	Function	Voltage	Type	Function description
B67	JTAG_TDO	1.8	DO-Z	JTAG data output
B68	JTAG_TRST_N		DI PD:nppukp	JTAG reset
B69	JTAG_SRST_N		DI-PU	JTAG reset for debug
B94	JTAG_TMS		DI PU:nppukp	JTAG mode select input
B95	JTAG_TCK		DI-PU	JTAG clock input
B97	JTAG_TDI		DI PU:nppukp	JTAG data input

2.3.12 Antenna Interface

Pad#	Function	Voltage	Type	Function description
A93	WIFI ANT	-	-	Wi-Fi antenna connector

3 Function Description

3.1 Input Power Management

Input power management functions include:

- Switching charger and battery charging
- Qualcomm battery gauge
- Battery interface module
- Battery current limiting
- Coin cell/keep alive capacitor

3.2 Charger Module

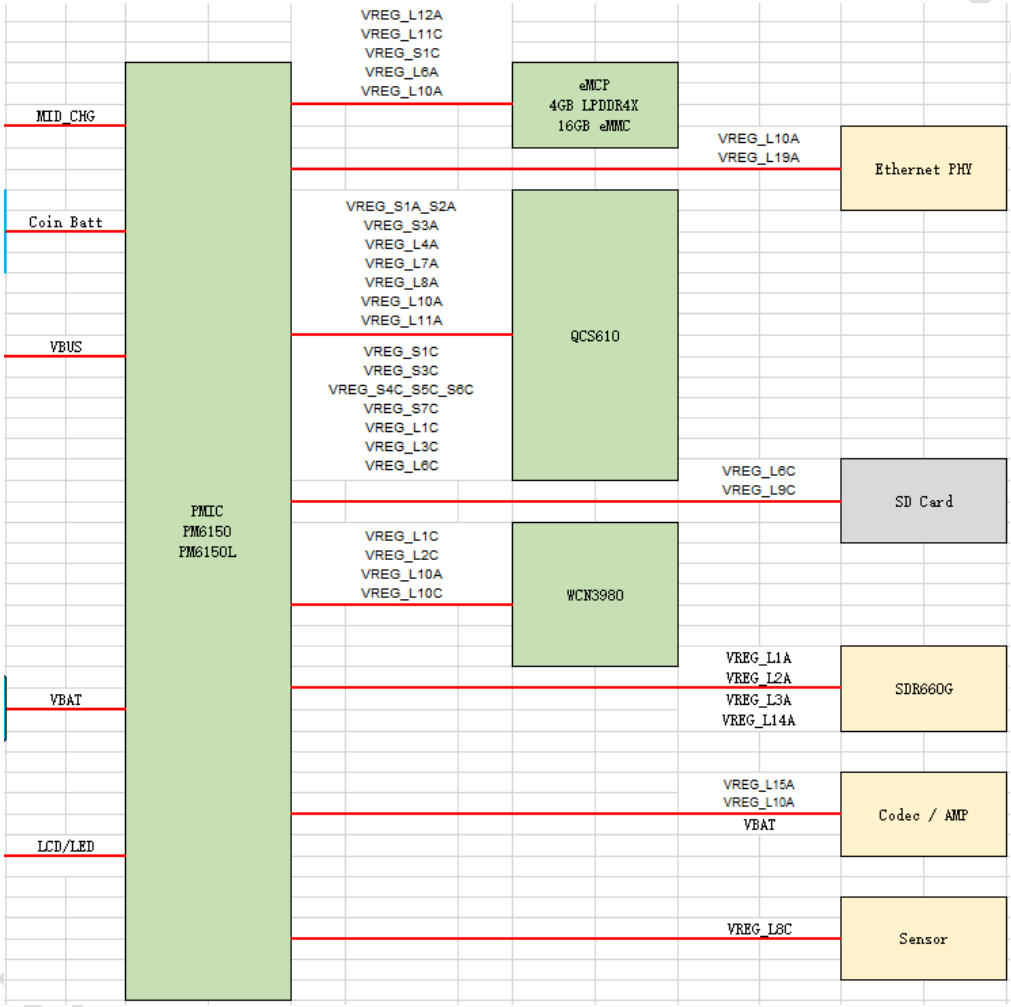
PM6150 incorporates a dual-input, high-efficiency switch-mode battery charger for single-cell lithium batteries.

3.3 Power on Sequence

Power-on Sequence	Signal Name	Device	Vout	Intended node
1	VIO_OUT	PM6150	1.800	PXO PMIC I0 pads
2	VREG_BOB	PM6150L	3.296	BOB
3	VREG_S8C	PM6150L	1.352	MV sub regulation
4	VREG_S5A	PM6150	2.040	HV sub regulation
5	VREG_S4A	PM6150	1.056	LV sub regulation
6	VREG_L3A	PM6150	1.000	WTR 1 V digital
7	VREG_S3A	PM6150	0.852	MX
8	VREG_L7A	PM6150	0.848	LPI MX
9	VREG_SIA_S2A	PM6150	0.800	CX
10	VREG_L8A	PM6150	0.800	LPI CX
11	VREG_L9A	PM6150	0.664	WCSS CX
12	VREG_L10A	PM6150	1.800	1.8 V PX3 LDO
13	VREF_MSM	PM6150	1.250	VREF HVPAD
14	VREG_S1C	PM6150L	1.128	LP4X VDD2 1.128
15	VREG_L6A	PM6150	0.600	LP4X VDDQ 0.6 V
16	VREG_L12A	PM6150	1.800	eMMC/UFS 1.8
17	VREG_L3C	PM6150L	1.232	1.23 V MSIPs
18	VREG_L4A	PM6150	0.928	0.9 V MSIPs
19	VREG_L11A	PM6150	1.800	1.8 V PLL VDDA MSIPs

20	VREG_L17A	PM6150	3.128	USB 3.1V
21	VREG_11C	PM6150L	2.960	UFS 2.96 V
22	VREG_L6C	PM6150L	2.960	PX_2
23	VREG_L9C	PM6150L	2.960	SD_MMC 3V
24	VREG_S7C	PM6150L	0.800	Modem
25	VREG_S3C	PM6150L	0.800	APC0

3.4 C610 System Power Tree



3.5 C610 Power On

There are 2 pads which can trigger Power on sequence.

- KPD_PWR_N:

Connected to a keypad power-on button and when grounded, initiates the power-on sequence.

If held at a logic low for longer durations. Can also be configured for generating a stage 2 and/or stage 3 reset Pulled up internally to 1.8V via the dVdd regulator.

- CBL_PWR_N:

Alternate input pad, which can be used to initiate the power-on sequence when grounded; pulled up internally to 1.8V via the dVdd regulator.

3.6 C610 Boot Configuration

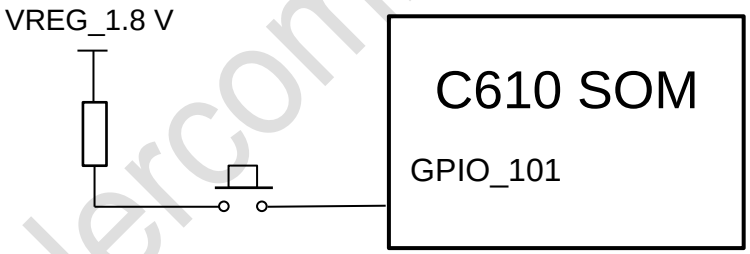
Special boot-related GPIO features:

- They are sensed for boot-purposes during IC reset (during fuse sense).
- After boot-up, use them for normal GPIO functions.
- Do not have pull-ups on Boot configuration GPIO

Forced USB boot:

During development or factory production, boot from USB3.1 port are forced by using GPIO_101.

- FORCED_USB_BOOT (GPIO_101) always takes precedence, regardless of the state of the BOOT_CONFIG GPIOs or FAST_BOOT_SEL fuses.
- FORCED_USB_BOOT is checked first during the boot device detection prior to BOOT_CONFIG GPIOs.
- GPIO_101 = 1 forces the SDM device to boot from USB0 port.



3.7 C610 USB Ports

QCS610 has two USB ports

- USB port 0 – 4-lane USB3 PHY and USB2 PHY connected to USB3 controller
- USB port 1 – USB2 PHY connected to USB2 controller and 4-lane DisplayPort connected to DP controller Over USB3 PHY.

During Development or factory production, we can download images to memory using USB port 0.

Please note the usage of TYPEC_uUSB_SEL.

C60	TYPEC_uUSB_SEL	AUX1，560Kohm to GND if use USB Type C connector on USB port 0. Float, if use Micro USB connector

3.8 Debug UART

QUP0 serial engine 0 (GPIO_16, GPIO_17) can be used for debugging.

4 Electrical Characteristics

4.1 Operating Conditions

Parameters	Min	Typical	Max	Units
Input Power voltage				
USB_IN	3.7		12.6	V
VBATT, VPH_PWR	+2.7	3.8	+4.8	V
MID_CHG	3.7	-	12.6	V
Thermal conditions				
Operating Junction temperature	-30	25	125	°C

4.2 Output Power

Function	Default voltage(V)	Programble range(V)	Rated current(mA)	Default State	Expected use
VREG_S4A_1P056	1.056	0.32 to 2.04	4000		LV sub-regulation;
VREG_S5A_2P04	2.04	0.32 to 2.04	3000		HV sub-regulation
VREG_S8C_1P3	1.352		3500		MV sub-regulated LDOs
VREG_BOB	3.3		2000		
VREG_L1A_1P2		0.32 to 1.304	1200	Off	WTR 1V2
VREG_L2A_1P0		0.32 to 1.304	1200	Off	WTR 1V0 Analog
VREG_L3A_1P0	1.000	0.32 to 1.304	600		WTR 1V0 Digital
VREG_L5A_2P7		1.504 to 3.544	150	Off	RFFE 2.7V
VREG_L10A_1P8	1.800	1.504 to 2.0	600		PX3 LDO
VREG_L13A_1P8		1.504 to 2.0	300	Off	Camaro IO 1.8V
VREG_L14A_1P8		1.504 to 2.0	600	Off	WTR 1V8
VREG_L15A_1P8		1.504 to 2.0	600	Off	Codec 1.8V
VREG_L16A_3P3		1.504 to 3.544	150	Off	RFFE 2.7V
VREG_L18A_3P3		1.504 to 3.544	150	Off	AMOLED 3V
VREG_L19A_2P85		1.504 to 3.544	600	Off	WCN3990
VREG_L6C_SDC2		1.504 to 3.544	150	Off	SDC IO/ Sensor
VREG_L7C_3P0		1.504 to 3.544	600	Off	ALS Sensor 3V
VREG_L8C_1P8		1.504 to 2.0	150	Off	1,8V environment sensors
VREG_L9C_2P95		1.504 to 3.544	600	Off	SD_MMC 3V
VREG_WLED		6 to 31.5	60	Off	LCD Back Light
VREG_DISP_P		4.4 to 6	80	Off	LCD bias
VREG_DISP_N		-6 to -4.4	80	Off	LCD bias

4.3 Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage.
The I2C, USB,SPI and UART are complied with their standards, no additional specifications are listed.
Performance specifications for all other digital I/Os are organized within this section.

4.3.1 Digital GPIO characteristics

The GPIOs can be programmed for a variety of configurations.
The following table shows the electrical characteristics for GPIOs:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.65* VIO	-	V
VIL	Low-level input voltage, CMOS/Schmitt,	-	0.35* VIO	V
VOH	High-level output voltage, CMOS	VIO-0.45	-	V
VOL	Low-level output voltage, CMOS	-	0.45	V

4.4 USB

USB standards and exceptions.

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later).	*Feature exceptions SS Gen2.*

4.5 I2S

I2S standards and exceptions:
Legacy I2S interfaces for primary and secondary microphones and speakers.
The multiple I2S (MI2S) interface for microphone and speaker functions, including audio for HDMI.

4.6 I2C

I2C standards and exceptions:

Applicable standard	Feature exceptions
I²C Specification, version 5.0, October 2012	None

4.7 RF Performance

Wi-Fi supports 2.4G & 5G, below table records the RF performance test results.

Table 0-1 WIFI Performance

2.4G WLAN performance					
Tx Characteristics					
Parameter	**Comments**	**Min**	**Typ**	**Max**	**Unit**
Tx frequency range		2.412		2.484	GHz
1. power level					
802.11b@11Mbps		14.5	16	18	dbm
802.11g @54Mbps		12.5	14	18	dbm
802.11n,2.4G@HT20-MCS7		11.5	13	17.5	dbm
802.11n,2.4G @HT40-MCS7		11.5	13	16.5	dbm
2. Frequency Error		-20		20	ppm
3.Modulation Accuracy(EVM)					
802.11b@11Mbps			-17	-9	db
802.11g@ 54Mbps			-34	-25	db
802.11n,2.4G, HT20-MCS7			-34	-28	db
802.11n,2.4G, HT40-MCS7			-34	-28	db
Rx Characteristics					
Rx input frequency range		2.412		2.484	GHz
Minimum Input Level Sensitivity					
802.11b@11Mbps(PER ≤ 8%)			-87	-76	dbm
802.11g@54Mbps(PER ≤ 10%)			-72	-65	dbm
802.11n, HT20-MCS7(PER ≤ 10%)			-70	-64	dbm
802.11n, HT40-MCS7(PER ≤ 10%)			-68	-61	dbm

Table 0-2WIFI Performance

5.8G WLAN performance					
Tx Characteristics					
Parameter	**Comments**	**Min**	**Typ**	**Max**	**Unit**
Tx frequency range		5.180		5.825	GHz

1. power level					
802.11a@54Mbps		10.5	12	15	dbm
802.11n @HT20-MCS7		9.5	11	14	dbm
802.11n @HT40-MCS7		9.5	11	13	dbm
802.11ac@VHT20-MCS8		8.5	10	14	dbm
802.11ac@VHT40-MCS9		8.5	10	13	dbm
802.11ac@VHT80-MCS9		8.5	10	12	dbm
2. Frequency Error		-20		20	ppm
3.Modulation Accuracy(EVM)					
802.11a@54Mbps			-34	-25	db
802.11n @HT20-MCS7			-34	-28	db
802.11n @HT40-MCS7			-37	-28	db
802.11ac@VHT20-MCS8			-37	-30	db
802.11ac@VHT40-MCS9			-39	-32	db
802.11ac@VHT80-MCS9			-38	-32	db
Rx Characteristics					
Rx input frequency range		5.180		5.825	GHz
Minimum Input Level Sensitivity					
802.11a@54Mbps (PER ≤ 10%)			-73	-65	dbm
802.11n @HT20-MCS7(PER ≤ 10%)			-70	-64	dbm
802.11n @HT40-MCS7(PER ≤ 10%)			-68	-61	dbm
802.11ac@VHT20-MCS8(PER ≤ 10%)			-61	-59	dbm
802.11ac@VHT40-MCS9(PER ≤ 10%)			-63	-54	dbm
802.11ac@VHT80-MCS9(PER ≤ 10%)			-60	-51	dbm

Statement

1. Conformity Assessment of the Radio Module to the RED

This radio module is for professional installation only. When installing this radio module permanently into a host product to a create new radio equipment device; the manufacturer responsible for placing the final radio product on the market in the EU must assess if the combination of this radio module and the host product complies with the essential requirements of the RE Directive 2014/53/EU.

2. Firmware version:

Test Antenna: PIFA Antenna and maximum gain 2dBi.

The final radio product will need to be fully assessed to Article 3.1a of the RED, for product safety With regard to RF exposure for Article 3.1a of the RED, the manufacturer of the final radio product will need to assess if the compliance assessment of the original radio equipment/module remains relevant to the final radio product, or if further action is necessary.

This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

If the final radio equipment is used at the same distance from a person or domesticated animal as the radio module was assessed, (for example: >20cm), then the final radio product assessment could conclude that the final radio product is compliant with the RF exposure requirements without additional actions.

If the final radio equipment is used at a closer distance from a person or domesticated animal than the radio module was assessed, then the final radio product assessment could not automatically conclude that the final radio product is compliant with the RF exposure requirements without additional actions; and further assessment is necessary.

The final radio product will need to be fully assessed to Article 3.1b of the RED, for EMC.

EMC testing of the radio module will have been performed on some sort of temporary host or test jig; but now the module is in a new host product and the EMC performance of the final radio product must be assessed. Most likely the host product will have its own EMC assessment for other functions, which should be performed with the radio module installed; and inclusion of the radio module into the host product will also require an assessment, such as to the relevant applicable part of EN 301 489, on the final radio product.

In theory, radio transmitter or receiver measurements made as conducted measurements at a radio module antenna port may be considered applicable to the radio performance of the final radio product. However, in this example, the radio module does not have an antenna port. The radio module has a pin which leads through a PCB trace to an antenna on the host product. If the manufacturer of the final radio product wishes to use conducted power, conducted emissions or receiver performance measurements from the radio module to show compliance of the final radio product, then they will need to exactly follow the detailed instructions from the radio module manufacturer; including input voltage, driver software, environmental conditions, antenna trace layout design construction and material, circuit board layout design construction and material,

nearby circuitry, etc. In reality, it is expected that manufacturers of final radio products will need to test the output power, conducted spurious emissions and receiver performance requirements on the final radio product; and not take the results of those test cases from the radio module test reports. Radiated test cases will also need to be performed on the final radio product.

3. FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

3.1.List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C has been investigated. It is applicable to the modular.

3.2.Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

3.3.Limited module procedures

Not applicable

3.4.Trace antenna designs

Not applicable

3.5.RF exposure considerations

To maintain compliance with FCC' s RF Exposure guidelines, This equipment should be installed and operated with minimum distance of 20cm from your body.

3.6.Antennas

This radio transmitter FCC ID: **2AOHHTURBOXC610** has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Internal Identification	Antenna Description	Antenna Type	Maximum Antenna Gain
Antenna 1	Bluetooth and Wi-Fi Antenna	PIFA Antenna	2dBi

3.7.Label and compliance information

The final end product must be labeled in a visible area with the following "**Contains FCC ID: 2AOHHTURBOXC610**" .

3.8.Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

3.9.Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B